

# DATA SHEET

## **TDA8426**

Hi-fi stereo audio processor;  
I<sup>2</sup>C-bus

Product specification  
File under Integrated Circuits, IC02

March 1991

**Hi-fi stereo audio processor; I<sup>2</sup>C-bus****TDA8426****GENERAL DESCRIPTION**

The TDA8426 is a stereo sound circuit with a loudspeaker channel facility, digital controlled via the I<sup>2</sup>C-bus, for application in hi-fi audio and television sound. Reduced spatial antiphase crosstalk (30%) makes the device especially suitable for application in projection television receivers.

**Features**

- Source and mode selector for two stereo channels
- Pseudo stereo, spatial stereo, linear stereo and forced mono switch
- Volume and balance control
- Bass, treble and mute control
- Power supply with power-on reset

**QUICK REFERENCE DATA**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (pin 4)	V <sub>CC</sub>	10.8	12.0	13.2	V
Input signal handling	V <sub>I</sub>	2	–	–	V
Input sensitivity full power at the output stage	V <sub>i</sub>	–	300	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	86	–	dB
Total harmonic distortion	THD	–	0.05	–	%
Channel separation	α	–	80	–	dB
Volume control range	G	–64	–	6	dB
Treble control range	G	–12	–	12	dB
Bass control range	G	–12	–	15	dB

**PACKAGE OUTLINE**

20-lead dual in-line; plastic (SOT146); SOT146-1; 1996 November 29.

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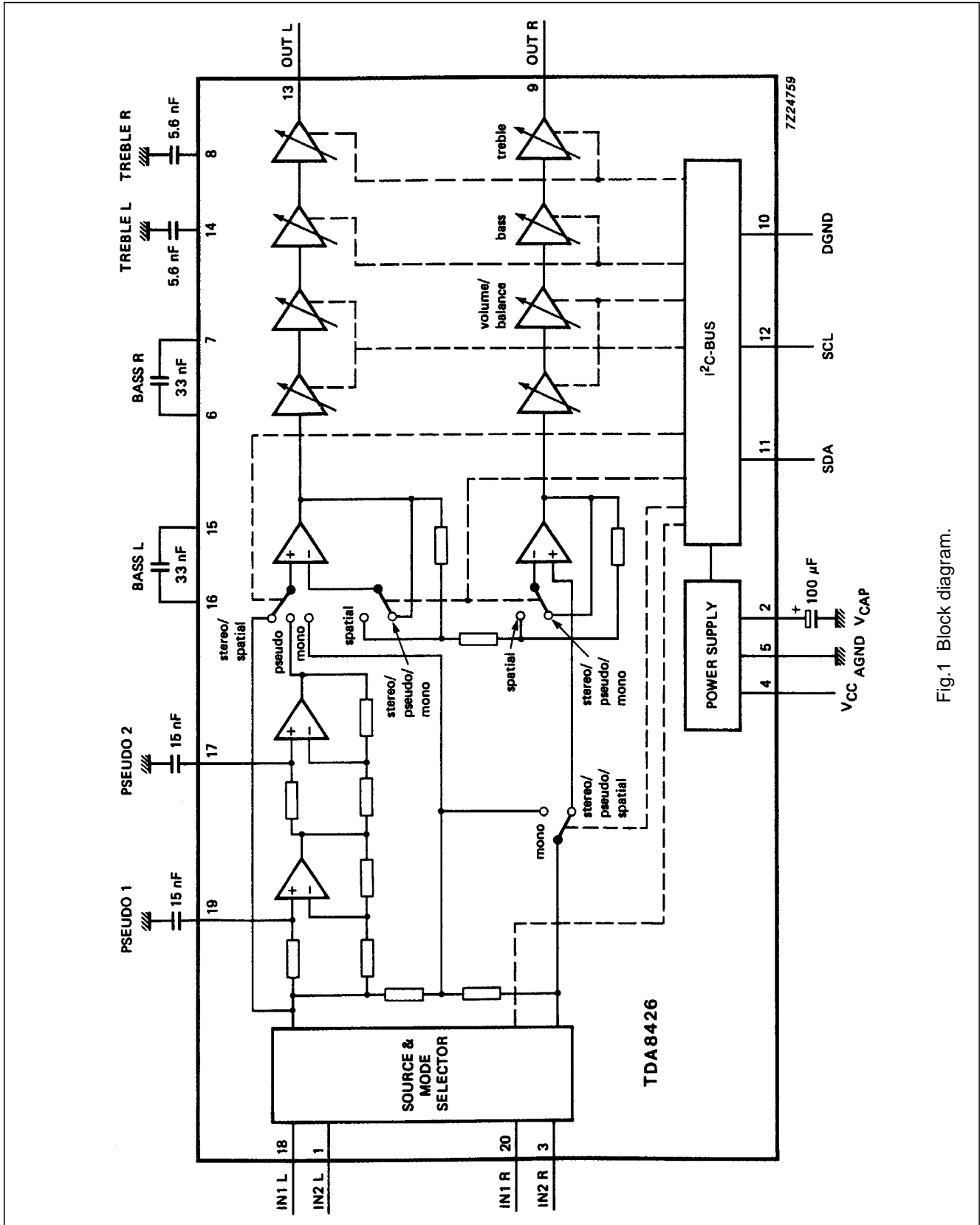
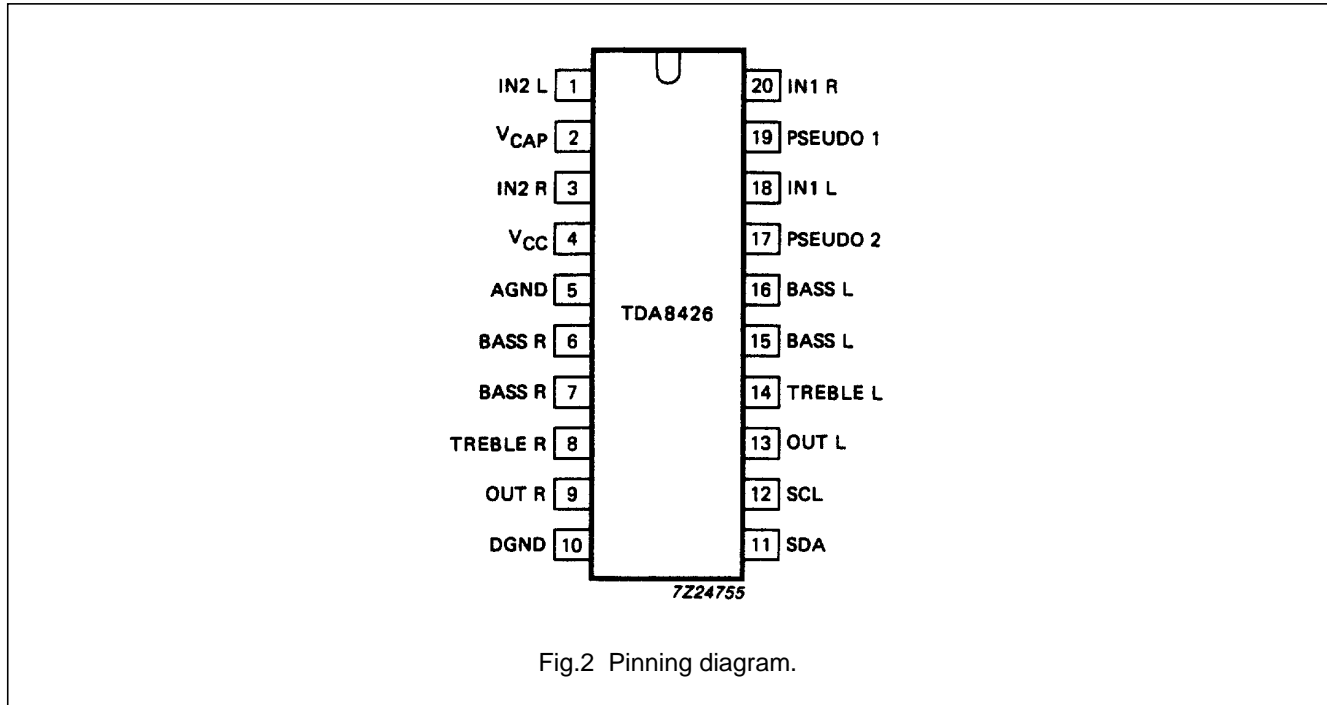


Fig.1 Block diagram.

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## PINNING



## FUNCTIONAL DESCRIPTION

## Source selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the source selector. The selection is made from the following AF input signals:

- IN1 L (pin 18); IN1 R (pin 20)  
or
- IN2 L (pin 1); IN2 R (pin 3)

## Mode selector

The mode selector selects between stereo, sound A and sound B (in the event of bilingual transmission) for OUT R and OUT L.

## Volume control and balance

The volume control consists of two stages (left and right). In each part the gain can be adjusted between +6 dB and -64 dB in steps of 2 dB. An additional step allows an attenuation of  $\geq 80$  dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right output channels.

Linear stereo, pseudo stereo, spatial stereo and forced mono mode<sup>(1)</sup>

It is possible to select four modes: linear stereo, pseudo stereo, spatial stereo or forced mono. The pseudo stereo mode handles mono transmissions, the spatial stereo mode handles stereo transmissions and the forced mono can be used in the event of stereo signals.

(1) During forced mono mode the pseudo stereo mode cannot be used.

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**Bass control**

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

**Treble control**

The treble control stage can be switched from +12 dB to -12 dB in steps of 3 dB.

**Bias and power supply**

The TDA8426 includes a bias and power supply stage, which generates a voltage of  $0.5 \times V_{CC}$  with a low output impedance and injector currents for the logic part.

**Power-on reset**

The on-chip power-on reset circuit sets the mute bit to active, which mutes both parts of the treble amplifier. The muting can be switched by transmission of the mute bit.

**I<sup>2</sup>C-bus receiver and data handling**

Bus specification

The TDA8426 is controlled via the 2-wire I<sup>2</sup>C-bus by a microcomputer.

The two wires (SDA – serial data, SCL – serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.

When the bus is free both lines are HIGH.

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.

A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.

The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition.

The bus is considered to be free again after a stop condition.

**Module address**

Data transmission to the TDA8426 starts with the module address MAD.

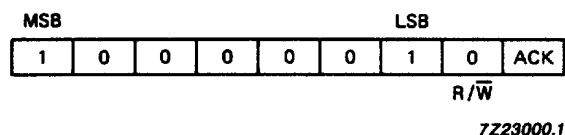


Fig.3 TDA8426 module address.

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**Subaddress**

After the module address byte a second byte is used to select the following functions:

- Volume left, volume right, bass, treble and switch functions

The subaddress SAD is stored within the TDA8426. Table 1 defines the coding of the second byte after the module address MAD.

**Table 1** Second byte after module address MAD

function	128	64	32	16	8	4	2	1
	MSB				LSB			
	7	6	5	4	3	2	1	0
volume left	0	0	0	0	0	0	0	0
volume right	0	0	0	0	0	0	0	1
bass	0	0	0	0	0	0	1	0
treble	0	0	0	0	0	0	1	1
switch functions	0	0	0	0	1	0	0	0
subaddress SAD								

The automatic increment feature of the slave address enables a quick slave receiver initialization, within one transmission, by the I<sup>2</sup>C-bus controller (see Fig.5).

**Definition of 3rd byte**

A third byte is used to transmit data to the TDA8426. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

**Table 2** Third byte after module address MAD and subaddress SAD

function		MSB							LSB
		7	6	5	4	3	2	1	0
volume left	VL	1	1	V05	V04	V03	V02	V01	V00
volume right	VR	1	1	V15	V14	V13	V12	V11	V10
bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS

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**Truth tables**

Truth tables for the switch functions

**Table 3** Source selector

function	ML1	ML0	IS	channel
stereo	1	1	0	1
stereo	1	1	1	2
sound A	0	1	0	1
sound B	1	0	0	1
sound A	0	1	1	2
sound B	1	0	1	2

**Table 4** Pseudo stereo/spatial stereo/linear stereo/forced mono

choice	STL	EFL
spatial stereo	1	1
linear stereo	1	0
pseudo stereo	0	1
forced mono <sup>(1)</sup>	0	0

**Table 5** Mute

mute	MU
active; automatic after POR <sup>(2)</sup>	1
not active	0

**Notes**

1. Pseudo stereo function is not possible in this mode.
2. Where: POR = Power-ON Reset.

Truth tables for the volume, bass and treble controls

**Table 6** Volume control

2 dB/step (dB)	V × 5	V × 4	V × 3	V × 2	V × 1	V × 0
6	1	1	1	1	1	1
4	1	1	1	1	1	0
−62	0	1	1	1	0	1
−64	0	1	1	1	0	0
≤ −80	0	1	1	0	1	1
≤ −80	0	0	0	0	0	0

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**Table 7** Bass control

3 dB/step (dB)	BA3	BA2	BA2	BA0
15	1	1	1	1
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
15	1	0	1	1
12	1	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
0	0	1	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
-12	0	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
-12	0	0	0	0

**Table 8** Treble control

3 dB/step (dB)	TR3	TR2	TR2	TR0
12	1	1	1	1
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
12	1	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
0	0	1	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
-12	0	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
-12	0	0	0	0



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### Sequence of data transmission

After a power-on reset all five functions have to be adjusted with five data transmissions. It is recommended that data information for switch functions are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 6. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

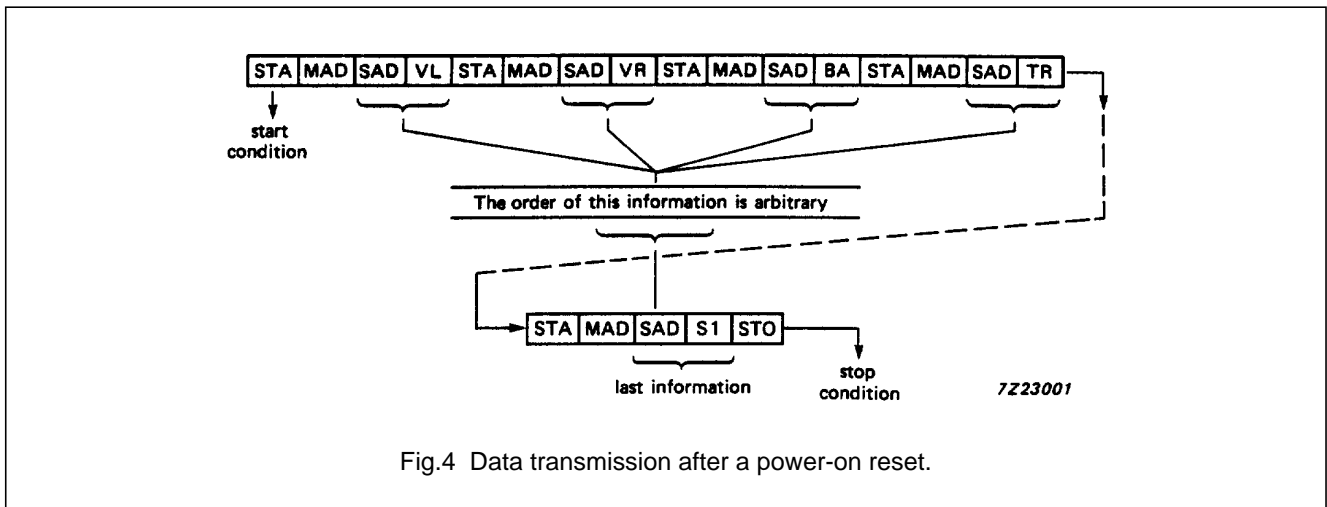


Fig.4 Data transmission after a power-on reset.

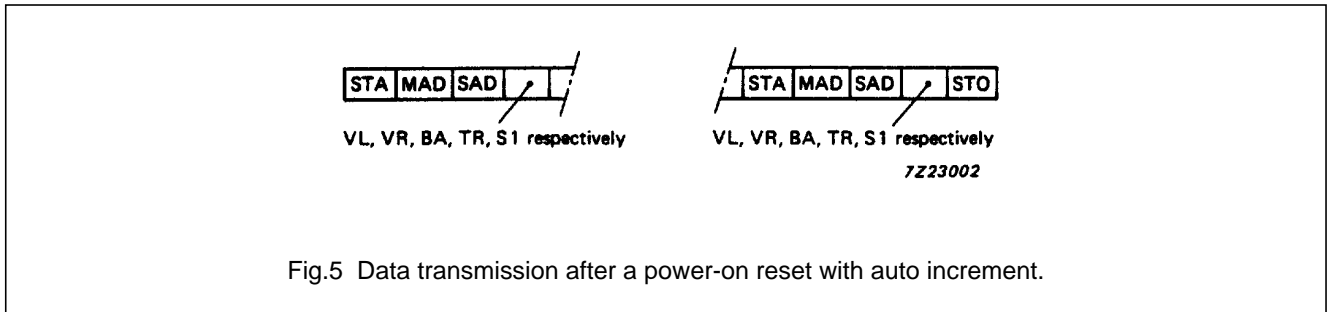


Fig.5 Data transmission after a power-on reset with auto increment.

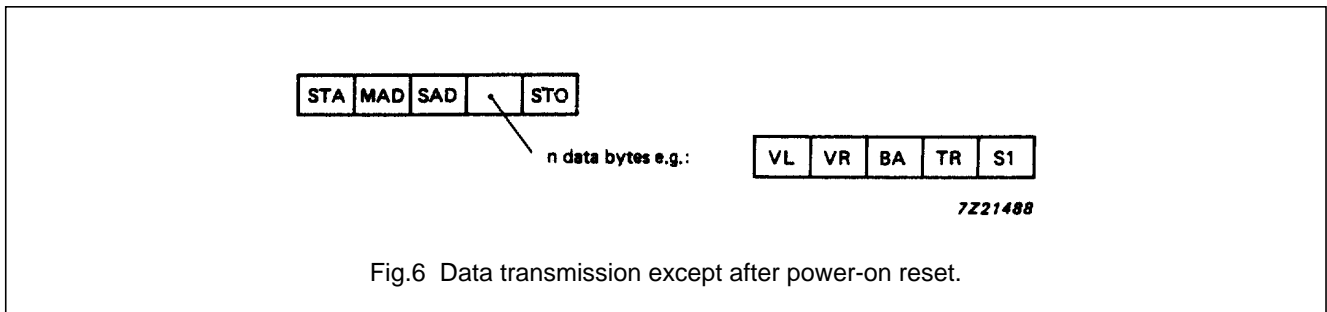


Fig.6 Data transmission except after power-on reset.

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**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply voltage	$V_{CC}$	0	16	V
Voltage range for pins with external capacitors	$V_{cap}$	0	$V_{CC}$	V
Voltage range for pins 11 and 12	$V_{SDA, SCL}$	0	$V_{CC}$	V
Voltage range at pins 1, 3, 9, 11, 12, 13, 18 and 20	$V_{I/O}$	0	$V_{CC}$	V
Output current at pins 9 and 13	$I_O$	–	45	mA
Total power dissipation at $T_{amb} < 70\text{ °C}$	$P_{tot}$	–	450	mW
Operating ambient temperature range	$T_{amb}$	0	70	°C
Storage temperature range	$T_{stg}$	–25	+150	°C
Electrostatic handling, classification A <sup>(1)</sup>				

**Note**

- Human body model: C = 100 pF, R = 1.5 k $\Omega$  and V  $\geq$  4 kV;  
charge device model: C = 200 pF, R = 0  $\Omega$  and V  $\geq$  500 V.

**DC CHARACTERISTICS** $V_{CC} = 12\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	$V_{CC}$	10.8	12.0	13.2	V
Supply current at $V_{CC} = 12\text{ V}$	$I_{CC}$	–	26	35	mA
Internal reference voltage	$V_{ref}$	5.4	$0.5 \times V_{CC}$	6.6	V
Internal voltage at pins 1, 3, 18 and 20 DC voltage internally generated; capacitive coupling recommended	$V_I$	–	$V_{ref}$	–	V
Internal voltage at pins 9 and 13	$V_O$	–	$V_{ref}$	–	V
SDA; SCL (pins 11 and 12) input voltage HIGH	$V_{IH}$	3.0	–	$V_{CC}$	V
input voltage LOW	$V_{IL}$	–0.3	–	1.5	V
input current HIGH	$I_{IH}$	–	–	+ 10	$\mu\text{A}$
input current LOW	$I_{IL}$	–10	–	–	$\mu\text{A}$
Output voltage at pins with external capacitors pins 6 to 8, 14 to 17, 19	$V_{cap.n}$	–	$V_{ref}$	–	V
pin 2	$V_{cap.2}$	–	$V_{CC} - 0.3$	–	V

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**AC CHARACTERISTICS<sup>(1)</sup>** $V_{CC} = 12\text{ V}$ ; bass/treble in linear position; pseudo and spatial stereo off;  $R_L > 10\text{ k}\Omega$ ;  $C_L < 1000\text{ pF}$ ; $T_{amb} = 25\text{ }^\circ\text{C}$ ; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
<b>I<sup>2</sup>C-bus timing</b> (see Fig.7)					
SDA, SCL (pin 11 and 12)					
Clock frequency range	$f_{SCL}$	0	–	100	kHz
The HIGH period of the clock	$t_{HIGH}$	4	–	–	$\mu\text{s}$
The LOW period of the clock	$t_{LOW}$	4.7	–	–	$\mu\text{s}$
SCL rise time	$t_r$	–	–	1	$\mu\text{s}$
SCL fall time	$t_f$	–	–	0.3	$\mu\text{s}$
Set-up time for start condition	$t_{SU; STA}$	4.7	–	–	$\mu\text{s}$
Hold time for start condition	$t_{HD; STA}$	4	–	–	$\mu\text{s}$
Set-up time for stop condition	$t_{SU; STO}$	4.7	–	–	$\mu\text{s}$
Time bus must be free before a new transmission can start	$t_{BUF}$	4.7	–	–	$\mu\text{s}$
Set-up time DATA	$t_{SU; DAT}$	250	–	–	ns
<b>INPUTS</b>					
IN1 L (pin 18) IN1 R (pin 20); IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (RMS value) at $V_u = -12\text{ dB}$ ; $THD \leq 0.5\%$	$V_{i(rms)}$	2	–	–	V
Input resistance	$R_i$	20	30	40	$\text{k}\Omega$
Frequency response ( $-0,5\text{ dB}$ ) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz
<b>OUTPUTS</b>					
OUT R (pin 9); OUT L (pin 13)					
Output voltage range (rms value) at $THD \leq 0.7\%$ ; $V_{i(max)} \leq 2\text{ V}$	$V_{o(rms)}$	0.6	–	–	V
Load resistance	$R_L$	10	–	–	$\text{k}\Omega$
Output impedance	$Z_O$	–	–	100	$\Omega$
Signal plus noise-to-noise ratio (weighted according to CCIR 468-2); $V_o = 600\text{ mV}$					
gain = 6 dB	(S+N)/N	–	78	–	dB
gain = 0 dB	(S+N)/N	–	86	–	dB
gain = $\leq -20\text{ dB}$	(S+N)/N	–	68	–	dB

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PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Crosstalk between inputs at gain = 0 dB; 1 kHz; opposite inputs grounded (50 Ω); IN1L (pin 18) to IN2L (pin 1) or IN1R (pin 20) to IN2R (pin 3)	$\alpha_{cr}$	–	100	–	dB
Total harmonic distortion (f = 20 Hz to 12.5 kHz) for $V_{i(rms)} = 0.3$ V; gain = +6 dB to –40 dB	THD	–	0.05	–	%
for $V_{i(rms)} = 0.6$ V; gain = 0 dB to –40 dB	THD	–	0.07	0.4	%
for $V_{i(rms)} = 2.0$ V; gain = –12 dB to –40 dB	THD	–	0.1	–	%
Channel separation at 10 kHz gain = 0 dB	$\alpha_{cs}$	–	80	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) $f_{ripple} = 100$ Hz	RR <sub>100</sub>	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	$\alpha_L$	–	100	–	dB
<b>VOLUME CONTROL</b>					
For truth table see Table 6					
Control range at f = 1 kHz (36 steps) maximum voltage gain (6 dB step)	$G_{max}$	5	6	–	dB
minimum voltage gain (–64 dB step)	$G_{min}$	–63	–64	–	dB
mute position	$G_{mute}$	–80	–90	–	dB
Gain tracking error; balance in mid-position	G	–	–	2	dB
Step resolution gain from 6 dB to –40 dB	$G_{step}$	1.5	2.0	2.5	dB/step
gain from –42 dB to –64 dB	$G_{step}$	1.0	2.0	3.0	dB/step
<b>TREBLE CONTROL</b>					
For truth table see Table 8					
Control range for $C_{8-5}, C_{14-5} = 5.6$ nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	$G_{step}$	2.5	3.0	3.5	dB/step

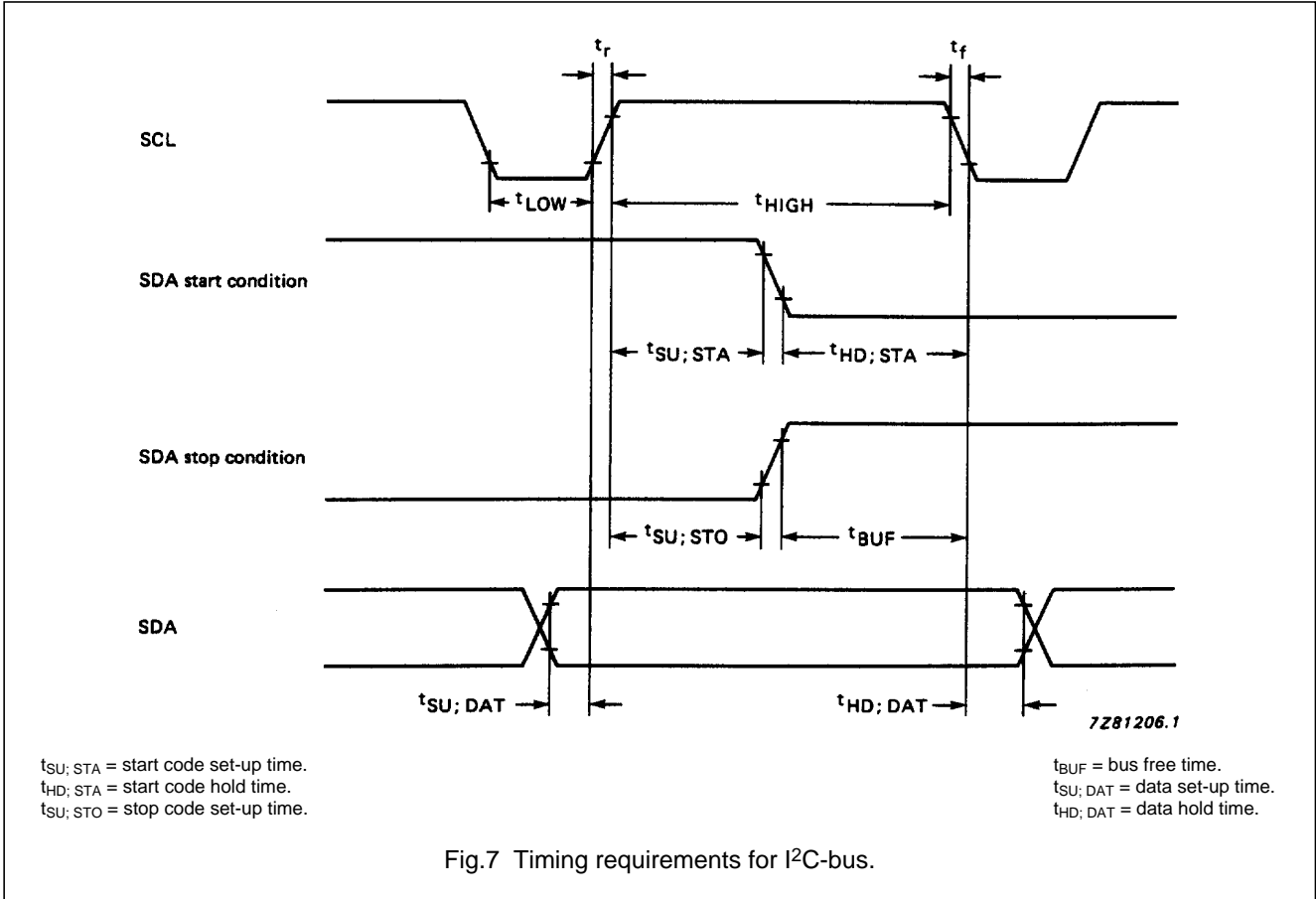
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PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
<b>BASS CONTROL</b>					
For truth table see Table 7					
Control range for C <sub>6-7</sub> ; C <sub>15-16</sub> = 33 nF					
Maximum emphasis at 40 Hz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 Hz with respect to linear position	G	11	12	13	dB
Resolution	G <sub>step</sub>	2.5	3.0	3.5	dB/step
<b>SPATIAL AND PSEUDO FUNCTION</b>					
Spatial:					
Antiphase crosstalk	α	–	30	–	%
Pseudo:					
Phase shift fig.8					

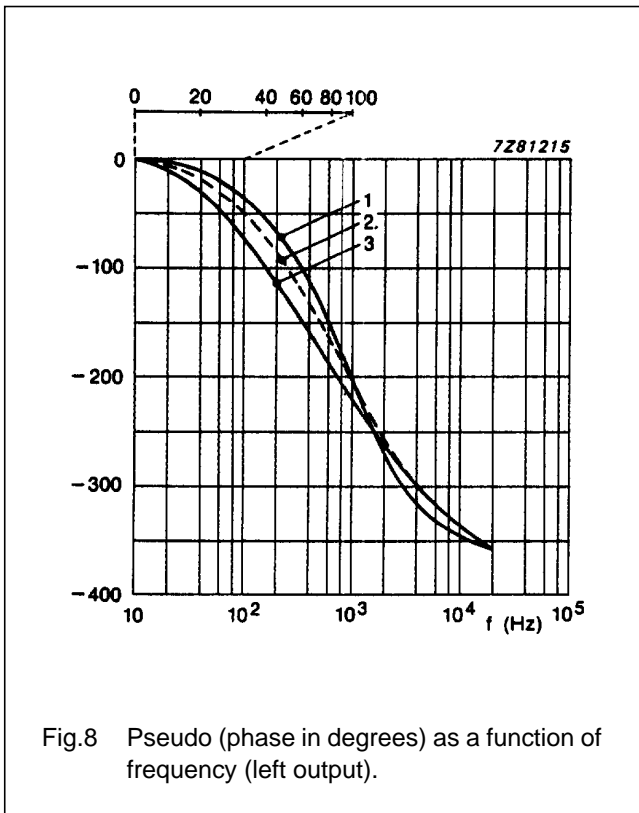
**Note to the AC characteristics**

1. Balance is realized via software by different volume settings in both channels (left and right).

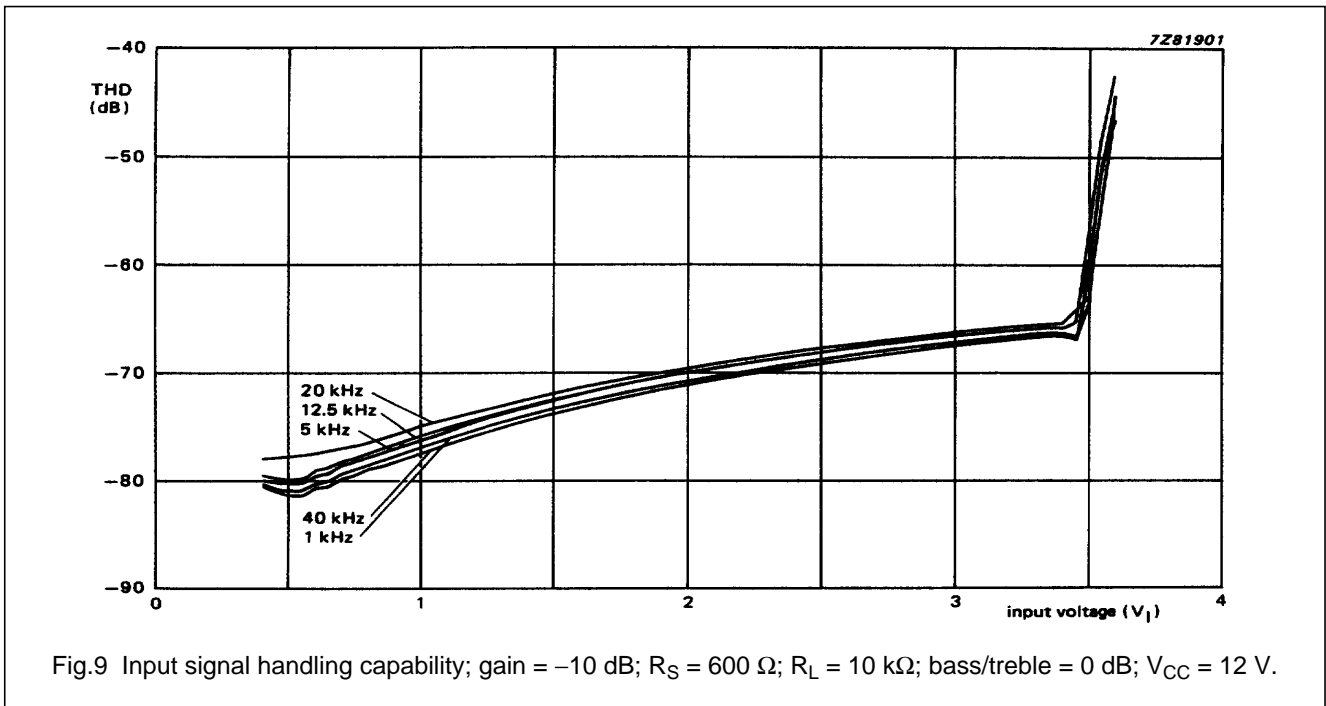


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curve	pin 17 (nF)	pin 19 (nF)	effect
1	15	15	normal
2	5.6	47	intensified
3	5.6	68	more intensified



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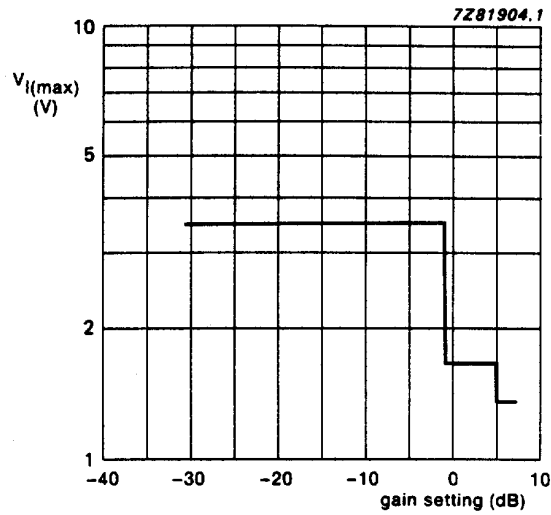


Fig.10 Input signal handling capability plotted against gain setting; THD = -60 dB;  $f = 1$  kHz;  $R_S = 600 \Omega$ ;  $R_L = 10 \text{ k}\Omega$ ; bass/treble = 0 dB;  $V_{CC} = 12 \text{ V}$ .

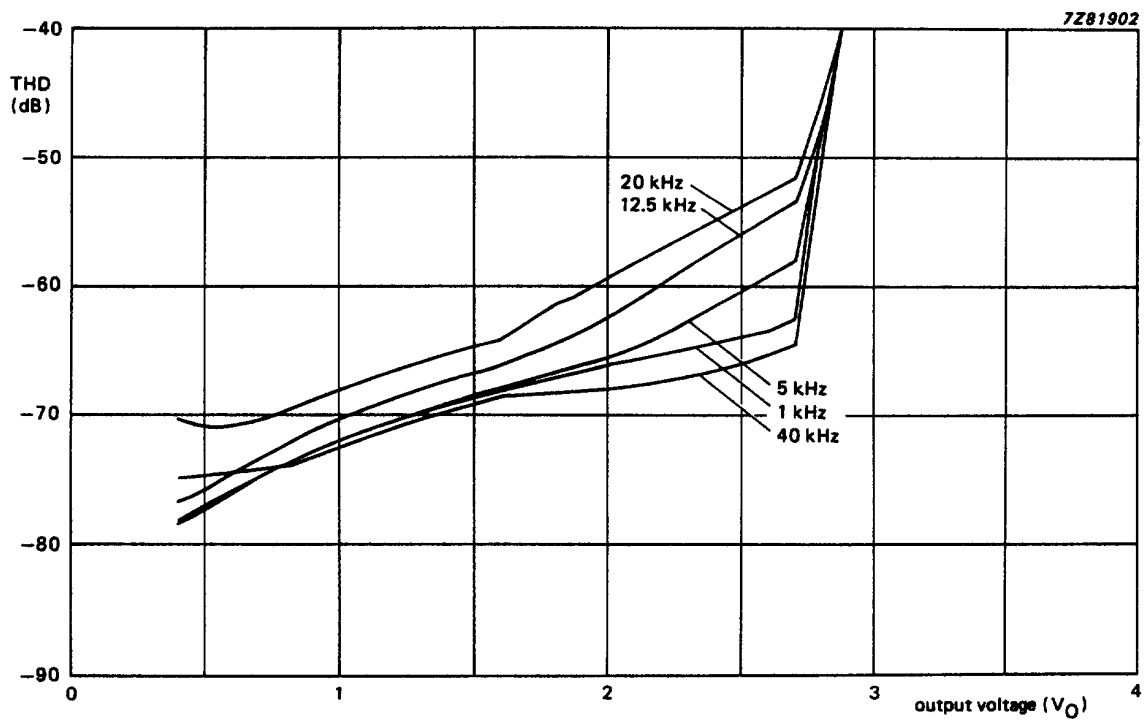


Fig.11 Output signal handling capability; gain = 6 dB;  $R_S = 600 \Omega$ ;  $R_L = 10 \text{ k}\Omega$ , bass/treble = 0 dB,  $V_{CC} = 12 \text{ V}$ .

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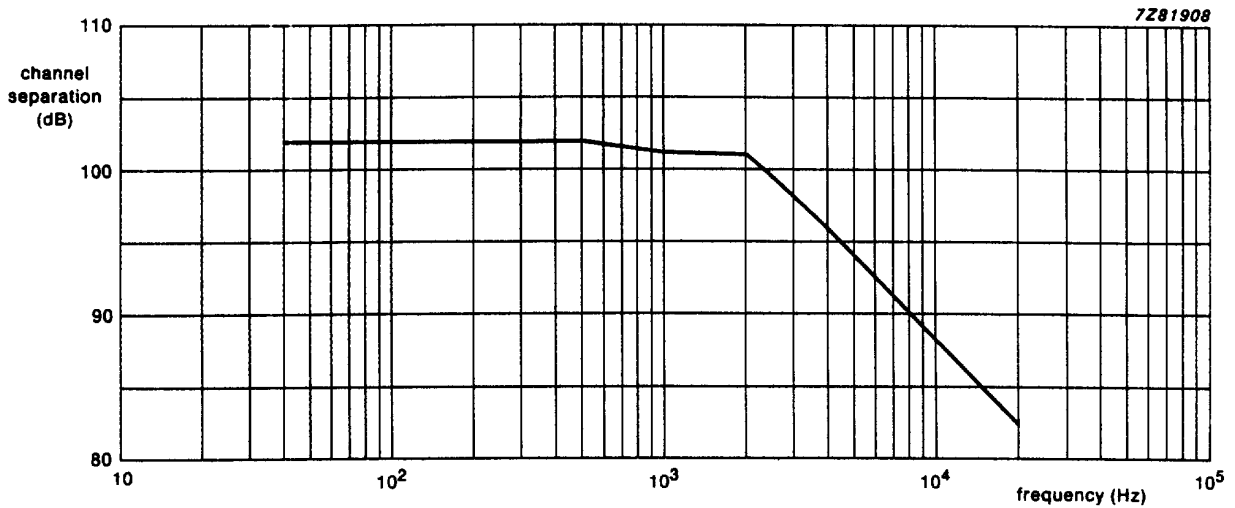
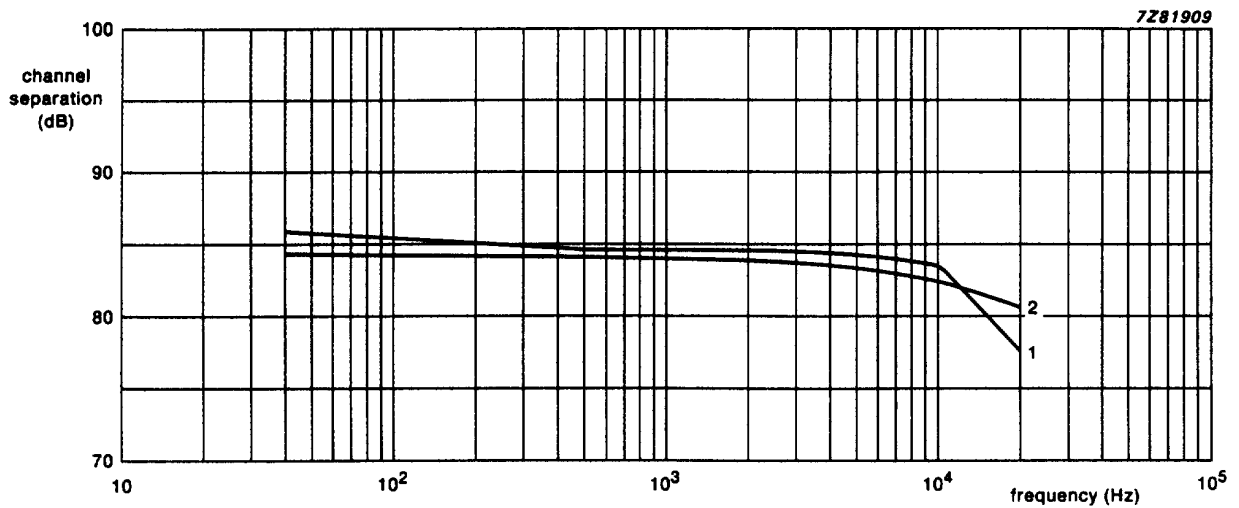


Fig.12 Source selector separation (channel 2 and channel 1); gain = 0 dB;  $V_{i1} = 0$  V;  $V_{i2} = 1$  V,  $R_S = 0 \Omega$ ;  $R_L = 10$  k $\Omega$ ; bass/treble = 0 dB;  $V_{CC} = 12$  V.



- (1) gain = 0 dB;  $V_i = 1.0$  V.
- (2) gain = 6 dB;  $V_i = 0.5$  V.

Fig.13 Stereo channel separation as a function of frequency;  $R_S = 0 \Omega$ ,  $R_L = 10$  k $\Omega$ ; bass/treble = 0 dB;  $V_{CC} = 12$  V.



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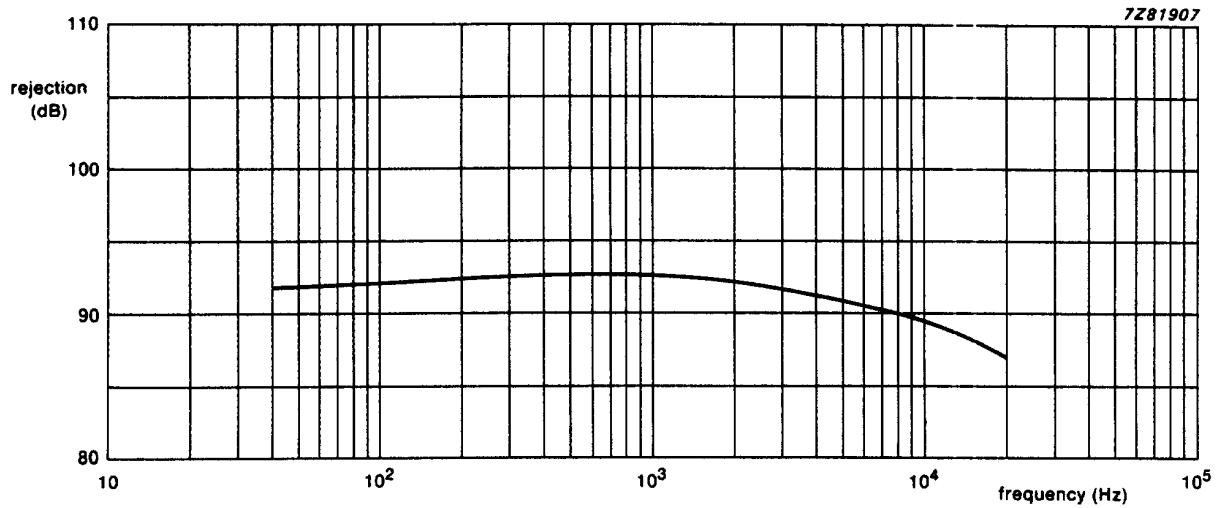


Fig. 14 Mute signal rejection as a function of frequency; gain = 0 dB;  $V_i = 1.0$  V;  $R_S = 0$   $\Omega$ ;  $R_L = 10$  k $\Omega$ ; bass/treble = 0 dB;  $V_{CC} = 12$  V.

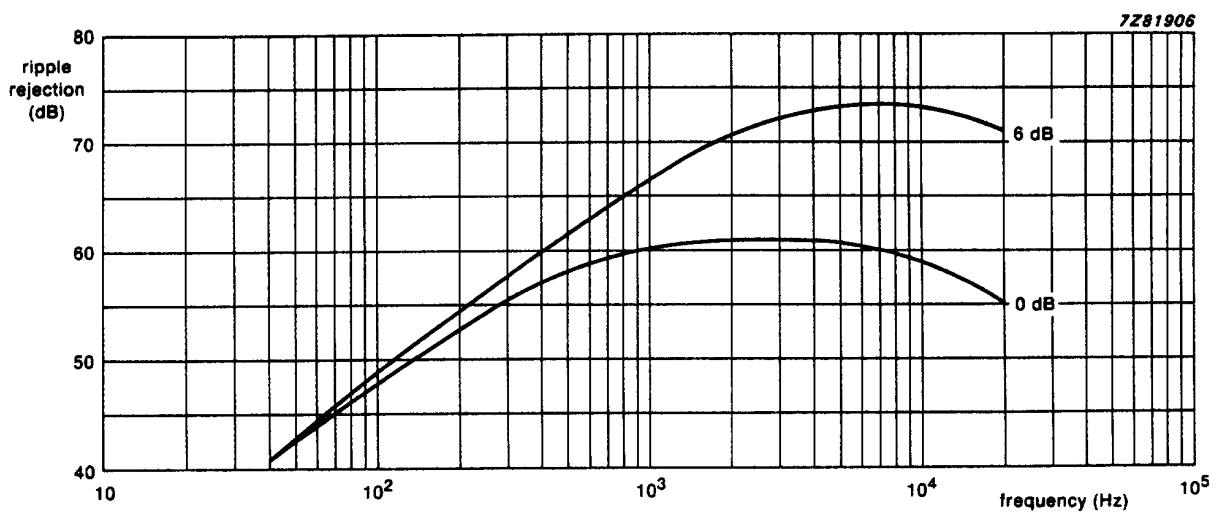
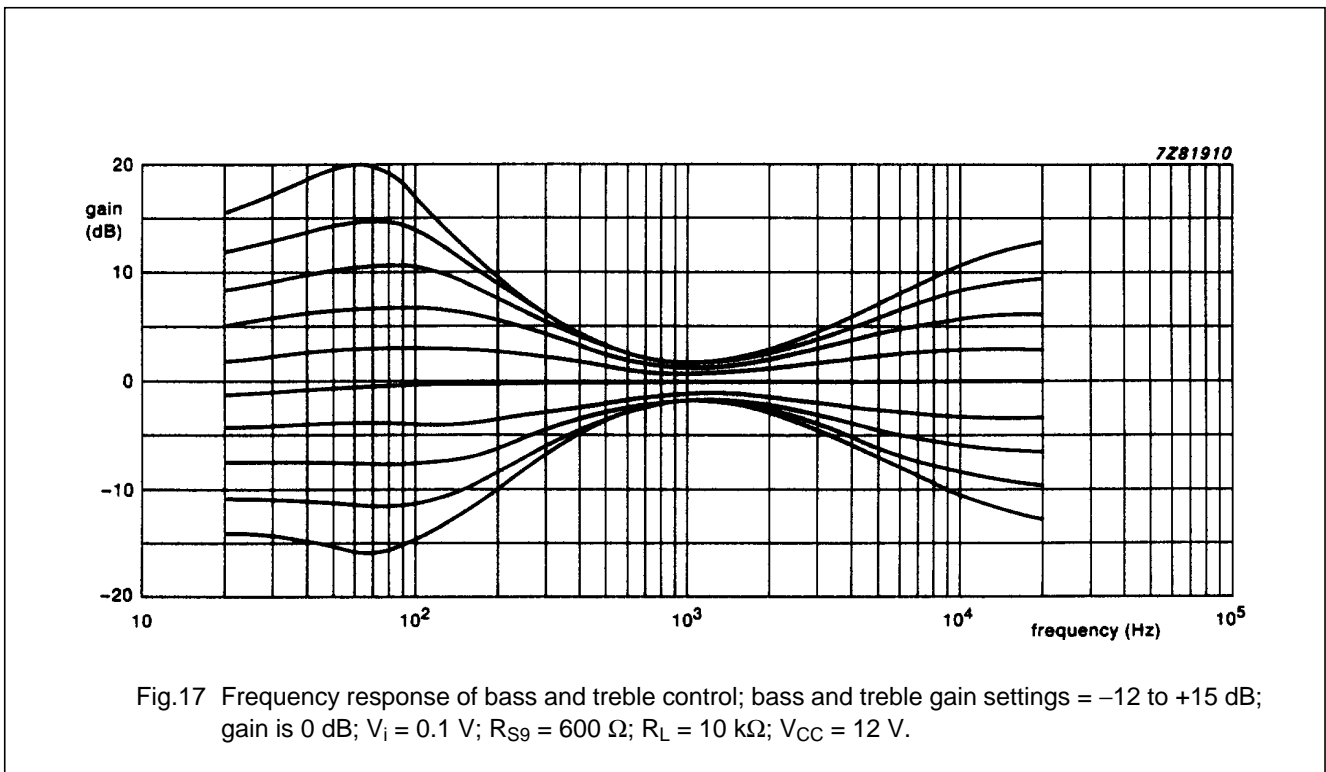
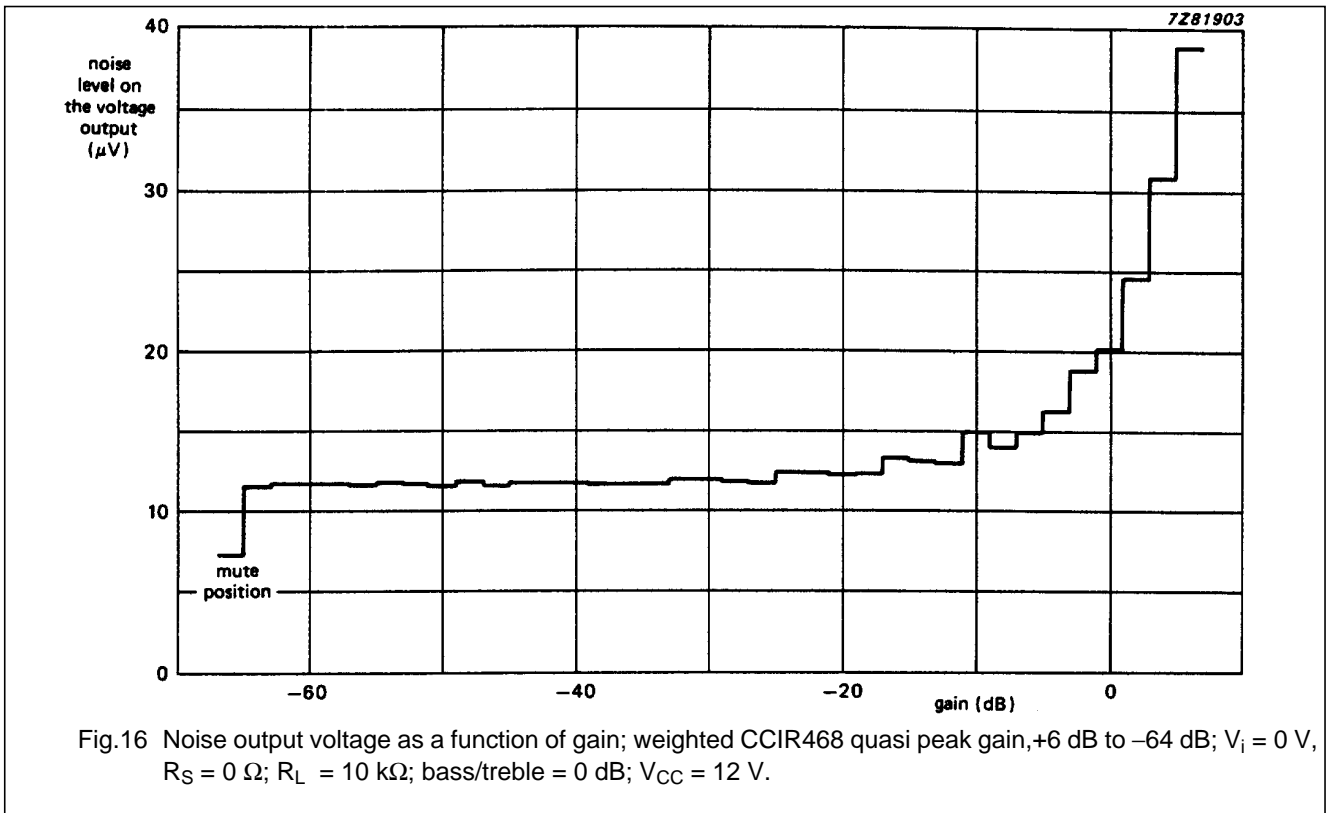


Fig. 15 Ripple rejection as a function of frequency; voltage ripple = 0.3 V (rms);  $R_S = 0$   $\Omega$ ;  $R_L = 10$  k $\Omega$ ; bass/treble = 0 dB;  $V_{CC} = 12$  V.

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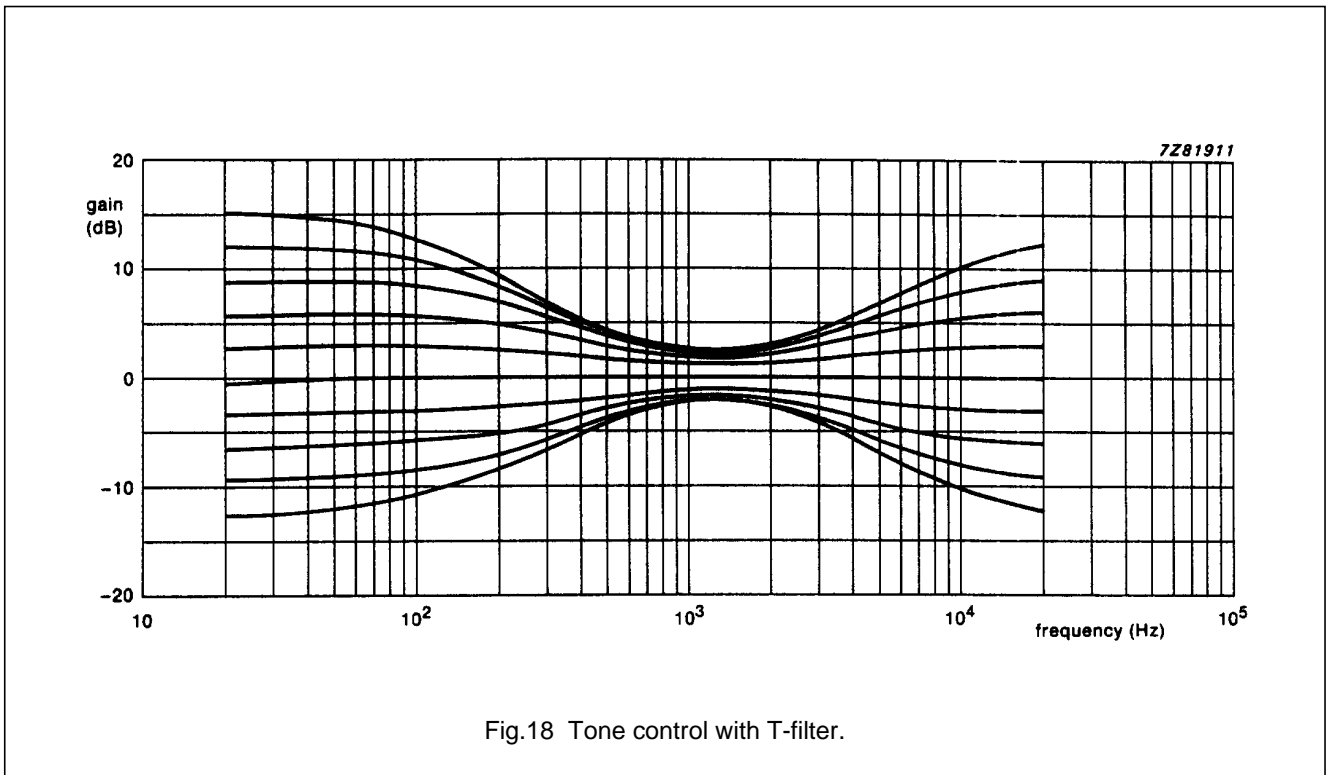


Fig.18 Tone control with T-filter.

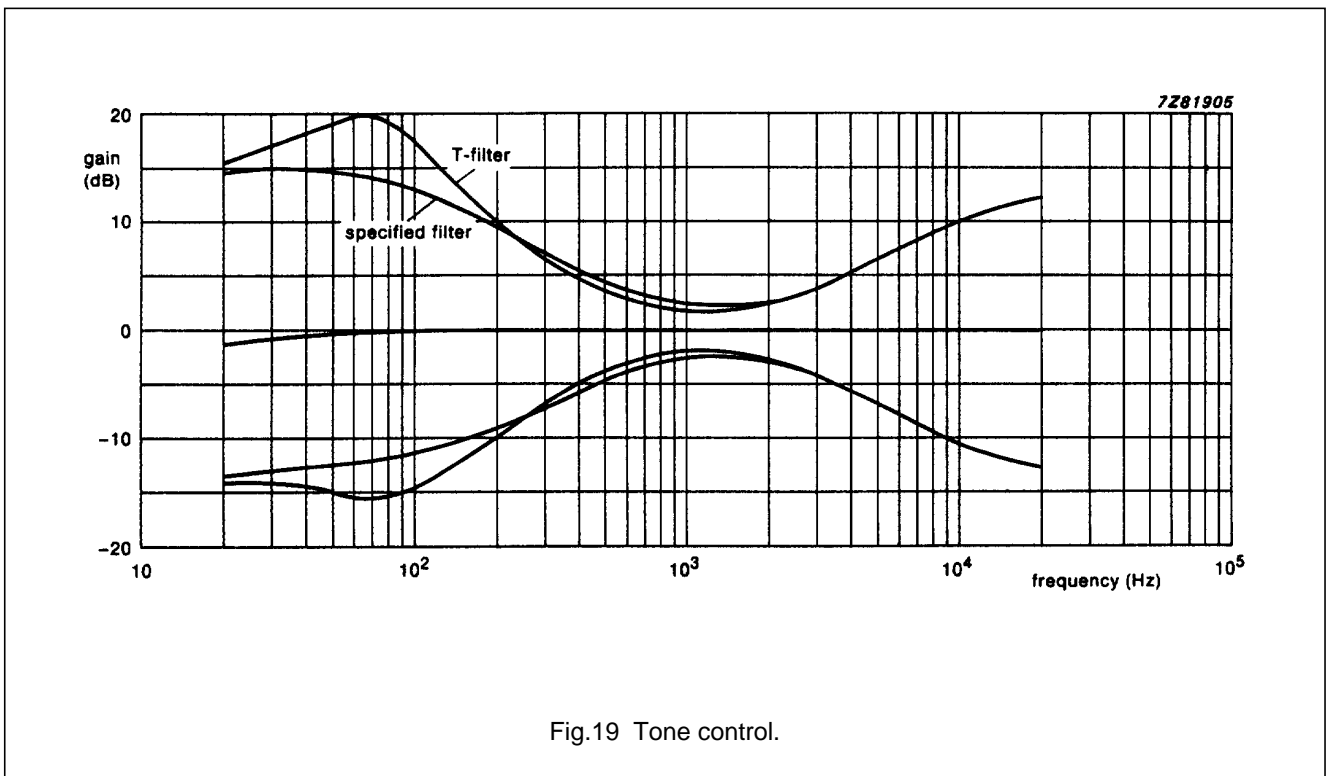
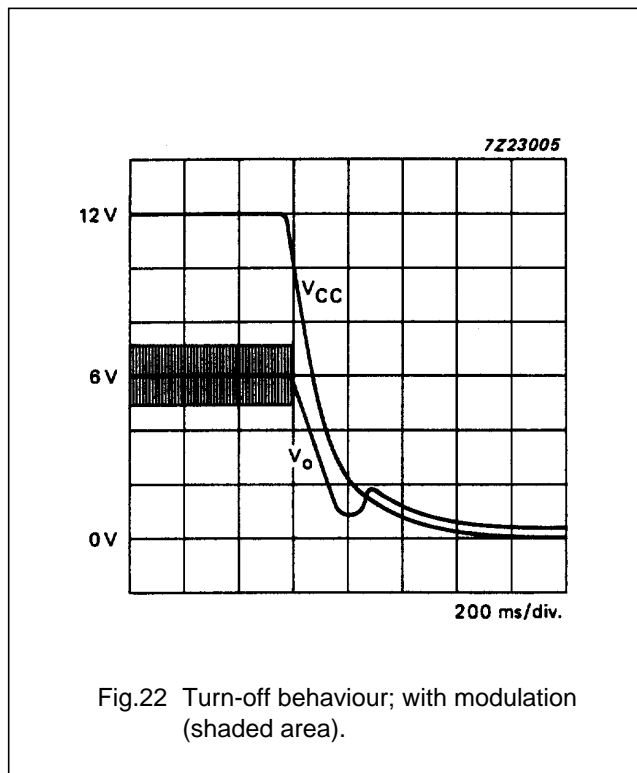
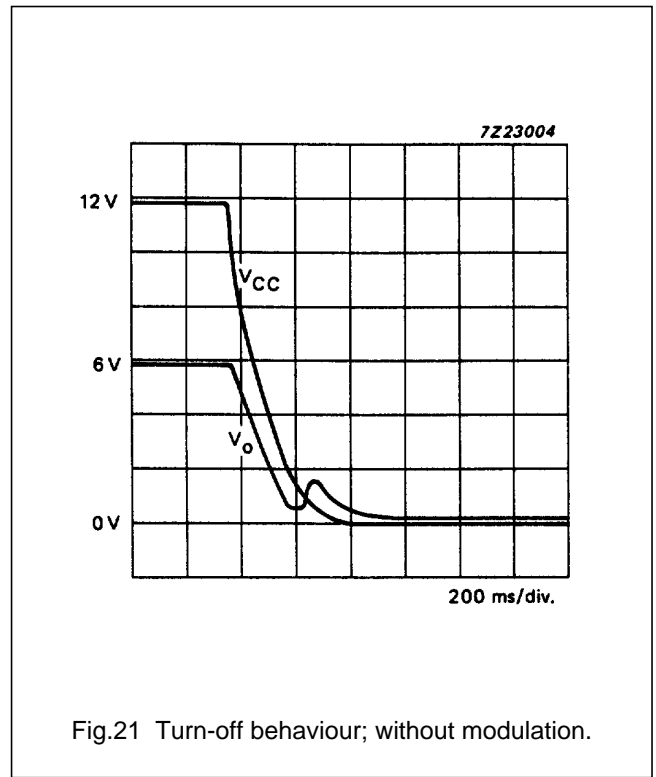
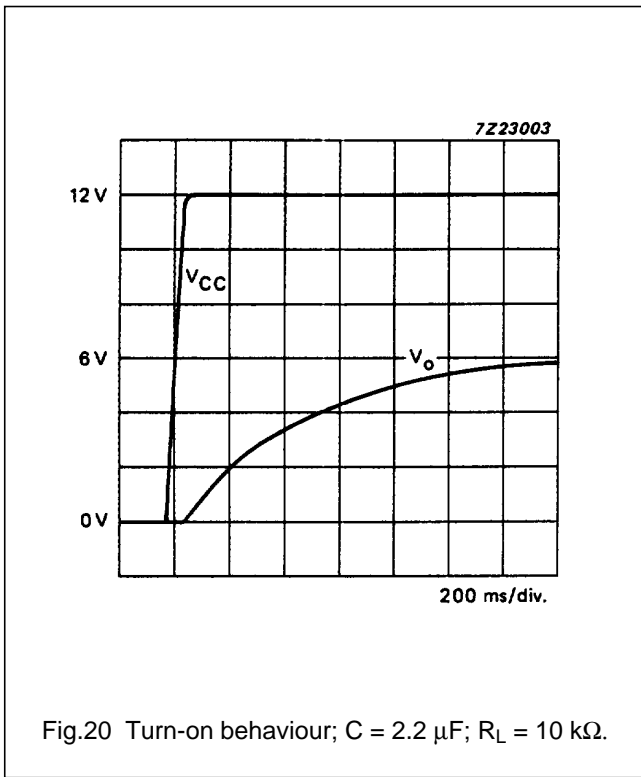


Fig.19 Tone control.

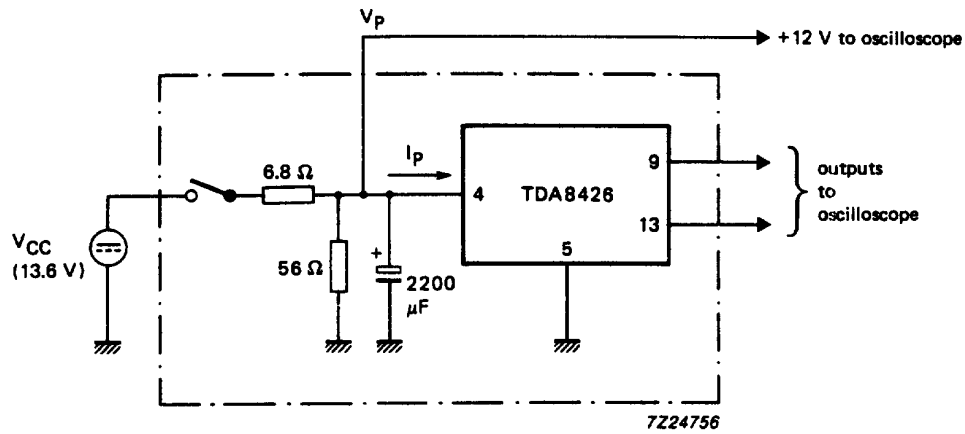
Hi-fi stereo audio processor; I<sup>2</sup>C-bus

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Hi-fi stereo audio processor; I<sup>2</sup>C-bus

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$I_{CC} = 25 \text{ mA}$   
 $I_{load} = 239 \text{ mA}$   
 $t_{on} = 15 \text{ ms}$   
 $t_{off} = 110 \text{ ms}$

Fig.23 Turn-on/off power supply circuit diagram.

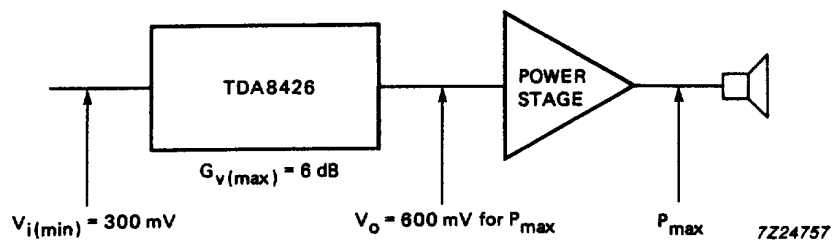


Fig.24 Level diagram.

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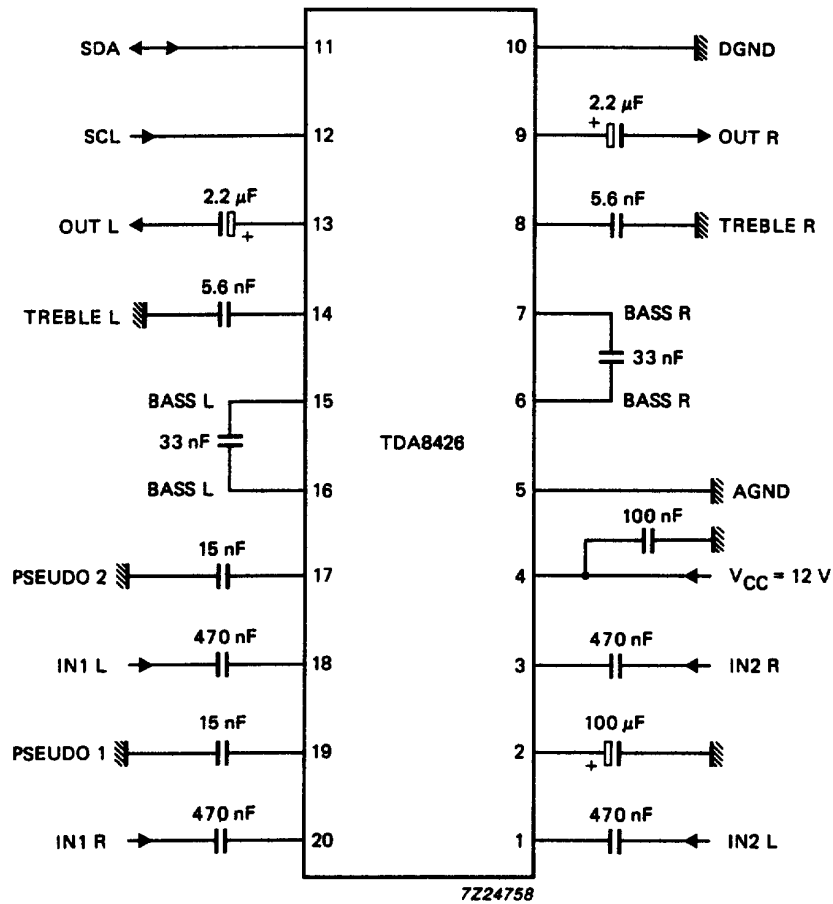


Fig.25 Test and application circuit diagram.

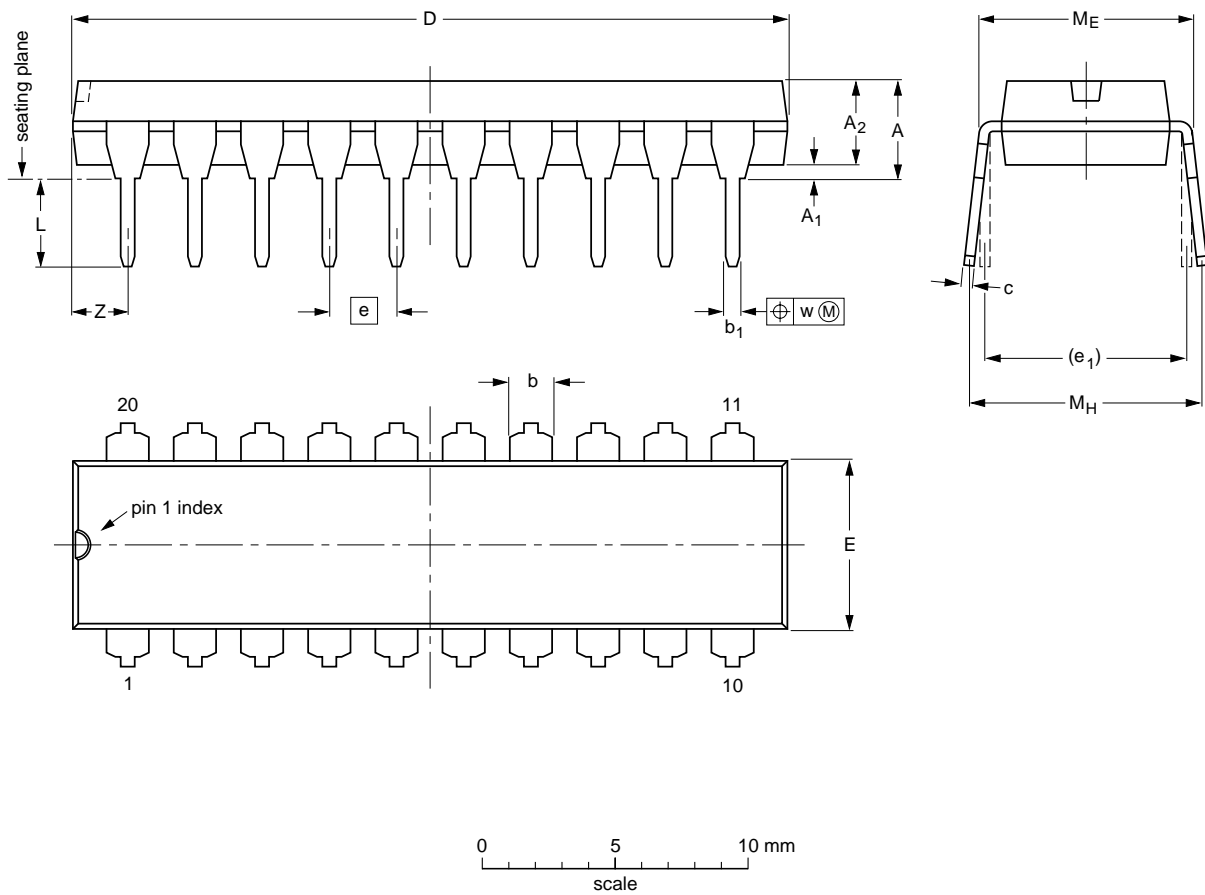
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PACKAGE OUTLINE

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

Hi-fi stereo audio processor; I<sup>2</sup>C-bus

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**SOLDERING****Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

**Soldering by dipping or by wave**

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact

with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

**Repairing soldered joints**

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**LIFE SUPPORT APPLICATIONS**

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