

FEATURES

- * 0.56-INCH (14.22-mm) DIGIT HEIGHT.
- * WIDE SUPPLY VOLTAGE OPERATION.
- * SERIAL DATA INPUT.
- * CONSTANT CURRENT DRIVERS.
- * CONTINUOUS BRIGHTNESS CONTROL.
- * SOLID STATE RELIABILITY-LONG OPERATION LIFE.
- * WIDE VIEWING ANGLE.
- * TTL COMPATIBLE.

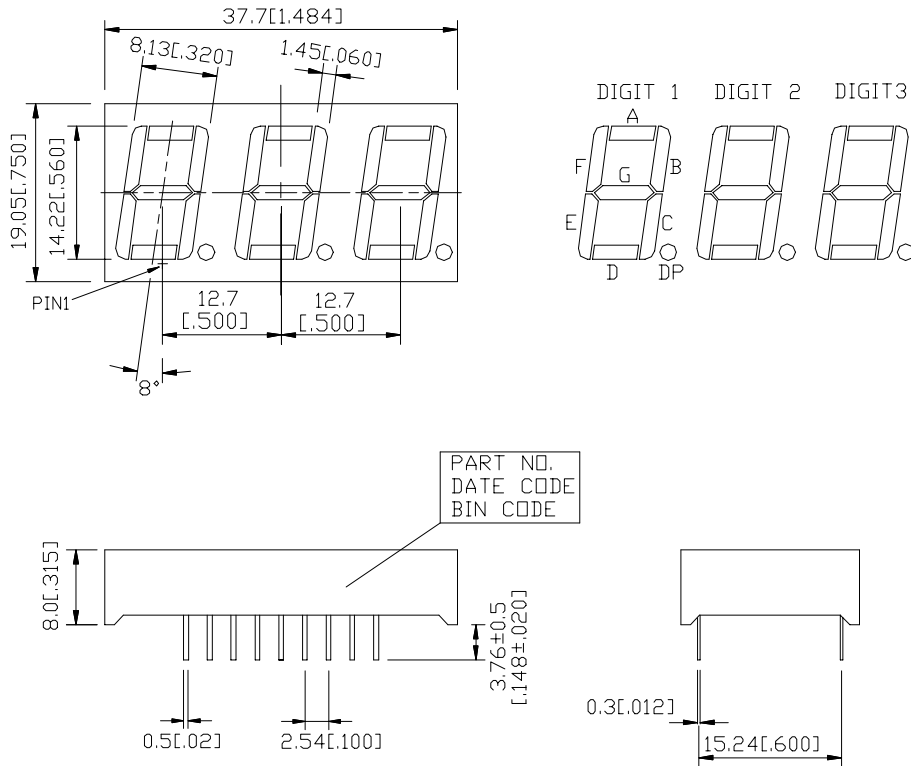
DESCRIPTION

The LTM-8522E is a 0.56-inch (14.22-mm) numeric display modules, and a built-in M5450 MOS integrated circuits. The integrated circuit contains serial data input, 35 bits shift register. 34 LED driver output and a brightness control. This device utilizes red orange LED chips, which are made from GaAsP on a transparent GaP substrate, and has a orange face and orange segments. The MOS integrated circuits are produced with N-channel silicon gate technology.

DEVICE

| PART NO. | DESCRIPTION |
|-----------------|--------------------|
| RED ORANGE | 3 Digit |
| LTM-8522E | Rt. Hand Decimal |

PACKAGE DIMENSIONS



NOTES: All dimensions are in millimeters. Tolerances are ± 0.25-mm (0.01“) unless otherwise noted.

PIN CONNECTION

| No. | CONNECTION |
|------------|-------------------|
| 1 | VSS |
| 2 | VLED |
| 3 | VLED |
| 4 | BIT 25 OUTPUT |
| 5 | BIT 26 OUTPUT |
| 6 | BIT 27 OUTPUT |
| 7 | BIT 28 OUTPUT |
| 8 | BIT 29 OUTPUT |
| 9 | BIT 30 OUTPUT |
| 10 | BIT 31 OUTPUT |
| 11 | BIT 32 OUTPUT |
| 12 | BIT 33 OUTPUT |
| 13 | BIT 34 OUTPUT |
| 14 | DATA ENABLE |
| 15 | DATA INPUT |
| 16 | CLOCK INPUT |
| 17 | VDD |
| 18 | BRT. CONTROL |

ABSOLUTE MAXIMUM RATING AT T_A=25°C

| PARAMETER | Symbol | Min. | Max. | UNIT |
|---|---------|------|------|------|
| Supply Voltage *1 | VDD | -0.3 | 12 | V |
| Input Voltage | VI | -0.3 | 12 | V |
| Off State Output Voltage | VO(off) | | 12 | V |
| LED Supply Voltage | VLED | 2.8 | 3.5 | V |
| Power Dissipation of IC *2 | PD(IC) | | 335 | mW |
| Supply Current | IDD | | 8.5 | mA |
| Operating Temperature Range | Top | -20 | +60 | °C |
| Storage Temperature Range | Tstg | -20 | +60 | °C |
| Solder Temperature 1/16 inch Below Seating Plane for 3 Seconds at 260°C | | | | |

RECOMMENDED OPERATING CONDITION AT T_A=25°C

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Condition |
|--------------------------|---------|--------|------|------|------|----------------------|
| Supply Voltage | VDD | 4.75 | | 11 | V | |
| Input Voltage | | | | | | |
| Logical "0" Level | | -0.3 | | 0.8 | V | ±10μA Input Bias |
| Logical "1" Level | VI | 2.2 | | VDD | V | 4.75V < VDD < 5.25V |
| Logical "1" Level | | VDD -2 | | VDD | V | VDD > 5.25V |
| Brightness Input Current | IB | 0 | | 0.75 | mA | |
| Brightness Input Voltage | VB | 3 | | 4.3 | V | Input Current=750 μA |
| Off State Voltage | VO(off) | | | 11 | V | |
| Output Sink Current | | | | | | |
| Segment Off | | | | 10 | μA | IB=0 μA |
| Segment On | | | 3 | | mA | IB=100 μA |
| | | | 6 | | mA | IB=200 μA |
| Input Clock Frequency | FCLOCK | 0 | | 0.5 | MHZ | |
| Output Matching | IO | | | ±20 | % | |

Note: Luminous intensity is measured with a light sensor and filter combination that approximates the CIE (Commision Internationale De L'Eclairage) eye-response curve.

ELECTRICAL/OPTICAL CHARACTERISTICS AT Ta=25°C

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITION |
|-----------------------------------|--------|------|------|------|------|----------------|
| Average Luminous Intensity | Iv | 800 | 2400 | | μcd | IB=0.4mA |
| Peak Emission Wavelength | λp | | 630 | | nm | IB=0.4mA |
| Spectral Line Half-Width | Δλ | | 40 | | nm | IB=0.4mA |
| Dominant Wavelength | λd | | 621 | | nm | IF=20mA |
| Luminous Intensity Matching Ratio | Iv-m | | | 2:1 | | IB=0.4mA |

FUNCTIONAL DESCRIPTION

Serial data transfer from the data source to the display driver is accomplished with 2 signals serial data and clock. Using a format of a leading “1” followed by the 35 data bits allow data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is completed, thus providing non multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time.

Brightness of display is determined by control the output current of LED display. A 1nF capacitor should be connected to brightness control, Pin 7 to prevent possible oscillations. The output current is typically 25 times greater than the current into Pin 7 which is set by an external variable resistor. There is an internal limiting resistor of 400 Ω nominal value.

Figure 1 shows the input data format. A start bit of logical “1” proceed the 35 bits of data. At the 36th clock, a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for master portion of the first register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers won’t clear. When power is first applied to the chip, an internal power ON, a reset signal is generated which reset all registers and all latches. The START bit and first clock return the chip on its normal operation. Bit 1 is the first following the start bit and it will appear on the segment A of the digit 1. A logical “1” at the input will turn on the appropriate LED. Figure 2 shows the timing relationship between data, clock, and DATA ENABLE. A max. clock frequency of 0.5 MHz is assumed.

FIGURE 1. INTERNAL BLOCK DIAGRAM

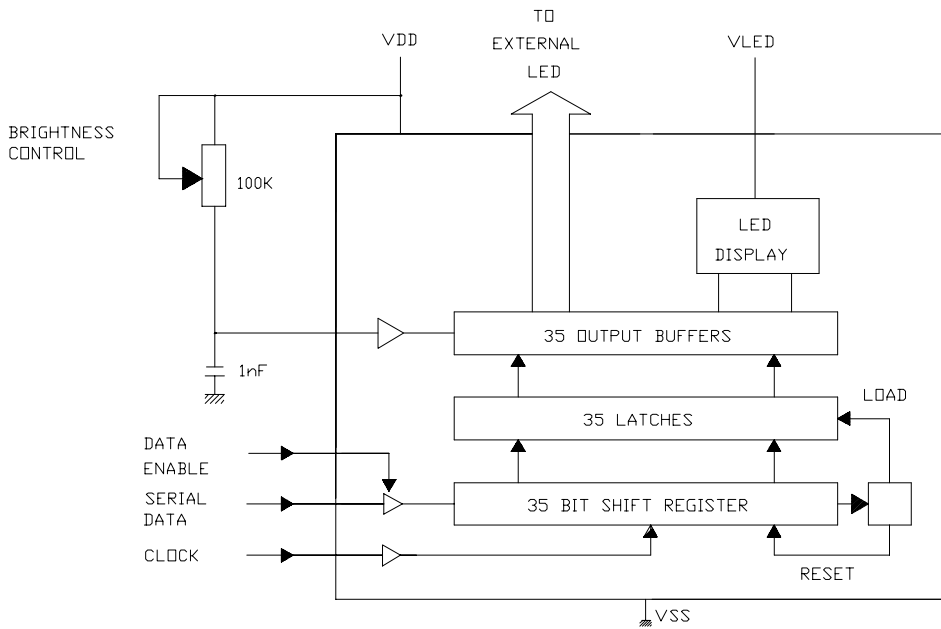


FIGURE 2. INPUT DATA FORMAT

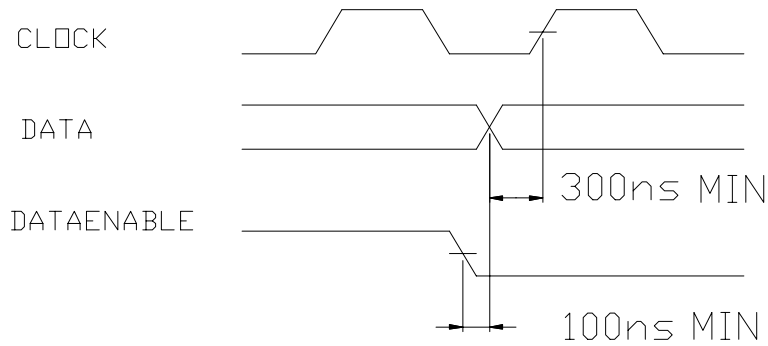


FIGURE 3. TIMING RELATIONSHIP

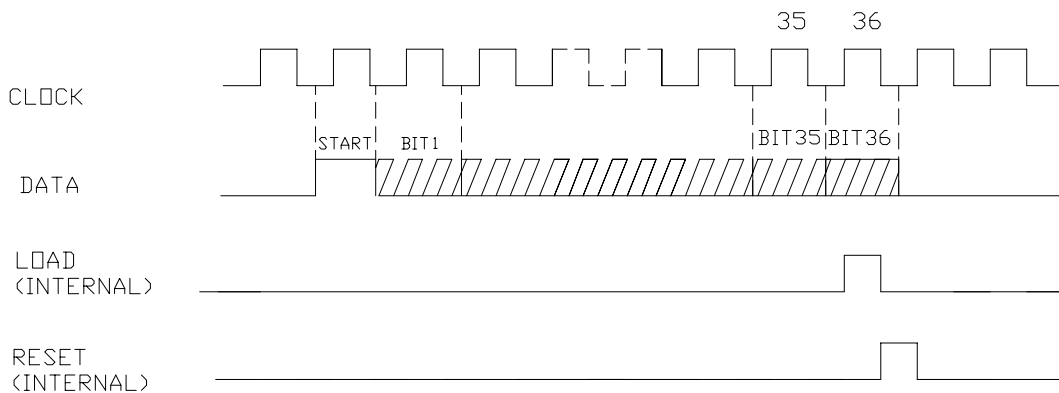


TABLE 1 SERIAL DATA INPUT SEQUENCE

| BIT | LTM-8522 | |
|-----|----------|---------|
| | DIGIT | SEGMENT |
| 1 | 1 | A |
| 2 | 1 | B |
| 3 | 1 | C |
| 4 | 1 | D |
| 5 | 1 | E |
| 6 | 1 | F |
| 7 | 1 | G |
| 8 | 1 | D.P. |
| 9 | 2 | A |
| 10 | 2 | B |
| 11 | 2 | C |
| 12 | 2 | D |
| 13 | 2 | E |
| 14 | 2 | F |
| 15 | 2 | G |
| 16 | 2 | D.P. |
| 17 | 3 | A |
| 18 | 3 | B |
| 19 | 3 | C |
| 20 | 3 | D |
| 21 | 3 | E |
| 22 | 3 | F |
| 23 | 3 | G |
| 24 | 3 | D.P. |
| 25 | | PIN 4 |
| 26 | | PIN 5 |
| 27 | | PIN 6 |
| 28 | | PIN 7 |
| 29 | | PIN 8 |
| 30 | | PIN 9 |
| 31 | | PIN 10 |
| 32 | | PIN 11 |
| 33 | | PIN 12 |
| 34 | | PIN 13 |

TYPICAL APPLICATION

