



AKD4550-E

Evaluation board Rev.0 for AK4550

GENERAL DESCRIPTION

AKD4550-E is an evaluation board for the portable digital audio 16bit A/D and D/A converter, AK4550. The AKD4550-E can evaluate A/D converter and D/A converter separately in addition to loopback mode (A/D → D/A). The A/D section can be evaluated by interfacing with AKM's DAC evaluation boards directly. The AKD4550 has the interface with AKM's ADC evaluation boards. Therefore, it's easy to evaluate the D/A section. The AKD4550-E also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ **Ordering guide**

AKD4550 -E --- Evaluation board for AK4550

FUNCTION

- **Compatible with 2 types of interface**
 - **Direct interface with AKM's A/D & D/A converter evaluation boards**
 - **DIT/DIR with optical input/output**

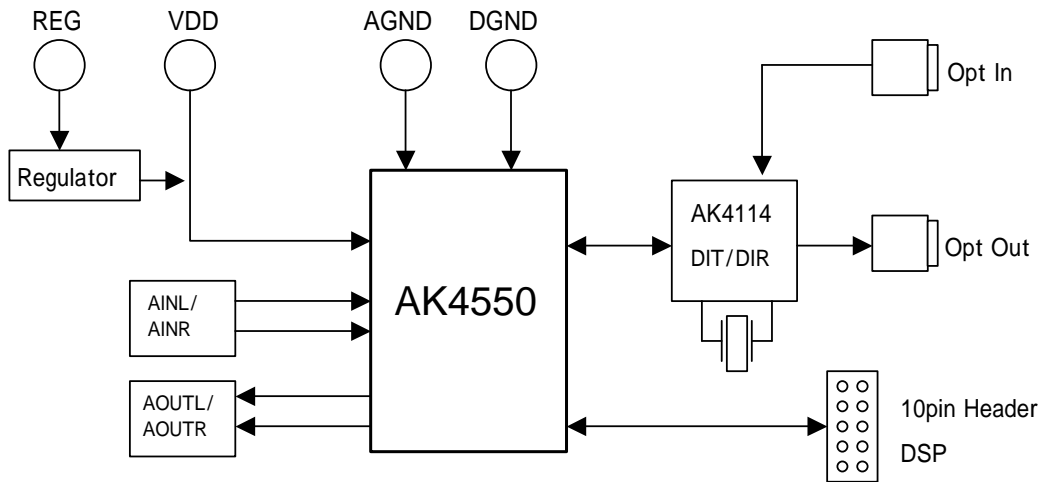


Figure 1. AKD4550-E Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

Evaluation Board Manual

■ Operation sequence

1) Set up the power supply lines.

[VDD] (Orange)	= 1.6 ~ 3.6V	: for VDD of AK4550
[REG] (Red)	= 5.0V	: for regulator
[AGND] (Black)	= 0V	: for analog ground (including VSS of AK4550)
[DGND] (Black)	= 0V	: for logic ground

Each supply line should be distributed from the power supply unit.

2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

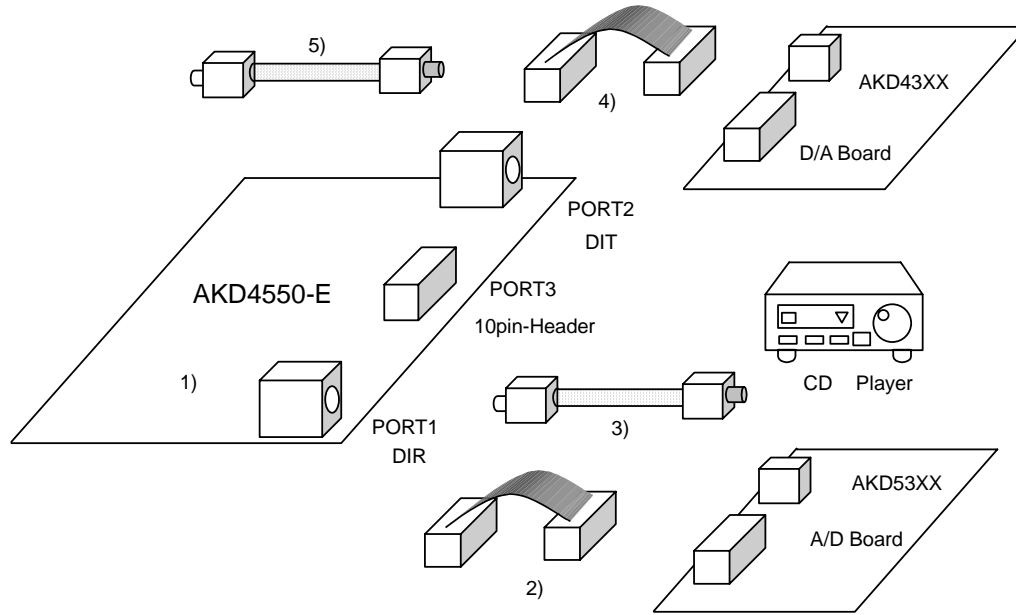
3) Power on.

The AK4550 should be reset once bringing SW2 (PDN) "OFF" upon power-up.

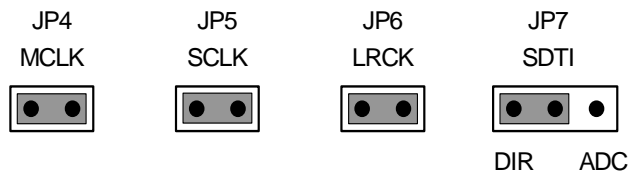
■ Evaluation mode

Applicable Evaluation Mode

- 1) Evaluation of loopback mode (default)
- 2) Evaluation of D/A using A/D converted data
- 3) Evaluation of D/A using DIR (Optical Link)
- 4) Evaluation of A/D using D/A converted data
- 5) Evaluation of A/D using DIT (Optical Link)
- 6) All interface signals including master clock are fed externally.

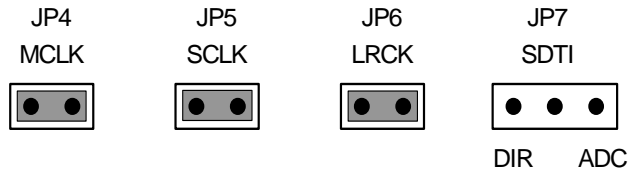


- 1) Evaluation of loopback mode. (default)
Nothing should be connected to PORT1/PORT3.



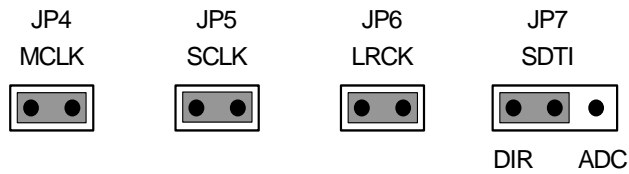
2) Evaluation of D/A using A/D converted data.

D/A part can be evaluated by connecting with AKM's A/D evaluation boards via PORT3.
Nothing should be connected to PORT1



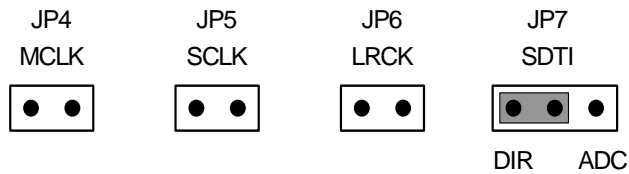
3) Evaluation of D/A using DIR. (Optical link)

PORT1 (TORX141) is used. DIR generates MCLK, SCLK, LRCK and SDATA from the received data through optical connector (TORX141). Used for the evaluation using CD test disk. Nothing should be connected to PORT2/PORT3.



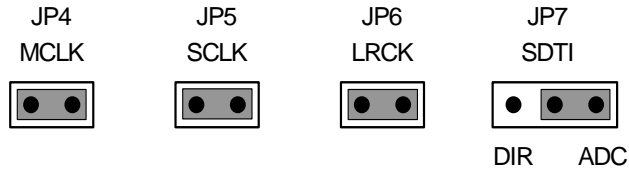
4) Evaluation of A/D using D/A converted data.

A/D part can be evaluated by connecting with AKM's D/A evaluation boards via PORT3.
Nothing should be connected to PORT1.



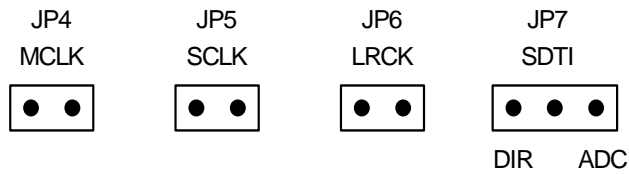
5) Evaluation of A/D using DIT. (Optical link)

PORT2 (TOTX141) is used. DIT generates audio bi-phase signal from received data and which is output through optical connector (TOTX141). It is possible to connect AKM's D/A converter evaluation boards on the digital-amplifier, which equips DIR input.



6) All interfacing signals (MCLK, SCLK, LRCK) are fed from the external circuit through PORT3.

Under the following set-up, all external signals needed for the AK4550 to operate could be fed through PORT3.



■ DIP switch set up

Upper-side is “ON” (“H”) and lower side is “OFF” (“L”).

[SW1]: Set up the AK4550 and AK4114.

SW No.	SW Name	Mode
1	DIF2, 0	AK4550 and AK4114 Audio Format Setting Always OFF.
2	DEM1	Set up the de-emphasis of AK4550 (See table 2)
3	DEM0	
4	NC	No use

Table 1. DIPswitch set-up of AK4114

DEM1 (SW1-#2)	DEM0 (SW1-#3)	Mode
OFF	OFF	44.1kHz
OFF	ON	OFF
ON	OFF	48kHz
ON	ON	32kHz

Table 2. DIPswitch set up of de-emphasis

■ Other jumper pins set up

[JP1] (GND): Connection between AGND and DGND
open: Both grounds are separated on board. <default>
short: Both grounds are connected on board.

[JP2] (REG): Select to regulator
open: On-board regulator is not used. <default>
short: On-board regulator is used. (The connector "VDD" can be open.)

[JP3] (PWR): Pull up power supply select for SDTO.
VDD: Connected to VDD of AK4550. <default>
D3V: Supplied from regulator (3V).

■ The function of the toggle SW.

Upper-side is "ON" and lower side is "OFF".

[SW2] (PDN): Resets the AK4550 and AK4114. Keep "ON" during normal operation.

■ Indication for LED

[LED1] (ERF): Monitor INT0 pin of the AK4114. LED turns on when some error has occurred to AK4114.

■ Input Circuit

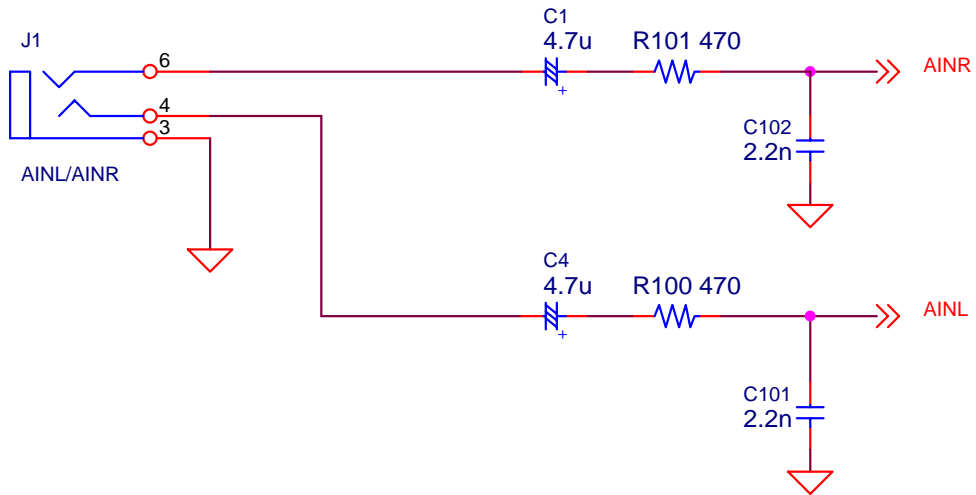


Figure 2. Input circuit on board

■ Output Circuit

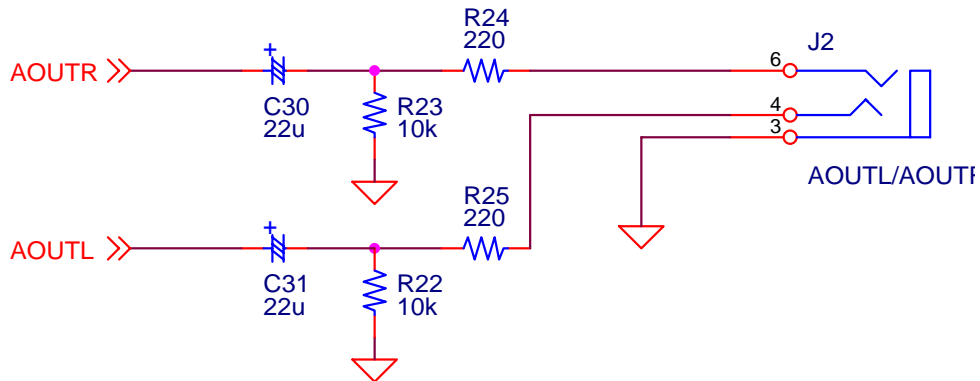


Figure 3. Output circuit on board

* AKM assumes no responsibility for the trouble when using the circuit examples.

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit : Audio Precision, System two
- MCLK : 256fs
- SCLK : 64fs (ADC, DAC)
- fs : 44.1kHz
- Bit : 16bit
- Power Supply : VDD = 2.5V, 3.0V, 3.6V
- Interface : DIT/DIR
- Temperature : Room

1. ADC

(2) SCLK = 64fs

VDD	Parameter	Measured Filter	fs = 44.1kHz
2.5V	S/(N+D) (-0.5dBFS)	20kHz LPF	81.6 dB
	D-Range (-60dBFS)	20kLPF + A-weighted	89.7 dB
	S/N (0 data)	20kLPF + A-weighted	89.7 dB
3.0V	S/(N+D) (-0.5dBFS)	20kHz LPF	80.7 dB
	D-Range (-60dBFS)	20kLPF + A-weighted	90.9 dB
	S/N (0 data)	20kLPF + A-weighted	90.9 dB
3.6V	S/(N+D) (-0.5dBFS)	20kHz LPF	79.6 dB
	D-Range (-60dBFS)	20kLPF + A-weighted	92.0 dB
	S/N (0 data)	20kLPF + A-weighted	92.0 dB

2. DAC

(1) SCLK = 64fs

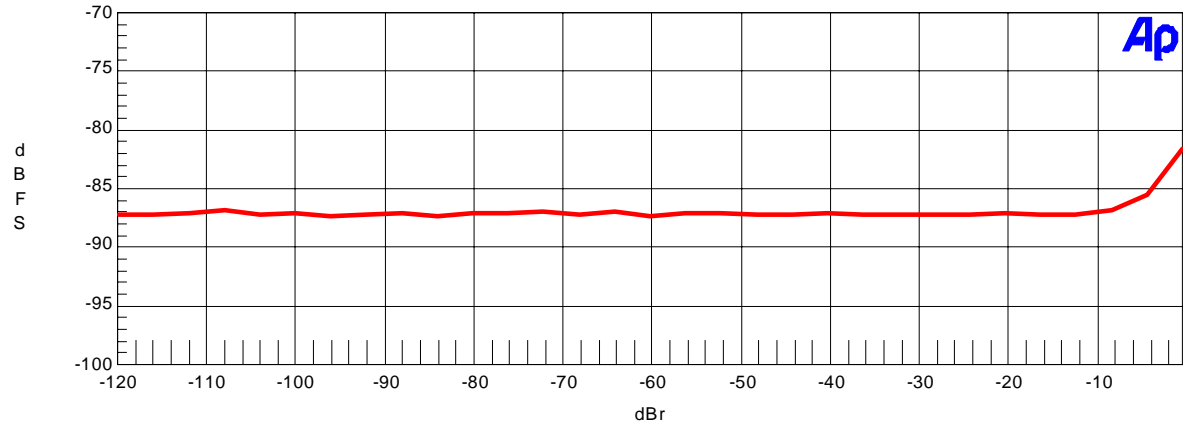
VDD	Parameter	Measured Filter	fs = 44.1kHz
2.5V	S/(N+D) (0dBFS)	20kHz LPF	87.5 dB
	D-Range (-60dBFS)	22kLPF + A-weighted	92.5 dB
	S/N (0 data)	22kLPF + A-weighted	93.2 dB
3.0V	S/(N+D) (0dBFS)	20kHz LPF	89.6 dB
	D-Range (-60dBFS)	22kLPF + A-weighted	93.8 dB
	S/N (0 data)	22kLPF + A-weighted	94.9 dB
3.6V	S/(N+D) (0dBFS)	20kHz LPF	91.3 dB
	D-Range (-60dBFS)	22kLPF + A-weighted	95.2 dB
	S/N (0 data)	22kLPF + A-weighted	96.6 dB

3.Graph

(1) ADC

AKM

AK4550 Rev.B ADC THD+N vs Input Level
 VDD=2.5V, SCLK=64fs, fs=44.1kHz

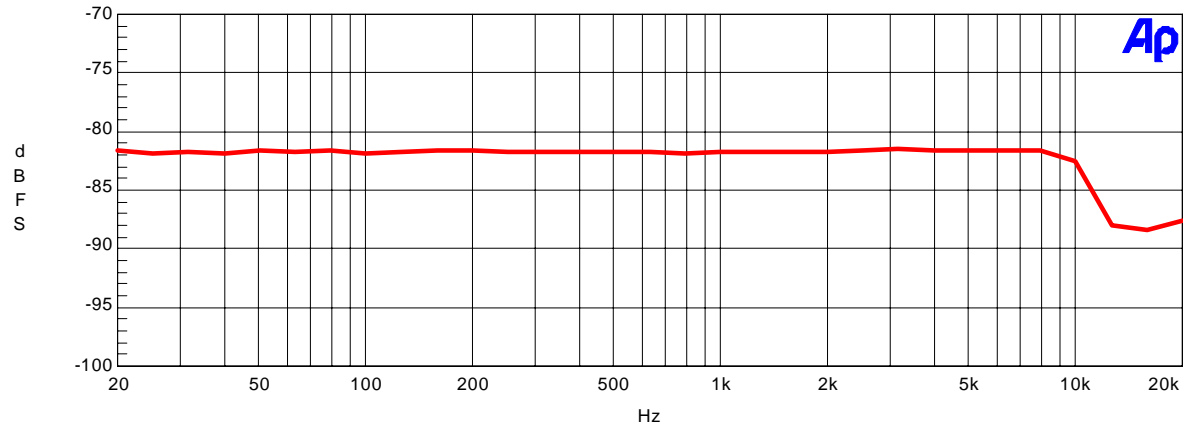


Color	Line Style	Thick	Data	Axis
Red	Solid	3	DSP Audio Anlr.TH+D+N Ampl	Left

last.at2

AKM

AK4550 Rev.B ADC THD+N vs Input Frequency
 VDD=2.5V, SCLK=64fs, fs=44.1kHz

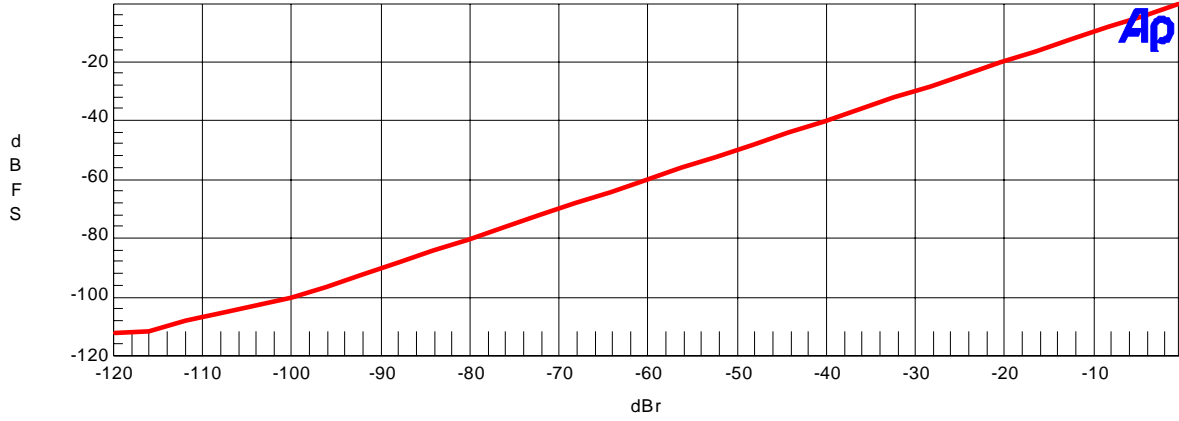


Color	Line Style	Thick	Data	Axis
Red	Solid	3	DSP Audio Anlr.TH+D+N Ampl	Left

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AKM

AK4550 Rev.B ADC Linearity
VDD=2.5V, SCLK=64fs, fs=44.1kHz

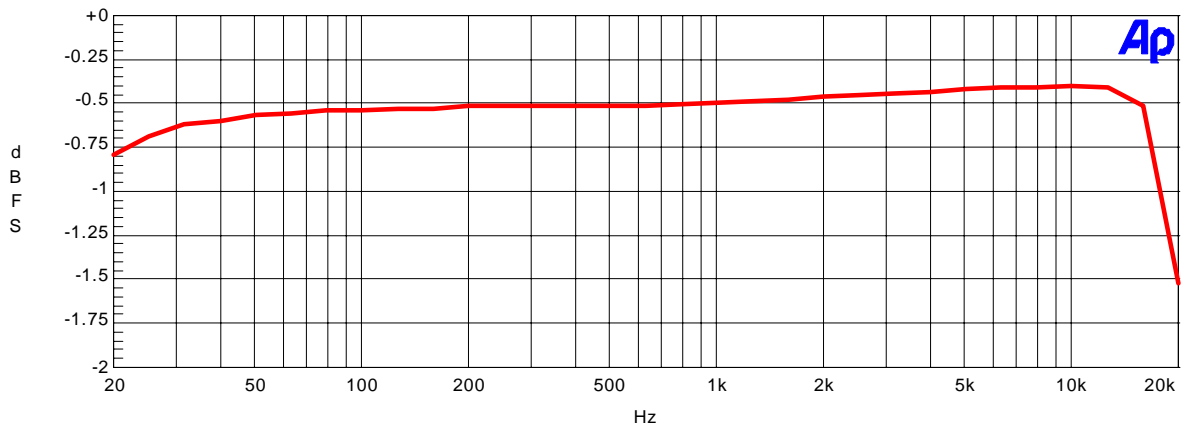


Color	Line Style	Thick	Data	Axis
Red	Solid	3	DSP Audio Anlr.Bandpass	Left

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AKM

AK4550 Rev.B ADC Frequency Response
VDD=2.5V, SCLK=64fs, fs=44.1kHz, Input=-0.5dBr

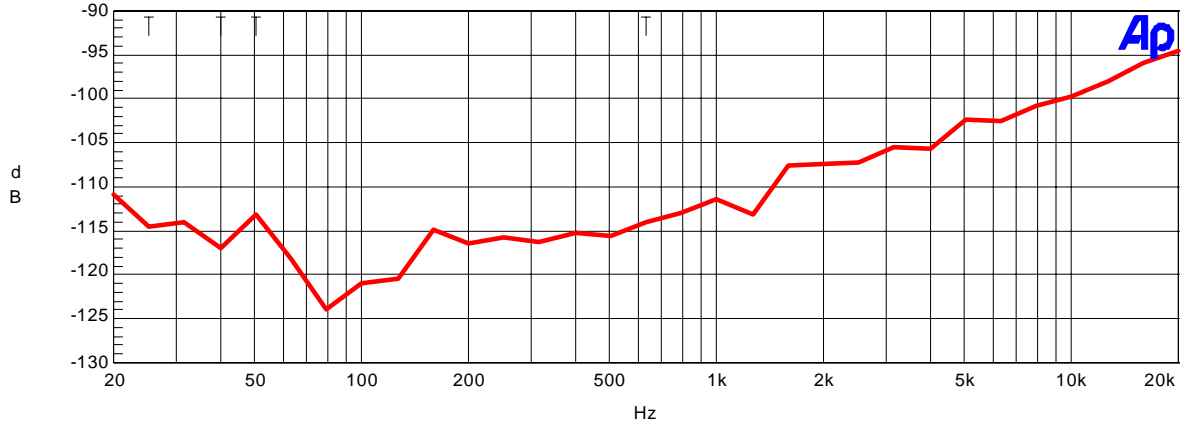


Color	Line Style	Thick	Data	Axis
Red	Solid	3	DSP Audio Anlr.Bandpass	Left

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AKM

AK4550 Rev.B ADC Crosstalk
 VDD=2.5V, SCLK=64fs, fs=44.1kHz

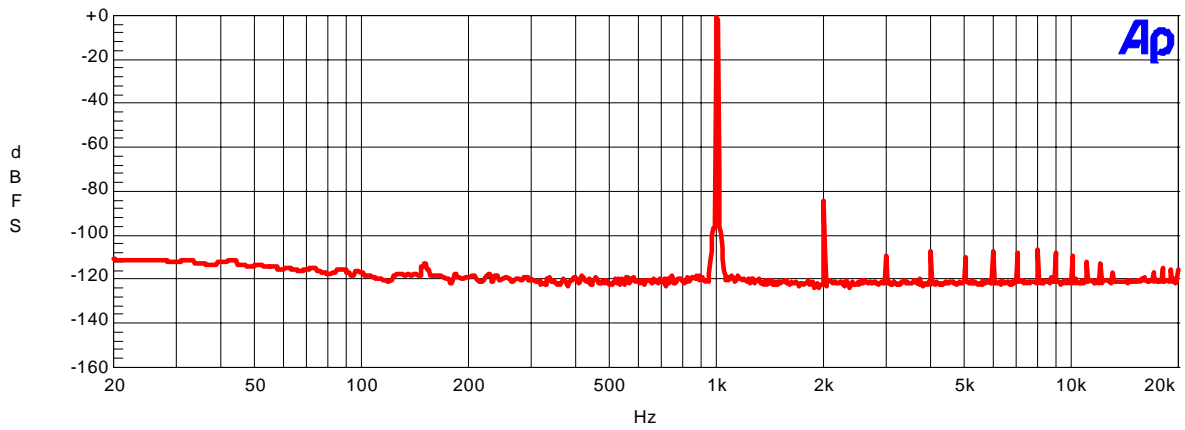


Color	Line Style	Thick	Data	Axis
Red	Solid	3	DSP Audio AnIr.Crosstalk	Left

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AKM

AK4550 Rev.B ADC FFT Plot
 VDD=2.5V, SCLK=64fs, fs=44.1kHz, Input=-0.5dB

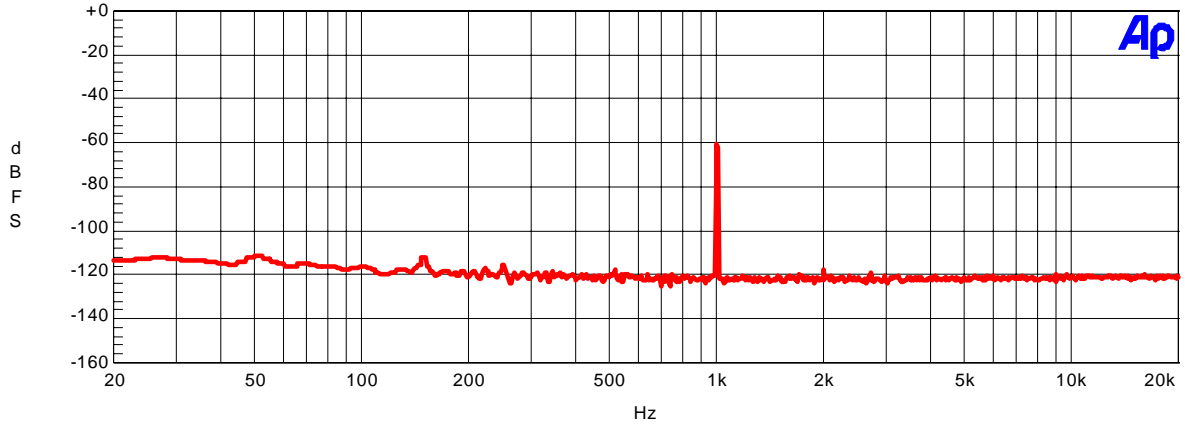


Color	Line Style	Thick	Data	Axis
Red	Solid	3	Fft.Ch.1 Ampl	Left

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AKM

AK4550 Rev.B ADC FFT Plot
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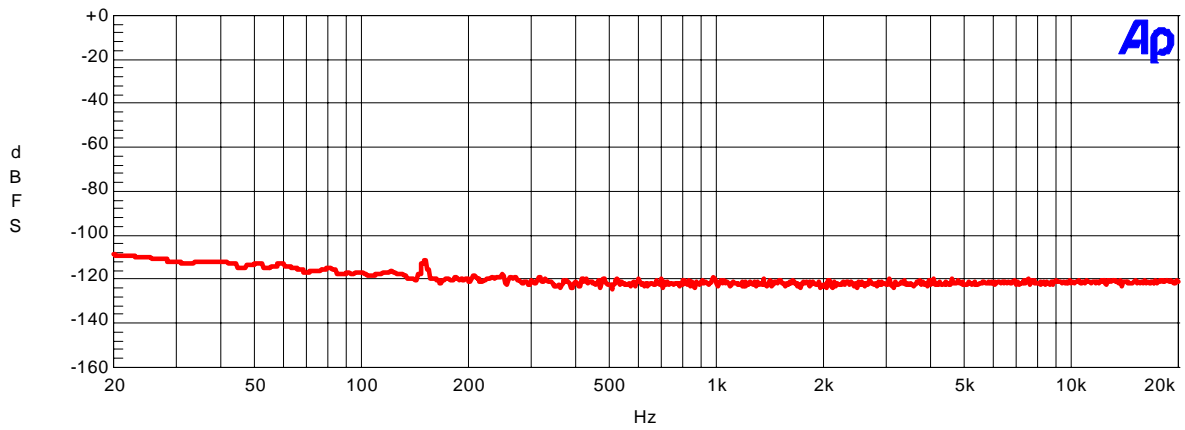


Color	Line Style	Thick	Data	Axis
Red	Solid	3	Fft.Ch.1 Ampl	Left

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AK4550 Rev.B ADC FFT Plot
VDD=2.5V, SCLK=64fs, fs=44.1kHz, Input=None



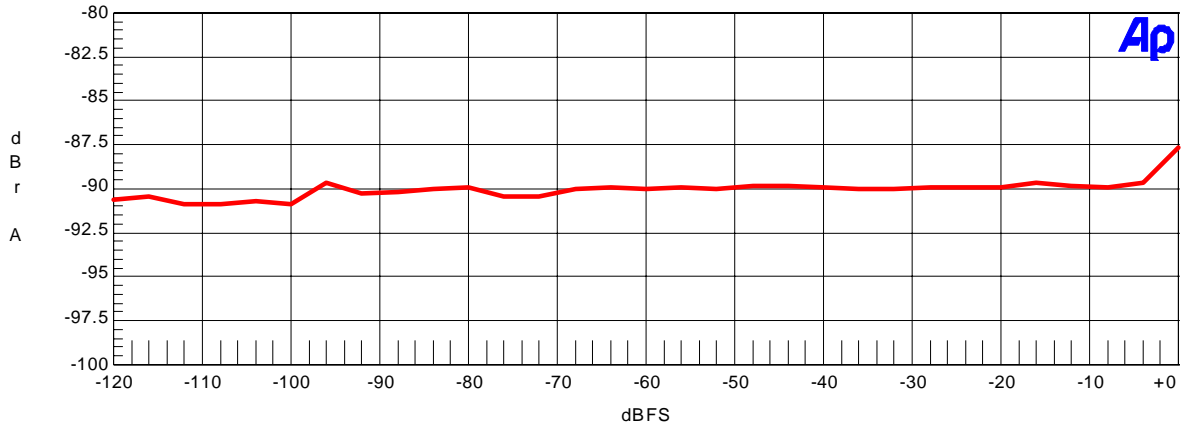
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(2) DAC

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AK4550 Rev.B DAC THD+N vs Input Level
VDD=2.5V, SCLK=64fs, fs=44.1kHz

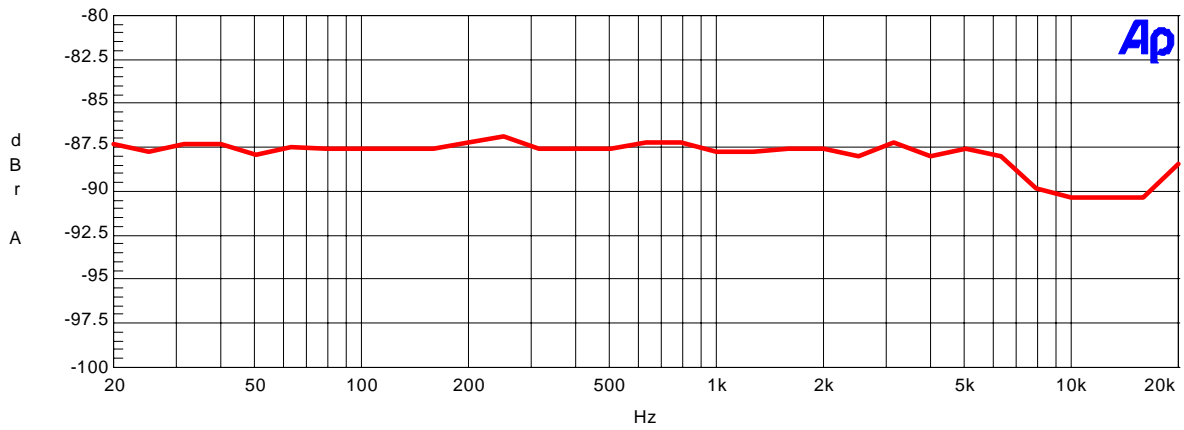


Color	Line Style	Thick	Data	Axis
Red	Solid	3	Anlr.TH+D+N Ampl	Left

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AKM

AK4550 Rev.B DAC THD+N vs Input Frequency
VDD=2.5V, SCLK=64fs, fs=44.1kHz

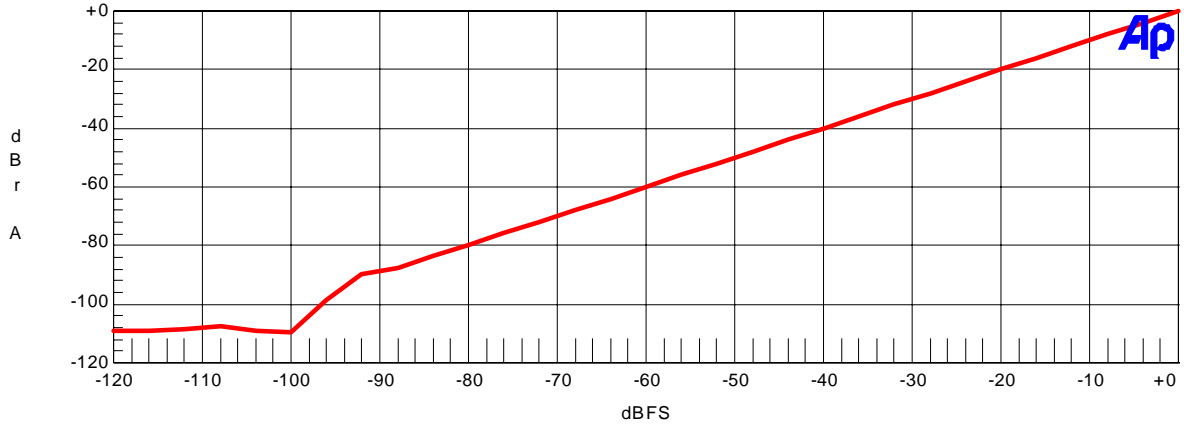


Color	Line Style	Thick	Data	Axis
Red	Solid	3	Anlr.TH+D+N Ampl	Left

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AKM

AK4550 Rev.B DAC Linearity
 VDD=2.5V, SCLK=64fs, fs=44.1kHz

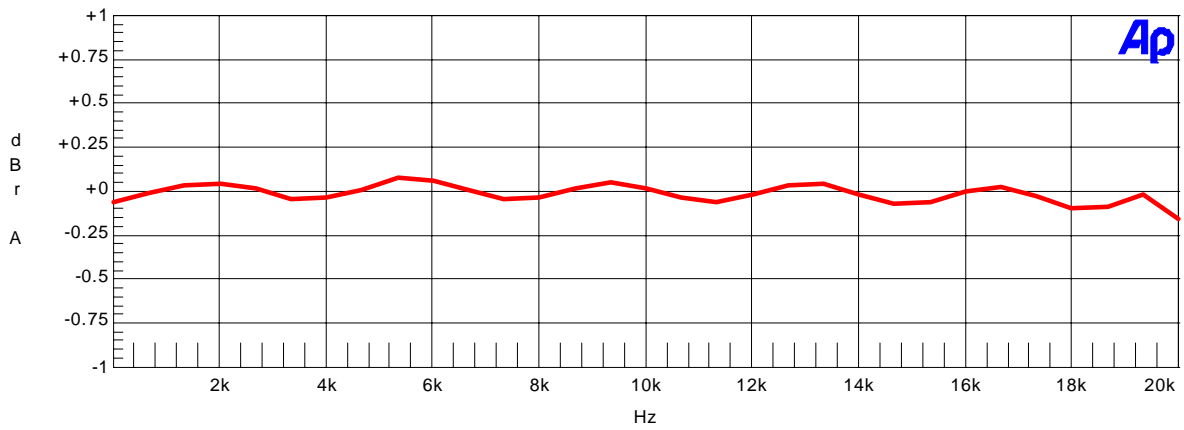


Color	Line Style	Thick	Data	Axis
Red	Solid	3	Anlr.Bandpass	Left

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AK4550 Rev.B DAC Frequency Response
 VDD=2.5V, SCLK=64fs, fs=44.1kHz, Input=0dBFS

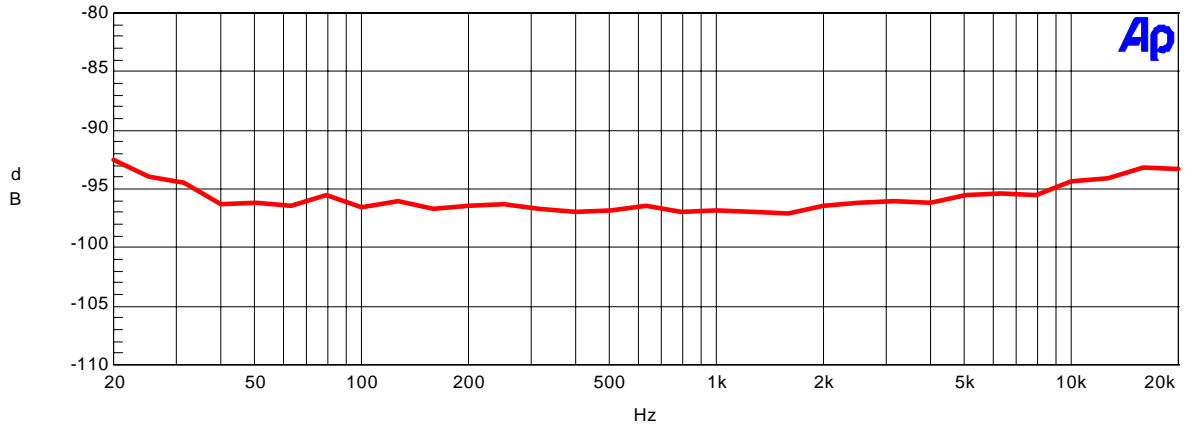


Color	Line Style	Thick	Data	Axis
Red	Solid	3	Anlr.Bandpass	Left

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AKM

AK4550 Rev.B DAC Crosstalk
VDD=2.5V, SCLK=64fs, fs=44.1kHz

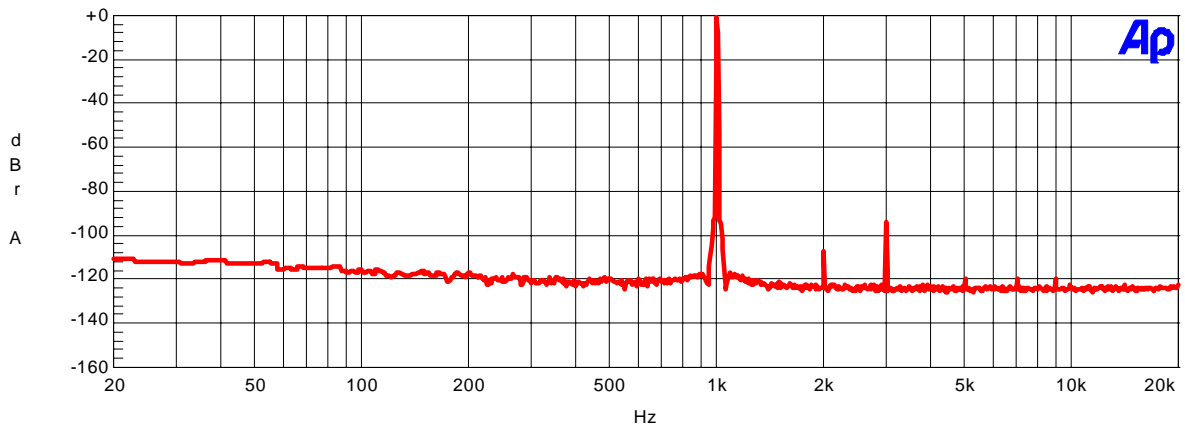


Color	Line Style	Thick	Data	Axis
Red	Solid	3	Anlr.Crosstalk	Left

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AK4550 Rev.B DAC FFT Plot
VDD=2.5V, SCLK=64fs, fs=44.1kHz, Input=0dBFS

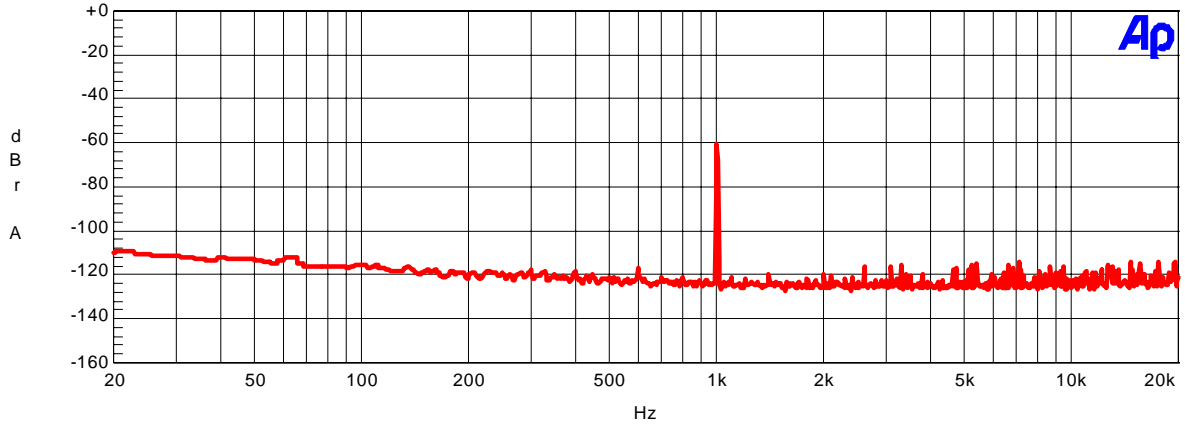


Color	Line Style	Thick	Data	Axis
Red	Solid	3	Fft.Ch.1 Ampl	Left

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AK4550 Rev.B DAC FFT Plot
VDD=2.5V, SCLK=64fs, fs=44.1kHz, Input=-60dBFS

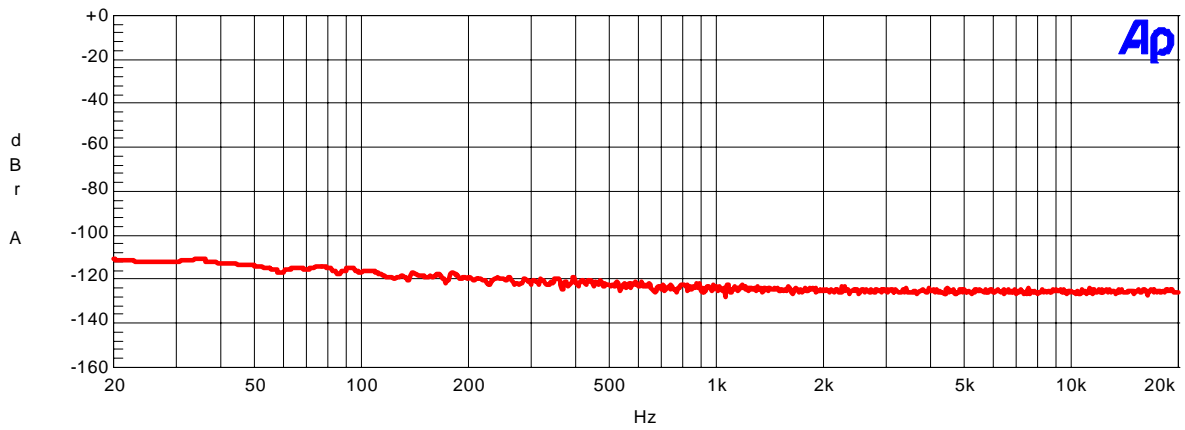


Color	Line Style	Thick	Data	Axis
Red	Solid	3	Fft.Ch.1 Ampl	Left

last.at2

AKM

AK4550 Rev.B DAC FFT Plot
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Color	Line Style	Thick	Data	Axis
Red	Solid	3	Fft.Ch.1 Ampl	Left

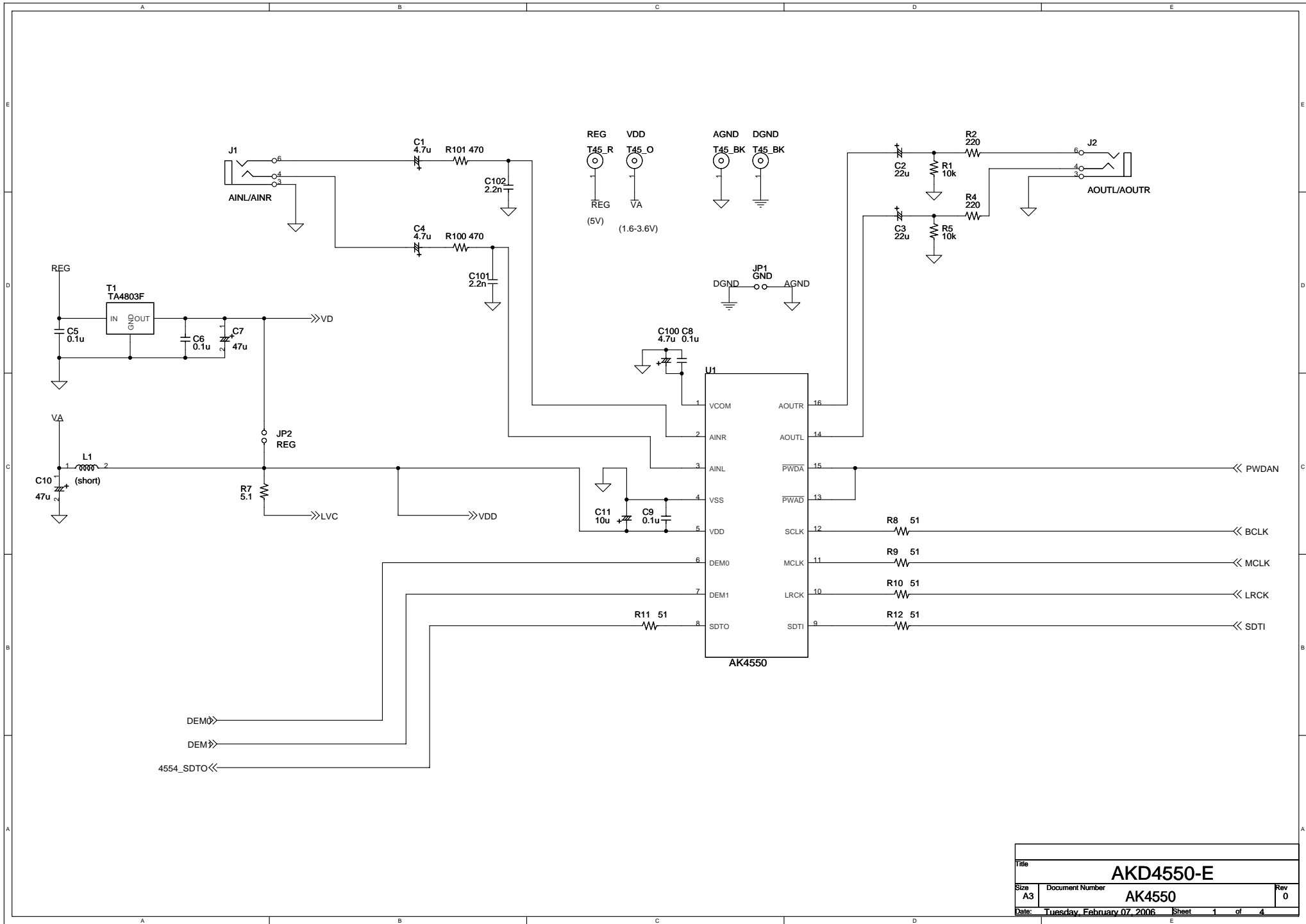
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Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
06/02/01	KM083000	0	First Edition	

IMPORTANT NOTICE

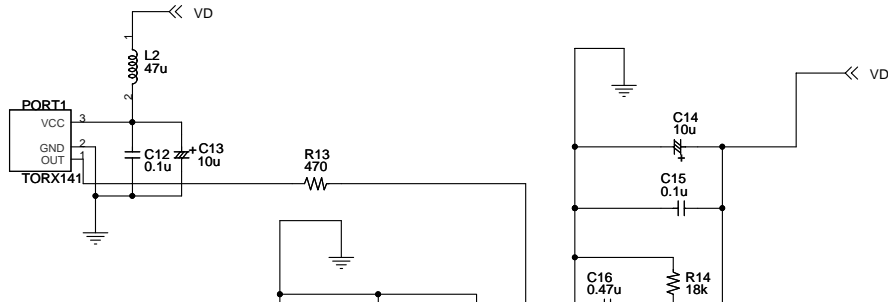
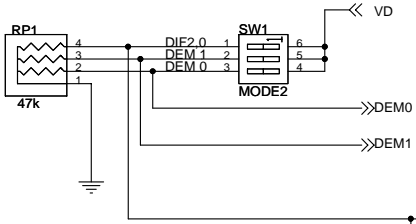
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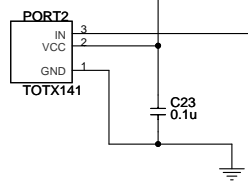
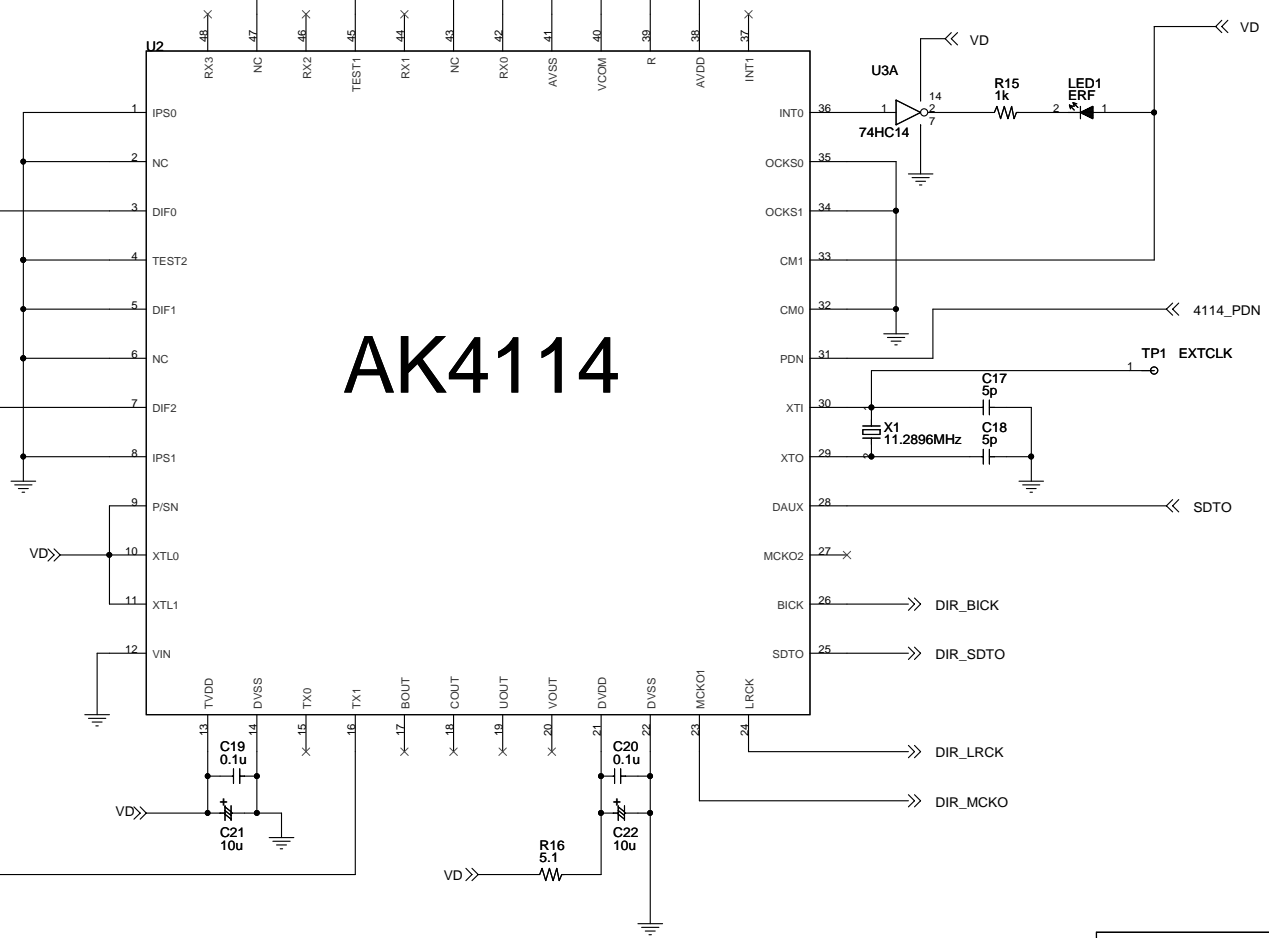
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DIP SW

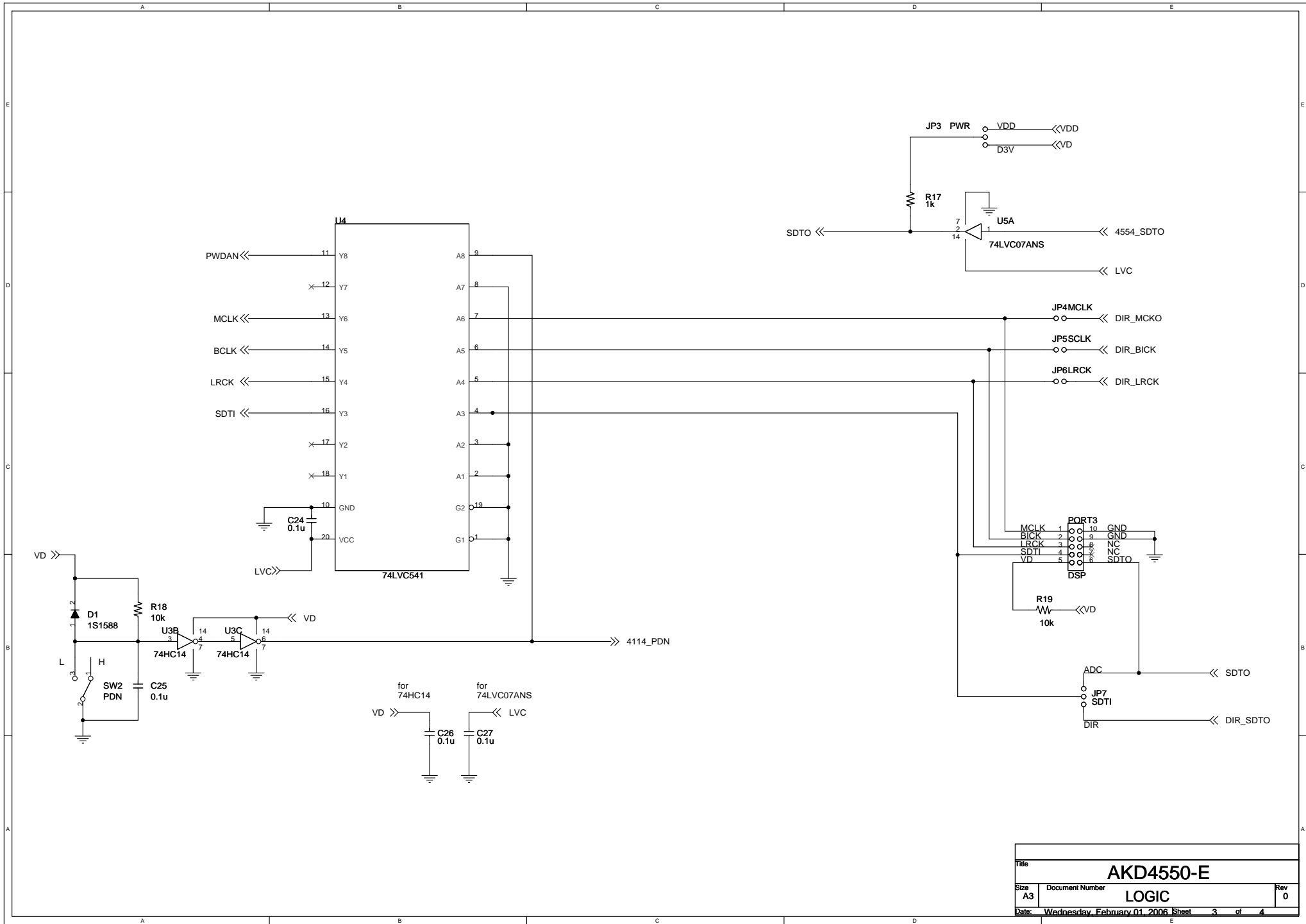
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		ON	ON	32k



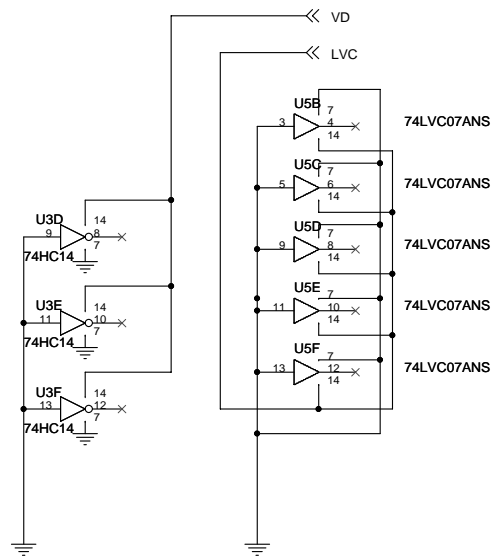
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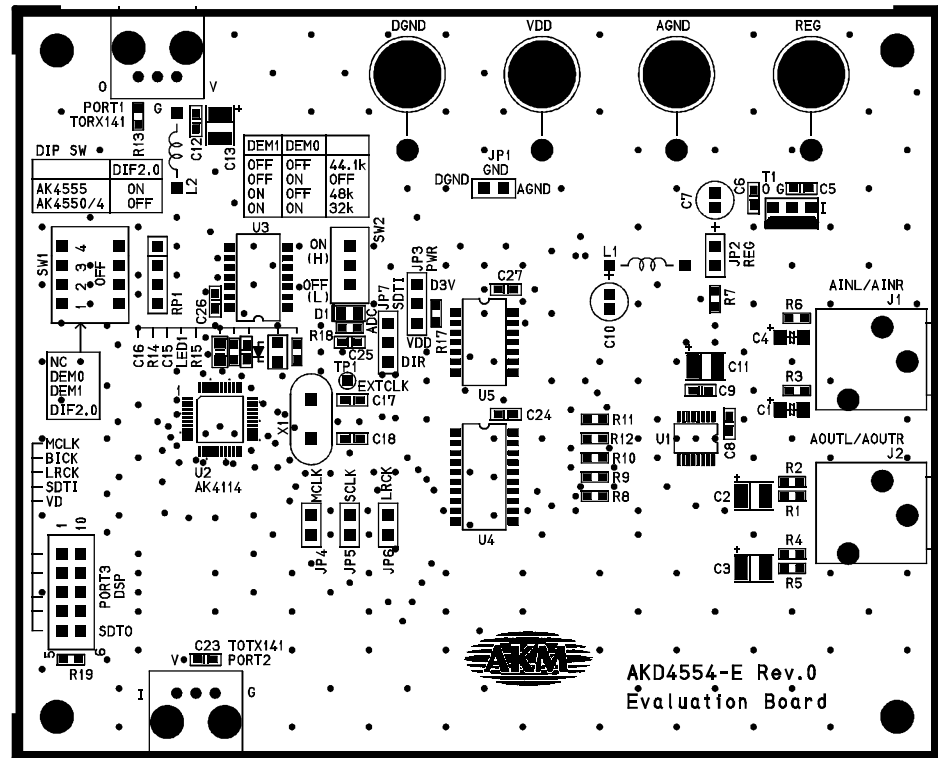
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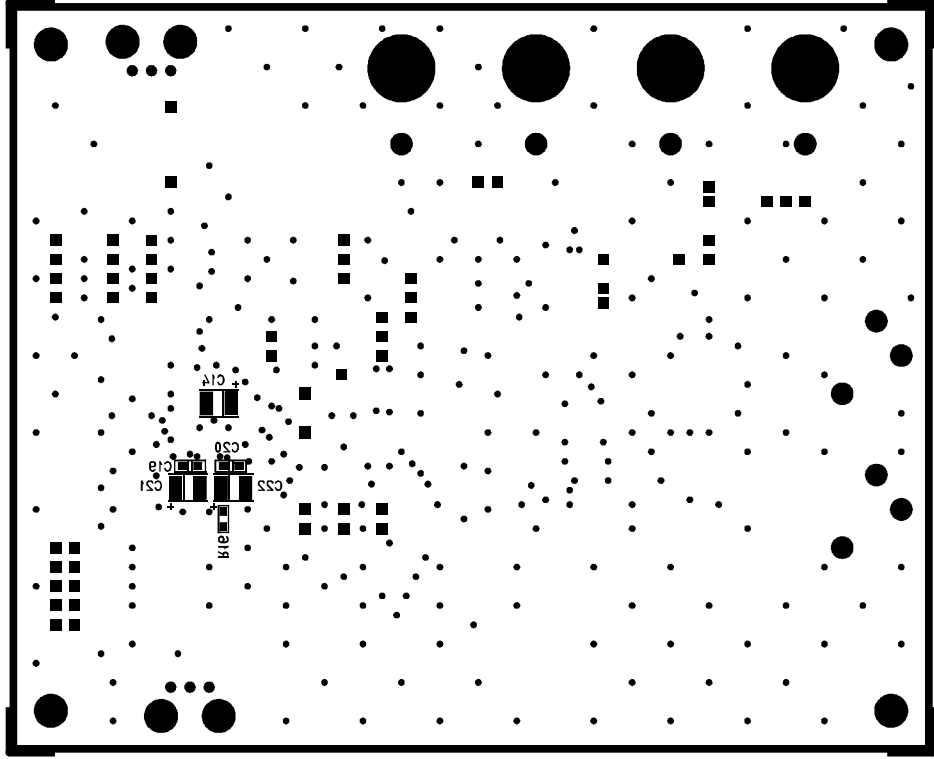
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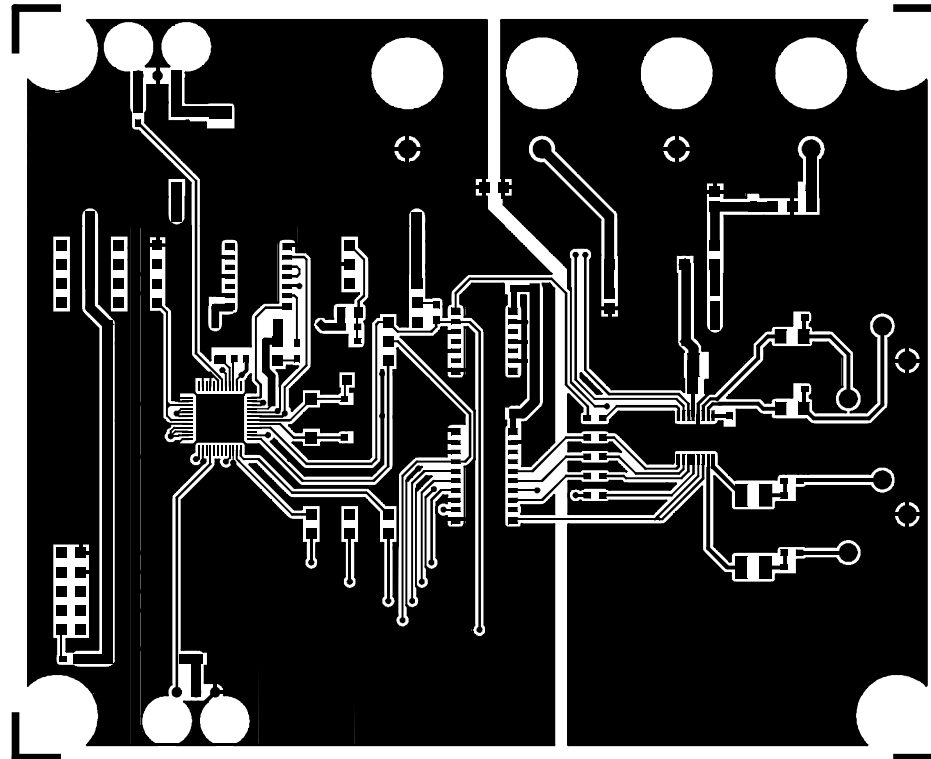
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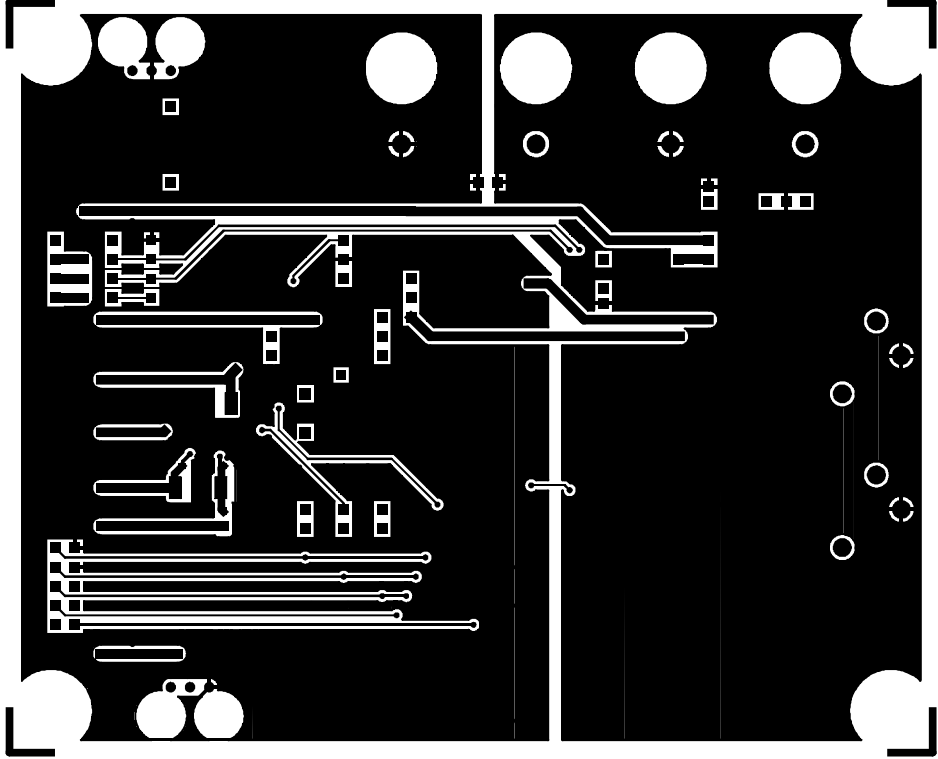
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AKD4554-E L1



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