mosaic

Mosaic Semiconductor Inc.

PUMA 2U8002

PUMA 2U8002-10/12/15/17/20/25

Issue 1.0 : March 1992

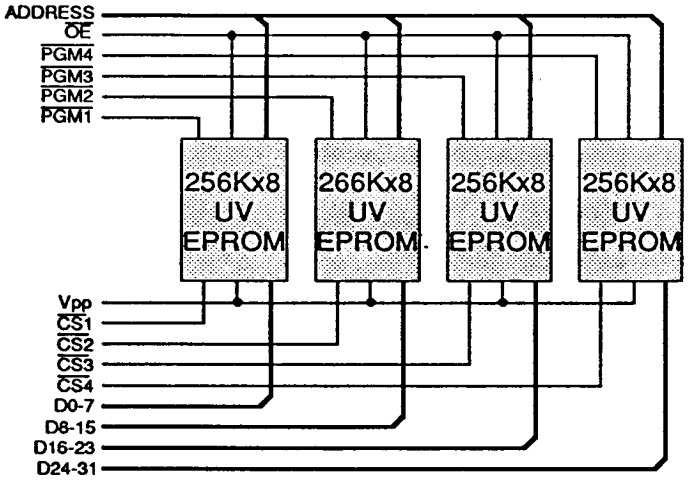
ADVANCE PRODUCT INFORMATION

8,388,608 bit CMOS UV Eraseable PROM

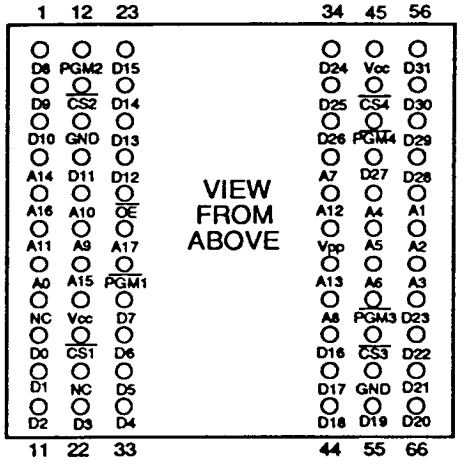
Features

Access times of 100/120/150/170/200/250 ns.
Pin grid array gives 2:1 improvement over DIL.
Package Suitable for Thermal Ladder Applications.
On board decoupling capacitors.
Configurable as 8 / 16 / 32 bit wide.
Operating Power 100 / 200 / 400 mW (typ)
Standby Power 1 mW (typ)
V_{PP} Voltage of 12.5V.
Complete Module Programming in 30 sec. (typ)
May be screened in accordance with MIL-STD-883D (not 100ns or 120ns modules - see ordering information)

Block Diagram



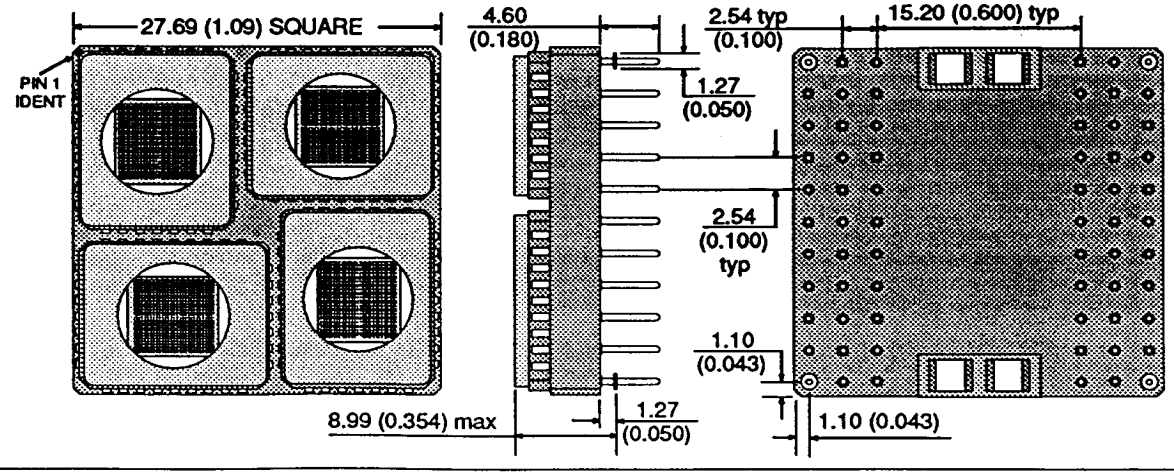
Pin Definition



Pin Functions

A0 - A17	Address Inputs
D0 - D31	Data Inputs/Outputs
$\overline{CS1\text{-}4}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{PGM1\text{-}4}$	Program Enable
NC	No Connect
V_{PP}	Programming Voltage
V_{CC}	Power (+5V)
GND	Ground

Package Details Dimensions in mm (inches).



Absolute Maximum Ratings (1)

Voltage on pins V_{PP} and A_9 (3)	V_{TPP}	-0.6V to +13.5	V	
Voltage on pin V_{CC}	V_{TCC}	-0.6V to + 7.0	V	
Voltage on any other pins (2)	V_T	-0.6V to $+V_{CC}+0.5$	V	
Power Dissipation	P_T	2	W	
Storage Temperature	T_{STG}	-65 to +150	°C	

Notes : (1) Stresses above those listed may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	-	$V_{CC}+0.5$	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Operating Temperature	T_A	0	-	70	°C (2U8002)
	T_{AI}	-40	-	85	°C (2U8002I)
	T_{AM}	-55	-	125	°C (2U8002M, MB)

DC Electrical Characteristics (T_A=-55°C to +125°C, V_{CC}=5V ± 10%)

Parameter		*Symbol*	*Test Condition*	*min*	*typ*(4)	*max*	*Unit*
Input Leakage Current	Address, $\overline{OE}$	I_{LI1}	V_{IN}=0V or V_{CC}, $V_{PP}=V_{PPL}$	-	-	4	µA
	Other Pins	I_{LI2}	V_{IN}=0V or V_{CC}	-	-	1	µA
Output Leakage Current		I_{LO}	V_{OUT}=0V or V_{CC}, 8 bit	-	-	20	µA
V_{PP} Read Current		I_{PP1}	$V_{PP}=V_{PPH}$	-	-	400	µA
V_{CC} Operating Supply Current	32 bit	I_{CC32}	$\overline{CS}=V_{IL}$ (1), I_{OUT}=0mA, f=5MHz(2)	-	80	240	mA
	16 bit	I_{CC16}	As above	-	42	122	mA
	8 bit	I_{CC8}	As above	-	23	63	mA
Standby Supply Current	TTL levels	I_{SB1}	$\overline{CS}=V_{IH}$ (1)	-	-	4	mA
	CMOS levels	I_{SB2}	$\overline{CS}=V_{CC}\pm0.3V$ (1)	-	80	400	µA
V_{PP} Voltage During Read Only		V_{PPL}		0	-	$V_{CC}+0.5$	V
Output Low Voltage		V_{OL}	I_{OL}=2.1mA.	-	-	0.45	V
Output High Voltage		V_{OH}	I_{OH}=-400µA.	2.4	-	-	V

Notes (1) $\overline{CS}$ above are accessed through $\overline{CS1\text{-}4}$. These inputs must be operated simultaneoulsy for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

(2) Maximum active current is the sum of I_{CC} and I_{PP}.

(3) **CAUTION: the PUMA 2U8002 must not be removed from or inserted into a socket when V_{CC} or V_{PP} is applied.**

(4) Typical values are measured at 25°C and nominal supply voltage.

Capacitance (V_{CC}=5V±10%, T_A=25°C)

Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	Address	C_{IN1}	V_{IN}=0V	38	51	pF
	$\overline{OE}$	C_{IN3}	V_{IN}=0V	33	46	pF
	$\overline{PGM1\text{-}4}$, $\overline{CS1\text{-}4}$	C_{IN3}	V_{IN}=0V	12	19	pF
I/O Capacitance	32 Bit Mode	$C_{I/O}$	$V_{I/O}$=0V	11	19	pF

Note: This parameter is calculated and not measured.

AC Test Conditions

*Input pulse levels: GND to 3.0V

*Input rise and fall times: 5 ns

*Input and Output timing reference levels: 1.5V

*Output load: 1 TTL gate + 100pF

*V_{CC}=5V±10%

Electrical Characteristics & Recommended AC Operating Conditions

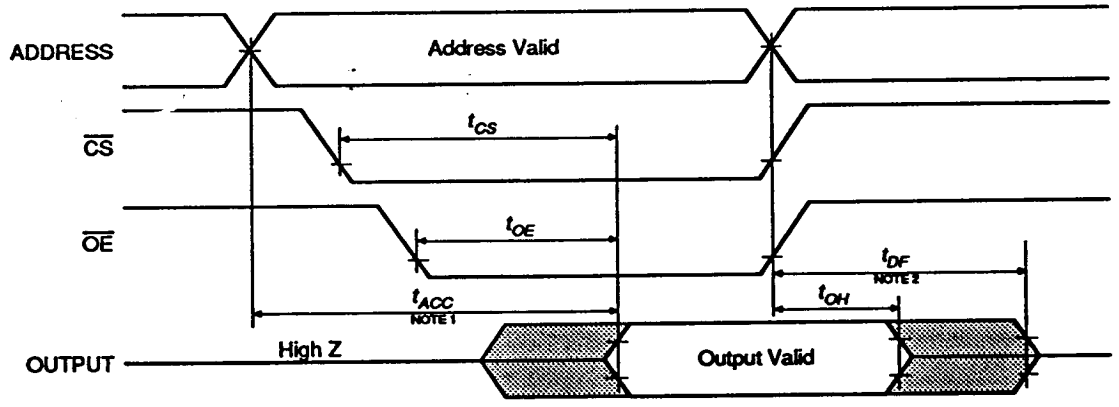
Read Cycle (1)

		-10		-12		-15		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Address to Output Delay	t_{ACC}	-	100	-	120	-	150	ns
Chip Select Access Time	t_{CE}	-	100	-	120	-	150	ns
Output Enable to Output Valid	t_{OE}	-	50	-	50	-	65	ns
Chip Deselect to O/P high Z (2)	t_{DF}	0	50	0	50	0	50	ns
Output Hold from Address Change	t_{OH}	0	-	0	-	0	-	ns

		-17		-20		-25		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Address to Output Delay	t_{ACC}	-	170	-	200	-	250	ns
Chip Select Access Time	t_{CE}	-	170	-	200	-	250	ns
Output Enable to Output Valid	t_{OE}	-	65	-	75	-	100	ns
Chip Deselect to O/P high Z (2)	t_{DF}	0	50	0	60	0	60	ns
Output Hold from Address Change	t_{OH}	0	-	0	-	0	-	ns

Notes (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
(2) This parameter is sampled, not 100% tested.
(3) See ordering information for speed and temperature restrictions.

Read Cycle Timing Waveform



Notes: (1) $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CS}$ without impact on t_{ACC}.
(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CS}$ whichever occurs first.

PROGRAMMING OPERATION

The following information is provided for design purposes only.

DC Electrical Characteristics (V_{CC}=6.25V±0.25V,V_{PP}=12.5V±0.5V,T_A=25°C±5°C)

Parameter		*Symbol*	*Test Condition*	*min*	*max*	*Unit*
Input Leakage Current	Address, $\overline{OE}$	I_{LI1}	$V_{CC}=V_{CC}$ max, V_{IN}=0V or V_{CC},$V_{PP}=V_{PPH}$	-	4	µA
	Other Pins	I_{LI2}	$V_{CC}=V_{CC}$ max, V_{IN}=0V or V_{CC},$V_{PP}=V_{PPH}$	-	1	µA
V_{PP} Program Current	32 bit	I_{PP32}	Program, $\overline{CS}=V_{IL}$, $\overline{OE}=V_{IH}$	-	120	mA
	16 bit	I_{PP16}	As above	-	60	mA
	8 bit	I_{PP8}	As above	-	30	mA
V_{CC} Operating Supply Current	32 bit	I_{CC32}	Program and Verify	-	200	mA
	16 bit	I_{CC16}	As above	-	102	mA
	8 bit	I_{CC8}	As above	-	53	mA
Standby Supply Current	TTL levels	I_{SB1}	$V_{CC}=V_{CC}$ max, $\overline{CS}=V_{IH}$(1)	-	4	mA
	CMOS levels	I_{SB2}	$V_{CC}=V_{CC}$ max, $\overline{CS}=V_{CC}$-0.2V(1)	-	400	µA
V_{CC} Supply Voltage During Program		V_{CC1}		6.0	6.5	V
V_{PP} Voltage During Program		V_{PPH}		12.5	13.0	V
Identifier Select Voltage		V_H		11.5	12.5	V
Output Low Voltage		V_{OL}	I_{OL}=2.1mA.	-	0.45	V
Output High Voltage		V_{OH}	I_{OH}=-400µA.	2.4	-	V

Notes (1) CS above are accessed through $\overline{CS1\text{-}4}$. These inputs must be operated simultaneoulsy for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

(2) V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

(3) A 0.1µF or greater capacitor is required between V_{PP} and GND to suppress voltage transients.

(4) **CAUTION: the PUMA 2U8002 must not be removed from or inserted into a socket when V_{CC} or V_{PP} is applied.**

(3) Programming characteristics are sampled but not 100% tested at worst case conditions.

Operating Modes

This table shows the inputs required to control the operating modes of the EPROMs on the PUMA 2U8002.

MODE		$\overline{CS}$	$\overline{OE}$	$\overline{PGM}$	A_0	A_9	V_{PP}	*OUTPUTS*
Read		V_{IL}	V_{IL}	X	X	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	X	High Z
Standby		V_{IH}	X	X	X	X	X	High Z
Program		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	High Z
Identifier (NOTE 1)	Manufacturer	V_{IL}	V_{IL}	X	V_{IL}	V_H	X	01_H
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	X	97_H

V_H=12.0V±0.5V
X=V_{IH} or V_{IL}
A1-A8=A10-A16=VIL

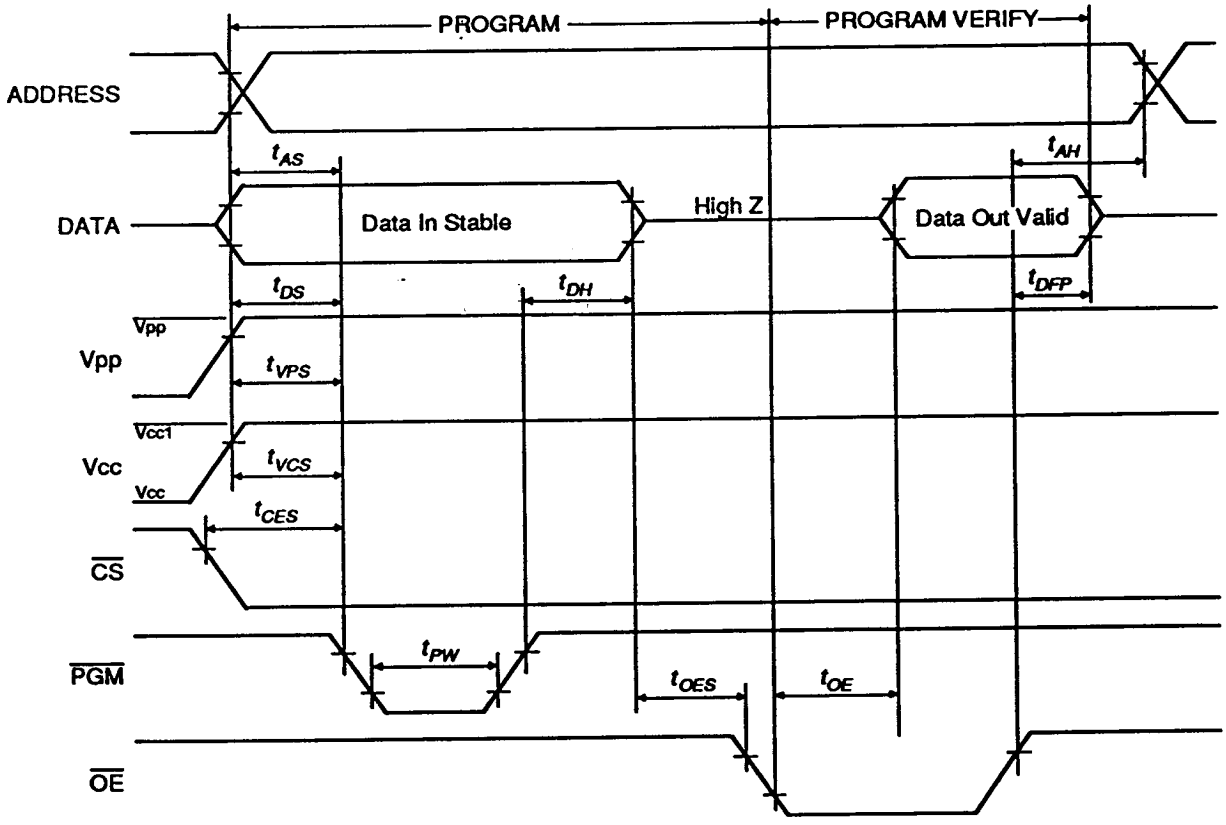
Notes (1) A1 - A8 = A10 - A17 = V_{IL}

(2) $\overline{CS}$ is accessed through $\overline{CS1\text{-}4}$, and $\overline{PGM}$ is accessed through $\overline{PGM1\text{-}4}$. For correct operation, $\overline{CS1\text{-}4}$ must operate simultaneously for 32 bit operation, in pairs for 16 bit operation, or singly for 8 bit operation. $\overline{PGM1\text{-}4}$ must also be operated in the same manner.

Programming Timing Characteristics

Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Address Setup Time	t_{AS}	2	-	-	µs
$\overline{OE}$ Setup Time	t_{OES}	2	-	-	µs
Data Setup Time	t_{DS}	2	-	-	µs
Address Hold Time	t_{AH}	0	-	-	µs
Data Hold Time	t_{DH}	2	-	-	µs
$\overline{OE}$ High to Output Float Delay	t_{DFP}	0	-	130	ns
V_{PP} Setup Time	t_{VPS}	2	-	-	µs
$\overline{PGM}$ Initial Pulse Width	t_{PW}	95	-	105	µs
V_{CC} Setup Time	t_{VCS}	2	-	-	µs
$\overline{CS}$ Setup Time	t_{CES}	2	-	-	µs
Data Valid from $\overline{OE}$	t_{OE}	-	-	150	ns

Programming Cycle Timing Waveform



High Performance Programming Algorithm

The PUMA2U8002 can be programmed using the alogorithm shown here. This allows faster programming times without stressing the device or causing deterioration in Data Retention Time. Each of the four devices used on this module is an AMD Am27C020; this information, together with the device identifier code, should allow the correct programming alogorithm to be selected automatically.

Although the flow chart specifically refers to a single EPROM, all four devices on the PUMA tile can be programmed simultaneously in 32 bit mode, in pairs in 16 bit mode or singly in 8 bit mode. Obviously 32 bit mode is potentially the fastest programming time, but this makes greater demands on the V_{PP} Supply Current as shown on the Programming Operation DC Characteristics on page 4.

Programming

Upon delivery, or after each erasure, the PUMA 2U8002 has all 8,388,608 bits in the ONE or HIGH state. ZEROs are loaded into the devices through the procedure of programming.

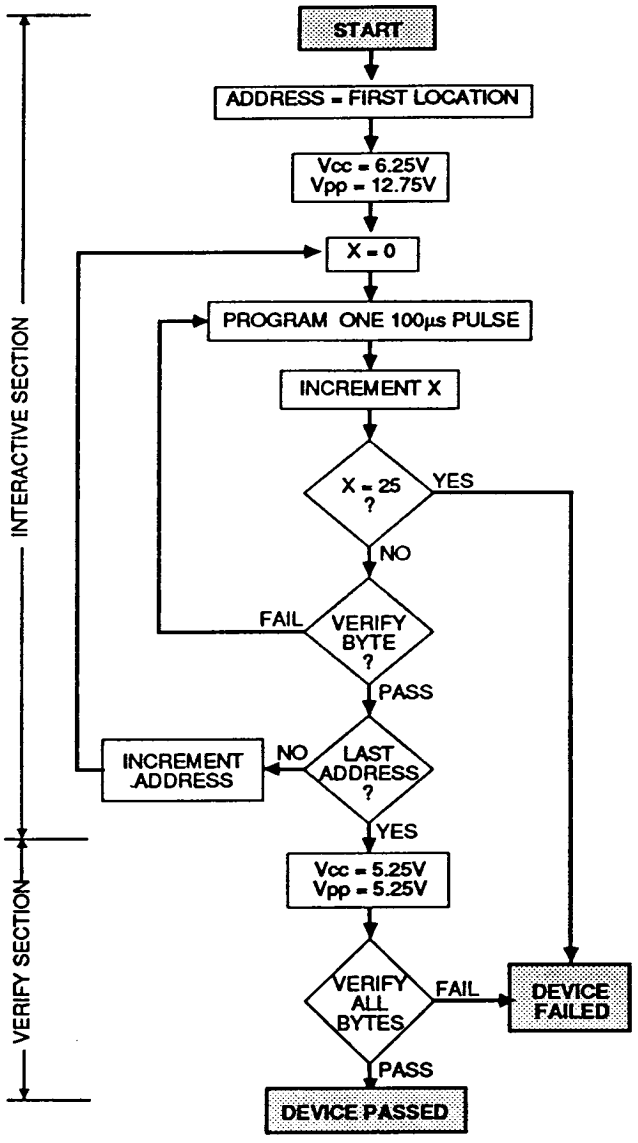
This mode is entered when 12.75V±0.25V is applied to the V_{PP} pin, $\overline{CS}$ and $\overline{PGM}$ are at V_{IL} and $\overline{OE}$ is at V_{IH}, as shown on the Table on page 2. Data may be applied in 8, 16 or 32 bits in parallel depending on how $\overline{CS1\text{-}4}$ and $\overline{PGM1\text{-}4}$ are controlled.

The algorithm reduces programming time by using 100µs pulses followed by byte verification to determine if the byte has been successfully programmed. If the data does not verify, up to 25 such pulses can be applied, after which, if verification fails, programming stops. This proccess is repeated for each memory location within the PUMA 2U8002.

This algorithm programs at V_{CC}=6.25V in order to ensure that each EPROM bit is programmed to a sufficiently high threshold voltage. After programming is complete, all bytes are compared with the original data with V_{CC}=5.25V.

In order to overcome the voltage drop caused by the inductive effects of the printed circuit board on which the PUMA 2U8002 module is used, it is recommended that a 4.7µF electrolytic capacitor is used between V_{CC} and GND for every two PUMA modules. This capacitor should be placed close to the point where the power supply is routed to the UV EPROM array.

PROGRAMMING ALGORITHM



NOTE: THE ALGORITHM SHOWN HERE MUST BE USED TO ENSURE CORRECT PROGRAMMING OF THE PUMA 2U8002. THIS MAXIMIZES THE DATA RETENTION TIME OF THE UV EPROMS AND DOES NOT STRESS THE MEMORY CELL.

DEVICE IDENTIFIER MODE

The device identifier mode allows the reading out of a binary code from an EPROM which identify its manufacturer and specific type. It is intended to be used to automatically match the device to be programmed with the correct algorithm. This mode operates over the 25°C±5°C temperature range.

In order to activate this mode 12.0V±0.5V must be placed onto address line A9, after which two identifier bytes may be read by toggling A0 from V_{IL} to V_{IH}. All other address lines are held at V_{IL} during this sequence.

The manufacturer code is accessed with A0=V_{IL} and the device code with A0=V_{IH}; the values for these codes are given in the Operating Mode Table on page 2. Note that all identifiers for manufacturer and device codes will possess odd parity, with D7 defined as the parity bit.

ERASE

Complete erasure of the devices used on the PUMA 2U8002 is performed by exposure to an ultraviolet light source giving a dosage of 15WS/cm². This dosage can be obtained by using an ultraviolet lamp with a wavelength of 2537 Å at a minimum intensity of 12,000µW/cm², for approximately 15 - 20 minutes. The PUMA 2U8002 should be directly under and about 1 inch from the light source.

Note that sunlight and fluorescent light may contain sufficient ultraviolet light to erase the programmed information. Although erasure times will be much longer at these levels, the transparent lids on this module should be covered with an opaque label to realise maximum system reliability.

Military Screening Procedure

Module Screening Flow for high reliability non-compliant product processed to MIL-STD-883D, Method 5004 is detailed below:

MB MODULE SCREENING FLOW		
SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
External visual	2017 Condition B (or manufacturers equivalent)	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Burn-In		
Pre Burn-in Electrical	Per Applicable device Specifications at T_A = +25°C (optional)	100%
Burn-In	Method 1015, Condition D, T_A = +125°C	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective Allowable (PDA)	Calculated at Post Burn-in at T_A=+25°C	10%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per MSI or customer specification	

Ordering Information

PUMA 2U8002MB-10

Speed	10	= 100 ns (see note below)
	12	= 120 ns (see note below)
	15	= 150 ns
	17	= 170 ns
	20	= 200 ns
	25	= 250 ns
Temp. range/screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
	M	= Military Temp.
	MB	= Processed to MIL-STD 883D Method 5004, non-compliant
Memory Type	U8002	= 256K x 32 UV EPROM (configurable as 512K x 16 or 1024 K x 8)

NOTE - The following devices are not available at present:

PUMA 2U8002I-10, M-10, MB-10, M-12, MB-12

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