

**ADVANCED INFORMATION**

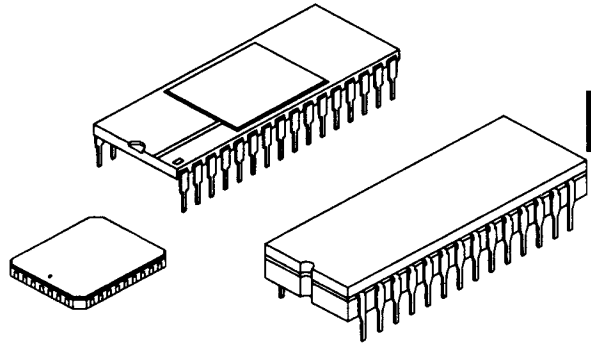
**DESCRIPTION:**

The DPS32M8A is a 32K X 8 CMOS Static Random Access Memory (SRAM). The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5V power supply is required.

The DPS32M8A is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

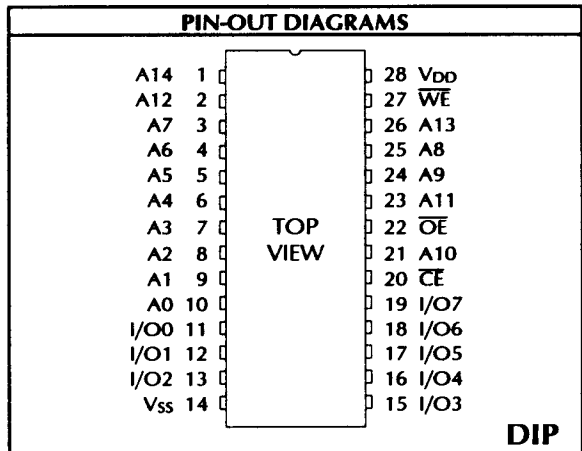
**FEATURES:**

- 32,768 by 8-Bits Organization
- Access Times: 25, 35, 45, 55, 70, 85ns (max.)
- Low Power: 110mW (max.) Full Standby
- Fully Static Operation; No Clock or Refresh Required
- TTL Compatible Input and Output
- Common Data Input and Output
- Single +5V Power Supply, ±10% Tolerance
- Three State Output
- Standard 28-Pin DIP or 32-Pad LCC Packages

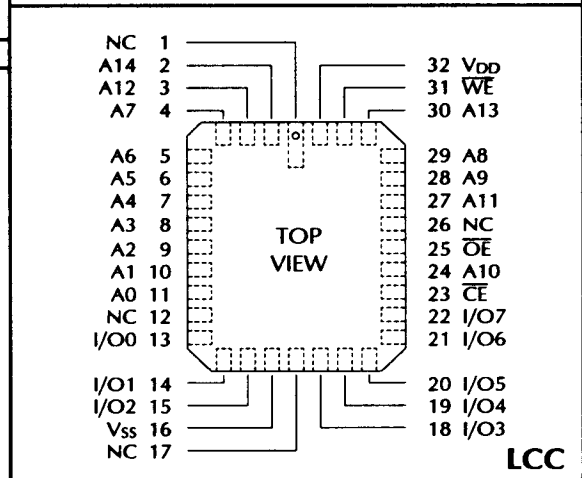
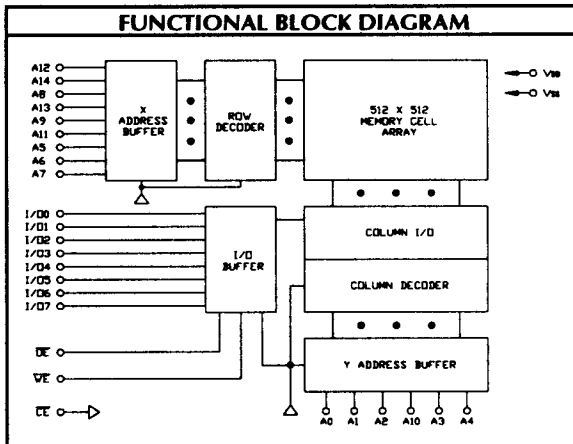


**3**

**PIN-OUT DIAGRAMS**



**FUNCTIONAL BLOCK DIAGRAM**



## ADVANCED INFORMATION

TRUTH TABLE					
Mode	CE	OE	WE	I/O Pin	Supply Current
Not Selected	H	X	X	HIGH-Z	Standby
DOUT Disable	L	H	H	HIGH-Z	Active
Read	L	L	H	DOUT	Active
Write	L	X	L	DIN	Active

L = LOW                      H = HIGH                      X = Don't Care

PIN NAMES	
A0-A14	Address Inputs
I/O0-I/O7	Data In/Out
CE	Chip Enable
WE	Write Enable
OE	Output Enable
VDD	Power (+5V)
VSS	Ground

RECOMMENDED OPERATING RANGE <sup>1</sup>					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input HIGH Voltage	2.2		VDD+0.3	V
V <sub>IL</sub>	Input LOW Voltage	-0.5 <sup>2</sup>		0.8	V

ABSOLUTE MAXIMUM RATINGS <sup>3</sup>			
Symbol	Parameter	Value	Unit
T <sub>STC</sub>	Storage Temperature	-65 to +150	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
VDD	Supply Voltage <sup>1</sup>	-0.5 to +7.0	V
V <sub>I/O</sub>	Input/Output Voltage <sup>1</sup>	-0.5 to +7.0	V

CAPACITANCE <sup>4</sup> : T <sub>A</sub> = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C <sub>IN</sub>	Input Capacitance	11	pF	V <sub>IN</sub> = 0V
C <sub>OUT</sub>	Output Capacitance	11		

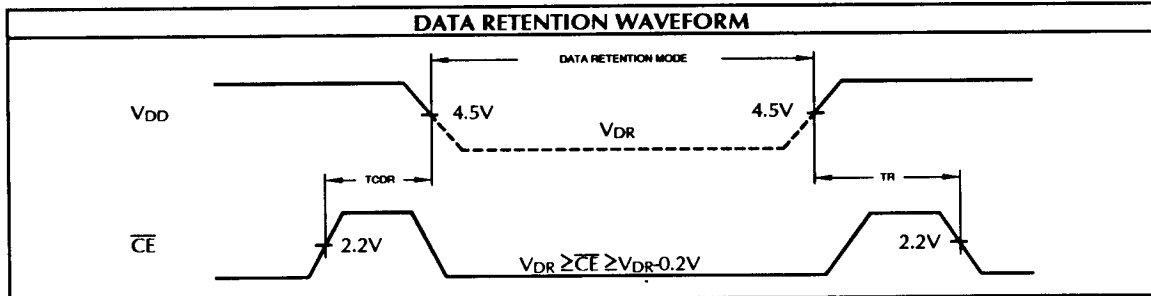
DC OPERATING CHARACTERISTICS: Over operating ranges									
Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 0V to VDD	-10	10	-10	10	-10	10	µA
I <sub>OUT</sub>	Output Leakage Current	V <sub>I/O</sub> = 0V to VDD, CE or OE = V <sub>IH</sub> , or WE = V <sub>IL</sub>	-10	10	-10	10	-10	10	µA
I <sub>CC1</sub>	Active Supply Current	CE = V <sub>IL</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OUT</sub> = 0mA		100		115		120	mA
I <sub>CC2</sub>	Operating Supply Current	Cycle = min., Duty = 100% I <sub>OUT</sub> = 0mA		140		160		160	mA
I <sub>SB1</sub>	Full Standby Supply Current (CMOS)	f = 0, Outputs Open CE ≥ VDD - 0.2V V <sub>IN</sub> ≥ VDD - 0.2V or V <sub>IN</sub> ≥ VDD - 0.2V	S	10		15		20	mA
			L	2		2		2	
I <sub>SB2</sub>	Standby Supply (TTL)	CE = V <sub>IH</sub> , f = 0, Outputs Open		30		35		35	mA
V <sub>OL</sub>	Output Low Voltage	I <sub>OUT</sub> = 8.0mA		0.4		0.4		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OUT</sub> = -4mA	2.4		2.4		2.4		V

DATA RETENTION DC CHARACTERISTICS: (L Versions only)									
Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I <sub>CCDR3</sub>	Data Retention Supply Current	V <sub>DR</sub> = 3V, CE ≥ V <sub>DR</sub> - 0.2V		350		400		800	µA
I <sub>CCDR2</sub>	Data Retention Supply Current	V <sub>DR</sub> = 2V, CE ≥ V <sub>DR</sub> - 0.2V		300		350		600	µA

DATA RETENTION CHARACTERISTICS (L Versions only)						
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V <sub>DR</sub>	Data Retention Voltage	CE ≥ VDD - 0.2V	2.0	5.0	5.5	V
t <sub>CDR</sub>	Chip Disable to Data Retention Time		0			ns
t <sub>R</sub>	Recovery Time	t <sub>RC</sub> = Read Cycle Timing	t <sub>RC</sub>			ns

ADVANCED INFORMATION

3



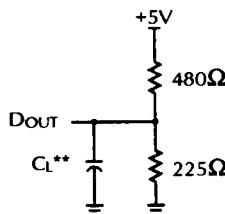
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5V

\* Transition between 0.8V and 2.2V.

OUTPUT LOAD		
Load	CL	Parameters Measured
1	100pF	except tCLZ, tCHZ, tOHZ, tOLZ, tWLZ and tWHZ
2	5pF	tCLZ, tCHZ, tOHZ, tOLZ, tWLZ and tWHZ

Figure 1. Output Load

\*\* Including Probe and Jig Capacitance.

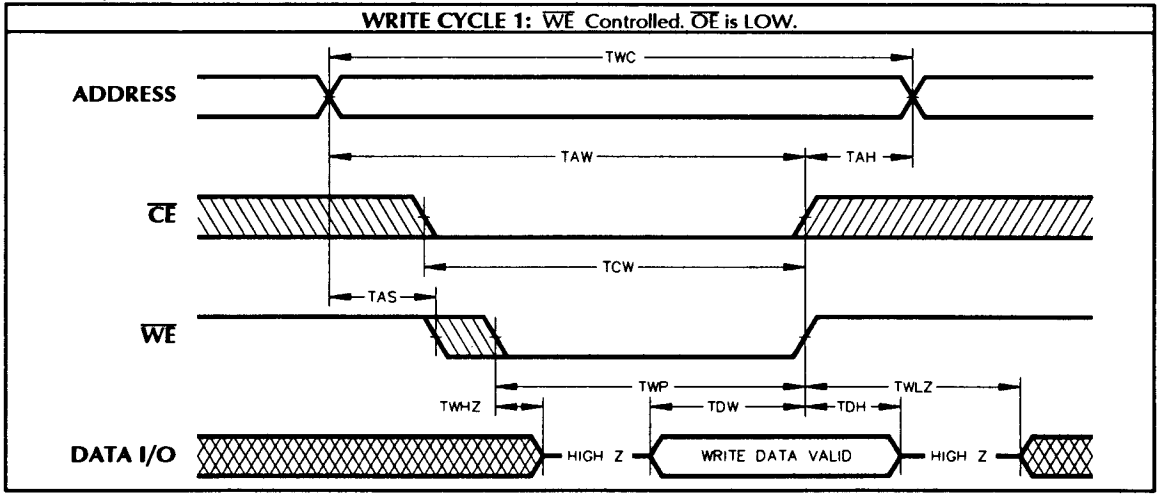
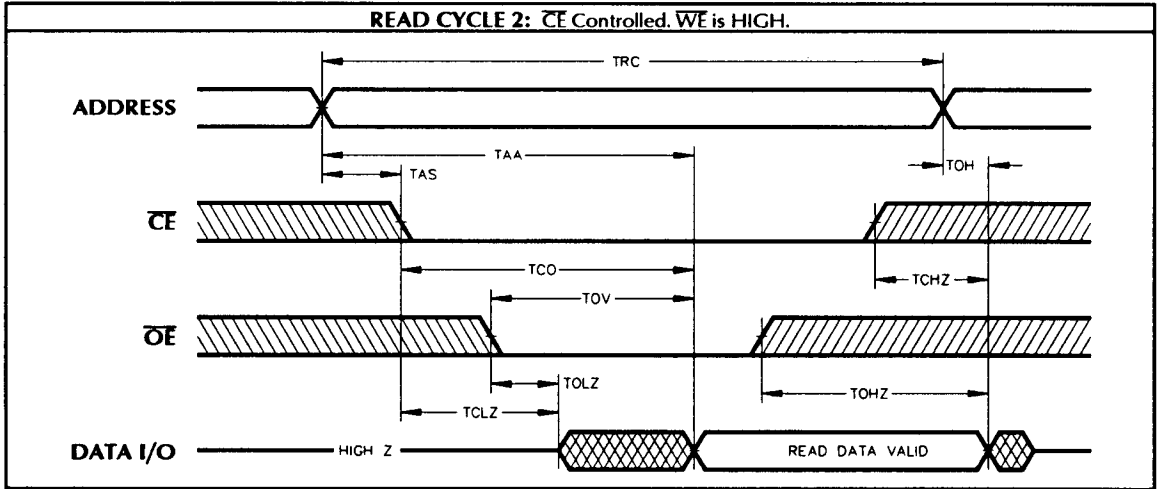
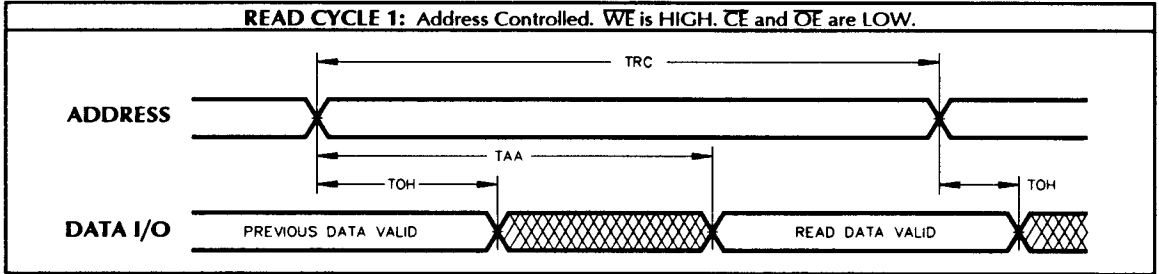


AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges															
No.	Symbol	Parameter	-25		-35		45		-55		-70		-85		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	tRC	Read Cycle Time	25		35		45		55		70		85		ns
2	tAA	Address Access Time		25		35		45		55		70		85	ns
3	tCO	Chip Enable to Output Valid		25		35		45		55		70		85	ns
4	tOV	Output Enable to Output Valid		15		20		20		25		30		35	ns
5	tOH	Output Hold from Address Change	5		5		5		5		5		5		ns
6	tCLZ	Chip Enable to Output in LOW-Z <sup>4, 5</sup>	5		5		5		5		5		5		ns
7	tOLZ	Output Enable to Output in LOW-Z <sup>4, 5</sup>	3		3		3		3		3		3		ns
8	tCHZ	Chip Enable to Output in HIGH-Z <sup>4, 5</sup>		15		20		20		25		30		35	ns
9	tOHZ	Output Enable to Output in HIGH-Z <sup>4, 5</sup>		15		20		20		25		30		35	ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE <sup>6,7</sup> : Over operating ranges															
No.	Symbol	Parameter	-25		-35		45		-55		-70		-85		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.			
10	tWC	Write Cycle Time	25		35		45		55		70		85		ns
11	tAW	Address Valid to End of Write	20		30		40		50		60		70		ns
12	tCW	Chip Enable to End of Write	20		30		40		50		60		70		ns
13	tDW	Data Valid to End of Write	15		18		20		25		30		35		ns
14	tDH	Data Hold Time	3		3		3		3		3		3		ns
15	tWP	Write Pulse Width	20		30		35		40		45		50		ns
16	tAS	Address Set-up Time <sup>***</sup>	0		0		0		0		0		0		ns
17	tAH	Address Hold Time	0		0		0		0		0		0		ns
18	tWHZ	Write Enable to Output in HIGH-Z <sup>4, 5</sup>		15		15		20		25		30		35	ns
19	tWLZ	Write Enable to Output in LOW-Z <sup>4, 5</sup>	5		5		5		5		5		5		ns

\*\*\* Valid for both Read and Write Cycles.

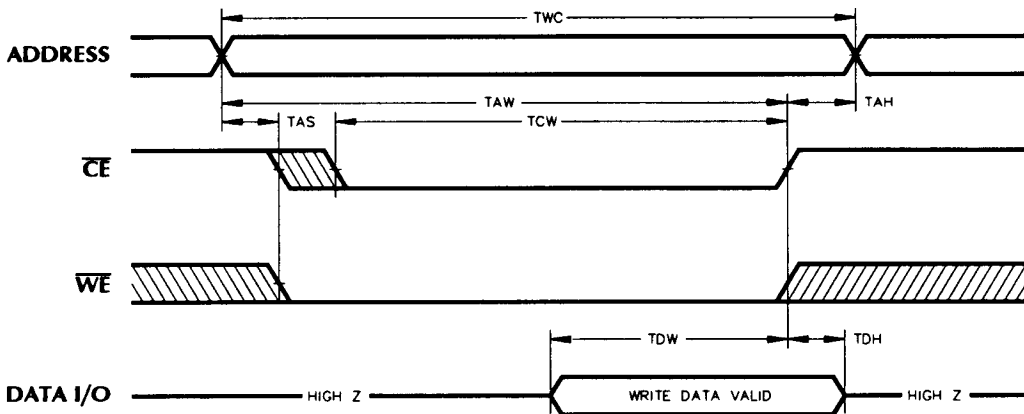
ADVANCED INFORMATION



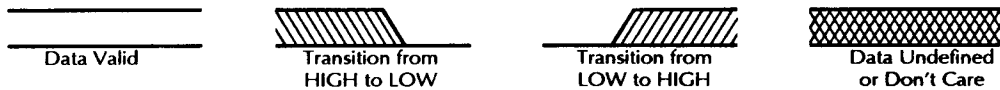
ADVANCED INFORMATION

3

WRITE CYCLE 2:  $\overline{CE}$  Controlled.  $\overline{OE}$  is HIGH.



WAVEFORM KEY



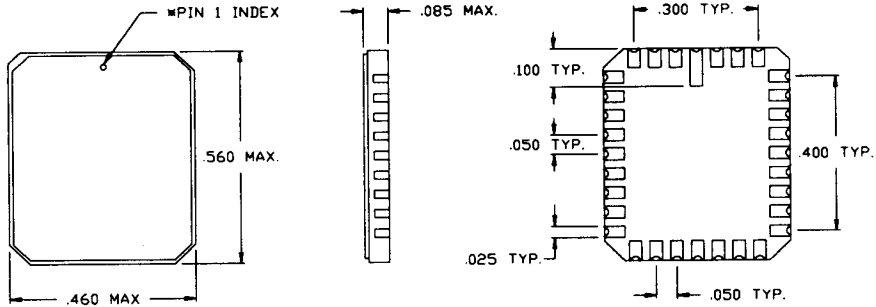
- NOTES:**
1. All voltages are with respect to  $V_{SS}$ .
  2. -2.0V min. for pulse width less than 20ns ( $V_{IL}$  min. = -0.5V at DC level).
  3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
  4. This parameter is guaranteed and not 100% tested.
  5. Transition is measured at the point of  $\pm 500mV$  from steady state voltage.
  6. When  $\overline{OE}$  and  $\overline{CE}$  are LOW and  $\overline{WE}$  is HIGH, I/O pins are in the output state; and, input signals of opposite phase to the outputs must not be applied.
  7. The outputs are in a high impedance state when  $\overline{WE}$  is LOW.

ORDERING INFORMATION

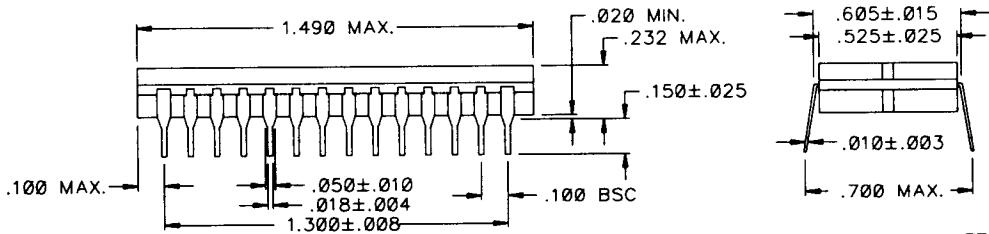
DP	S32M8A	X	X	-	XX	X		
PREFIX	DEVICE TYPE	PACKAGE	POWER		SPEED	GRADE		
C							COMMERCIAL	0°C to +70°C
I							INDUSTRIAL	-40°C to +85°C
M							MILITARY	-55°C to +125°C
B							MIL-PROCESSED	-55°C to +125°C
25							25ns	
35							35ns	
45							45ns	
55							55ns	
70							70ns	
85							85ns	
S							STANDARD POWER	
L							LOW POWER	
G							32 PAD LCC	
N							28 LEAD SIDE BRAZED DIP	
NONE							28 LEAD CERDIP	
							HIGH SPEED 32K X 8 CMOS SRAM	

## ADVANCED INFORMATION

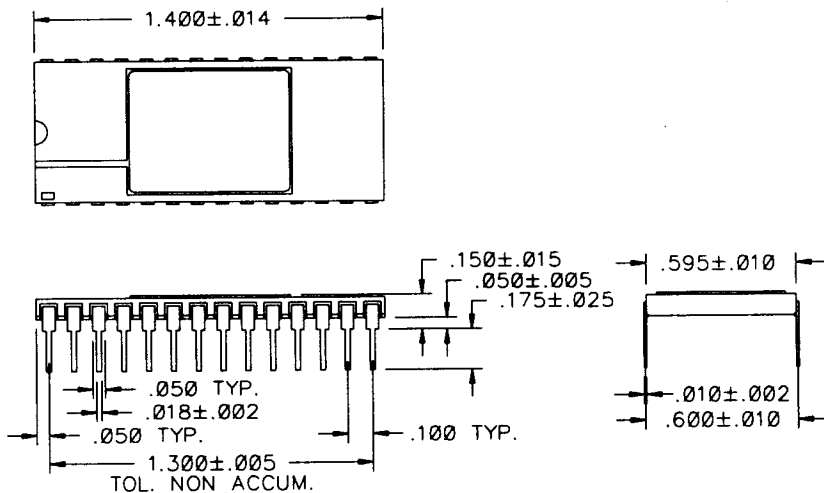
### MECHANICAL DIAGRAMS



LCC



CERDIP



SIDE BRAZED DIP

### Dense-Pac Microsystems, Inc.

7321 Lincoln Way • Garden Grove, California 92641-1428  
 (714) 898-0007 • (800) 642-4477 (Outside CA) • FAX: (714) 897-1772