DATA SHEET

UAA2062
Analog cordless telephone IC

Product specification
File under Integrated Circuits, IC17

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Philips Semiconductors

PHILIPS

Analog cordless telephone IC UAA2062

FEATURES

RF RX (double superheterodyne FM receiver)

- Integrated Low Noise Amplifier (LNA) with programmable gain and input impedance
- 1st mixer with external filter at 10.7 MHz
- 2nd mixer with external filter at 455 or 450 kHz (depending on country application)
- FM detector including a fully integrated IF limiter, a wide-band PLL and a Received Signal Strength Indicator (RSSI) output
- Carrier Detector (CD) with programmable threshold.

RF TX

- Buffer driving an internal Power Amplifier (PA) with programmable gain
- Narrow-band PLL including VCO
- Data transmission summing operational amplifier.

Synthesizer

- 10.24 or 11.15 MHz crystal reference oscillator (LO2) and reference frequency divider
- Programmable TX VCO with phase detector and frequency divider
- Programmable RX VCO (LO1) with phase detector and frequency divider
- Programmable clock divider with output buffer to drive the microcontroller.

Baseband RX section

- Programmable RX gain
- Expander
- Fully integrated earpiece amplifier with fixed gain.

Baseband TX section

- Microphone amplifier
- Compressor
- Programmable TX gain.

Microcontroller interface

- 3-wire serial interface.

Other features

- Voltage regulator to supply internal PLLs and the microcontroller
- Programmable low-battery detector time multiplexed with RSSI carrier detector.

APPLICATIONS

- World-wide analog cordless telephone set (CT0).

GENERAL DESCRIPTION

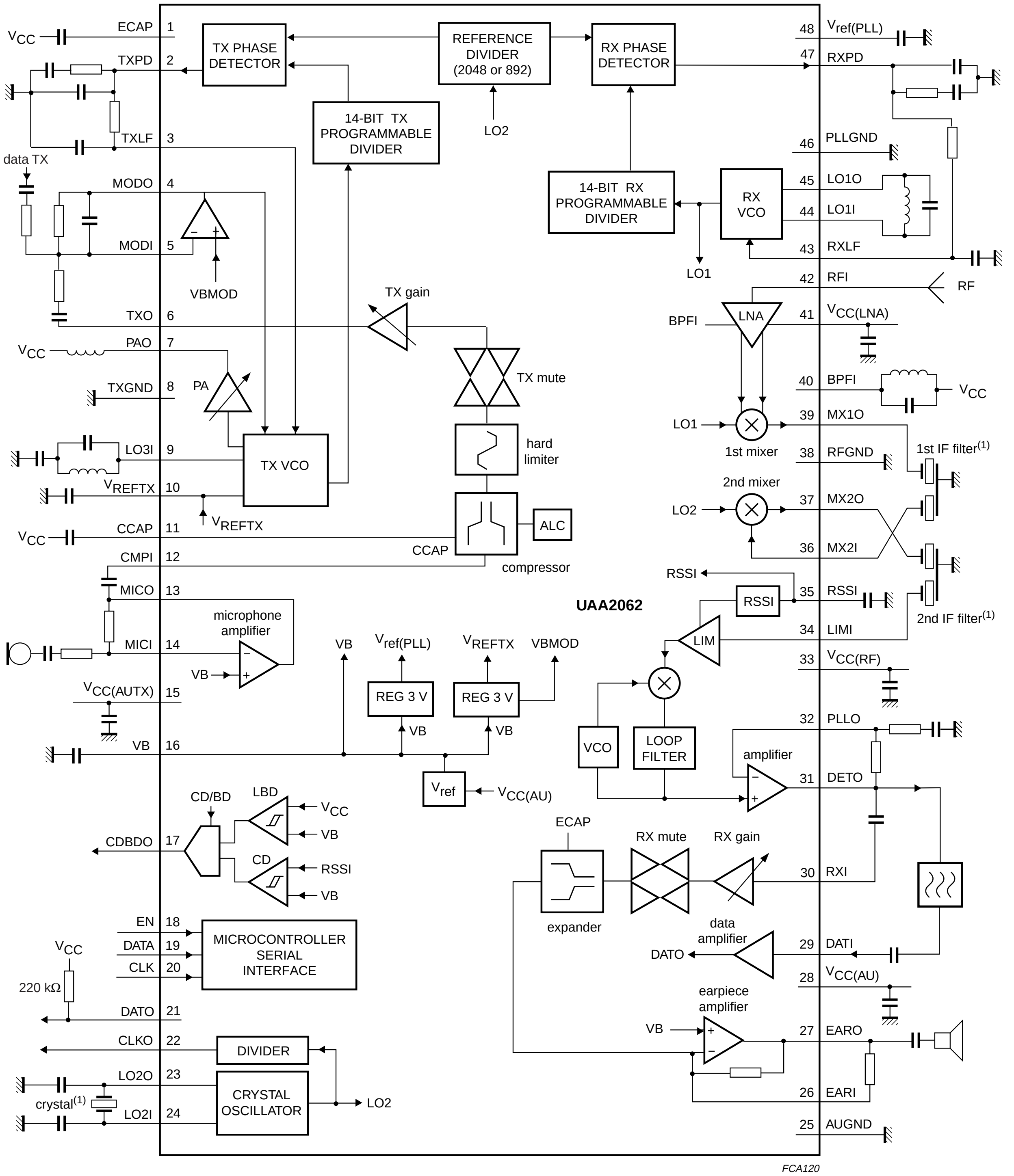
The UAA2062 is a BiCMOS integrated circuit that performs all functions from the antenna to the microcontroller for reception and transmission for both the base station and the handset in a cordless telephone.

This IC integrates most of the functions required for a cordless telephone into a single integrated circuit. The implemented programming enables the device to be used for the CT0 standard in many countries. Additionally, the implemented programming significantly reduces the amount of external components, board space requirements and external adjustments.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2062TS	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1

BLOCK DIAGRAM



(1) Values are depending on country application (see definition in Chapter “Channel frequencies”).

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
ECAP	1	output pin for external capacitor from expander
TXPD	2	phase detector output voltage for TX PLL
TXLF	3	input from loop filter to TX VCO
MODO	4	summing amplifier output voltage
MODI	5	summing amplifier inverting input
TXO	6	TX baseband output voltage
PAO	7	power amplifier output
TXGND	8	ground for RF TX chain and PA
LO3I	9	TX VCO input
V_{REFTX}	10	output pin for decoupling capacitor for regulated voltage for TX VCO
CCAP	11	output pin for external capacitor from compressor
CMPI	12	compressor input voltage
MICO	13	microphone amplifier output voltage
MICI	14	microphone amplifier inverting input
$V_{CC(AUTX)}$	15	supply voltage for TX audio
VB	16	internal voltage reference
CDBDO	17	multiplexed output from carrier detector or low-battery detector
EN	18	enable signal for serial interface
DATA	19	data signal for serial interface
CLK	20	clock signal for serial interface
DATO	21	data comparator output
CLKO	22	output pin for external clock
LO2O	23	crystal oscillator output

SYMBOL	PIN	DESCRIPTION
LO2I	24	crystal oscillator input
AUGND	25	ground for audio part
EARI	26	earpiece amplifier inverting input
EARO	27	earpiece amplifier output voltage
$V_{CC(AU)}$	28	supply voltage for audio part
DATI	29	data comparator input
RXI	30	RX audio input voltage
DETO	31	amplifier FM PLL output voltage
PLLO	32	amplifier FM PLL inverting input
$V_{CC(RF)}$	33	supply voltage for RF RX
LIMI	34	limiter input voltage
RSSI	35	output pin for external capacitor from RSSI
MX2I	36	2nd mixer input
MX2O	37	2nd mixer output
RFGND	38	ground for RF RX
MX1O	39	1st mixer output voltage
BPFI	40	LNA output for external LC
$V_{CC(LNA)}$	41	supply voltage for LNA
RFI	42	LNA input voltage
RXLF	43	input from loop filter to RX VCO
LO1I	44	input pin to connect the external LC for RX VCO
LO1O	45	output pin to connect the external LC for RX VCO
PLLGND	46	ground for digital part of the PLL
RXPD	47	phase detector output voltage for RX PLL
$V_{ref(PLL)}$	48	output pin for decoupling capacitor for regulated voltage for internal PLLs and microcontroller

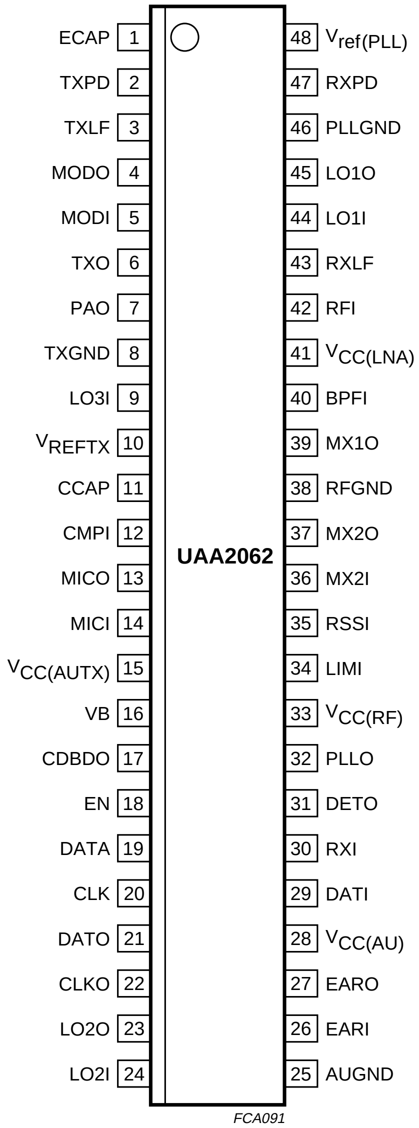


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Power supply and power management

POWER SUPPLY VOLTAGE

The UAA2062 is used in a cordless telephone handset and in a base unit. The handset unit is battery powered and can operate on three NiCad cells. The minimum supply voltage (V_{CC}) is 3.0 V. However the low-battery detector, crystal oscillator, clock divider and internal voltage regulator will function with a supply voltage of 2.85 V.

POWER SAVING OPERATION MODES

When the UAA2062 is used in a handset, it is important to reduce the current consumption. There are 3 power saving modes in addition to the active mode:

1. In the active mode all blocks are powered.
2. In the RX mode, all circuitry in the receiver part is powered.
3. In the standby mode, all circuitry is powered down except the crystal oscillator, the microcontroller interface and the $V_{ref(PLL)}$ block.
4. In the inactive mode, all circuitry is powered down except the microcontroller interface and the $V_{ref(PLL)}$ block.

Latch memory is maintained in all modes. Table 1 shows which blocks are powered in each mode.

Table 1 Power saving operation modes

CIRCUIT BLOCK	ACTIVE MODE	RX MODE	STANDBY MODE	INACTIVE MODE
Microcontroller interface	X	X	X	X
$V_{ref(PLL)}$	X	X	X(1)	X(1)
Crystal oscillator	X	X	X	–
RF receiver and RX PLL	X	X	–	–
VB reference	X	X	–	–
Carrier and low-battery detectors	X	X	–	–
Data comparator	X	X	–	–
TX PLL and PA	X	–	–	–
RX and TX audio paths	X	–	–	–

Note

1. In the standby mode and in the inactive mode, by default, $V_{ref(PLL)}$ remains regulated but is not calibrated (bit V_{REFPLL} disable is logic 0). If bit V_{REFPLL} disable is logic 1, $V_{ref(PLL)}$ is not regulated and fluctuates with V_{CC}.

MAXIMUM CURRENT CONSUMPTION

Table 2 shows the typical and the maximum current consumption in the active mode and the three current saving modes under the following conditions: IP3 HIGH mode (bit IP3 is logic 1), see Table 6; LNA gain is step 3 (bits LNA are logic 11), see Table 12 and the PA output level is step 3 (bits PA are logic 11), see Table 15.

In the standby mode and in the inactive mode, pin $V_{ref(PLL)}$ is not powered (bit V_{REFPLL} disable is logic 1) and the clock output signal is disabled (bits clock divider ratio are logic 00).

Table 2 Current consumption in the 4 operating modes (V_{CC} = 3.6 V; T_{amb} = 25 °C); see Table 5 for programming of the power saving operation modes

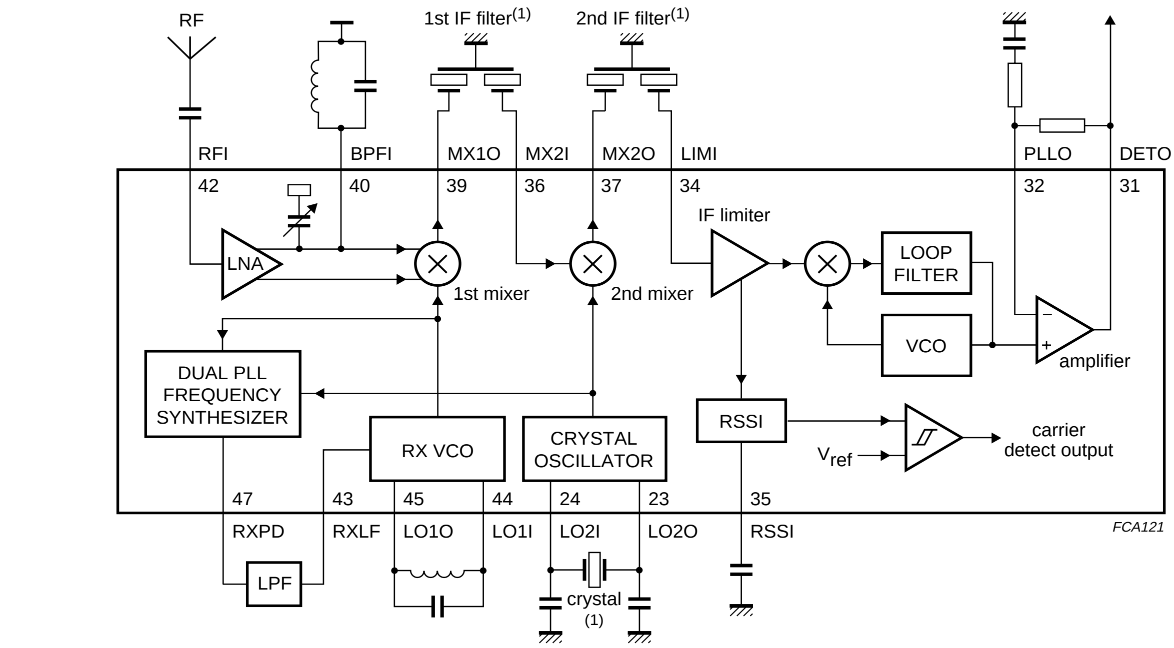
POWER OPERATING MODE	TYPICAL CURRENT CONSUMPTION (mA)	MAXIMUM CURRENT CONSUMPTION (mA)
active mode	27	36
RX mode	11	15
standby mode	0.35	0.5
inactive mode	0.05	0.1

The FM receiver part

FM RECEIVER

The FM receiver has the programmability to operate for all country channels, including the 25 U.S. channels, without the need for external switching circuitry (see Fig.3).

The gain and input impedance of the LNA are programmable. The LNA also includes a programmable capacitance to avoid external manual fine tuning.



(1) Values depend on the country application (see definition in Chapter “Channel frequencies”).

Fig.3 FM receiver schematic diagram.

DATA COMPARATOR

The data comparator is an inverting hysteresis comparator. An external filter is connected between pins DETO and DATI (AC-coupled). The open-collector output is current limited to control the output signal slew rate. The external resistor at pin DATO, connected to V_{CC}, should be 220 kΩ. An external capacitor in parallel with this resistor will reduce the slew rate.

The transmit part

The transmitter architecture is of the direct modulation type. The transmit VCO can be frequency modulated either by speech or data (see Fig.4).

TRANSMIT VCO

Before the VCO, an amplifier sums the modulating signal and the data TX signal. The Colpitts type transmit VCO includes integrated varicaps. Fixed external capacitors are used to extend the tuning range for all countries.

The internal capacitors are programmed via the serial bus interface. The power amplifier is capable of driving 50 Ω AC. The output level is also programmed with 2 bits via the serial bus interface. An internal regulator supplies the TX VCO.

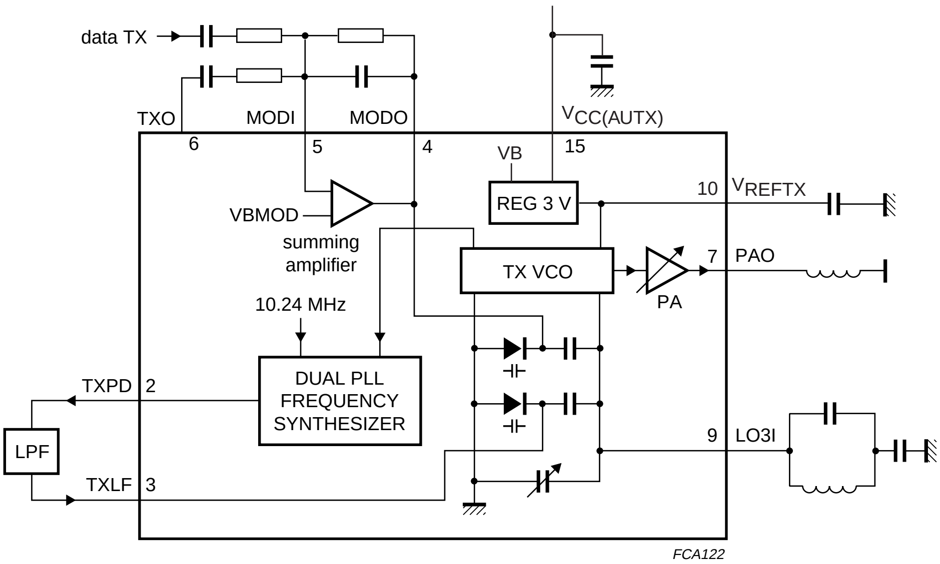


Fig.4 Transmit schematic diagram.

The synthesizer

The synthesizer has been designed to support most country channel frequencies between 25 and 50 MHz (see Chapter "Channel frequencies").

The local oscillator LO2 and the reference divider provide the reference frequency for the RX and TX PLL loops. A single bit programmes the divider value for the reference divider. A 5 kHz reference frequency (respectively 12.5 kHz) is used with a 10.24 MHz crystal frequency (respectively 11.15 MHz). The clock divider ratio can be programmed to 2.5 or to 80. The ratio 80 can be chosen when the IC is in sleep mode to obtain current saving in the microcontroller. The clock output is a CMOS output inverter, supplied by $V_{ref(PLL)}$.

The 14-bit TX counter is programmed for the desired transmit channel frequency. The 14-bit RX counter is programmed for the desired RX VCO frequency.

All counters power-up in the proper default state and for a 10.24 MHz reference crystal. Both RX and TX phase detectors have current drive type outputs of 400 µA.

The RX VCO is connected to an external capacitor and inductor as illustrated in Fig.5. The varicaps are integrated.

Operating in the 25 US channels, there is a large frequency difference between the minimum and the maximum channel frequencies. The sensitivity of the RX VCO is not large enough to accommodate this large frequency range. Internal programmable capacitors can be connected across the RX VCO tank circuit to change the RX VCO sensitivity. The TX VCO also has internal programmable capacitors to accommodate a large frequency range. Chapter "Channel frequencies" shows the frequency selection for all countries.

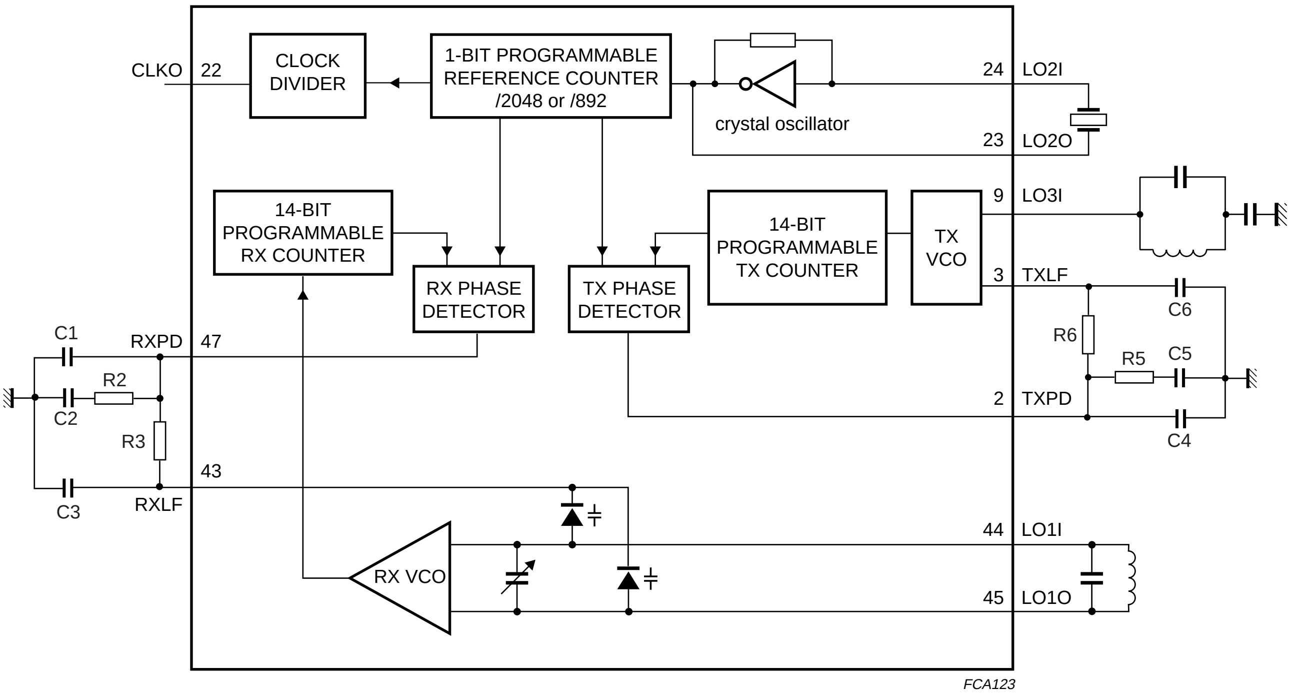


Fig.5 Synthesizer schematic diagram.

The RX baseband

This section covers the RX audio path from pins RXI to EARO. The RXI input signal is AC-coupled.

The microcontroller sets the value of the RX gain by 32 linear steps of 0.5 dB. The RX baseband has a mute and an expander with the characteristics shown in Fig.7.

EARPIECE AMPLIFIER

The earpiece amplifier is an inverting rail-to-rail operational amplifier. The non-inverting input is connected to the internal reference voltage VB. Internal resistors are used to set the gain at 6 dB. An external resistor (connected between pins EARI and EARO) can be used to reduce the gain.

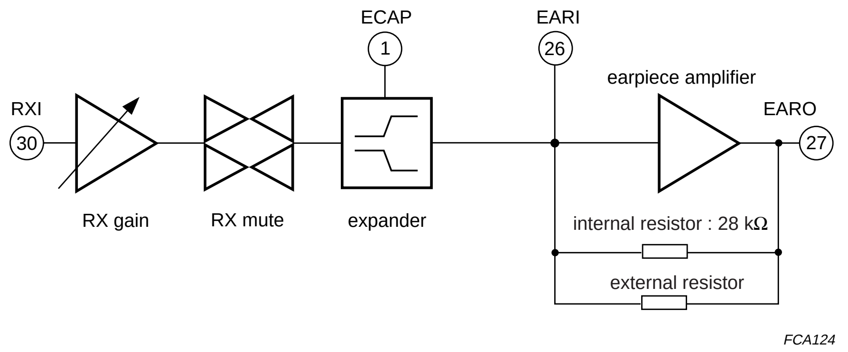
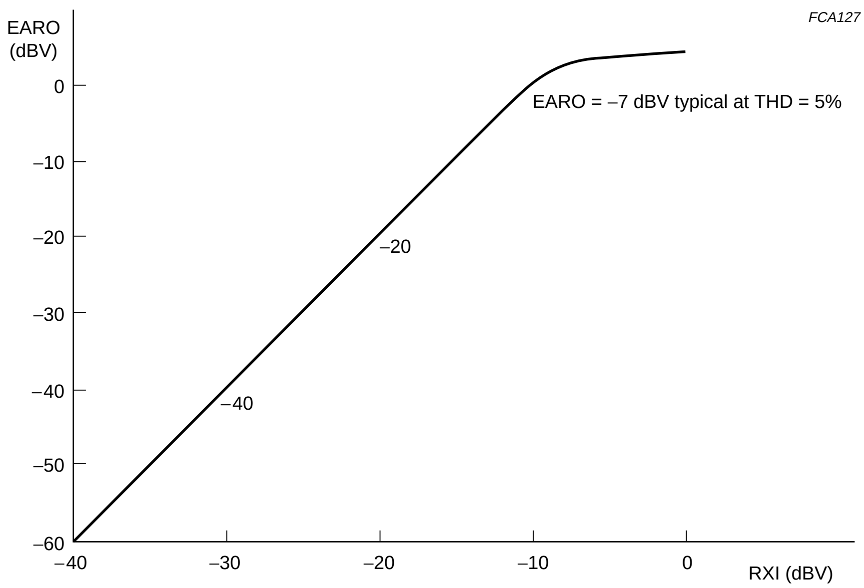


Fig.6 RX baseband schematic diagram.



(1) ΔG_{ARX} = 0 dB, G_{EAR} = 0 dB (external resistor of 28 kΩ).

Fig.7 Expander characteristic.

The TX baseband

This section covers the TX audio path from pins MICI to TXO.

The microphone amplifier is an inverting operational amplifier whose gain can be set by external resistors. The input signal at pin MICI and the output signal at pin MOCO are both AC-coupled. The non-inverting input is connected to the internal reference voltage VB. External resistors are used to set the gain and frequency response.

The TX baseband has a compressor with the characteristic shown in Fig.9. The Automatic Level Control (ALC) provides a ‘soft’ limit to the output signal swing as the input voltage increases slowly (i.e. a sine wave is maintained at the output). A hard limiter clamps the compressor output voltage at 1.26 V (p-p). The ALC and the hard limiter can be disabled via the microcontroller interface. The hard limiter is followed by a mute circuit. The TX gain is digitally programmable in 32 steps of 0.5 dB.

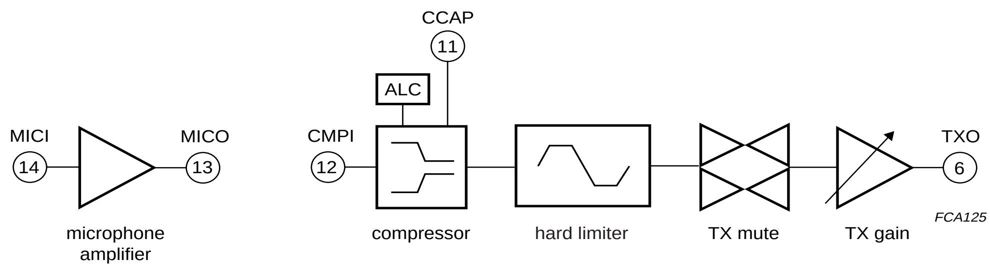


Fig.8 TX baseband schematic diagram.

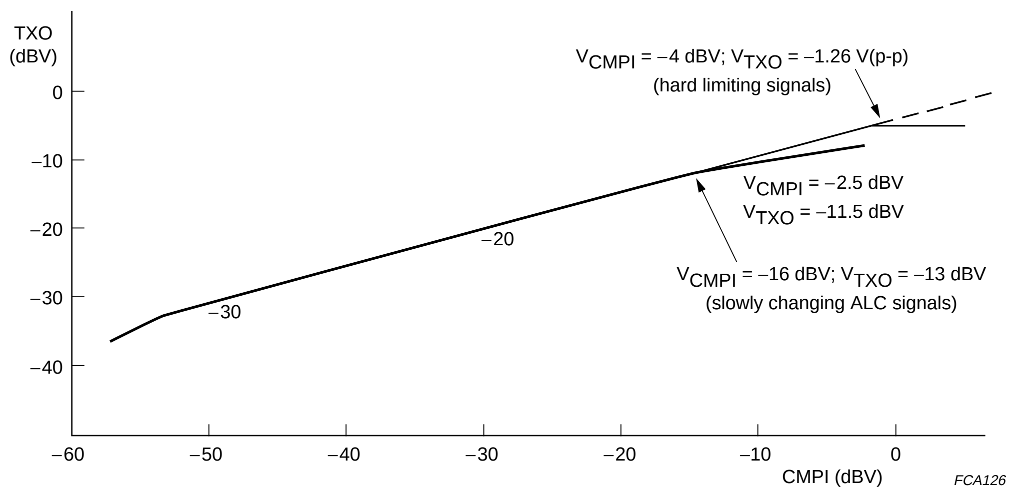


Fig.9 Compressor characteristic.

Other features

PLL VOLTAGE REGULATOR

Pin $V_{ref(PLL)}$ provides the internal supply voltage for the RX and TX PLLs. It is regulated at 3 V. Pin $V_{CC(AU)}$ provides the supply voltage input for the internal voltage regulator. Two capacitors of 47 µF and 100 nF must be connected to pin $V_{ref(PLL)}$ to filter and stabilize this regulated voltage. The tolerance of the regulated voltage is initially ±8% but is improved to ±4% after the internal band gap voltage reference is adjusted via the microcontroller.

The voltage regulator is always turned on. In the inactive mode the calibration is turned off to reduce current consumption. In this mode, the $V_{ref(PLL)}$ block supplies 300 µA to the microcontroller. The output drive capability is 3 mA. The voltage regulator is able to supply the microcontroller.

The local oscillator LO2 and the RX and TX phase detectors are powered by the internal voltage regulator at pin $V_{ref(PLL)}$. Therefore, the maximum input and output level for most I/O pins (LO2I and LO2O) equals the regulated voltage at pin $V_{ref(PLL)}$.

LOW-BATTERY DETECTOR

The low-battery detector measures the voltage level of the $V_{CC(AU)}$ using a resistance divider and a comparator. One input of the comparator is connected to VB, the other to the middle point of the resistance divider.

The comparator has a built-in hysteresis to prevent spurious switching. The precision of the detection depends on the divider accuracy, the comparator offset and the accuracy of the reference voltage VB. The output is multiplexed at pin CDBDO. When the battery voltage level is below the threshold voltage the output CDBDO is going LOW.

Microcontroller serial interface

Pins DATA, CLK and EN provide a 3-wire unidirectional serial interface for programming the reference counters, the transmit and receive channel divider counters and the control functions.

The interface consists of 18-bit shift registers connected to a matrix of registers organized as 6 words of 18 bits. The leading 15 bits include the data D14 to D0. The trailing 3 bits set up the address AD2 to AD0. The data is entered with the most significant bit D14 first. The last bit is bit AD0.

Pins DATA and CLK are used to load data into the shift register. Figure 10 shows the timing required on all pins. Data is clocked into the shift registers on negative clock transitions.

The serial interface pins DATA, CLK and EN, are supplied by $V_{ref(PLL)}$. Internal level shifters are provided after the pins which allow the logic and registers to be internally powered by $V_{CC(AU)}$.

The ESD protection diodes on these pins are connected to $V_{CC(AU)}$. All the digital outputs (CDBDO and DATO) are open-collector outputs.

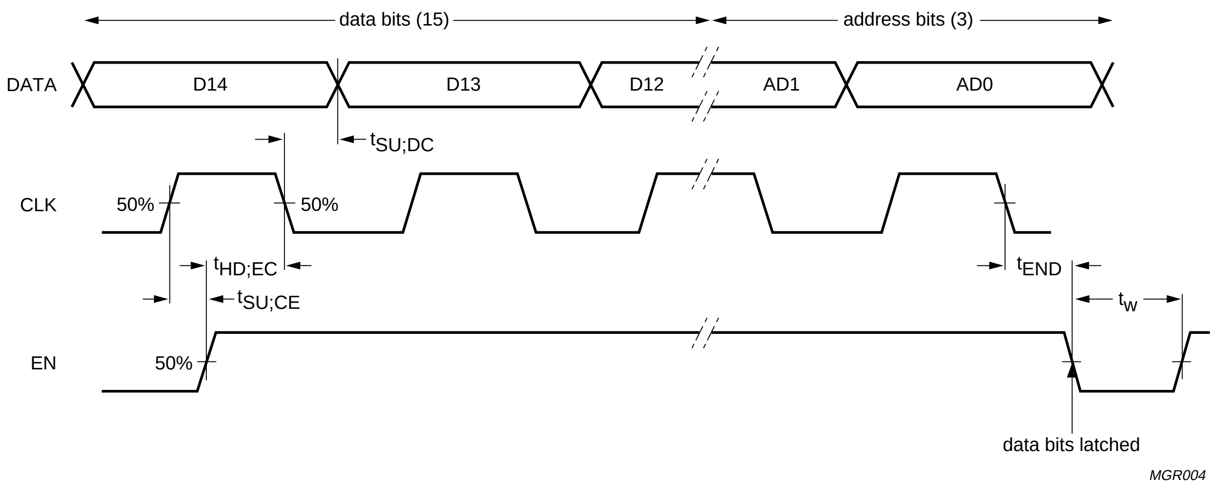


Fig.10 Digital signals timing requirement.

DATA REGISTERS AND ADDRESSES

Table 3 shows the data latches and addresses which are used to select each of the registers. bit D14 is the MSB and is written and loaded first.

Table 3 Data register and addresses

ADDR	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
001	–	TX counter [13 to 0]													
010	–	RX counter [13 to 0]													
011	voltage reference adjust [2 to 0]			Clk Div [1 and 0]		Ref Div	IP3	LNA gain [1 and 0]		LNA RIN [1 and 0]		V_{REFPLL} disable	HLim	–	
100	test modes [2 to 0][1]			LNA capacitor [3 to 0]				RX VCO capacitor [3 to 0]				FM PLL centre frequency shift [3 to 0]			
101	BD active	low-battery detector threshold [2 to 0]			CD threshold control [4 to 0]					RX mute	RX gain control[4 to 0]				
110	active modes [1 and 0]		PA [1 and 0]		TX VCO capacitor selection[3 to 0]				ALC disable	TX mute	TX gain control[4 to 0]				

Note

1. The three bits must be set at 000 in normal operation.

Table 4 Data register default value

ADDR	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
001	–	1	0	0	1	1	0	1	1	1	0	1	1	1	0
010	–	0	1	1	1	0	0	0	0	1	0	1	1	1	1
011	0	1	1	0	1	0	0	0	0	0	0	0	1	–	–
100	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
101	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
110	0	0	1	1	0	1	1	1	0	0	0	1	1	1	1

ACTIVE MODES BITS SELECTION

Table 5 Active modes bits selection

BIT 1	BIT 0	DESCRIPTION
0	0	active mode
0	1	RX mode
1	0	standby mode
1	1	inactive mode

REGISTER CONTENT DESCRIPTION

Table 6 Register content description

DATA REGISTER	BIT	DESCRIPTION
IP3	1	IP3 HIGH mode for 2nd mixer
	0	IP3 LOW mode for 2nd mixer
ALC disable	1	automatic level control disabled
	0	normal operation
HLim	1	hard limiter disabled
	0	normal operation
RX mute	1	RX channel muted
	0	normal operation
TX mute	1	TX channel muted
	0	normal operation
LBD enable	1	low-battery detector enabled
	0	carrier detector enabled
V_{REFPLL} disable	1	V_{REFPLL} disabled (tied to V_{CC})
	0	V_{REFPLL} enabled
Ref Div	1	divider ratio 892 (conversion from 11.15 MHz to 12.5 kHz)
	0	divider ratio 2048 (conversion from 10.24 MHz to 5 kHz)

TX AND RX GAIN SELECTION

The TX and RX audio signal paths have a programmable gain block. If a TX or RX voltage gain other than the nominal power-up default is desired it can be programmed via the microcontroller interface.

The gain blocks can be used during final test of the telephone to electronically adjust for gain tolerances in the telephone system. The RX gain and the TX gain selection covers a dynamic range from –7.5 to +8 dB in steps of 0.5 dB and can be programmed independently from each other.

Table 7 TX and RX gain selection

BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	STEP	TX GAIN (dB)	RX GAIN (dB)
0	0	0	0	0	0	–7.5	–7.5
0	0	0	0	1	1	–7.0	–7.0
0	0	0	1	0	2	–6.5	–6.5
0	0	0	1	1	3	–6.0	–6.0
0	0	1	0	0	4	–5.5	–5.5
0	0	1	0	1	5	–5.0	–5.0
0	0	1	1	0	6	–4.5	–4.5
0	0	1	1	1	7	–4.0	–4.0
0	1	0	0	0	8	–3.5	–3.5
0	1	0	0	1	9	–3.0	–3.0
0	1	0	1	0	10	–2.5	–2.5
0	1	0	1	1	11	–2.0	–2.0
0	1	1	0	0	12	–1.5	–1.5
0	1	1	0	1	13	–1.0	–1.0
0	1	1	1	0	14	–0.5	–0.5
0	1	1	1	1	15	0	0
1	0	0	0	0	16	+0.5	+0.5
1	0	0	0	1	17	+1.0	+1.0
1	0	0	1	0	18	+1.5	+1.5
1	0	0	1	1	19	+2.0	+2.0
1	0	1	0	0	20	+2.5	+2.5
1	0	1	0	1	21	+3.0	+3.0
1	0	1	1	0	22	+3.5	+3.5
1	0	1	1	1	23	+4.0	+4.0
1	1	0	0	0	24	+4.5	+4.5
1	1	0	0	1	25	+5.0	+5.0
1	1	0	1	0	26	+5.5	+5.5
1	1	0	1	1	27	+6.0	+6.0
1	1	1	0	0	28	+6.5	+6.5
1	1	1	0	1	29	+7.0	+7.0
1	1	1	1	0	30	+7.5	+7.5
1	1	1	1	1	31	+8.0	+8.0

CARRIER DETECTOR THRESHOLD SELECTION

The carrier detector indicates if a carrier signal is present on the selected channel. The nominal value and tolerance of the carrier detector threshold is given in the carrier detector specification section. If a different carrier detector threshold value is desired, it can be selected via the microcontroller interface.

If it is required to scale the carrier detector range, an external resistor should be connected between pin RSSI and ground. The carrier detector threshold step 19 (10011) corresponds to a typical level on pin RSSI of 0.86 V DC.

Table 8 Carrier detector threshold selection

BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	STEP	CARRIER DETECTOR THRESHOLD (V)
0	0	0	0	0	0	0.1
0	0	0	0	1	1	0.14
0	0	0	1	0	2	0.18
0	0	0	1	1	3	0.22
0	0	1	0	0	4	0.26
0	0	1	0	1	5	0.3
0	0	1	1	0	6	0.34
0	0	1	1	1	7	0.38
0	1	0	0	0	8	0.42
0	1	0	0	1	9	0.46
0	1	0	1	0	10	0.5
0	1	0	1	1	11	0.54
0	1	1	0	0	12	0.58
0	1	1	0	1	13	0.62
0	1	1	1	0	14	0.66
0	1	1	1	1	15	0.7
1	0	0	0	0	16	0.74
1	0	0	0	1	17	0.78
1	0	0	1	0	18	0.82
1	0	0	1	1	19	0.86
1	0	1	0	0	20	0.9
1	0	1	0	1	21	0.94
1	0	1	1	0	22	0.98
1	0	1	1	1	23	1.02
1	1	0	0	0	24	1.06
1	1	0	0	1	25	1.1
1	1	0	1	0	26	1.14
1	1	0	1	1	27	1.18
1	1	1	0	0	28	1.22
1	1	1	0	1	29	1.26
1	1	1	1	0	30	1.3
1	1	1	1	1	31	1.34

LOW-BATTERY DETECTOR LEVEL SELECTION

When the LBD register is set HIGH, the low-battery detector is enabled and the low-battery detect output signal is routed to the output pin CDBDO. The low-battery detector level selection functions only in a programmable mode. The power-up default value is step 7 (111).

Table 9 Low-battery detector level selection

BIT 2	BIT 1	BIT 0	STEP	NOMINAL LOW-BATTERY DETECTOR VOLTAGE (V)
0	0	0	0	3.6
0	0	1	1	3.5
0	1	0	2	3.4
0	1	1	3	3.3
1	0	0	4	3.2
1	0	1	5	3.1
1	1	0	6	3.0
1	1	1	7	2.9

VOLTAGE REFERENCE SELECTION

An internal 1.5 V band gap reference voltage provides the voltage reference for the low-battery detector circuit, the $V_{ref(PLL)}$ voltage regulator, the VB reference and all internal analog references.

Table 10 Voltage reference selection

BIT 2	BIT 1	BIT 0	STEP	NOMINAL VOLTAGE REFERENCE (%)
0	0	0	0	–7
0	0	1	1	–5
0	1	0	2	–3
0	1	1	3	–1
1	0	0	4	+1
1	0	1	5	+3
1	1	0	6	+5
1	1	1	7	+7

LNA CAPACITOR SELECTION

The LNA has an external capacitor and inductor that together form a band-pass filter. A programmable on-chip capacitor is integrated which gives, in parallel with an external L and C, the possibility to tune the band-pass filter characteristic during production. A parasitic capacitor has to be added to the internal capacitor value.

Table 11 LNA capacitor selection

BIT 3	BIT 2	BIT 1	BIT 0	STEP	LNA CAPACITOR VALUE (pF)
0	0	0	0	0	0
0	0	0	1	1	0.8
0	0	1	0	2	1.6
0	0	1	1	3	2.4
0	1	0	0	4	3.2
0	1	0	1	5	4.0
0	1	1	0	6	4.8
0	1	1	1	7	5.6
1	0	0	0	8	6.4
1	0	0	1	9	7.2
1	0	1	0	10	8.0
1	0	1	1	11	8.8
1	1	0	0	12	9.6
1	1	0	1	13	10.4
1	1	1	0	14	11.2
1	1	1	1	15	12.0

LNA GAIN SELECTION

The LNA has an internal programmable voltage conversion gain. This allows to tune the gain in order to achieve the best compromise in term of performance. The LNA gain is given with a reference value of L = 390 nH (Q_{loaded} = 40) at 50 MHz.

Table 12 LNA gain selection; L = 390 nH at BPFI; Q_{Loaded} = 40; f = 50 MHz

BIT 1	BIT 0	STEP	LNA GAIN (dB)
0	0	0	17
0	1	1	19
1	0	2	21
1	1	3	23

LNA INPUT RESISTIVE IMPEDANCE SELECTION

The LNA has an internal programmable input resistive impedance (RIN) in order to improve the duplexer and LNA performance. To calculate the input resistive impedance we must know the typical LNA gain (i.e. the value of the external inductance and its Q). A small capacitance at the LNA input is needed to improve matching between LNA and duplexer. The programmability of tuning the input impedance allows to obtain an optimum sensitivity performance in the active and in the RX mode of operation.

Table 13 LNA input resistive impedance selection

BIT 1	BIT 0	STEP	TYPICAL LNA INPUT RESISTIVE IMPEDANCE	
			LNA VOLTAGE GAIN = 17 dB	LNA VOLTAGE GAIN = 23 dB
0	0	0	1.2 kΩ	645 Ω
0	1	1	3.0 kΩ	1.6 kΩ
1	0	2	7.1 kΩ	3.8 kΩ
1	1	3	22.9 kΩ	14.5 kΩ

RX AND TX VCO CAPACITOR SELECTION

The RX VCO and the TX VCO have an external LC tank circuit. A programmable internal capacitor is integrated in parallel with the external L and C in order to tune the VCO and to keep the PLL in lock for large frequency steps.
A parasitic capacitor has to be added to these values. The RX VCO capacitor value and the TX VCO capacitor value can be programmed independently one from the other.

Table 14 RX and TX VCO capacitor selection

BIT 3	BIT 2	BIT 1	BIT 0	STEP	INTERNAL RX VCO CAPACITOR VALUE (pF)	INTERNAL TX VCO CAPACITOR VALUE (pF)
0	0	0	0	0	0	0
0	0	0	1	1	0.9	0.45
0	0	1	0	2	1.8	0.9
0	0	1	1	3	2.7	1.35
0	1	0	0	4	3.6	1.8
0	1	0	1	5	4.5	2.25
0	1	1	0	6	5.4	2.7
0	1	1	1	7	6.3	3.15
1	0	0	0	8	7.2	3.6
1	0	0	1	9	8.1	4.05
1	0	1	0	10	9.0	4.5
1	0	1	1	11	9.9	4.95
1	1	0	0	12	10.8	5.4
1	1	0	1	13	11.7	5.85
1	1	1	0	14	12.6	6.3
1	1	1	1	15	13.5	6.75

PA OUTPUT LEVEL SELECTION

The power amplifier has 2 bits to select the output voltage level. The power-up default value is step 3 (11). V_{CC} = 3.6 V.

Table 15 PA output level selection

BIT 1	BIT 0	STEP	PA OUTPUT POWER (dB)
0	0	0	–4
0	1	1	–2
1	0	2	0
1	1	3	+2

FM PLL CENTRE FREQUENCY SHIFT SELECTION

This programming enables to shift the centre frequency of the VCO, within the FM PLL, in order to align the frequency as close as possible to the 2nd IF frequency (nominal frequency 455 kHz).

Table 16 FM PLL centre frequency shift selection

BIT 3	BIT 2	BIT 1	BIT 0	STEP	CENTRE FREQUENCY SHIFT (kHz)
0	0	0	0	0	–154
0	0	0	1	1	–132
0	0	1	0	2	–110
0	0	1	1	3	–88
0	1	0	0	4	–66
0	1	0	1	5	–44
0	1	1	0	6	–22
0	1	1	1	7	0
1	0	0	0	8	+22
1	0	0	1	9	+44
1	0	1	0	10	+66
1	0	1	1	11	+88
1	1	0	0	12	+110
1	1	0	1	13	+132
1	1	1	0	14	+154
1	1	1	1	15	+176

CLOCK DIVIDER RATIO SELECTION

The clock output signal CLKO is derived from the local oscillator LO2 and can be used to drive a microcontroller. The LO2 signal is divided with a programmable divider value. The divider is followed by a filter that controls the slew rate of the signal in order to avoid radiation noise on the PCB. The CLKO output also has the option to disable the output signal. The default value is step 1 (01).

Table 17 Clock divider ratio selection

BIT 1	BIT 0	STEP	CLOCK DIVIDER RATIO
0	0	0	output disabled
0	1	1	2.5
1	0	2	80

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.3	+6.0	V
T_{stg}	storage temperature	–55	+125	°C
T_{amb}	ambient temperature	–10	+70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	in free air	100	K/W

CHARACTERISTICS

V_{CC} = 3.6 V; T_{amb} = 25 °C; specified for US handset applications; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage		3	3.6	5.25	V
T_{amb}	ambient temperature		–10	–	+70	°C
FM receiver part						
GENERAL FM RECEIVER SYSTEM CHARACTERISTICS; note 1						
S_{RFI}	sensitivity at duplexer input (50 Ω)	matched duplexer (3 dB loss)				
		for 20 dB SINAD	–	–112	–	dBm
		for 12 dB SINAD RX mode	–	–117	–	dBm
		for 12 dB SINAD active mode	–	–116	–	dBm
THD_{FM}	total harmonic distortion	without CCITT filter	–	2.0	3.0	%
$V_{DETO(rms)}$	AC output level at pin DETO (RMS value)	$V_{i(RFI)}$ = –65 dBm	–	100	–	mV
S/N_{FM}	signal-to-noise ratio	$V_{i(RFI)}$ = –65 dBm	–	45	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LOW-NOISE AMPLIFIER; note 2						
$G_{v(LNA)}$	voltage conversion gain	from pin RFI to pin BPFI; LNA gain step 2; LNA RIN step 3	–	21	–	dB
$\Delta G_{v(LNA)}$	voltage conversion gain adjustment range	from pin RFI to pin BPFI	–	6	–	dB
$N_{steps(LNA)}$	voltage conversion gain adjust steps	from pin RFI to pin BPFI	–	4	–	
$V_{i(LNA)}$	input voltage		–125	–	–10	dBm
$CP1_{LNA(rms)}$	1 dB compression point (RMS value)	referenced to pin RFI	–	35	–	mV
F_{LNA}	noise figure	from pin RFI to pin BPFI; LNA gain step 2; LNA RIN step 3	–	3	–	dB
1ST MIXER; note 3						
$Z_{o(MX1)}$	output impedance	referenced to pin BPFI	–	330	–	Ω
$G_{cp(MX1)}$	voltage conversion gain	Z_L = 330 Ω; referenced to pin BPFI	–	11.5	–	dB
$IP3_{MX1(rms)}$	3rd-order intercept point (RMS value)	referenced to pin BPFI	–	260	–	mV
$CP1_{MX1(rms)}$	1 dB compression point (RMS value)	referenced to pin BPFI	–	100	–	mV
F_{MX1}	input referenced noise	referenced to pin BPFI	–	12	–	nV/√Hz
2ND MIXER; note 4						
$Z_{i(MX2)}$	input impedance		–	1.5	–	kΩ
$Z_{o(MX2)}$	output impedance		–	1.5	–	kΩ
$G_{cp(MX2)}$	voltage conversion gain	measured at pin MX2O				
		IP3 HIGH	–	15	–	dB
		IP3 LOW	–	18	–	dB
NF_{MX2}	noise figure from pin MX2I to pin MX2O		–	15	18	dB
$IP3_{MX2(rms)}$	3rd order intercept (RMS value)	measured at pin MX2O; referenced to pin MX2I				
		IP3 HIGH	–	210	–	mV
		IP3 LOW	–	150	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$CP1_{MX2(rms)}$	1 dB compression point (RMS value)	measured at pin MX2O; referenced to pin MX2I				
		IP3 HIGH	–	70	–	mV
		IP3 LOW	–	50	–	mV
LIMITER						
$Z_{i(LIM)}$	input impedance	f_0 = 455 kHz	–	1.5	–	kΩ
$G_{v(LIM)}$	voltage gain	f_0 = 455 kHz; $V_{i(LIM)}$ = 100 μV (RMS)	–	85	–	dB
PLL DEMODULATOR; note 5						
$\Delta f_{VCO}/\Delta V$	VCO gain	after calibration	–	50	–	kHz/V
f_{VCO}	VCO centre frequency	free running; open loop	200	455	650	kHz
$N_{step(VCO)}$	number of steps for VCO frequency adjustment		–	16	–	
$f_{VCO(st)}$	VCO centre frequency step		–	22	–	kHz
$R_{L(PLL)}$	demodulator external load on pin DETO		5	–	–	kΩ
$V_{o(PLL)(rms)}$	output voltage on pin DETO (RMS value)	$R_{L(PLL)}$ = 5 kΩ	–	–	0.4	V
RSSI CARRIER DETECTOR; note 6						
RSSI	output current dynamic range		–	65	–	dB
V_{OH}	HIGH-level output voltage at pin CDBDO	CD step 19; $V_{i(LIM)}$ = 0.1 V (RMS)	$0.9V_{CC}$	–	–	V
V_{OL}	LOW-level output voltage at pin CDBDO	$V_{i(LIM)}$ = 0 V (RMS); CD step 19	–	–	$0.1V_{CC}$	V
R_i	internal resistance	between pins RSSI and $V_{CC(RF)}$	–	170	–	kΩ
V_{det}	voltage detection		0.05	–	1.3	V
$V_{det(st)}$	voltage detection step		–	40	–	mV
V_{hys}	hysteresis voltage		–	60	–	mV
$N_{step(CD)}$	number of steps for carrier sense threshold	programmable through microcontroller	–	32	–	
DATA COMPARATOR						
$V_{ac(DATI)(p-p)}$	AC input voltage (peak-to-peak value)		75	–	–	mV
$V_{th(DATI)}$	threshold voltage on pin DATI		–	V_{CC} – 0.9	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$Z_{i(DATI)}$	input impedance at pin DATI		–	240	–	kΩ
$V_{OH(DATO)}$	HIGH-level output voltage on pin DATO	$V_{i(DATI)} = V_{CC} – 1.4$ V	$0.9V_{CC}$	–	–	V
$V_{OL(DATO)}$	LOW-level output voltage on pin DATO	$V_{i(DATI)} = V_{CC} – 0.4$ V	–	–	$0.1V_{CC}$	V
$I_{o(sink)}$	output sink current	$V_{i(DATI)} = V_{CC} – 0.4$ V; $V_{o(DATO)} = 0.1V_{CC}$	–	20	–	μA
The transmit part; note 7						
General						
THD_{TX}	total harmonic distortion after demodulation	V_{MICI} = 1 mV (RMS); CCITT filter (P53)	–	2	–	%
Summing amplifier						
$V_{o(SUM)}$	summing amplifier output voltage on pin MODO		–	–10	–	dBV
$R_{f(SUM)}$	summing amplifier external feedback resistor	between pins MODI and MODO	10	–	–	kΩ
$V_{bias(SUM)}$	DC voltage at pin MODI		–	2.4	–	V
Voltage controlled oscillator and power amplifier; note 8						
V_{PA}	PA output voltage	f_o = 49.97 MHz; PA step 3	–	2	–	dBm
$N_{step(PA)}$	number of steps of VCO output voltage		–	4	–	
$V_{o(PA)}$	PA output voltage		–4	–	+2	dB
$H2_{PA}$	attenuation 2nd harmonic		14	18	–	dB
$H3_{PA}$	attenuation 3rd harmonic		26	34	–	dB
$\frac{\Delta f}{\Delta V}$ (MODO)	VCO modulation gain	V_{MODO} = 2.4 V	–	15.5	–	kHz/V
$\frac{\Delta f}{\Delta V}$ (TXLF)	VCO gain	V_{TXLF} = 0.9 V	–	550	–	kHz/V
		V_{TXLF} = 1.2 V	–	380	–	kHz/V
$Q_{L(VCO)}$	Q factor of external L filter	L = 330 nH	40	–	–	
$N_{VCO(TX)}$	TX VCO phase noise	$f_{carrier}$ = 25 to 50 MHz				
		f_{offset} = 5 kHz	–	–96	–80	dBc/Hz
		f_{offset} = 12.5 kHz	–	–104	–87	dBc/Hz
The synthesizer						
PLL LOOP FILTER; note 9						
f_{xtal}	LO frequency		–	–	12	MHz
$C_{i(LO2)}$	parasitic capacitance between pins LO2I and LO2O		–	–	3	pF
$C_{L(LO2)}$	load capacitance between pins LO2I and LO2O		–	15	30	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{RX}	RX VCO frequency		25	–	55	MHz
$N_{VCO(RX)}$	RX VCO phase noise at pin LO2O	$f_{carrier}$ = 25 to 37 MHz				
		f_{offset} = 5 kHz	–	–96	–90	dBc/Hz
		f_{offset} = 12.5 kHz	–	–104	–98	dBc/Hz
$t_{strt(RXPLL)}$	RX PLL start time	measured by switching from inactive to active mode	–	10	–	ms
$t_{res(RXPLL)}$	RX PLL step response time	from channel 8 to channel 10; measured within ±500 Hz from final frequency	–	12	–	ms
$t_{strt(TXPLL)}$	TX PLL start time	measured by switching from inactive to active mode	–	60	–	ms
$t_{res(TXPLL)}$	TX PLL step response time	from CH 7 to CH 10; measured within ±500 Hz from final frequency	–	40	–	ms
f_{TX}	TX VCO frequency		20	–	55	MHz
$C_{o(RXPD)}$	output capacitance at pin RXPD		–	–	8	pF
$C_{o(TXPD)}$	output capacitance at pin TXPD		–	–	8	pF
The RX baseband						
RX AUDIO PATH; note 10						
ΔG_{ARX}	RX gain adjustment	programmable through microcontroller	–7.5	–	+8	dB
$N_{step(ARX)}$	RX gain adjust steps	programmable through microcontroller	–	32	–	
$\Delta G_{v(m)}$	RX mute	$V_{i(RXI)}$ = –20 dBV	–	–70	–60	dB
G_{EXP}	expander gain level	$V_{i(RXI)}$ = –20 dBV	–4	0	+4	dB
		$V_{i(RXI)}$ = –30 dBV	–14	–10	–6	dB
		$V_{i(RXI)}$ = –40 dBV	–	–20	–	dB
$Z_{i(RXI)}$	input impedance		–	15	–	kΩ
$t_{att(EXP)}$	expander attack time	C_{ECAP} = 0.47 μF	–	3.0	–	ms
$t_{rel(EXP)}$	expander release time	C_{ECAP} = 0.47 μF	–	13.5	–	ms
$\alpha_{ct(EARO)}$	compressor to expander crosstalk attenuation	from pin CMPI to pin EARO; V_{RXI} = 0 V (RMS); V_{CMPI} = –20 dBV	–	70	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EARPIECE AMPLIFIER; note 11						
$V_{o(EARO)(p-p)}$	output swing voltage (peak-to-peak value)	THD < 4%	–	2.2	–	V
G_{ear}	gain earpiece amplifier	no external resistor	–	6	–	dB
$R_{L(EARO)}$	earpiece resistance	note 12	–	150	–	Ω
THD_{ARX}	total harmonic distortion	$V_{i(RXI)}$ = –20 dBV	–	0.5	1	%
N_{ARX}	audio path noise	B = 400 Hz to 3 kHz	–	–83	–	dBV
The TX baseband						
MICROPHONE AMPLIFIER; note 13						
$V_{o(MICO)}$	output swing	R_L = 10 kΩ	–	–27	–12	dBV
ΔG_V	voltage gain adjustment		0	–	34	dB
THD_{MICO}	total harmonic distortion	f = 1 kHz; $V_{o(MICO)}$ = –12 dBV	–	0.2	–	%
TX AUDIO PATH; note 14						
G_{COMP}	compressor gain	ALC disabled				
		$V_{i(CMPI)}$ = –10 dBV	–4	0	+4	dB
		$V_{i(CMPI)}$ = –30 dBV	6	10	14	dB
		$V_{i(CMPI)}$ = –50 dBV	16	20	24	dB
$G_{COMP(max)}$	maximum compressor gain	$V_{i(CMPI)}$ = –70 dBV	–	23	–	dB
$V_{HLIM(p-p)}$	output voltage hard limiter (peak-to-peak value)	HLim disabled; ALC disabled; $V_{i(CMPI)}$ = –4 dBV	–	1.26	–	V
$V_{i(CMPI)}$	input voltage range		–	–26	–12	dBV
$V_{o(TXO)}$	output voltage	ALC normal operation				
		$V_{i(CMPI)}$ = –12 dBV	–	–12.5	–	dBV
		$V_{i(CMPI)}$ = –10 dBV	–	–12.3	–	dBV
		$V_{i(CMPI)}$ = –2.5 dBV	–	–11.5	–	dBV
THD_{COMP}	total harmonic distortion	ALC disabled; $V_{i(CMPI)}$ = –10 dBV	–	0.5	1	%
$Z_{i(CMPI)}$	input impedance		–	15	–	kΩ
$t_{att(COMP)}$	compressor attack time	C_{CCAP} = 0.47 µF	–	3.0	–	ms
$t_{rel(COMP)}$	compressor release time	C_{CCAP} = 0.47 µF	–	13.5	–	ms
$\alpha_{ct(COMP)}$	expander to compressor crosstalk attenuation	$V_{i(CMPI)}$ = 0 V (RMS); from RXI to TXO; $V_{i(RXI)}$ = –10 dBV	–	40	–	dB
$\Delta G_{v(m)}$	TX mute	ALC disabled; $V_{i(CMPI)}$ = –10 dBV	–	–70	–60	dB
ΔG_{ATX}	TX gain adjustment	programmable through microcontroller	–7.5	–	+8	dB
$N_{step(ATX)}$	TX gain adjustment steps	programmable through microcontroller	–	32	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$Z_{o(TXO)}$	output impedance at pin TXO		–	500	–	Ω
Other features						
PLL VOLTAGE REGULATOR						
$V_{ref(PLL)}$	regulated output level	before VB adjustment	2.75	3	3.25	V
		after VB adjustment	2.95	3	3.05	V
$\Delta V_{ref(PLL)}$	load regulation	V_{CC} = 3.6 V; I_o = 0 to 3 mA	–	100	–	mV
I_o	output current	V_{CC} = 3.6 V	–	–	3	mA
LOW-BATTERY DETECTOR: LBD ENABLED						
$\Delta V_{CC}/V_{CC}$	battery detection accuracy	after VB adjustment; low-battery detect level step 0	–3	–	+3	%
Characteristics of digital pins						
MICROCONTROLLER						
V_{IL}	LOW-level input voltage at pins DATA, CLK and EN		–	–	0.5	V
V_{IH}	HIGH-level input voltage at pins DATA, CLK and EN		$V_{ref(PLL)}$ – 0.5	–	$V_{CC(AU)}$	V
I_{IL}	LOW-level input current at pins DATA, CLK and EN	V_{IL} = 0.3 V	–5	–	–	μA
I_{IH}	HIGH-level input current at pins DATA, CLK and EN	$V_{IH} = V_{ref(PLL)}$ – 0.3 V	–	–	5	μA
C_i	input capacitance at pins DATA, CLK and EN		–	–	8	pF
CDBDO OUTPUT						
I_{OL}	LOW-level output current at pin CDBDO		0.7	–	–	mA
I_{OH}	HIGH-level output current at pin CDBDO		–	–	–0.7	mA
V_{OL}	LOW-level output voltage at pin CDBDO	R_L = 100 kΩ	–	–	$0.1V_{CC}$	V
V_{OH}	HIGH-level output voltage at pin CDBDO	R_L = 100 kΩ	$0.9V_{CC}$	–	–	V
TIMING (see Fig.10)						
$t_{SU;CE}$	set-up time CLK to EN	50% of signals	200	–	–	ns
$t_{SU;DC}$	set-up time DATA to CLK	50% of signals	200	–	–	ns
$t_{HD;EC}$	hold time EN to CLK	50% of signals	200	–	–	ns
f_{clk}	clock frequency		–	–	300	kHz
t_r	input rise time	10% to 90%	–	–	10	ns
t_f	input fall time	10% to 90%	–	–	10	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{END}	hold time enable at the end of a word		100	–	–	ns
t_W	input pulse width at pin EN	note 15	$1/f_{COMP}$	–	–	ns
t_{strt}	microcontroller interface start-up time	90% of $V_{ref(PLL)}$ to DATA, CLK and EN	–	–	200	µs

Notes

1. f_0 = 46.97 MHz; f_{dev} = 1.5kHz; f_{mod} = 1 kHz; LPF = 2.4 kHz at DETO; all with CCITT filter.
2. f_0 = 46.97 MHz; L = 390 nH; Q_{loaded} = 40; the input impedance and the gain of the LNA can be programmed individually (see Tables 12 and 13).
3. With 10.7 MHz filter load (input impedance 330 Ω); measured at pin MX1O.
4. f_{RF} = 10.695 MHz; f_{LO} = 10.24 MHz with 455 kHz ceramic filter load (input impedance 1500 Ω).
5. f_0 = 455 kHz; f_{dev} = 1.5kHz; f_{mod} = 1 kHz.
6. VB = 1.5 V.
7. f_0 = 49.97 MHz.
8. Voltage controlled oscillator: at pin LO3I, an inductance of 330 nH in parallel with a capacitor of 12 pF are connected to ground via a capacitor of 10 nF. Power amplifier: at PAO an inductance of 180 nH in parallel with a capacitor of 27 pF. The PAO is AC-coupled to the duplexer with a capacitor of 100 pF to filter the 2nd and 3rd harmonic.
9. PLL loop (see Fig.5): values for the RX loop filter components: C1 = 6.8 nF; C2 = 68 nF; C3 = 1.5 nF; R2 = 22 kΩ; R3 = 47 kΩ; values for the TX loop filter components: C4 = 15 nF; C5 = 150 nF; C6 = 3.9 nF; R5 = 22 kΩ; R6 = 47 kΩ.
10. RX gain adjust, RX mute and expander (see Fig.6): VB = 1.5 V; f = 1 kHz; RX gain step 15.
11. VB = 1.5 V; f = 1 kHz; no external feedback resistor; R_L = 150 Ω in series with 10 µF.
12. For stable amplifier operation.
13. VB = 1.5 V; f = 1 kHz. Gain can be adjusted with external resistors.
14. Compressor, ALC/TX mute, TX gain adjust (see Fig.8): VB = 1.5 V; f = 1 kHz; TX gain step 15.
15. The minimum pulse width should be equal to the period of the comparison frequency, depending on the country.

CHANNEL FREQUENCIES

France: CT0 base set and handset channel frequencies

Crystal frequency = 11.15 MHz; reference divider = 892; f_{ref} = 12.5 kHz; 1st IF = 10.7 MHz.

CHANNEL NUMBER	BASE SET				HANDSET			
	TX CHANNEL FREQ (MHz)	TX DIVIDER	LO1 FREQ (MHz)	RX DIVIDER	TX CHANNEL FREQ (MHz)	TX DIVIDER	LO1 FREQ (MHz)	RX DIVIDER
1	26.3125	2105	30.6125	2449	41.3125	3305	37.0125	2961
2	26.3250	2106	30.6250	2450	41.3250	3306	37.0250	2962
3	26.3375	2107	30.6375	2451	41.3375	3307	37.0375	2963
4	26.3500	2108	30.6500	2452	41.3500	3308	37.0500	2964
5	26.3625	2109	30.6625	2453	41.3625	3309	37.0625	2965
6	26.3750	2110	30.6750	2454	41.3750	3310	37.0750	2966
7	26.3875	2111	30.6875	2455	41.3875	3311	37.0875	2967
8	26.4000	2112	30.7000	2456	41.4000	3312	37.1000	2968
9	26.4125	2113	30.7125	2457	41.4125	3313	37.1125	2969
10	26.4250	2114	30.7250	2458	41.4250	3314	37.1250	2970
11	26.4375	2115	30.7375	2459	41.4375	3315	37.1375	2971
12	26.4500	2116	30.7500	2460	41.4500	3316	37.1500	2972
13	26.4625	2117	30.7625	2461	41.4625	3317	37.1625	2973
14	26.4750	2118	30.7750	2462	41.4750	3318	37.1750	2974
15	26.4875	2119	30.7875	2463	41.4875	3319	37.1875	2975

Australia: CT0 base set and handset channel frequencies

Crystal frequency = 11.15 MHz; reference divider = 892; f_{ref} = 12.5 kHz; 1st IF = 10.7 MHz.

CHANNEL NUMBER	BASE SET				HANDSET			
	TX CHANNEL FREQ (MHz)	TX DIVIDER	LO1 FREQ (MHz)	RX DIVIDER	TX CHANNEL FREQ (MHz)	TX DIVIDER	LO1 FREQ (MHz)	RX DIVIDER
1	30.075	2406	29.075	2326	39.775	3182	40.775	3262
2	30.125	2410	29.125	2330	39.825	3186	40.825	3266
3	30.175	2414	29.175	2334	39.875	3190	40.875	3270
4	30.225	2418	29.225	2338	39.925	3194	40.925	3274
5	30.275	2422	29.275	2342	39.975	3198	40.975	3278
6	30.100	2408	29.100	2328	39.800	3184	40.800	3264
7	30.150	2412	29.150	2332	39.850	3188	40.850	3268
8	30.200	2416	29.200	2336	39.900	3192	40.900	3272
9	30.250	2420	29.250	2340	39.950	3196	40.950	3276
10	30.300	2424	29.300	2344	40.000	3200	41.000	3280

Spain: CT0 base set and handset channel frequencies

Crystal frequency = 11.15 MHz; reference divider = 892; f_{ref} = 12.5 kHz; 1st IF = 10.7 MHz.

CHANNEL NUMBER	BASE SET				HANDSET			
	TX CHANNEL FREQ (MHz)	TX DIVIDER	LO1 FREQ (MHz)	RX DIVIDER	TX CHANNEL FREQ (MHz)	TX DIVIDER	LO1 FREQ (MHz)	RX DIVIDER
1	31.025	2482	29.225	2338	39.925	3194	41.725	3338
2	31.050	2484	29.250	2340	39.950	3196	41.750	3340
3	31.075	2486	29.275	2342	39.975	3198	41.775	3342
4	31.100	2488	29.300	2344	40.000	3200	41.800	3344
5	31.125	2490	29.325	2346	40.025	3202	41.825	3346
6	31.150	2492	29.350	2348	40.050	3204	41.850	3348
7	31.175	2494	29.375	2350	40.075	3206	41.875	3350
8	31.200	2496	29.400	2352	40.100	3208	41.900	3352
9	31.250	2500	29.450	2356	40.150	3212	41.950	3356
10	31.275	2502	29.475	2358	40.175	3214	41.975	3358
11	31.300	2504	29.500	2360	40.200	3216	42.000	3360
12	31.325	2506	29.525	2362	40.225	3218	42.025	3362

Netherlands: CT0 base set and handset channel frequencies

Crystal frequency = 11.15 MHz; reference divider = 892; f_{ref} = 12.5 kHz; 1st IF = 10.7 MHz.

CHANNEL NUMBER	BASE SET				HANDSET			
	TX CHANNEL FREQ (MHz)	TX DIVIDER	LO1 FREQ (MHz)	RX DIVIDER	TX CHANNEL FREQ (MHz)	TX DIVIDER	LO1 FREQ (MHz)	RX DIVIDER
1	31.0375	2483	29.2375	2339	39.9375	3195	41.7375	3339
2	31.0625	2485	29.2625	2341	39.9625	3197	41.7625	3341
3	31.0875	2487	29.2875	2343	39.9875	3199	41.7875	3343
4	31.1125	2489	29.3125	2345	40.0125	3201	41.8125	3345
5	31.1375	2491	29.3375	2347	40.0375	3203	41.8375	3347
6	31.1625	2493	29.3625	2349	40.0625	3205	41.8625	3349
7	31.1875	2495	29.3875	2351	40.0875	3207	41.8875	3351
8	31.2125	2497	29.4125	2353	40.1125	3209	41.9125	3353
9	31.2325	2499	29.4375	2355	40.1375	3211	41.9375	3355
10	31.2625	2501	29.4625	2357	40.1625	3213	41.9625	3357
11	31.2875	2503	29.4875	2359	40.1875	3215	419875	3359
12	31.3125	2505	29.5125	2361	40.2125	3217	42.0125	3361

New Zealand: CT0 base set and handset channel frequencies

Crystal frequency = 11.15 MHz; reference divider = 892; f_{ref} = 12.5 kHz; 1st IF = 10.7 MHz.

CHANNEL NUMBER	BASE SET				HANDSET			
	TX CHANNEL FREQ (MHz)	TX DIVIDER	LO1 FREQ (MHz)	RX DIVIDER	TX CHANNEL FREQ (MHz)	TX DIVIDER	LO1 FREQ (MHz)	RX DIVIDER
11	34.250	2740	29.550	2364	40.250	3220	44.950	3596
12	34.275	2742	29.575	2366	40.275	3222	44.975	3598
13	34.300	2744	29.600	2368	40.300	3224	45.000	3600
14	34.325	2746	29.625	2370	40.325	3226	45.025	3602
15	34.350	2748	29.650	2372	40.350	3228	45.050	3604
16	34.375	2750	29.675	2374	40.375	3230	45.075	3606
17	34.400	2752	29.700	2376	40.400	3232	45.100	3608
18	34.425	2754	29.725	2378	40.425	3234	45.125	3610
19	34.450	2756	29.750	2380	40.450	3236	45.150	3612
20	34.475	2758	29.775	2382	40.475	3238	45.175	3614

Korea: CT0 base set and handset channel frequencies

Crystal frequency = 10.24 MHz; reference divider = 2048; f_{ref} = 5 kHz; 1st IF = 10.695 MHz.

CHANNEL NUMBER	BASE SET				HANDSET			
	TX CHANNEL FREQ (MHz)	TX DIVIDER	LO1 FREQ (MHz)	RX DIVIDER	TX CHANNEL FREQ (MHz))	TX DIVIDER	LO1 FREQ (MHz)	RX DIVIDER
1	46.610	9322	38.970	7794	49.670	9934	35.910	7182
2	46.630	9326	39.145	7829	49.845	9969	35.930	7186
3	46.670	9334	39.160	7832	49.860	9972	35.970	7194
4	46.710	9342	39.070	7814	49.770	9954	36.010	7202
5	46.730	9346	39.175	7835	49.875	9975	36.030	7206
6	46.770	9354	39.130	7826	49.830	9966	36.070	7214
7	46.830	9366	39.190	7838	49.890	9978	36.130	7226
8	46.870	9374	39.230	7846	49.930	9986	36.170	7234
9	46.930	9386	39.290	7858	49.990	9998	36.230	7246
10	46.970	9394	39.270	7854	49.970	9994	36.270	7254
11	46.510	9302	38.995	7799	49.695	9939	35.810	7162
12	46.530	9306	39.010	7802	49.710	9942	35.830	7166
13	46.550	9310	39.025	7805	49.725	9945	35.850	7170
14	46.570	9314	39.040	7808	49.740	9948	35.870	7174
15	46.590	9318	39.055	7811	49.755	9951	35.890	7178

USA: CT0 base set and handset channel frequencies

Crystal frequency = 10.24 MHz; reference divider = 24848048; f_{ref} = 5 kHz; 1st IF = 10.695 MHz.

CHANNEL NUMBER	BASE SET				HANDSET			
	TX CHANNEL FREQ (MHz)	TX DIVIDER	LO1 FREQ (MHz)	RX DIVIDER	TX CHANNEL FREQ (MHz)	TX DIVIDER	LO1 FREQ (MHz)	RX DIVIDER
1	46.610	9322	38.975	7795	49.670	9934	35.915	7183
2	46.630	9326	39.150	7830	49.845	9969	35.935	7187
3	46.670	9334	39.165	7833	49.860	9972	35.975	7195
4	46.710	9342	39.075	7815	49.770	9954	36.015	7203
5	46.730	9346	39.180	7836	49.875	9975	36.035	7207
6	46.770	9354	39.135	7827	49.830	9966	36.075	7215
7	46.830	9366	39.195	7839	49.890	9978	36.135	7227
8	46.870	9374	39.235	7847	49.930	9986	36.175	7235
9	46.930	9386	39.295	7859	49.990	9998	36.235	7247
10	46.970	9394	39.275	7855	49.970	9994	36.275	7255
New channels								
11	43.720	8744	38.065	7613	48.760	9752	33.025	6605
12	43.740	8748	38.145	7629	48.840	9768	33.045	6609
13	43.820	8764	38.165	7633	48.860	9772	33.125	6625
14	43.840	8768	38.225	7645	48.920	9784	33.145	6629
15	43.920	8784	38.325	7665	49.020	9804	33.225	6645
16	43.960	8792	38.385	7677	49.080	9816	33.265	6653
17	44.120	8824	38.405	7681	49.100	9820	33.425	6685
18	44.160	8832	38.465	7693	49.160	9832	33.465	6693
19	44.180	8836	38.505	7701	49.200	9840	33.485	6697
20	44.200	8840	38.545	7709	49.240	9848	33.505	6701
21	44.320	8864	38.585	7717	49.280	9856	33.625	6725
22	44.360	8872	38.665	7733	49.360	9872	33.665	6733
23	44.400	8880	38.705	7741	49.400	9880	33.705	6741
24	44.460	8892	38.765	7753	49.460	9892	33.765	6753
25	44.480	8896	38.805	7761	49.500	9900	33.785	6757

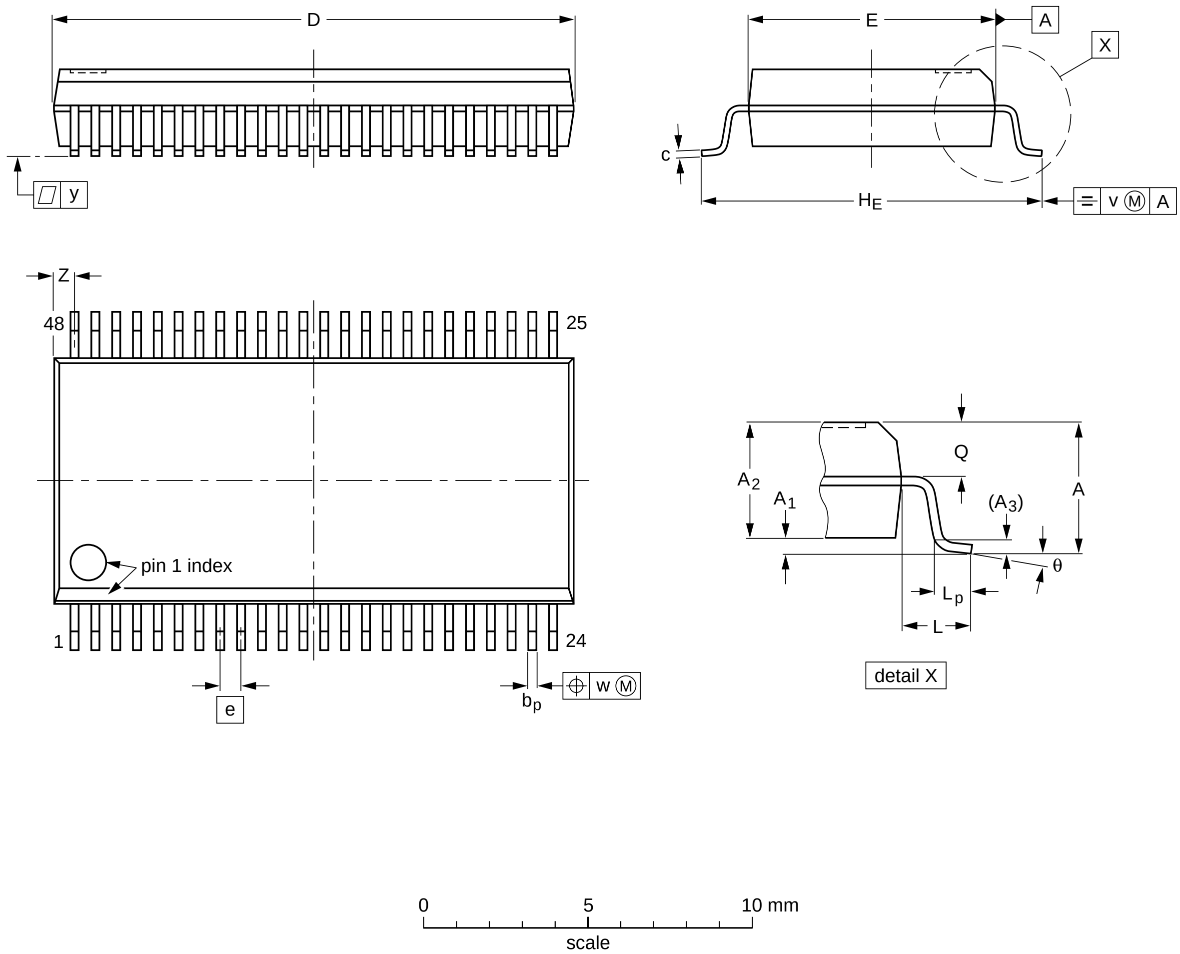
China: CT0 base set and handset channel frequencies

Crystal frequency = 10.24 MHz; reference divider = 2048; f_{ref} = 5 kHz; 1st IF = 10.695 MHz.

CHANNEL NUMBER	BASE SET				HANDSET			
	TX CHANNEL FREQ (MHz)	TX DIVIDER	LO1 FREQ (MHz)	RX DIVIDER	TX CHANNEL FREQ (MHz)	TX DIVIDER	LO1 FREQ (MHz)	RX DIVIDER
1	45.250	9050	37.550	7510	48.250	9650	34.550	6910
2	45.275	9055	37.575	7515	48.275	9655	34.575	6915
3	45.300	9060	37.600	7520	48.300	9660	34.600	6920
4	45.325	9065	37.625	7525	48.325	9665	34.625	6925
5	45.350	9070	37.650	7530	48.350	9670	34.650	6930
6	45.375	9075	37.675	7535	48.375	9675	34.675	6935
7	45.400	9080	37.700	7540	48.400	9680	34.700	6940
8	45.425	9085	37.725	7545	48.425	9685	34.725	6945
9	45.450	9090	37.750	7550	48.450	9690	34.750	6950
10	45.475	9095	37.775	7555	48.475	9695	34.775	6955

PACKAGE OUTLINE

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118				~~95-02-04~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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