UT163
USB2.0 Flash Drive Controller

Datasheet

Rev. 3.1

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USBest Technology Inc.

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Revision History

Date	Rev	Owner	Description
June 20, 2006	1.0	William Fu	Initial Release
July 5, 2006	1.01	William Fu	Update chip description in “Features” chapter
July 28, 2006	2.0	William Fu	Update L4 package pin assignment
Aug. 7, 2006	3.0	William Fu	Add 46pin QFN package
Aug. 7, 2006	3.1	William Fu	Modify 46pin QFN package outlook

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1 Overview

1.1 Description

UT163 is an Advanced Hi-speed USB Flash Disk Controller intended for supporting Flash memory device and pin-to-pin compatible with UT168/UT166/UT161. It provides enhanced read/write and power performance. With flexible firmware code design, UT163 can support comprehensive Flash technologies, including Single Level Cell (SLC), Mutli-Level Cell (MLC) NAND Flash, AG-AND, NROM and ORNAND Flash memory. It allows the manufacturer to improve device performance and maximize flexibility in flash decision.

UT163 is a highly integrated single chip for USB2.0 Flash Disk controller, it integrates USB2.0 Transceiver Macrocell Interface (UTMI), the Serial Interface Engine (SIE), one cycle 8032 compatible 8-bit micro-controller and voltage regulators. The highly integration reduces overall cost by minimizing component amount. Employed leading 0.18um CMOS technology, UT163 is the most cost and power efficient solution for manufacture.

UT163 has both of hardware and software write-protect capability to prevent writing data into flash memory unexpectedly and one LED indicator pin to show access status by three operation modes, Busy, Waiting and OFF. The auto-run function enables comprehensive driver free applications. With provided utility and mass production tool, UT163 also embodies all best value-added functions, such as customized VID/PID/Serial Number, disk partitions, boot function, and the security function to protect the data against forbid access with password identification.

With excellent compatibility, UT163 can runs smoothly on all PC platforms and support all major Flash memory. It can support Windows ME/2000/XP, Mac9.x above and Linux 2.4 above without extra driver and also support Windows 98/98SE through provided driver. UT163 is available in 64, 48 and 80 pin package. It can accommodate up to 8 flash “CE” pins in 48/64/80 pin packages.

There are 8 IO pins in 64/80pin packages and 16 OUTPUT pins in 80pin package. These 8 GPIO and 16 OUTPUT pins in 80pin package can be used as external NOR flash data and address buses respectively if “EXT_ROM_ENn” is connected to ground.

1.2 Product Information

Part No	Description	Package Type
UT163-L6	Enhanced USB2.0 Flash Drive Controller NAND flash single/dual channel access with max. 8 CE pins	64Pin LQFP 7x7x1.4 mm
UT163-T6	Green Process without special specify	64Pin TQFP 7x7x1.0 mm
UT163-L4	Enhanced USB2.0 Flash Drive Controller NAND flash single/dual channel access with 4 CE pins Green Process without special specify	48Pin LQFP 7x7x1.4 mm
UT163-Q4	Enhanced USB2.0 Flash Drive Controller NAND flash single/dual channel access with 4 CE pins Green Process without special specify	46Pin QFN 6.5x4.5x0.7 mm
UT163-LH	Enhanced USB2.0 Flash Drive Controller NAND flash single/dual channel access with max. 8 CE pins	80Pin LQFP 10x10x1.4 mm

	External NOR flash interface ready Green Process without special specify	

2 Features

- **USB Interface**
  - High-speed USB 2.0 interface; backward compatible with USB 1.1
  - Integrated USB 2.0 Transceiver Macrocell Interface (UTMI) and Serial Interface Engine (SIE)
- **Flash Interface**
  - Supports Multi-Flash, including SLC/MLC NAND, AG-AND, NROM and ORNAND Flashes
  - Support NAND flash word and byte access modes
  - Dual-channel & interleave mode support to achieve best performance
  - Supports flash chip up to 8 “CE” pins; Flash Disk capacity up to 8GB
  - Integrated ECC circuits for 4-byte error correction
- **8032 8-bit Micro-controller with enhanced feature**
  - One clock per instruction cycle
  - Embedded RAM and ROM
- **Highest data transfer rate, supports single/dual channel interleave access**
- **Hardware implemented Auto-Run feature both in “Administrator” and “User” modes**
- **Write-Protect switch for security**
- **LED indicator to show three different access status, Busy, Waiting, and Off**
- **Integrated voltage regulators to reduce BOM cost**
- **Companion user friendly utilities**
- **Customized VID/PID and serial number**
- **0.18um CMOS technology, 1.8 Volt low power core operation**
- **OS Compatibility**
  - Windows 98/ME/2000/XP, Mac9.x above and Linux kernel 2.4 above are compatible

3 Application Notes

- **UT163-L6/T6 are backward compatible with UT161-T6(G)**
  - 64pin LQFP and TQFP packages are **backward compatible with UT161-T6 part**, there is no PCB circuit change required.
  - For those new added NC pins, please contact with USBest FAEs for more detail.
- **UT163-L4 is not pin to pin compatible with UT161-T4(G). New PCB design is required.**
- **UT163-LH is not pin to pin compatible with UT161-LH(G). Existing 80 pin PCB needs minor modification to fit new pin assignment. Please contact with USBest FAEs for more detail.**

4 Block Diagram

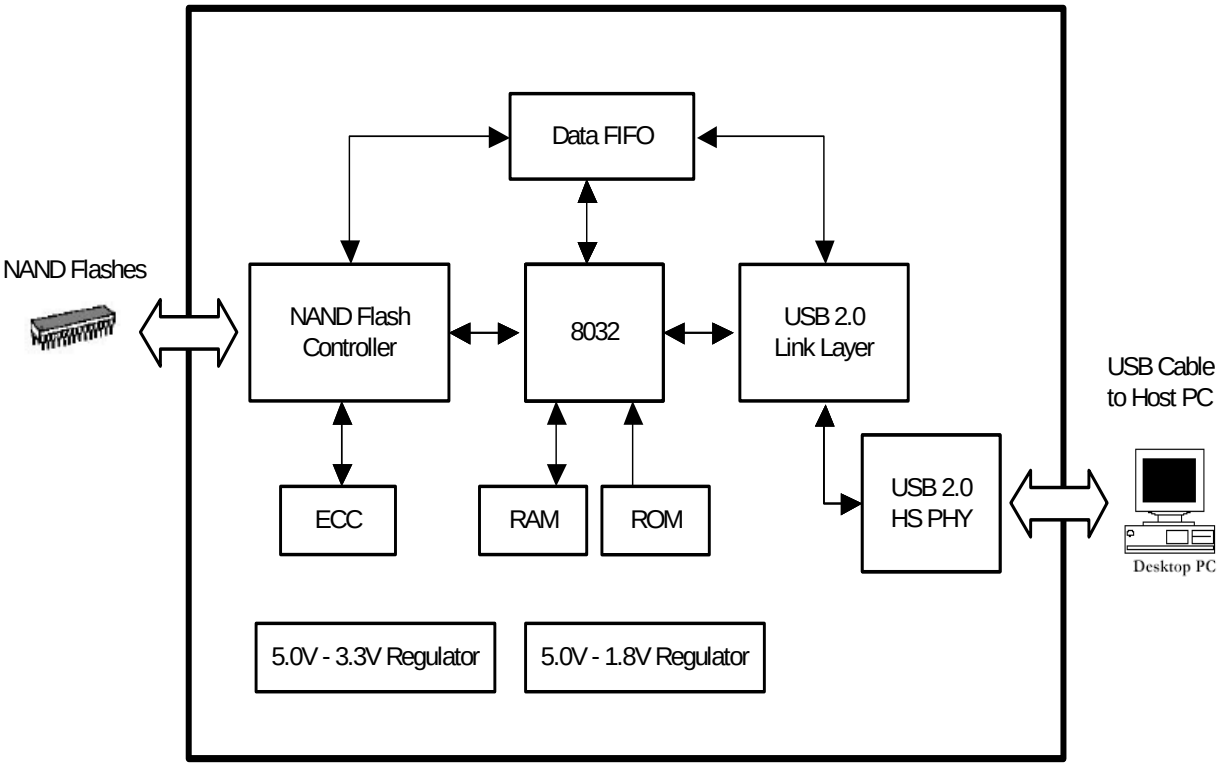
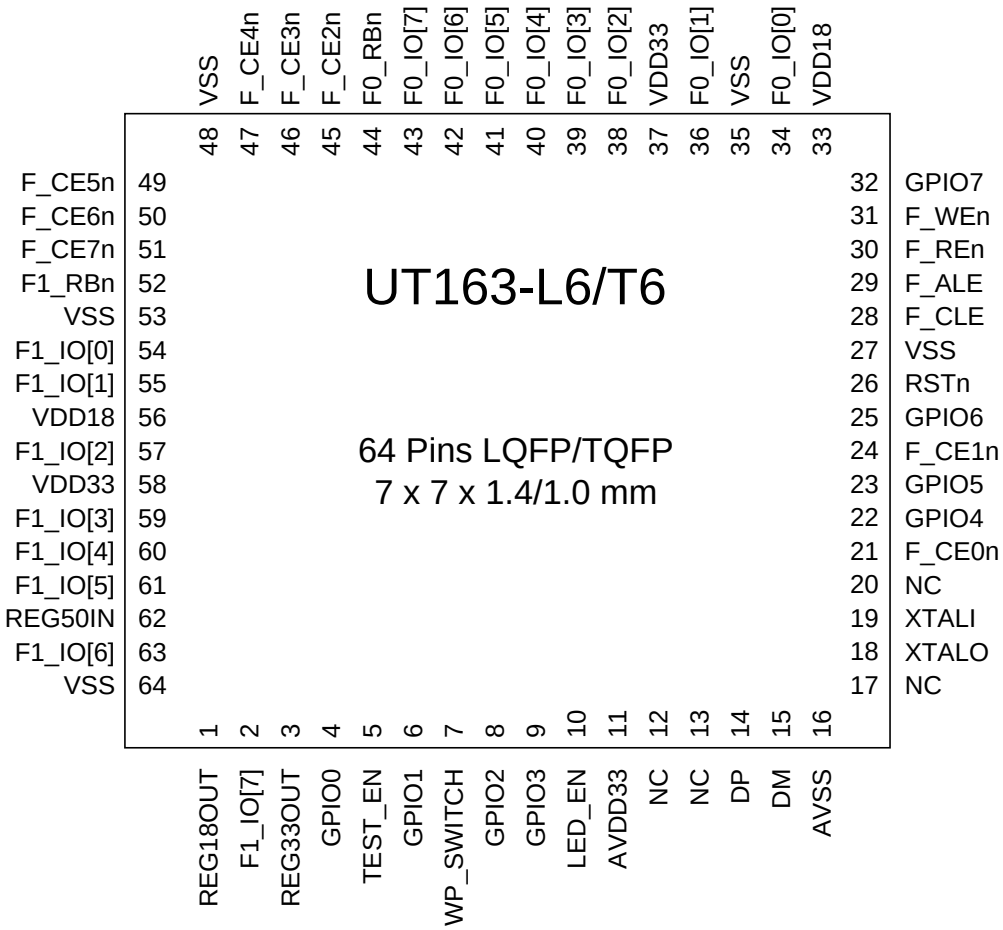


Figure 1 Block Diagram

5 Pin Assignment

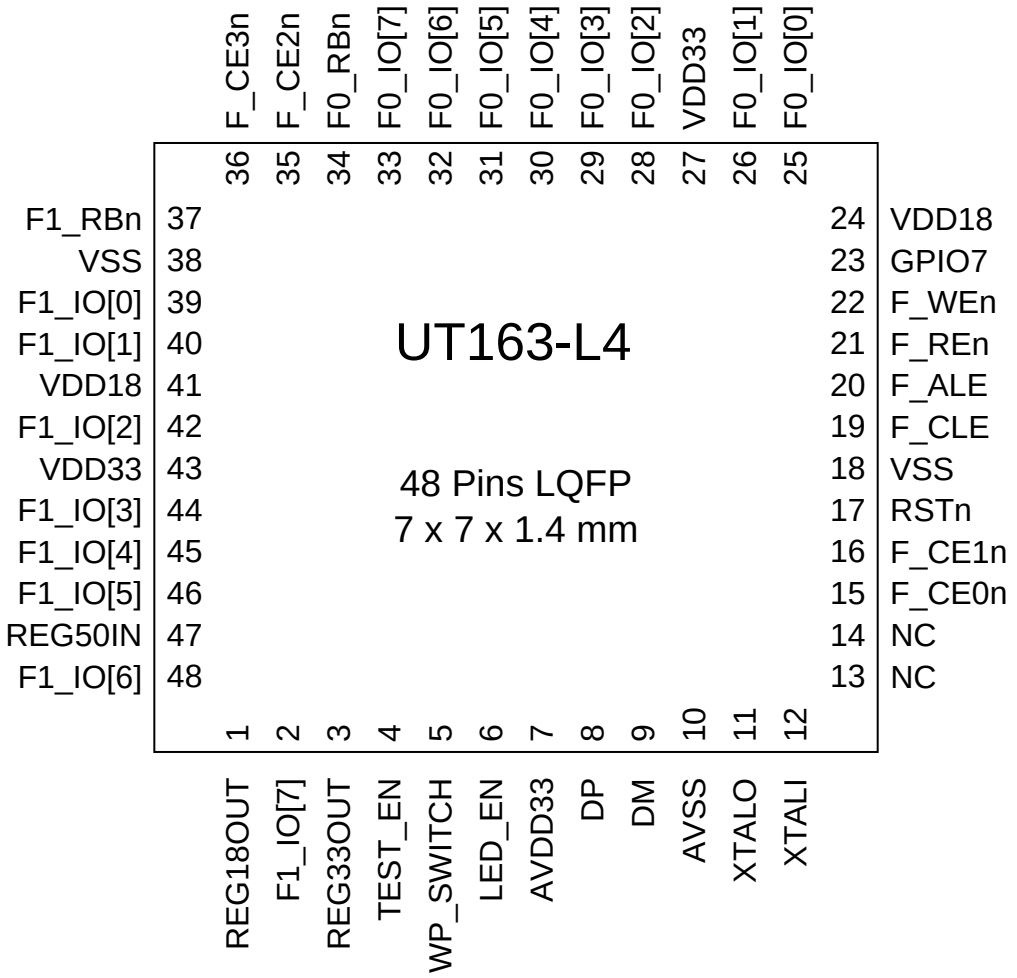
5.1 UT163-L6/T6 64Pin LQFP/TQFP Pin Assignment

Figure 2 UT163-L6/T6 Pin Assignment



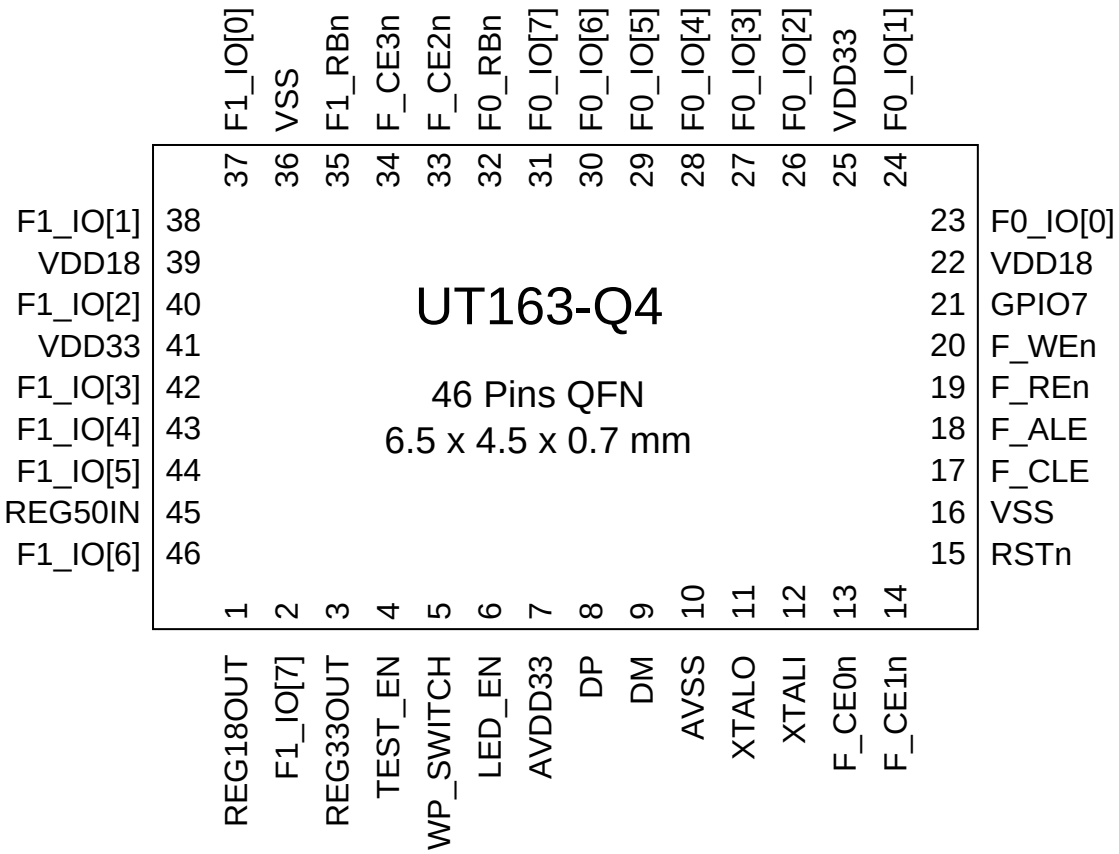
5.2 UT163-L4 48Pin LQFP Pin Assignment

Figure 3 UT163-L4 Pin Assignment



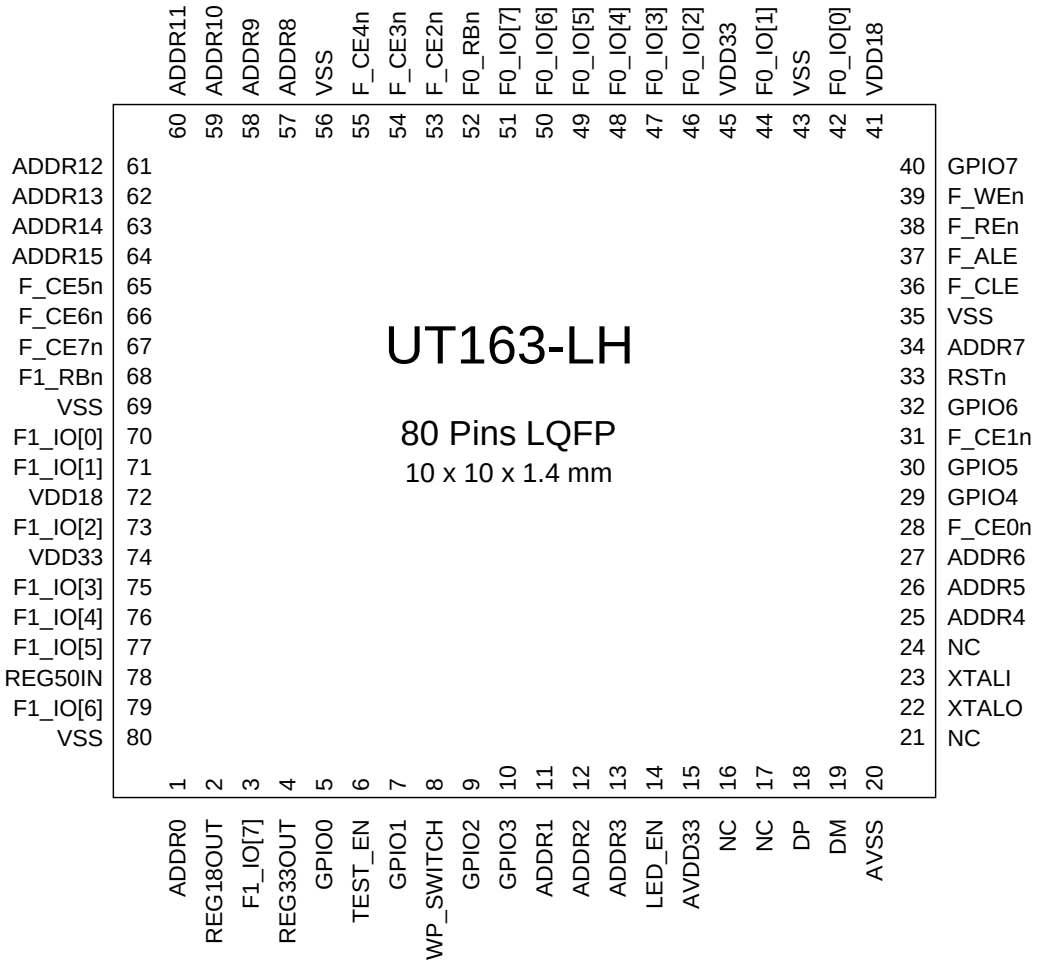
5.3 UT163-Q4 46Pin QFN Pin Assignment

Figure 4 UT163-Q4 Pin Assignment



5.4 UT163-LH 80Pin LQFP Pin Assignment

Figure 5 UT163-LH Pin Assignment



6 Pin Description

Brief UT163 pin functions are shown in the following tables.

I : Input signal

O : Output signal

I/O : Bi-direction signal

P : Power or ground signal

- : Not available

6.1 UT163-L6/T6 Pin Description

TABLE 1 UT163-L6/H6 PIN DESCRIPTION

Pin No.	Pin Name	Type	Description
1	REG18OUT	P	Regulator 1.8V Power Out (Connect External Capacitor (10 || 0.1 uF) to Ground)
2	F1_IO[7]	I/O	Group 1 Flash Data Bus - bit 7 or GPIO Bus – Port 1 bit 7
3	REG33OUT	P	Regulator 3.3V Power Out (Connect External Capacitor (10 || 0.1 uF) to Ground)
4	GPIO0	I/O	GPIO Bus – Port 3 bit 0
5	TEST_EN	I	Test Mode Enable Pin
6	GPIO1	I/O	GPIO Bus – Port 3 bit 1
7	WP_SWITCH	I	Write Protect Switch Input (active low)
8	GPIO2	I/O	GPIO Bus – Port 3 bit 2
9	GPIO3	I/O	GPIO Bus – Port 3 bit 3
10	LED_EN	O	LED Indication
11	AVDD33	P	Analog 3.3V Power
12	NC	-	NC
13	NC	-	NC
14	DP	I/O	USB Data Positive Pin
15	DM	I/O	USB Data Negative Pin
16	AVSS	P	Analog Ground
17	NC	-	NC
18	XTALO	O	Crystal Output
19	XTALI	I	Crystal Input (12 MHz)
20	NC	-	NC
21	F_CE0n	O	Flash Chip Enable - Chip 0 (active low)

Pin No.	Pin Name	Type	Description
22	GPIO4	I/O	GPIO Bus – Port 3 bit 4
23	GPIO5	I/O	GPIO Bus – Port 3 bit 5
24	F_CE1n	O	Flash Chip Enable - Chip 1 (active low)
25	GPIO6	I/O	GPIO Bus – Port 3 bit 6
26	F_WPn	O	Flash Write Protect (active low)
	RSTn	I	External Reset Pin (active low)
27	VSS	P	Logic Ground
28	F_CLE	O	Flash Command Latch Enable
29	F_ALE	O	Flash Address Latch Enable
30	F_REn	O	Flash Read Enable (active low)
31	F_WEn	O	Flash Write Enable (active low)
32	GPIO7	I/O	GPIO Bus – Port 3 bit 7
33	VDD18	P	Logic 1.8V Power
34	F0_IO[0]	I/O	Group 0 Flash Data Bus - bit 0
35	VSS	P	Logic Ground
36	F0_IO[1]	I/O	Group 0 Flash Data Bus - bit 1
37	VDD33	P	Logic 3.3V Power
38	F0_IO[2]	I/O	Group 0 Flash Data Bus - bit 2
39	F0_IO[3]	I/O	Group 0 Flash Data Bus - bit 3
40	F0_IO[4]	I/O	Group 0 Flash Data Bus - bit 4
41	F0_IO[5]	I/O	Group 0 Flash Data Bus - bit 5
42	F0_IO[6]	I/O	Group 0 Flash Data Bus - bit 6
43	F0_IO[7]	I/O	Group 0 Flash Data Bus - bit 7
44	F0_RBn	I	Group 0 Flash Ready_Busy (active low)
45	F_CE2n	O	Flash Chip Enable - Chip 2 (active low)
46	F_CE3n	O	Flash Chip Enable - Chip 3 (active low)
47	F_CE4n	O	Flash Chip Enable - Chip 4 (active low)
48	VSS	P	Logic Ground
49	F_CE5n	O	Flash Chip Enable - Chip 5 (active low)
50	F_CE6n	O	Flash Chip Enable - Chip 6 (active low)
51	F_CE7n	O	Flash Chip Enable - Chip 7 (active low)
52	F1_RBn	I	Group 1 Flash Ready_Busy (active low)
53	VSS	P	Logic Ground
54	F1_IO[0]	I/O	Group 1 Flash Data Bus - bit 0 or

Pin No.	Pin Name	Type	Description
			GPIO Bus – Port 1 bit 0
55	F1_IO[1]	I/O	Group 1 Flash Data Bus - bit 1 or GPIO Bus – Port 1 bit 1
56	VDD18	P	Logic 1.8V Power
57	F1_IO[2]	I/O	Group 1 Flash Data Bus - bit 2 or GPIO Bus – Port 1 bit 2
58	VDD33	P	Logic 3.3V Power
59	F1_IO[3]	I/O	Group 1 Flash Data Bus - bit 3 or GPIO Bus – Port 1 bit 3
60	F1_IO[4]	I/O	Group 1 Flash Data Bus - bit 4 or GPIO Bus – Port 1 bit 4
61	F1_IO[5]	I/O	Group 1 Flash Data Bus - bit 5 or GPIO Bus – Port 1 bit 5
62	REG50IN	P	Regulator 5.0V Power In
63	F1_IO[6]	I/O	Group 1 Flash Data Bus - bit 6 or GPIO Bus – Port 1 bit 6
64	VSS	P	Logic Ground

6.2 UT163-L4 Pin Description

TABLE 2 UT163-L4 PIN DESCRIPTION

Pin No.	Pin Name	Type	Description
1	REG18OUT	P	Regulator 1.8V Power Out (Connect External Capacitor (10 || 0.1 uF) to Ground)
2	F1_IO[7]	I/O	Group 1 Flash Data Bus - bit 7
3	REG33OUT	P	Regulator 3.3V Power Out (Connect External Capacitor (10 || 0.1 uF) to Ground)
4	TEST_EN	I	Test Mode Enable Pin
5	WP_SWITCH	I	Write Protect Switch Input (active low)
6	LED_EN	O	LED Indication
7	AVDD33	P	Analog 3.3V Power
8	DP	I/O	USB Data Positive Pin
9	DM	I/O	USB Data Negative Pin
10	AVSS	P	Analog Ground
11	XTALO	O	Crystal Output

Pin No.	Pin Name	Type	Description
12	XTALI	I	Crystal Input (12 MHz)
13	NC	-	NC
14	NC	-	NC
15	F_CE0n	O	Flash Chip Enable - Chip 0 (active low)
16	F_CE1n	O	Flash Chip Enable - Chip 1 (active low)
17	F_WPn RSTn	O I	Flash Write Protect (active low) External Reset Pin (active low)
18	VSS	P	Logic Ground
19	F_CLE	O	Flash Command Latch Enable
20	F_ALE	O	Flash Address Latch Enable
21	F_REn	O	Flash Read Enable (active low)
22	F_WEn	O	Flash Write Enable (active low)
23	GPIO7	I/O	GPIO Bus – Port 3 bit 7
24	VDD18	P	Logic 1.8V Power
25	F0_IO[0]	I/O	Group 0 Flash Data Bus - bit 0
26	F0_IO[1]	I/O	Group 0 Flash Data Bus - bit 1
27	VDD33	P	Logic 3.3V Power
28	F0_IO[2]	I/O	Group 0 Flash Data Bus - bit 2
29	F0_IO[3]	I/O	Group 0 Flash Data Bus - bit 3
30	F0_IO[4]	I/O	Group 0 Flash Data Bus - bit 4
31	F0_IO[5]	I/O	Group 0 Flash Data Bus - bit 5
32	F0_IO[6]	I/O	Group 0 Flash Data Bus - bit 6
33	F0_IO[7]	I/O	Group 0 Flash Data Bus - bit 7
34	F0_RBn	I	Group 0 Flash Ready_Busy (active low)
35	F_CE2n	O	Flash Chip Enable - Chip 2 (active low)
36	F_CE3n	O	Flash Chip Enable - Chip 3 (active low)
37	F1_RBn	I	Group 1 Flash Ready_Busy (active low)
38	VSS	P	Logic Ground
39	F1_IO[0]	I/O	Group 1 Flash Data Bus - bit 0
40	F1_IO[1]	I/O	Group 1 Flash Data Bus - bit 1
41	VDD18	P	Logic 1.8V Power
42	F1_IO[2]	I/O	Group 1 Flash Data Bus - bit 2
43	VDD33	P	Logic 3.3V Power
44	F1_IO[3]	I/O	Group 1 Flash Data Bus - bit 3

Pin No.	Pin Name	Type	Description
45	F1_IO[4]	I/O	Group 1 Flash Data Bus - bit 4
46	F1_IO[5]	I/O	Group 1 Flash Data Bus - bit 5
47	REG50IN	P	Regulator 5.0V Power In
48	F1_IO[6]	I/O	Group 1 Flash Data Bus - bit 6

6.3 UT163-Q4 Pin Description

TABLE 3 UT163-Q4 PIN DESCRIPTION

Pin No.	Pin Name	Type	Description
1	REG18OUT	P	Regulator 1.8V Power Out (Connect External Capacitor (10 || 0.1 uF) to Ground)
2	F1_IO[7]	I/O	Group 1 Flash Data Bus - bit 7
3	REG33OUT	P	Regulator 3.3V Power Out (Connect External Capacitor (10 || 0.1 uF) to Ground)
4	TEST_EN	I	Test Mode Enable Pin
5	WP_SWITCH	I	Write Protect Switch Input (active low)
6	LED_EN	O	LED Indication
7	AVDD33	P	Analog 3.3V Power
8	DP	I/O	USB Data Positive Pin
9	DM	I/O	USB Data Negative Pin
10	AVSS	P	Analog Ground
11	XTALO	O	Crystal Output
12	XTALI	I	Crystal Input (12 MHz)
13	F_CE0n	O	Flash Chip Enable - Chip 0 (active low)
14	F_CE1n	O	Flash Chip Enable - Chip 1 (active low)
15	F_WPn RSTn	O I	Flash Write Protect (active low) External Reset Pin (active low)
16	VSS	P	Logic Ground
17	F_CLE	O	Flash Command Latch Enable
18	F_ALE	O	Flash Address Latch Enable
19	F_REn	O	Flash Read Enable (active low)
20	F_WEn	O	Flash Write Enable (active low)
21	GPIO7	I/O	GPIO Bus – Port 3 bit 7
22	VDD18	P	Logic 1.8V Power
23	F0_IO[0]	I/O	Group 0 Flash Data Bus - bit 0

Pin No.	Pin Name	Type	Description
24	F0_IO[1]	I/O	Group 0 Flash Data Bus - bit 1
25	VDD33	P	Logic 3.3V Power
26	F0_IO[2]	I/O	Group 0 Flash Data Bus - bit 2
27	F0_IO[3]	I/O	Group 0 Flash Data Bus - bit 3
28	F0_IO[4]	I/O	Group 0 Flash Data Bus - bit 4
29	F0_IO[5]	I/O	Group 0 Flash Data Bus - bit 5
30	F0_IO[6]	I/O	Group 0 Flash Data Bus - bit 6
31	F0_IO[7]	I/O	Group 0 Flash Data Bus - bit 7
32	F0_RBn	I	Group 0 Flash Ready_Busy (active low)
33	F_CE2n	O	Flash Chip Enable - Chip 2 (active low)
34	F_CE3n	O	Flash Chip Enable - Chip 3 (active low)
35	F1_RBn	I	Group 1 Flash Ready_Busy (active low)
36	VSS	P	Logic Ground
37	F1_IO[0]	I/O	Group 1 Flash Data Bus - bit 0
38	F1_IO[1]	I/O	Group 1 Flash Data Bus - bit 1
39	VDD18	P	Logic 1.8V Power
40	F1_IO[2]	I/O	Group 1 Flash Data Bus - bit 2
41	VDD33	P	Logic 3.3V Power
42	F1_IO[3]	I/O	Group 1 Flash Data Bus - bit 3
43	F1_IO[4]	I/O	Group 1 Flash Data Bus - bit 4
44	F1_IO[5]	I/O	Group 1 Flash Data Bus - bit 5
45	REG50IN	P	Regulator 5.0V Power In
46	F1_IO[6]	I/O	Group 1 Flash Data Bus - bit 6

6.4 UT163-LH Pin Description

TABLE 4 UT163-LH PIN DESCRIPTION

Pin No.	Pin Name	Type	Description
1	ADDR0	O	External ROM Address Bus - bit 0
2	REG18OUT	P	Regulator 1.8V Power Out (Connect External Capacitor (10 || 0.1 uF) to Ground)
3	F1_IO[7]	I/O	Group 1 Flash Data Bus - bit 7 or GPIO Bus – Port 1 bit 7
4	REG33OUT	P	Regulator 3.3V Power Out (Connect External Capacitor (10 || 0.1 uF) to Ground)

Pin No.	Pin Name	Type	Description
5	GPIO0	I/O	GPIO Bus – Port 3 bit 0 or External ROM Data Bus – bit 0
6	TEST_EN	I	Test Mode Enable Pin
7	GPIO1	I/O	GPIO Bus – Port 3 bit 1 or External ROM Data Bus – bit 1
8	WP_SWITCH	I	Write Protect Switch Input (active low)
9	GPIO2	I/O	GPIO Bus – Port 3 bit 2 or External ROM Data Bus – bit 2
10	GPIO3	I/O	GPIO Bus – Port 3 bit 3 or External ROM Data Bus – bit 3
11	ADDR1	O	External ROM Address Bus - bit 1
12	ADDR2	O	External ROM Address Bus - bit 2
13	ADDR3	O	External ROM Address Bus - bit 3
14	LED_EN EXT_EN_ROMn	O I	LED Indication External ROM Enable (active low)
15	AVDD33	P	Analog 3.3V Power
16	NC	-	NC
17	NC	-	NC
18	DP	I/O	USB Data Positive Pin
19	DM	I/O	USB Data Negative Pin
20	AVSS	P	Analog Ground
21	NC	-	NC
22	XTALO	O	Crystal Output
23	XTALI	I	Crystal Input (12 MHz)
24	NC	-	NC
25	ADDR4	O	External ROM Address Bus - bit 4
26	ADDR5	O	External ROM Address Bus - bit 5
27	ADDR6	O	External ROM Address Bus - bit 6
28	F_CE0n	O	Flash Chip Enable - Chip 0 (active low)
29	GPIO4	I/O	GPIO Bus – Port 3 bit 4 or External ROM Data Bus – bit 4
30	GPIO5	I/O	GPIO Bus – Port 3 bit 5 or External ROM Data Bus – bit 5
31	F_CE1n	O	Flash Chip Enable - Chip 1 (active low)
32	GPIO6	I/O	GPIO Bus – Port 3 bit 6 or

Pin No.	Pin Name	Type	Description
			External ROM Data Bus – bit 6
33	F_WPn RSTn	O I	Flash Write Protect (active low) External Reset Pin (active low)
34	ADDR7	O	External ROM Address Bus - bit 7
35	VSS	P	Logic Ground
36	F_CLE	O	Flash Command Latch Enable
37	F_ALE	O	Flash Address Latch Enable
38	F_REn	O	Flash Read Enable (active low)
39	F_WEn	O	Flash Write Enable (active low)
40	GPIO7	I/O	GPIO Bus – Port 3 bit 7 or External ROM Data Bus – bit 7
41	VDD18	P	Logic 1.8V Power
42	F0_IO[0]	I/O	Group 0 Flash Data Bus - bit 0
43	VSS	P	Logic Ground
44	F0_IO[1]	I/O	Group 0 Flash Data Bus - bit 1
45	VDD33	P	Logic 3.3V Power
46	F0_IO[2]	I/O	Group 0 Flash Data Bus - bit 2
47	F0_IO[3]	I/O	Group 0 Flash Data Bus - bit 3
48	F0_IO[4]	I/O	Group 0 Flash Data Bus - bit 4
49	F0_IO[5]	I/O	Group 0 Flash Data Bus - bit 5
50	F0_IO[6]	I/O	Group 0 Flash Data Bus - bit 6
51	F0_IO[7]	I/O	Group 0 Flash Data Bus - bit 7
52	F0_RBn	I	Group 0 Flash Ready_Busy (active low)
53	F_CE2n	O	Flash Chip Enable - Chip 2 (active low)
54	F_CE3n	O	Flash Chip Enable - Chip 3 (active low)
55	F_CE4n	O	Flash Chip Enable - Chip 4 (active low)
56	VSS	P	Logic Ground
57	ADDR8	O	External ROM Address Bus - bit 8
58	ADDR9	O	External ROM Address Bus - bit 9
59	ADDR10	O	External ROM Address Bus - bit 10
60	ADDR11	O	External ROM Address Bus - bit 11
61	ADDR12	O	External ROM Address Bus - bit 12
62	ADDR13	O	External ROM Address Bus - bit 13
63	ADDR14	O	External ROM Address Bus - bit 14

Pin No.	Pin Name	Type	Description
64	ADDR15	O	External ROM Address Bus - bit 15
65	F_CE5n	O	Flash Chip Enable - Chip 5 (active low)
66	F_CE6n	O	Flash Chip Enable - Chip 6 (active low)
67	F_CE7n	O	Flash Chip Enable - Chip 7 (active low)
68	F1_RBn	I	Group 1 Flash Ready_Busy (active low)
69	VSS	P	Logic Ground
70	F1_IO[0]	I/O	Group 1 Flash Data Bus - bit 0 or GPIO Bus – Port 1 bit 0
71	F1_IO[1]	I/O	Group 1 Flash Data Bus - bit 1 or GPIO Bus – Port 1 bit 1
72	VDD18	P	Logic 1.8V Power
73	F1_IO[2]	I/O	Group 1 Flash Data Bus - bit 2 or GPIO Bus – Port 1 bit 2
74	VDD33	P	Logic 3.3V Power
75	F1_IO[3]	I/O	Group 1 Flash Data Bus - bit 3 or GPIO Bus – Port 1 bit 3
76	F1_IO[4]	I/O	Group 1 Flash Data Bus - bit 4 or GPIO Bus – Port 1 bit 4
77	F1_IO[5]	I/O	Group 1 Flash Data Bus - bit 5 or GPIO Bus – Port 1 bit 5
78	REG50IN	P	Regulator 5.0V Power In
79	F1_IO[6]	I/O	Group 1 Flash Data Bus - bit 6 or GPIO Bus – Port 1 bit 6
80	VSS	P	Logic Ground

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 1 shows UT163 stress ratings only. Extended exposure to the maximum ratings might degrade device reliability. Although UT163 has protective circuitry to resist damage from electrostatic discharge (ESD), precautions should always be taken to avoid high voltage or electric field.

TABLE 5 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit	Notes
Tstorage	Storage Temperature	-40	85	°C	
Ta	Ambient Operating Temperature	0	75	°C	
Vcc3	3.3V Supply Voltage	-0.3	3.6	V	
Vcc18	1.8V Supply Voltage	-0.3	2	V	
Vin3.3	3.3V Buffer Input Voltage	-0.3	3.6	V	
Vin3/5	3.3V/5V Buffer Input Voltage	-0.3	5	V	
Vin1.8	1.8V Buffer Input Voltage	-0.3	2	V	

7.2 Operating Conditions

Table 5 shows UT163 operating conditions.

TABLE 6 OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$USBV_{IN}$	USB 5V Supply Voltage	3.2	5.5	V
V_{DD33}	3.3V Supply Voltage	3.0	3.6	V
V_{DD18}	1.8V Supply Voltage	1.6	2	V

7.3 DC Characteristics

Unless otherwise noted, all test conditions are as follows:

Gnd=0V, Vcc33=3.3V±5%, Vcc18=1.8V±5%

TABLE 7 DC CHARACTERISTICS OF I/O INTERFACE

Symbol	Parameter	Min	Max	Unit	Notes
V_{IH_TTL}	TTL Input High Voltage	2	Vcc3+0.3	V	1

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL_TTL}	TTL Input Low Voltage	-0.3	0.8	V	1
V_{OH_TTL}	TTL Output High Voltage	0.9Vcc3		V	1
V_{OL_TTL}	TTL Output Low Voltage		0.45	V	1
I_{OH_TTL}	TTL Output High Current	-4		mA	1
I_{OL_TTL}	TTL Output Low Current		4	mA	1
V_{IH_USB}	USB Input High Voltage for Low-/full-speed	2.0		V	2
V_{IL_USB}	USB Input Low Voltage for Low-/full-speed		0.8	V	2
$V_{I\_USB\_DIFF}$	Differential Input Sensitivity for Low-/full-speed	TBD		V	2
$V_{I\_USB\_CM}$	Differential Common Mode Input Range for Low-/full-speed	0.8	2.5	V	2
$V_{I\_USB\_HSSQ}$	USB High-speed squelch Input detection threshold	0.1	0.15	V	2
$V_{I\_USB\_HSDSC}$	USB High-speed disconnect Input detection threshold	0.525	0.625	V	2
$V_{I\_USB\_HSCM}$	USB High-speed Signaling Common Mode Range	-0.05	0.5	V	2
V_{OH_USB}	USB Output High Voltage for Low-/full-speed	2.8	3.6	V	2
V_{OL_USB}	USB Output Low Voltage for Low-/full-speed	0	0.3	V	2
$V_{OH\_USB\_HS}$	USB Output High Voltage for High-speed	0.36	0.44	V	2
$V_{OL\_USB\_HS}$	USB Output Low Voltage for High-speed	-0.01	0.01	V	2
I_{OH_USB}	USB Output High Current for Low-/full-speed	-10		mA	2
I_{OL_USB}	USB Output Low Current for Low-/full-speed		10	mA	2
$I_{OH\_USB\_HS}$	USB Output High Current for High-speed	-40		mA	2
$I_{OL\_USB\_HS}$	USB Output Low Current for High-speed		40	mA	2

NOTES:

1. Parameter applies to following pins: TBD.
2. Parameter applies to following pins: TBD

7.4 AC Characteristics

TABLE 8 AC CHARACTERISTICS OF I/O INTERFACE

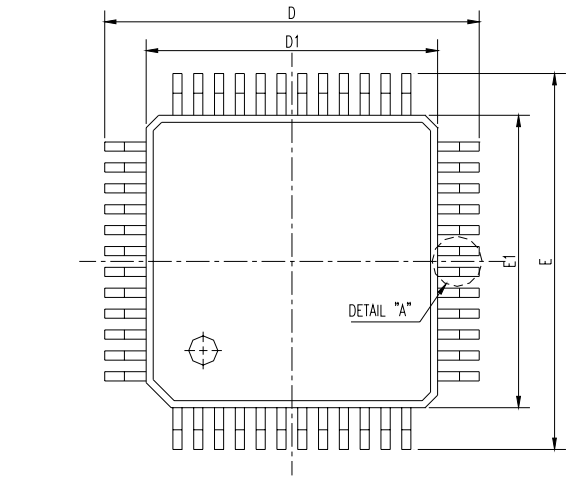
Symbol	Parameter	Min.	Typ.	Max.	Unit
TP_{ILH}	Input Rising Delay	0.61 (0.8pF)	0.72 (2.4pF)	0.92 (4.8pF)	ns

TP_{IHL}	Input falling Delay	0.88 (0.8pF)	1.03 (2.4pF)	1.24 (4.8pF)	ns
TP_{OLH}	Output Rising Delay	2.40 (10pF)	3.42 (30pF)	4.88 (60pF)	ns
TP_{OHL}	Output falling Delay	2.61 (10pF)	3.62 (30pF)	5.03 (60pF)	ns
TR	Output Rising Time	2.26 (10pF)	4.45 (30pF)	7.83 (60pF)	ns
TF	Output falling Time	1.90 (10pF)	3.63 (30pF)	6.23 (60pF)	ns

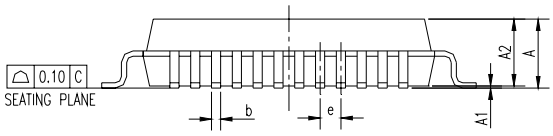
8 Mechanical Dimensions

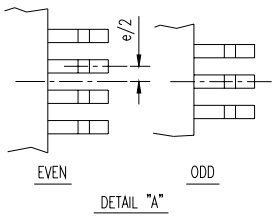
8.1 UT163-L6 64Pin LQFP Package Outline Dimension

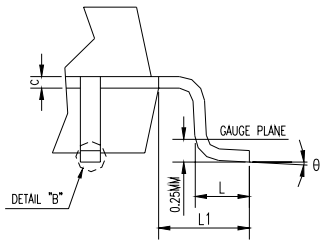
DOC No.: 0064-LQ 7.0X7.0-01-A

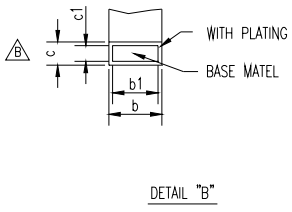


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.90	7.00	7.10	0.272	0.276	0.280
B c	0.178 TYP.			0.007 TYP.		
c1	0.127 TYP.			0.005 TYP.		
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	0	3.5	7	0	3.5	7
JEDEC						







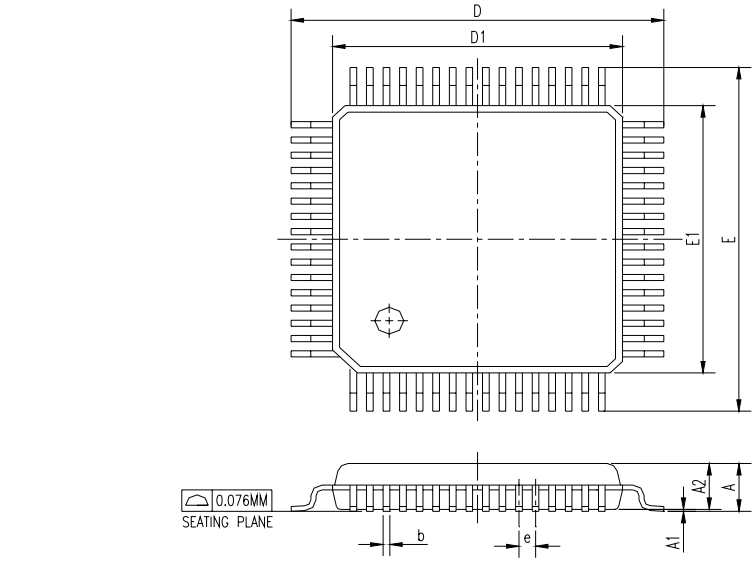


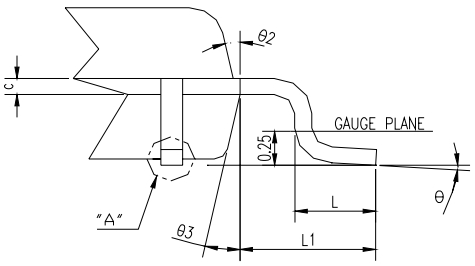
	b (MM)			b1 (MM)			e (MM)			JEDEC
N	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	
48L	0.19	0.22	0.25	0.17	0.20	0.23	0.50 BSC.			
64L	0.13	0.16	0.19	0.13	0.16	0.19	0.40 BSC.			

Figure 6 64 Pin LQFP 7.0x7.0x1.4 mm Package Outline Dimension

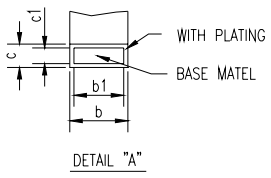
8.2 UT163-T6 64Pin TQFP Package Outline Dimension

DOC No.: 0064-TQ 7.0X7.0-01-A





SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.156			0.046
A1	0.05		0.15	0.002		0.006
A2	0.94	1.00	1.06	0.037	0.039	0.042
c	0.119		0.185	0.005		0.007
c1	0.127 TYP.			0.005 TYP.		
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.95	7.00	7.05	0.273	0.276	0.278
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.95	7.00	7.05	0.273	0.276	0.278
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	1.5	3.5	5.5	1.5	3.5	5.5
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13

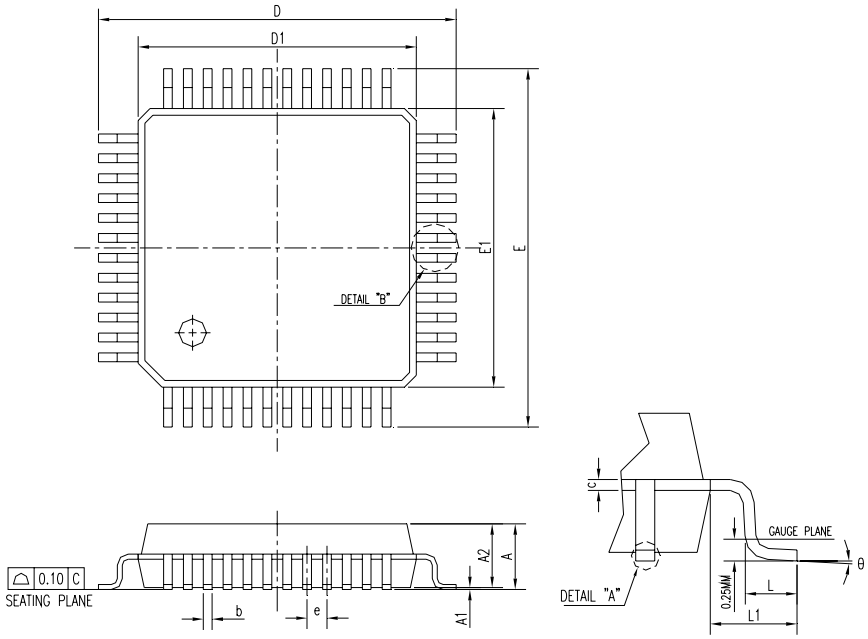


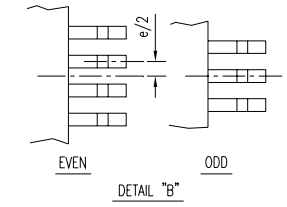
	MIN.	NOM.	MAX.	NOM.	MIN.	MAX.	NOM.	MIN.	MAX.
b	0.34		0.45	0.15		0.26	0.15		0.26
b1	0.34	0.37	0.40	0.15	0.18	0.21	0.15	0.18	0.21
e	0.80BSC.			0.50BSC.			0.40BSC.		
N	32			48			64		
JEDEC	MS-026 ABA			MS-026 ABC			MS-026 ABD		

Figure 7 64 Pin TQFP 7.0x7.0x1.0 mm Package Outline Dimension

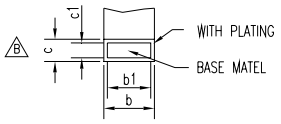
8.3 UT163-L4 48Pin LQFP Package Outline Dimension

DOC No.: 0048-LQ 7.0X7.0-01-A





SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.90	7.00	7.10	0.272	0.276	0.280
B c	0.178 TYP.			0.007 TYP.		
c1	0.127 TYP.			0.005 TYP.		
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	0	3.5	7	0	3.5	7
JEDEC						



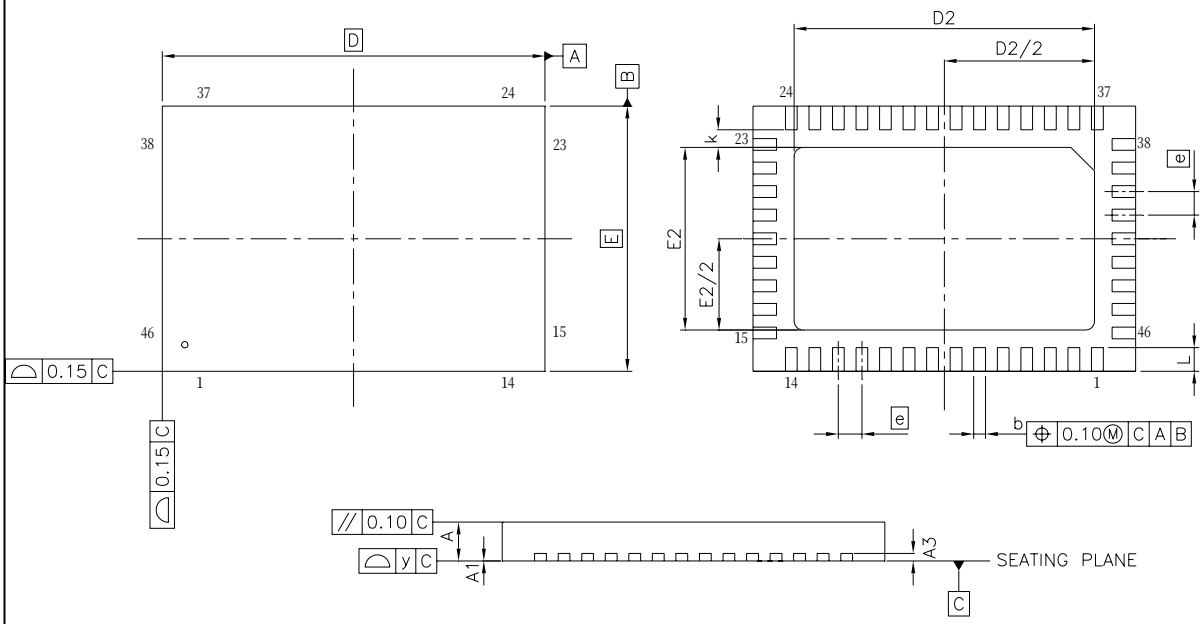
	b (MM)			b1 (MM)			e (MM)			JEDEC
N	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	
48L	0.19	0.22	0.25	0.17	0.20	0.23	0.50 BSC.			

DETAIL "A"

Figure 8 48 Pin LQFP 7.0x7.0x1.4 mm Package Outline Dimension

8.4 UT163-Q4 46Pin QFN Package Outline Dimension

DOC No.: 0046-QF 6.5X4.5-01-A

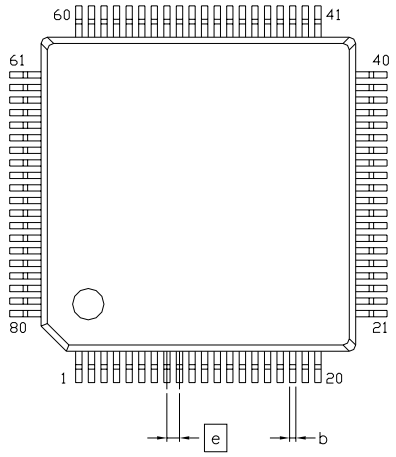


SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.61	0.66	0.70	24	26	28
A1	0	0.02	0.05	0	0.79	1.97
A3	0.127 REF			5 REF		
b	0.13	0.20	0.25	5.12	7.87	9.84
D	6.40	6.50	6.60	251.97	255.91	259.84
D2	5.00	5.10	5.20	196.85	200.79	204.72
E	4.40	4.50	4.60	173.23	177.17	181.10
E2	3.00	3.10	3.20	118.11	122.05	125.98
e	0.40 BSC			15.75 BSC		
k	0.30			11.8		
L	0.30	0.40	0.50	11.8	15.7	19.7
y	0.08			3.15		

Figure 9 46 Pin QFN 6.5 x 4.5 x 0.7 mm Package Outline Dimension

8.5 UT163-LH 80Pin LQFP Package Outline Dimension

DOC No.: 0080-LQ 10X10-01-A



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.13	0.18	0.23	5	7	9
b1	0.13	0.16	0.19	5	6	7
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	12.00 BSC			472 BSC		
D1	10.00 BSC			394 BSC		
E	12.00 BSC			472 BSC		
E1	10.00 BSC			394 BSC		
e	0.40 BSC			16 BSC		
L	0.45	0.60	0.75	18	24	30
L1	1.00 REF			39 REF		
R1	0.08			3		
R2	0.08		0,.20	3		8
Y			0,075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

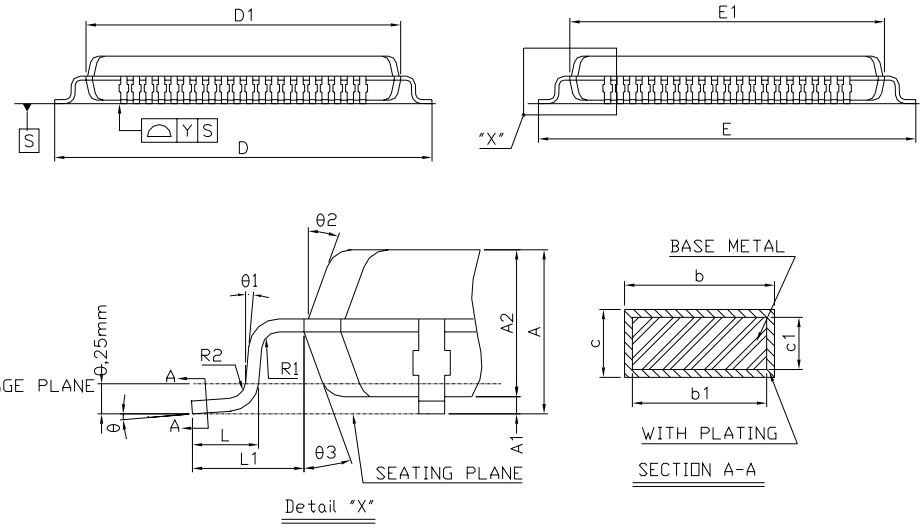


Figure 10 80 Pin LQFP 10.0x10.0x1.4 mm Package Outline Dimension

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