CIRRUS LOGIC®

CL-SH4600

Advance Product Bulletin

FEATURES

General

- Automated PC XT/AT disk controller
- Complete hardware automation of host-to-disk and disk-to-host transfers
- Automatic update of PC/AT task file registers
- Increased disk data rates with support for single- and double-bit NRZ interfaces
- 100-pin VQFP package
- Low-power, CMOS technology

Buffer Manager

- Supports streaming mode: automatic host and disk operation in the same circular buffer simultaneously with a pacing mechanism to prevent buffer overrun and underrun
- Direct buffer addressing up to 128K bytes of SRAM and 4 Mbytes of DRAM
- Buffer memory throughput of up to 16 Mbytes/second for SRAM and DRAM
- Five-channel (local microcontroller, host, disk, 'on-the-fly' correction, and DRAM refresh) circular buffer control with priority resolution
- Separate address pointers for local microcontroller, host, and disk operations
- Fixed or variable buffer segmentation with byte resolution for user-defined caching and read look-ahead
- Supports concurrent host and disk transfers from separate segments

(cont.)

Fully Automated PC XT/AT Disk Controller

OVERVIEW

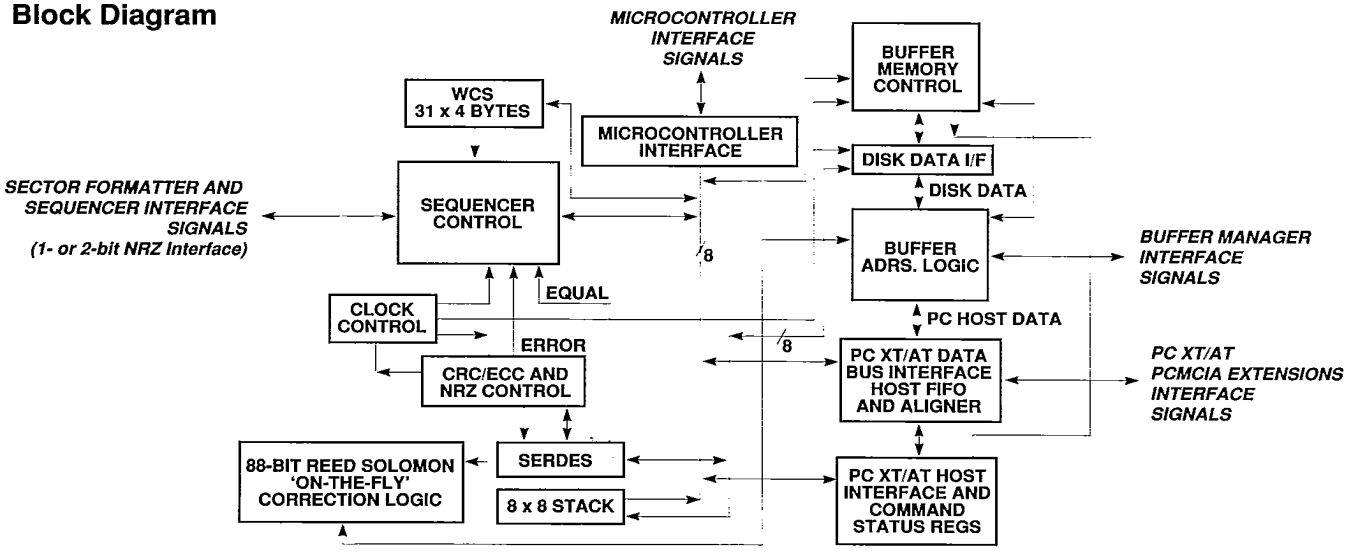
The CL-SH4600, employing Cirrus Logic's third-generation disk controller architecture, provides a large portion of the hardware necessary to build a PC XT/AT Winchester disk controller. The CL-SH4600 is typically configured with buffer memory and a microcontroller (with system RAM and ROM) to create a complete intelligent PC XT/AT Winchester disk controller. The CL-SH4600 design combines an advanced Winchester disk formatter, a five-channel buffer memory manager, and extensive hardware support for the PC XT/AT host interface.

The CL-SH4600 performs, in hardware, many of the buffer management, task file updating, and disk handling functions previously handled by firmware. The result is minimal microprocessor intervention during data transfers. The high level of automation makes the CL-SH4600 ideal for both high-performance and low-cost, single microprocessor disk drive designs.

The full streaming feature of the CL-SH4600 Buffer Manager allows the host and disk to transfer data from the same circular buffer simultaneously with a mechanism to prevent buffer overrun/underrun. Registers, pointers, and timers are updated by hardware to control the

(cont.)

Functional Block Diagram



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PC XT/AT Disk Controller

FEATURES (cont.)

- Supports multi-track minimal latency operations with correct ordering of data in the buffer
- Auto-write buffer pointer

Formatter Interface

- Single- and double-bit NRZ rates of 40 and 64 Mbits/second, respectively
- Automatic full-track read/write operations with overrun/underrun logic to stop multi-sector transfers when the buffer is full/empty
- Full-track multi-sector transfer capability without local processor intervention
- Automatic WCS branch commands automate retry algorithms and defect management
- 88-bit Reed-Solomon Error Correction Code (ECC) with enhanced 8-, 11-, 14-, 17-, or 20-bit burst automatic 'on-the-fly' hardware correction
- Split data field operation for embedded servo positioning systems
- Programmable read synchronization timeout and two-index timeout circuits for sector searches
- Programmable RAM-based disk formatter writable control store (WCS) of 31 x 4 bytes

Microcontroller Interface

- Support for high-speed processors (e.g., 16 MHz 8051, 16 MHz 68HC11, 30 MHz HPC460X3, 16 MHz 80196)
- Support for multiplexed and non-multiplexed address and data bus microcontroller interfaces
- Supports interrupt or polled processor interface
- Supports Intel®– or Motorola®-type processor register map
- Supports direct microcontroller access to buffer memory and five external switches
- Supports scheduled access to WCS and buffer memory
- Supports separate host and disk interrupt structures
- Three-level power-down capability when idle

PC XT/AT Interface

- True real time hardware and software compatibility with PC XT/AT computers
- Supports automatic update of PC/AT task file and release of data blocks
- Provides programmable logic to speed command response
- Supports automatic write and multiple-mode PC AT transfers
- Host data transfer under programmed I/O, DMA, or demand mode DMA (EISA Type 'B')
- 8- and 16-bit data transfers on the host bus
- Programmable and auto wait state generation for compatibility with any host speed
- Direct bus interface with 24-mA drivers on-chip
- AT master/slave protocol

OVERVIEW (cont.)

transfer of data between the disk and buffer and between the buffer and host without microprocessor intervention.

The automatic task file management feature updates the PC AT task file registers whenever a sector is transferred to or from the host, without generating an interrupt to the disk drive microprocessor. The CL-SH4600 provides handshake for programmed I/O or DMA data transfer on the PC XT/AT bus at rates up to 6 Mwords per second.

The CL-SH4600 Disk Formatter comprises a serializer/deserializer, a flexible RAM-based Sequencer, and CRC/ECC generation circuitry. It supports disk data rates of up to 40 Mbits per second for the single-bit NRZ interface and 64 Mbits per second for the two-bit NRZ interface. To ensure data integrity and maintain performance, the CL-SH4600 performs 88-bit Reed-Solomon Error Correction Code (ECC) with 8, 11, 14, 17, or 20-bit burst 'on-the-fly' hardware correction, while transferring disk data at a continuous 40 Mbits/second using single-bit NRZ or 64 Mbits/second using double-bit NRZ. The industry standard 16-bit CRC-CCITT for ID fields and proprietary 88-bit Reed Solomon ECC polynomial for data fields are supported in hardware. A proprietary split-data-field technique optimizes disk capacity by allowing use of embedded servo positioning systems.

The CL-SH4600 Buffer Manager controls up to 128 KBytes of SRAM and 4 Mbytes of DRAM buffer memory with five channel circular buffer control and priority resolution. The five channels supported are local microcontroller, host, disk, 'on-the-fly' correction, and DRAM refresh. The Buffer Manager supports full track multi-sector data transfers without microprocessor intervention, enabling lower-cost, single-microprocessor disk drive designs. It also allows buffer segmentation for user-defined caching algorithms or a protected-memory area in buffer memory.

The CL-SH4600 works with a local microcontroller and supports both multiplexed address and data bus architecture, similar to the Intel 8051 family and Motorola 68HC11 microcontrollers, as well as non-multiplexed bus processor architectures. Both interrupt and polled processor interface operations are supported. Extensive interrupt masking capability allows for user selection of the required disk and host interface events.

CL-SH4600

PC XT/AT Disk Controller

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ADVANTAGES

Unique Features	*Benefits*
• *Full streaming mode*	Better performance with minimal firmware and microcontroller overhead
• *Automatic task file management*	Less firmware overhead
• *DRAM Support*	Allows larger buffer sizes for better caching performance
• *Disk data rates of up to 64 Mbits/second*	Ideal for high-performance disk drive applications.
• *Reed Solomon 'on-the-fly' error correction*	Supports true 'on-the-fly' error correction during full-speed data reads.
• *Proprietary split data field support*	Optimizes disk capacity, enables use of zoned recording formats.

System Block Diagram