4th Generation USB 2.0 Flash Media Controller with Integrated Card Power FETs and HS Hub

PRODUCT FEATURES

Hub Controller

- Provides Three USB 2.0 Downstream Ports via internal USB 2.0 Hub
  - Multi Transaction Translator for FS/LS devices attached

Flash Media Controller

- Complete System Solution for interfacing SmartMedia[TM] (SM) or xD Picture Card[TM] (xD)[1], Memory Stick[TM] (MS), High Speed Memory Stick (HSMS), Memory Stick PRO (MSPRO), MS Duo[TM], Secure Digital (SD), Mini-Secure Digital (Mini-SD), TransFlash (SD), MultiMediaCard[TM] (MMC), Reduced Size MultiMediaCard (RS-MMC), NAND Flash, Compact Flash[TM] (CF) and CF Ultra[TM] I & II, and CF form-factor ATA hard drives to USB 2.0 bus
  - Supports USB Bulk Only Mass Storage Compliant Bootable BIOS
- Support for simultaneous operation of all above devices. (only one at a time of each of the following groups supported: CF or ATA drive, SM or XD or NAND, SD or MMC)
- On-Chip 4-Bit High Speed Memory Stick and MS PRO Hardware Circuitry
- On-Chip firmware reads and writes High Speed Memory Stick and MS PRO
- 1-bit ECC correction performed in hardware for maximum efficiency
- Hardware support for SD Security Command Extensions
- 3.3 Volt I/O with 5V input tolerance on VBUS, Port Power and Over-Current Sense pins
- On-chip power FETs for supplying flash media card power with minimum board components
- 8051 8 bit microprocessor
  - Provides low speed control functions
  - 30 Mhz execution speed at 4 cycles per instruction average
  - 12K Bytes of internal SRAM for general purpose scratchpad

- 768 Bytes of internal SRAM for general purpose scratchpad or program execution while re-flashing external ROM
- Double Buffered Bulk Endpoint
- Bi-directional 512 Byte Buffer for Bulk Endpoint
- 64 Byte RX Control Endpoint Buffer
- 64 Byte TX Control Endpoint Buffer
- Internal Program Memory Interface
  - 64K Byte Internal Code Space
- On Board 24Mhz Crystal Driver Circuit
- Can be clocked by an external 24MHz source
- On-Chip 1.8V Regulator for Low Power Core Operation
- Internal PLL for 480Mhz USB 2.0 Sampling, Configurable MCU clock
- 11 GPIOs for special function use: LED indicators, button inputs, power control to memory devices, etc.
  - Inputs capable of generating interrupts with either edge sensitivity
- Configuration of Hub and Flash Media features controlled either by internal defaults or via single external EEPROM. User configurable features:
  - Full or Partial Card compliance checking
  - LUN configuration and assignment
  - Write Protect Polarity
  - Cover Switch operation for xD compliance
  - Inquiry Command operation
  - SD Write Protect operation
  - Older CF card support
  - Force USB 1.1 reporting
  - Internal or External Power FET operation
- Compatible with Microsoft WinXP, WinME, Win2K SP3&4, Apple OS10 and Linux Multi-LUN Mass Storage Class Drivers
- Win2K, Win98/98SE and Apple OS8.6 and OS9 Multi-LUN Mass Storage Class Drivers are available from SMSC
- 128-Pin TQFP package (1.0mm height, 14mm x14mm footprint); lead-free RoHS compliant package also available

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1.xD Picture Card not applicable to USB2601

ORDER NUMBERS:

USB2601/USB2602-NE-XX FOR 128 PIN, TQFP PACKAGE

USB2601/USB2602-NU-XX FOR 128 PIN, TQFP LEAD-FREE ROHS COMPLIANT PACKAGE

"XX" in the order number indicates the internal ROM firmware revision level.
PLEASE CONTACT YOUR SMSC SALES REPRESENTATIVE FOR MORE INFORMATION.

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SMSC®

General Description

The USB2601/USB2602 is an Integrated "combo" High-Speed USB hub and Flash Media Controller. The Flash media controller permanently resides on Port 1 of the Integrated USB hub.

High-Speed Hub

The integrated SMSC Hub is fully compliant with the USB 2.0 Specification and will attach to a USB host as a Full-Speed Hub or as a Full-/High-Speed Hub. The Hub supports Low-Speed, Full-Speed, and High-Speed (if operating as a High-Speed Hub) downstream devices on all of the enabled downstream ports.

A dedicated Transaction Translator (TT) is available for each downstream facing port. This architecture ensures maximum USB throughput for each connected device when operating with mixed-speed peripherals.

The Hub works with an external USB power distribution switch device to control V_{BUS} switching to downstream ports, and to limit current and sense over-current conditions.

All required resistors on the USB ports are integrated into the Hub. This includes all series termination resistors on D+ and D– pins and all required pull-down and pull-up resistors on D+ and D– pins. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

Throughout this document the upstream facing port of the hub will be referred to as the upstream port, and the downstream facing ports will be called the downstream ports.

Three externally available ports are available for general USB device connectivity.

Flash Media Controller

The Bulk Only Mass Storage Class Peripheral Controller intended for supporting CompactFlash (CF and CF Ultra I/II) in True IDE Mode only, SmartMedia (SM) and XD cards, Memory Stick (MS), Memory Stick DUO (MSDUO) and Memory Stick Pro (MSPRO), Secure Digital (SD), and MultiMediaCard (MMC) flash memory devices. It provides a single chip solution for the most popular flash memory cards in the market.

The device consists of buffers, Fast 8051 microprocessor with expanded scratchpad, and program SRAM, and CF, MS, SM and SD controllers. The SD controller supports both SD and MMC devices. SM controller supports both SM and xD cards.

12K bytes of scratchpad SRAM and 768 Bytes of program SRAM are also provided.

Eleven GPIO pins are provided for indicators, external serial EEPROM for OEM ID and system configuration information, and other special functions.

Internal power FETs are provided to directly supply power to the xD/SM, MMC/SD and MS/MSPro cards.

The internal ROM program is capable of implementing any combination of single or multi-LUN CF/SD/MMC/SM/MS reader functions with individual card power control and activity indication. SMSC also provides licenses** for Win98 and Win2K drivers and setup utilities. Note: Please check with SMSC for precise features and capabilities for the current ROM code release.

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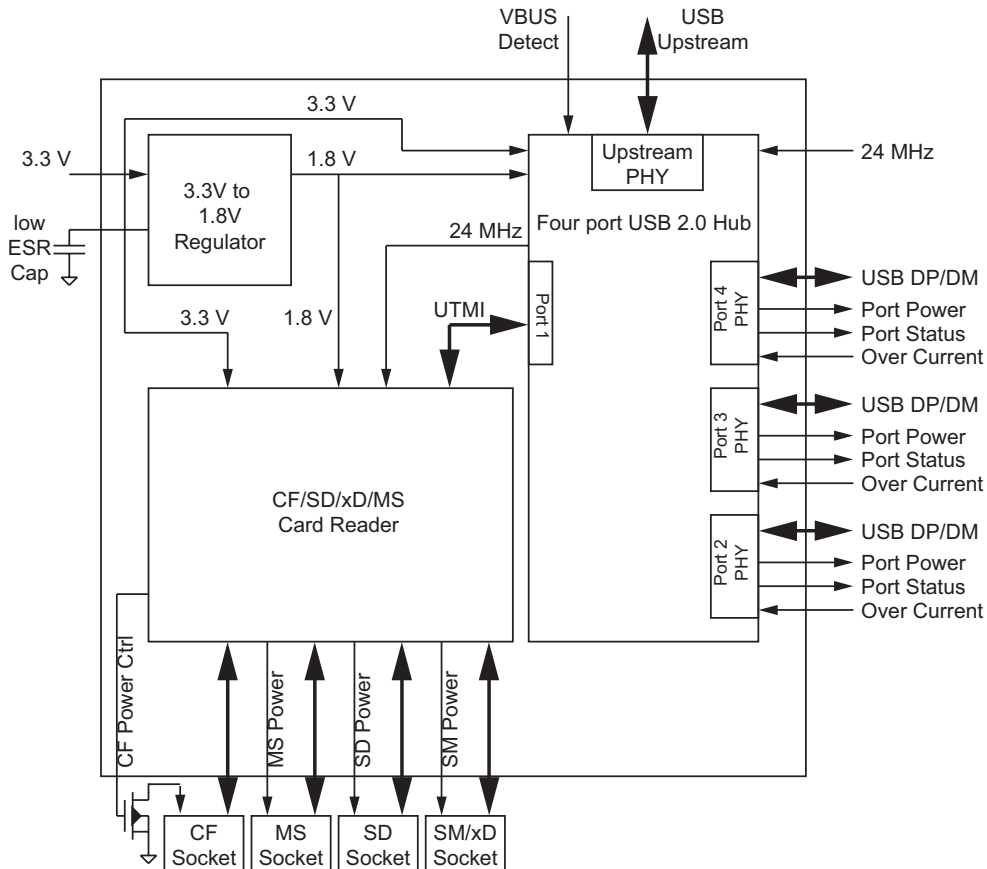
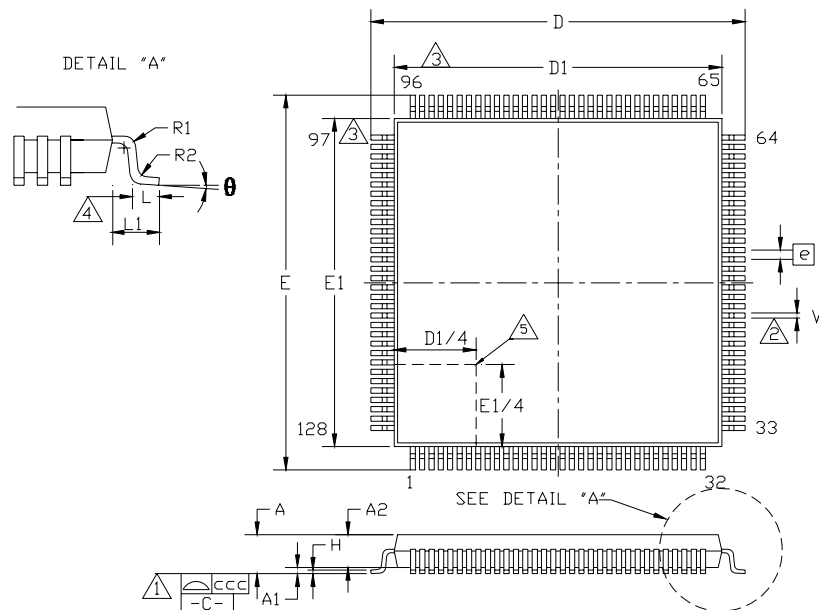# Block Diagram

Figure 1 USB2601/USB2602 Block Diagram

PRODUCT PREVIEW

Package Outline

Figure 2 USB2601/USB2602 128-Pin TQFP Package Outline

Table 1 USB2601/USB2602 128-Pin TQFP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	1.20	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	0.95	~	1.05	Body Thickness
D	15.80	~	16.20	X Span
D1	13.80	~	14.20	X body Size
E	15.80	~	16.20	Y Span
E1	13.80	~	14.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e	0.40 Basic			Lead Pitch
q	0°	~	7°	Lead Foot Angle
W	0.13	0.18	0.23	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:

1. Controlling Unit: millimeter.
2. Tolerance on the true position of the leads is ± 0.035 mm maximum.
   Package body dimensions D1 and E1 do not include the mold protrusion.
3. Maximum mold protrusion is 0.25 mm.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.

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