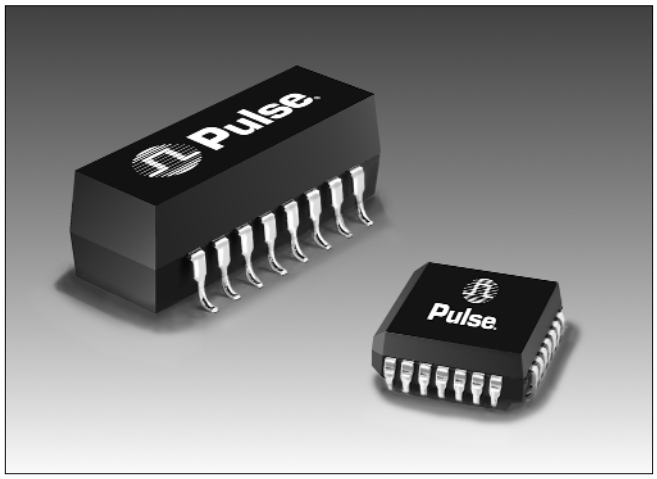
FASTPULSE MediaCAT



HIGH SPEED LAN TRANSCEIVERS

- Twisted pair transceiver kit for TP-FDDI, 100BaseTX and ATM 155 Mbps
- Matched integrated circuit and magnetic module
- Flexible, cost-effective frontend solution

Part Number	Description	Application
PE-95000	Transceiver IC	100Base-TX & TP-FDDI
PE-95010	Transceiver IC	ATM 155 Mbps
PE-68517L	Magnetic Module	100Base-TX ATM 155 Mbps TP-FDDI
PE-69016	Magnetic Module	100Base-TX

General Description

FASTPULSE *MediaCAT* (**C**hip **A**nd **T**ransformer) is a transceiver component kit which enables the design of high performance, low-cost frontends for high speed LAN products. *MediaCAT* consists of a monolithic twisted pair transceiver which implements the core Transmit/Receive signal processing and a matched magnetic module which provides the wideband transformer coupling and EMI filtering. The *MediaCAT* transceiver forms the analog interface between the digital PHY controller and the twisted pair cable (UTP-5 or STP). The matched nature of the devices and proven performance reduces the design effort and risk of implementing 100 Mbps+ frontends.

Employing *FASTPULSE* technology, the *MediaCAT* transceiver PE-95000/10 incorporates transmit conditioning, receiver adaptive equalization to compensate for cable losses and baseline restoration to correct DC drifts in receiver datastream. The two key encode/decode schemes which the ICs can implement are MLT3 (PE-95000) and Binary (PE-95010). MLT3 is a three level coding scheme which is used in TP-FDDI and 100Base-TX applications to support 125 Mbaud (100 Mbps) data transmission over 100 m of shielded (STP) or unshielded twisted pair (UTP) Category 5 cable (2 pair). Binary coding (NRZ) is used principaly for ATM 155 Mbps applications, to support 155 Mbps transmission over 100 m STP or UTP Category 5 cable. The device has a high degree of flexibility to allow it to be used in various standard applications and to enable performance tailoring for customer specific requirements.

The PE-68517L is an integrated magnetic module device designed for TP-FDDI, 10/100Base-TX and ATM155 Mbps applcations. It provides a balanced, wideband transformer with dual common mode chokes to minimize EMI emissions. The device characteristics are tuned to the *MediaCAT* transceiver resulting in an optimized device pair. For certain 10/100 Mbps applications the PE-69016 provides the 10 Mbps and 100 Mbps magnetic interface with integrated passive mixer.

MediaCAT devices meet or exceed the electrical specifications of the following standards: ANSI X3.263 TP-PMD for TP-FDDI, IEEE 802.3u for Fast Ethernet 100Base-TX and ATM-UNI-PMD STS3c for ATM 155 Mbps applications.

Features

- High performance twisted pair transceiver solution
- Flexible frontend kit for 100Base-TX, ATM 155 & TP-FDDI
- Full compliance with PMD standards IEEE, ANSI and ATM
- Supports 100m of Unshielded Twisted Pair (UTP), Category 5 or Shielded Twisted Pair (STP) cable

MediaCAT IC

- **I**ntegrates high performance and programmable adaptive equalizer
- Integrates compliant base line wander correction circuitry
- Versions for MLT3 and binary operation
- Programmable drive current
- Direct interface to PHY controllers
- EMC optimized design — edge rate control, CMRR
- BiCMOS device/PLCC28 package

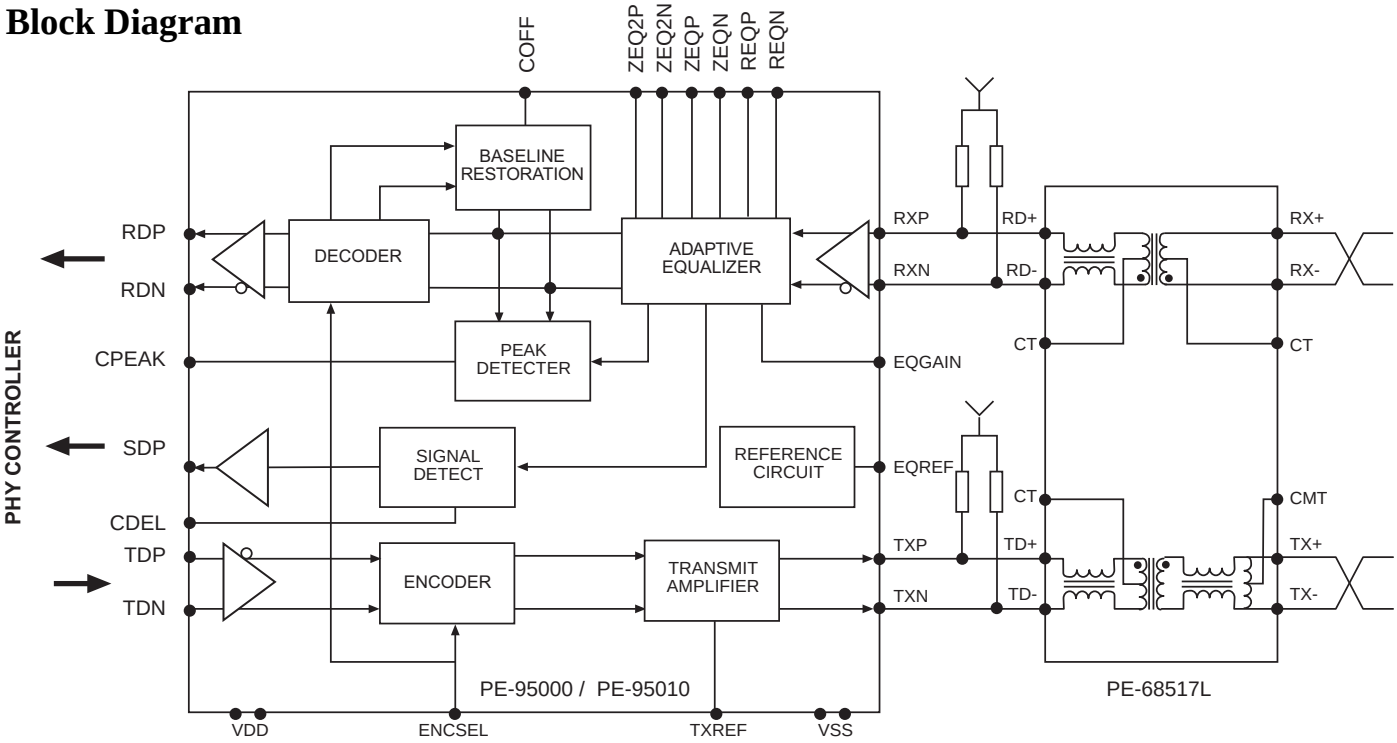
MediaCAT Magnetics

- Integrated transformer/choke device — tuned to MediaCAT IC
- Provides TX/RX wide bandwidth isolation and EMI filtering
- SMD package for IR reflow compatibility

Applications

- Network adapter cards (ISA, PCI, VME etc.)
- Hubs or concentrators
- Motherboards (PC, workstation, industrial)
- Bridges, routers, switches
- Switch uplink modules
- Point to point links (Telecom)
- Peripherals: storage, print servers, etc.

Block Diagram



Functional Description

The transmitter inputs (TDP, TDN) receive a differential data stream at pseudo ECL levels from the physical layer controller. The signal is fed to an encoder which converts the binary data (NRZI) to MLT3 format, or passes it through unencoded, (NRZ-NRZ) depending on the setting of the ENCSEL pin (see Fig. 2). The signal is then fed to a current output driver whose maximum signal amplitude is controlled by an external resistor at TXREF. The differential current output at TXP, TXN drives the cable via the transformer/Choke module. The pull-up resistors for transmit outputs effectively form the line termination for the cable (Zcable/2 since transformer is 1:1). The wide band transformers provide the high voltage isolation and exhibit a high inductance in order to minimize signal droop in presence of DC bias, i.e baseline shift. The dual common mode chokes and further decoupling schemes ensure minimal EMI emissions.

In the receive channel, the incoming differential signal from the cable passes through the transformer/choke before being terminated and fed to the RXP/RXN inputs of the IC. The termination is performed by the pull-up resistors (Zcable/2). The core function of the receiver circuitry is the adaptive equalizer which compensates for the cable losses.

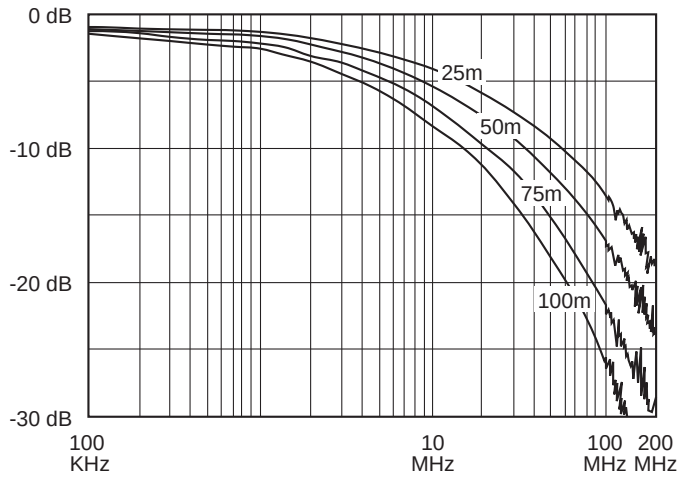
This attenuation and phase distortion will vary with frequency and cable length. These cable characteristics are defined by EIA/TIA 568 standard — Figure 1 shows typical UTP-5 cable attenuation curves which incorporate “real world” connector and punch-down block contributions, as well as typical equalizer response curve to compensate for these losses. The equalizer transfer function of PE-95000/10 is fully controlled by external components resulting in a low cost and flexible architecture. The application circuit section details the filters required (at REQP/REQPN, ZEPQ/ZEQPN and ZEQP2/ZEQPN2 pins) for standard applications over standard twisted pair cable. The effect of the external filter networks on the signal is varied from zero to full compensation by a feedback loop which senses the incoming amplitude (with peak detector) and optimizes the applied equalization.

The equalized signal is fed to the decoding circuit which converts the analog signal to a digital PECL datastream, converting from MLT3 or NRZ waveforms as selected by the ENCSEL pin. The baseline restoration loop compensates for baseline wander i.e DC drifts in incoming signal which may occur due to data pattern dependent DC shifts and the inherent low frequency bandwidth of the channel and AC coupling transformers. If not corrected this baseline wander effect can cause degradation in signal/noise ratio and furthermore, result in data errors/link failure. The feedback loop compares the incoming equalized signal with a reconstructed reference. The difference is filtered and used to effect low frequency compensation in order to maintain the equalized signal at the reference level. The filter characteristic is determined by the external capacitor at COFF. Its value has been chosen to remove disruptive high frequency components while allowing the circuit to track baseline changes limited by the time constant of the transformers. The receiver outputs are then driven out by PECL buffers to be connected to physical layer controller.

The signal detect circuit monitors the gain control to give a reliable indication of the presence of a valid equalized signal in accordance with the TP-PMD specification.

FIGURE 1

Typical UTP CAT5 Cable Loss Curves



Typical Equalizer Transfer Function

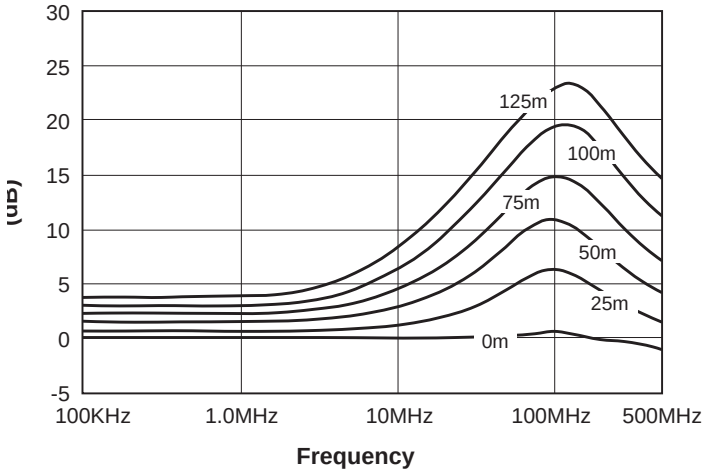
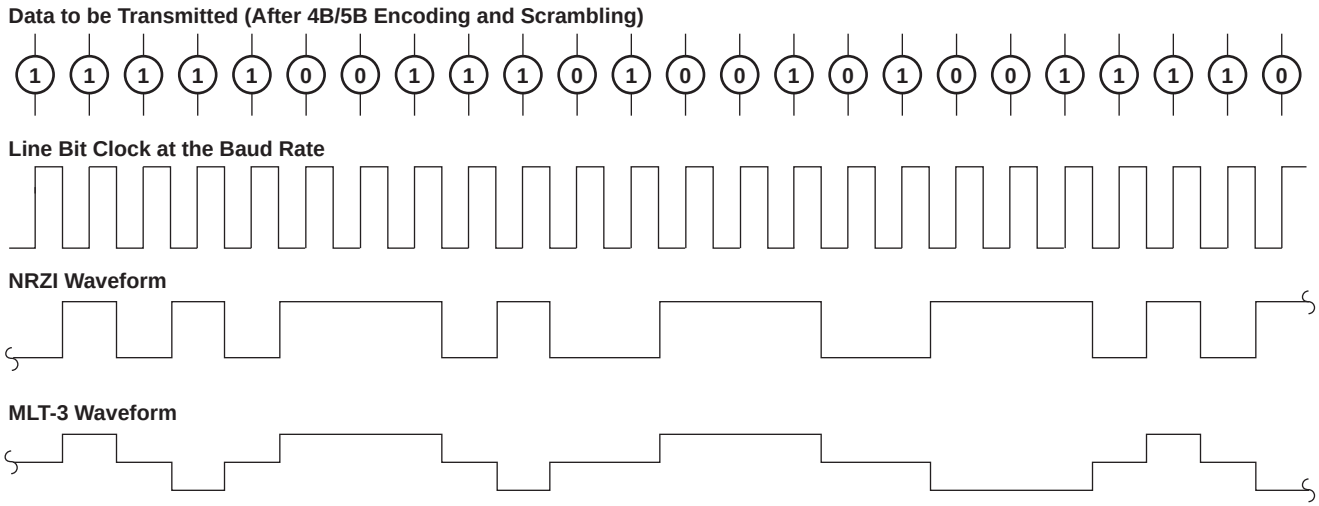
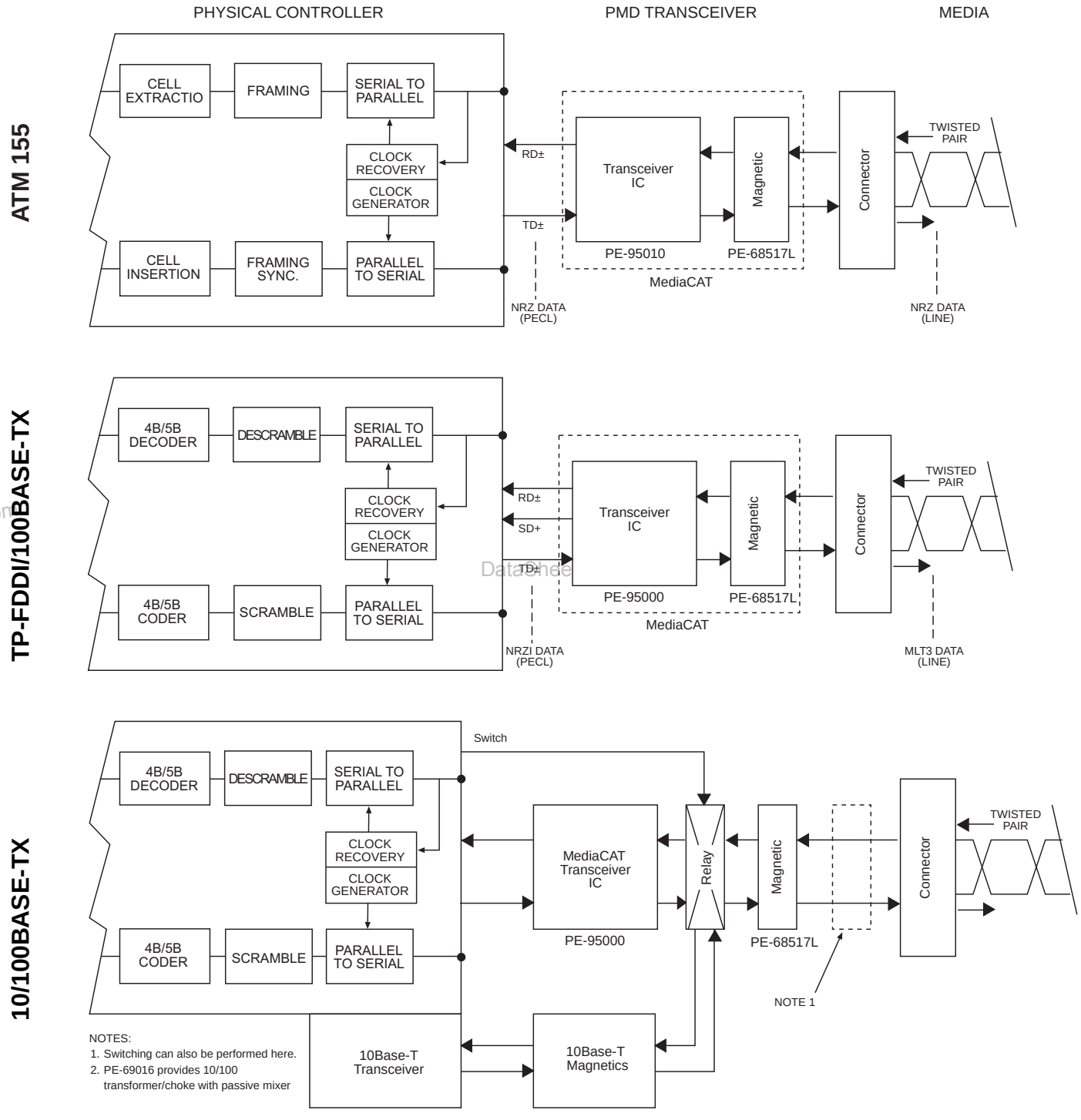


FIGURE 2 NRZI-MLT3 Line Coding



FASTPULSE MediaCAT

System Application

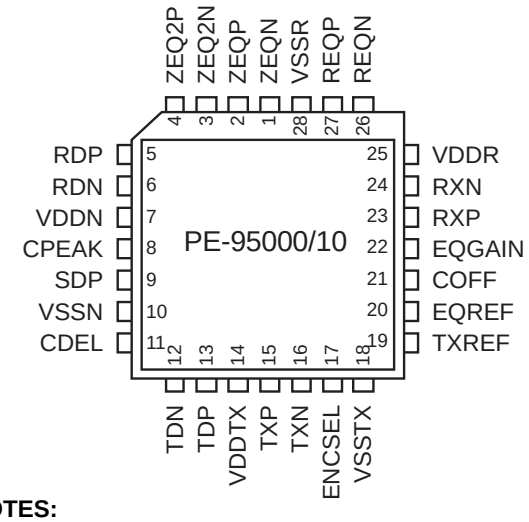


***MediaCAT* enables implementation of any of the following 100Base-TX product architectures:**

1. 100Base-TX only adapters and repeaters.
2. 10/100-TX adapters with separate 10/100 cable connectors.
3. 10/100-TX products which employ 10/100 switching (on primary or secondary of magnetics).
4. 10/100-TX products which employ common magnetic module (PE-69016) with inherent 10/100 mixing. The 10/100 system diagram indicates a generic switching arrangement.

Pin Descriptions

Signal	Pin #	Description	I/O	Type
ZEQN	1	Equalizer Network 1 - (1)	I/O	Voltage
ZEQP	2	Equalizer Network 1 + (1)	I/O	Voltage
ZEQ2N	3	Equalizer Network 2 - (2)	I/O	Voltage
ZEQ2P	4	Equalizer Network 2+ (2)	I/O	Voltage
RDP	5	Receive Data + (To controller)	O	PECL
RDN	6	Receive Data - (To controller)	O	PECL
VDDN	7	Supply Voltage (Receive)	–	Supply
CPEAK	8	Peak detector capacitor (3)	O	Current
SDP	9	Signal Detect +	O	PECL
VSSN	10	Ground (Receive)	–	Supply
CDEL	11	Signal Detect delay capacitor (4)	O	Current
TDN	12	Transmit input - (From Controller)	I	PECL
TDP	13	Transmit input + (From Controller)	I	PECL
VDDTX	14	Supply Voltage (Transmit)	–	Supply
TXP	15	Transmit Data output + (To cable)	O	Current
TXN	16	Transmit Data output - (To Cable)	O	Current
ENCSEL	17	MLT3/Binary mode select (5)	I	CMOS
VSSTX	18	Ground (Transmit)	–	Supply
TXREF	19	Transmit Amplitude reference (6)	I	Current
EQREF	20	Equalizer reference current (7)	I	Current
COFF	21	DC offset correction capacitor (8)	O	Current
EQGAIN	22	Equalizer gain control (9)	O	Current
RXP	23	Receive input + (from cable)	I	Voltage
RXN	24	Receive input - (from Cable)	I	Voltage
VDDR	25	Supply Voltage (Receive)	–	Supply
REQN	26	Equalizer gain resistor - (10)	I/O	Voltage
REQP	27	Equalizer gain resistor + (10)	I/O	Voltage
VSSR	28	Ground (Receive)	–	Supply

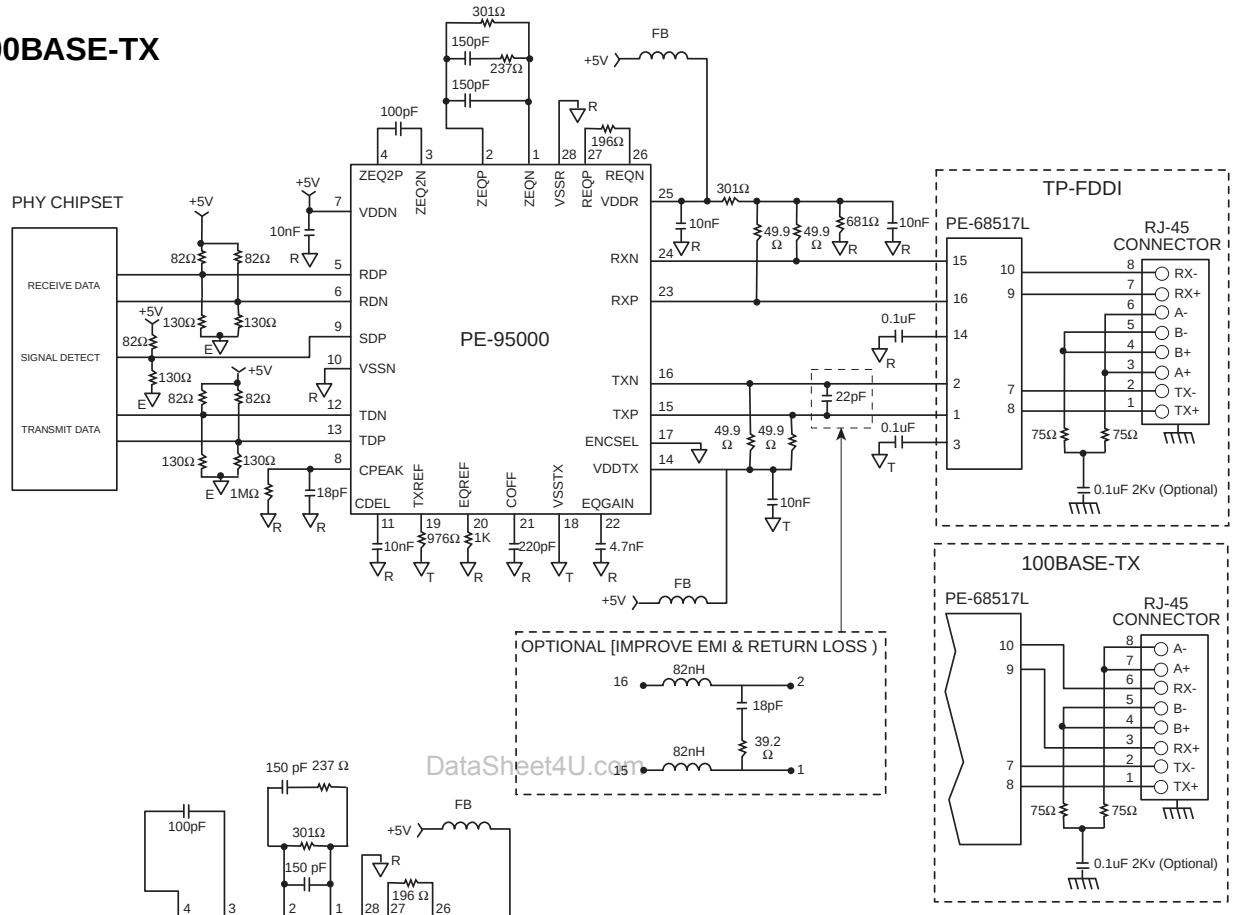


NOTES:

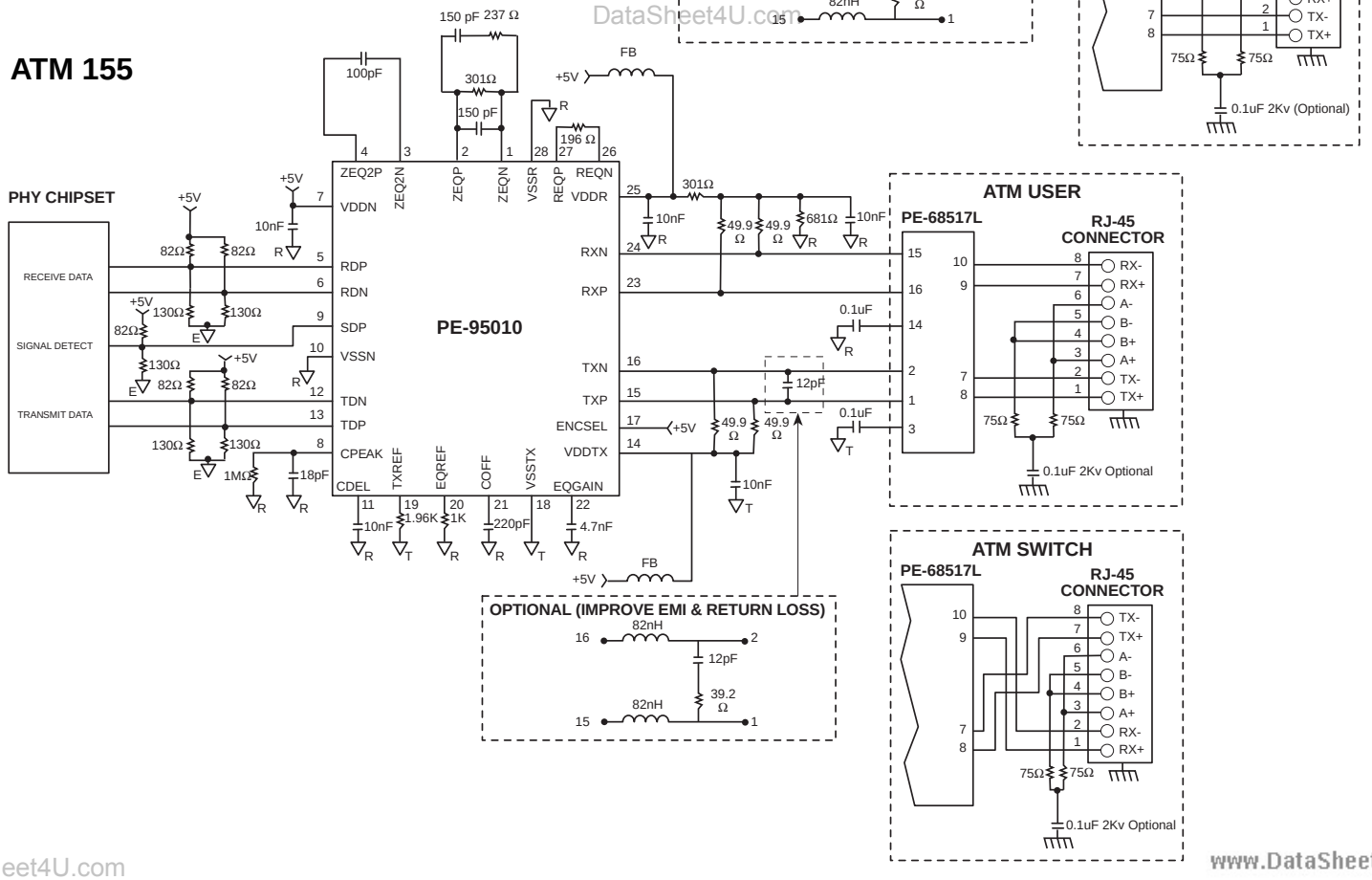
1. **ZEQP/N:** The RC network between these pins sets a frequency dependent gain which is increased linearly from zero to maximum as the equalization level increases from minimum to maximum.
2. **ZEQ2P/N:** The RC network between these pins sets a frequency dependent gain which is increased linearly from zero to maximum as the equalization level increases from its mid point to maximum. This provides gain boost for longer lengths of cable.
3. **CPEAK:** The RC network at CPEAK pin control the frequency response of the on chip peak detector.
4. **CDEL:** The capacitor at CDEL delays assertion of the SD signal to allow the equalizer to stabilize. Max assert time (us)=C(EQGAIN)(nF)X40 + C(CDEL)(nF)X25.
5. **ENCSEL:** TTL compatible CMOS selection pin of encode/decode mode. High = Binary, Low = MLT3.
6. **TXREF:** Resistor controls the amplitude of the current outputs, which determines the transmit signal voltage amplitude. For the total system (Chip + Transformer), the resistor value can be determined as follows: R(TXREF) = (20 x Zcable) / Vpp where Vpp = peak-peak differential amplitude (line output) (V) Zcable = Characteristic differential cable impedance
7. **EQREF:** The resistor at EQREF pin sets internal reference currents for the receiver circuitry.
8. **COFF:** Capacitor determines time constant of BLW loop.
9. **EQGAIN:** Indicates gain factor of equalizer. The capacitor at this pin determines the maximum SD deassert time. Maximum deassert time (us) = C(EQGAIN) (nF) x 20
10. **REQP/N:** The resistor at REQP/N sets the minimum signal gain through the equalizer.

Application Circuits

TP-FDDI/100BASE-TX

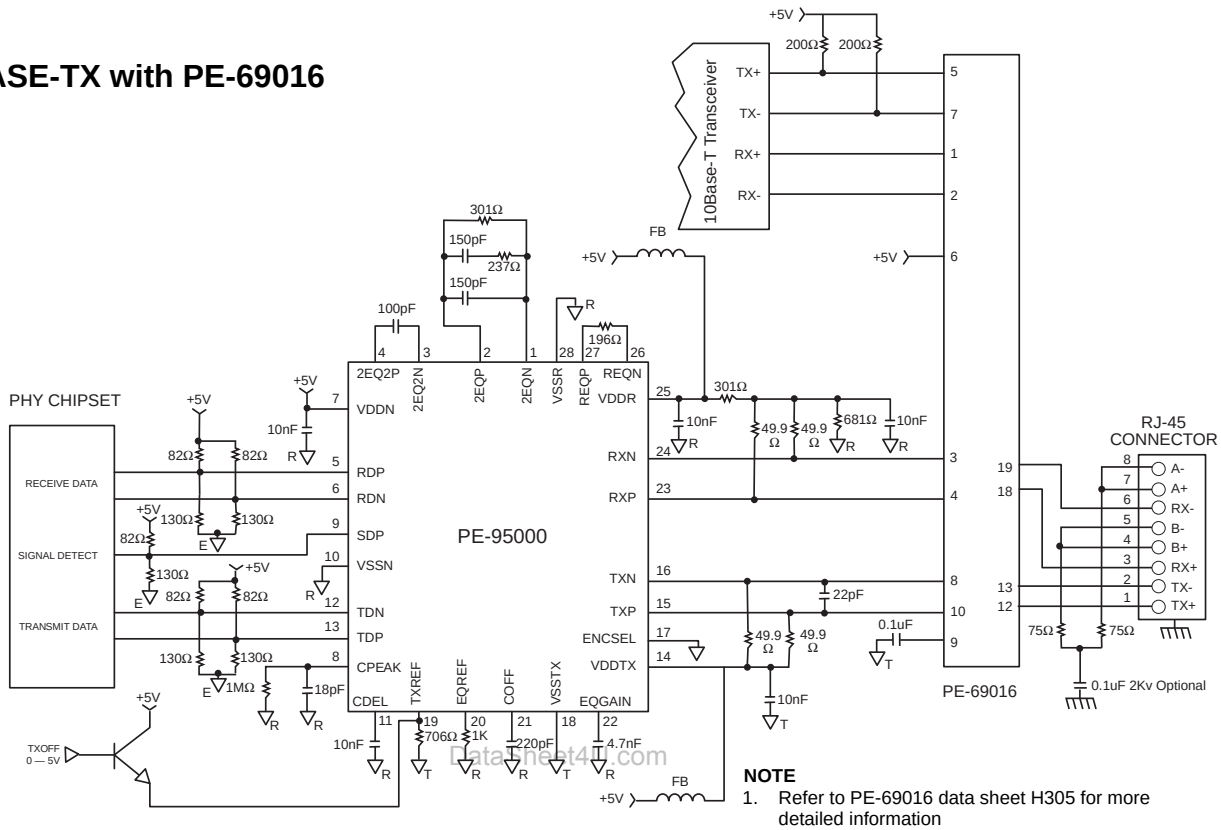


ATM 155



Application Circuit

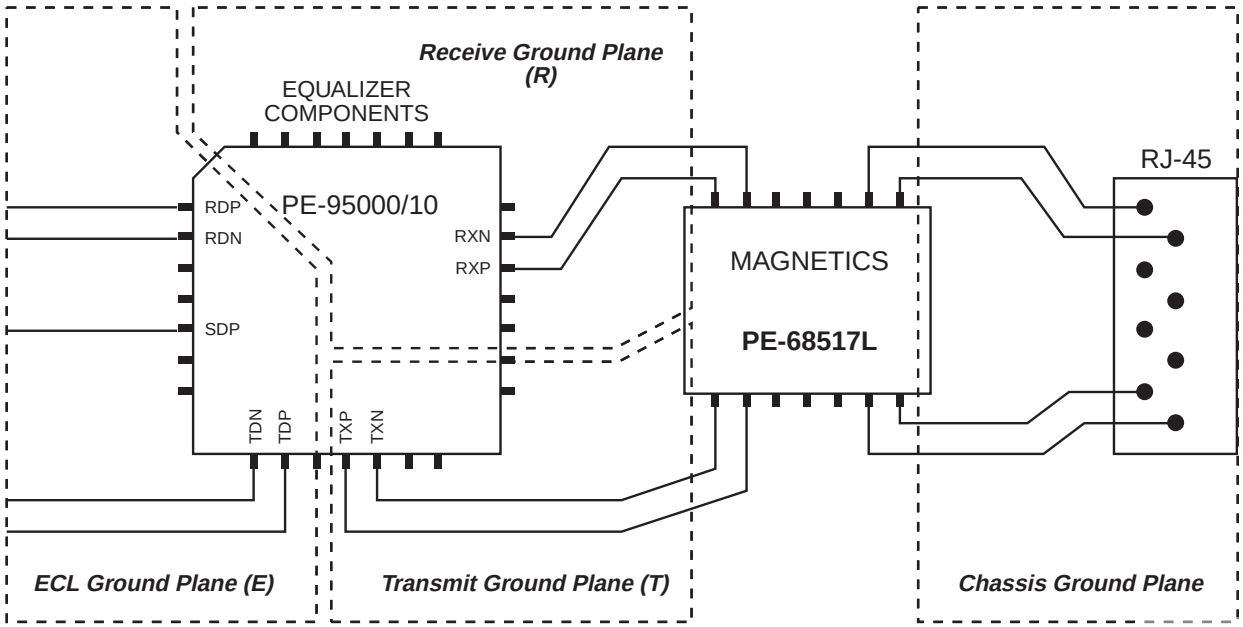
10/100BASE-TX with PE-69016



NOTE

1. Refer to PE-69016 data sheet H305 for more detailed information

Layout Guide



Application Notes

1 TP-FDDI/100Base-TX UTP-5 application circuit shows RJ45 pinout for TP-FDDI application with 100Base-TX pinout shown in the insert box.

2 ATM 155 Mbps UTP-5 application circuit shows RJ45 pinout for adapter (user) node with pinout for ATM switch (equipment) node shown in the insert box.

3 All resistors are 1% tolerance, capacitors 5% except for bypass capacitors.

4 The equalizer components connected to REQP/N, ZEQP/N, ZEQ2P/N are sensitive and should be placed as close as possible to the pins to avoid coupling high frequency noise into the receiver signal path. Keep area in immediate vicinity of these signals as free as possible of other signal routing. Keep layout as symmetric as possible to avoid uneven parasitic loading.

5 PCB traces connecting external components to TXREF, EQREF, COFF and CPEAK pins should also be kept as short as possible.

6 The termination resistors on the receiver inputs must be connected to a common mode voltage of 3.5 V. This is generated from the receiver 5 V supply by the divider network shown. Decoupling of this voltage is recommended for noise immunity.

7 The transmit signal rise-time can be adjusted by a shunt capacitor between signals TXP and TXN. The capacitor values shown result in Tr~3.7 ns for TP-FDDI/100Base-TX and Tr~2.8ns for ATM155 to comply with the relevant standards.

8 The PECL termination networks shown (Thevenin 50 Ω) are typical. Signal traces should be effective 50 Ω transmission lines. Other suitable termination schemes may be used.

9 Place termination networks near input data pins of Transceiver (TD) and PHY device (SD,RD) for optimum termination .

10 For controller chipsets with differential SD inputs, the unused SD- signal can be terminated with a divider network of 68 Ω to Vcc/180 Ω to ground.

11 Make all differential signal paths short and of the same length to avoid unbalancing effects and unwanted loops.

12 Decouple Vcc signals thoroughly close to IC. Use series ferrite beads and ideally a 10 µF tantalum may be placed in parallel with the 0.1 µF low inductance ceramic bypass capacitor. Device ground pins should be directly connected to low impedance ground plane.

13 For TP-FDDI over STP (150 Ω) applications, the followiing modifications are required: R (Txref) = 1.21K; R (REQP/REQN) = 261 Ω; Receiver termination = 2X 75 Ω; Transmit termination = 2 X 75 Ω. Pinout of DB9 connector is as follows — Transmit: TX+ = P5, TX- = P9; Receive: RX+ = P1, RX- = P6. There is no need to consider termination of unused pairs because of the inherent shielding of the cable.

14 For 10/100Base-TX there are a number of architecture choices. The circuit shown utilizes a single magnetic module PE-69016 which integrates the 10/100 transformer/choke and incorporates passive mixing of 10/100 transmit signals (see data sheet H305 for detailed information). For the 10Base-T port, the module is designed for a number of transceivers which have integrated filtering including SEEQ 80C24 and Micro Linear ML2652/2653.

15 For the 10/100Base-TX application circuit, it should be noted that termination resistors are present at both 10Base-T and 100Base-TX IC transmitter outputs, but only at the 100Base-TX IC receiver input. A switching transistor is shown connected to the TXREF pin which can be used to disable the 100Base-TX transmit output signal. Forcing the TXREF pin above its normal operating voltage (1.25 V) disables the current to the TX output driver effectively disabling it. For this application, it is not essential to disable the 100TX outputs — it would also suffice to ensure that transmit lines from the controller remain “quiet.”

16 For 10/100TX applications, one can also use switching (relay or solid-state) on primary or secondary of the magnetic module, as indicated in the System Application section. This allows one to use standard 10Base-T transceiver/10Base-T filter module, with the switch typically controlled by the Physical controller/MAC device.

17 It is important to implement a PCB layout which adheres to good analog layout rules for optimum network and EMC performance. An example of such a layout is as shown in the Layout Guide, which minimizes the noise coupling through use of distinct power and ground partitions. Power islands should be connected by ferrite beads. Please refer to the EMC section for more EMC specific application guidelines.

18 Implementation of circuits as recommended will result in nominal Vpp = 2 V for TP/FDDI, 100Base-TX and Vpp = 1 V for ATM 155 applications.

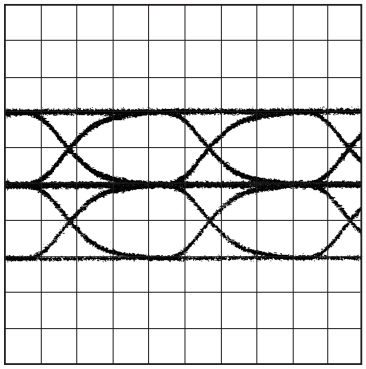
19 Note the signal ground symbols used: E = ECL or Digital Ground, T = Transmit Ground, and R = Receive Ground.

Performance

The following eye pattern measurements show the operation of the adaptive equalizer and the jitter performance on a design using the *MediaCAT* solution. Figure A shows the MLT3 transmit output waveform at 0 m cable. Figure B shows the waveform at receiver input after the attenuation and phase distortion effects of 100m UTP-5 cable. Figure C shows the recovered NRZI data for same signal. Similar measurements are repeated in Figures D, E and F for ATM 155 Mbps NRZ signals.

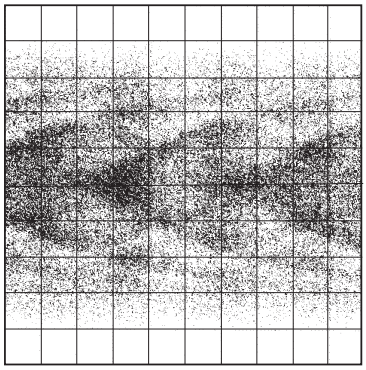
TP-FDDI/100Base-TX

MLT3 Transmit Output (TX±)



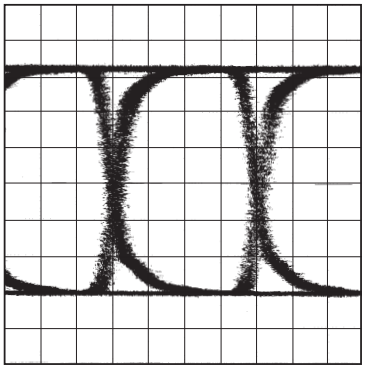
A 0 Meter UTP-5 Cable
500mV/DIV, 2ns/DIV

Receiver Input (RX±)



B 100 Meter UTP-5 Cable
200mV/DIV, 2ns/DIV

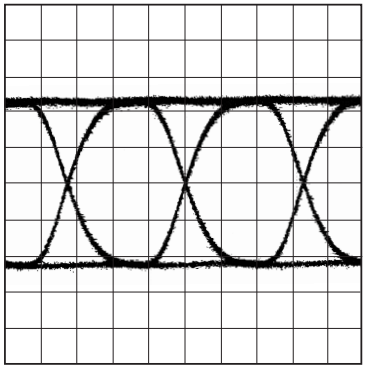
NRZI Receiver Output (RD±)



C 100 Meter UTP-5 Cable
200mV/DIV, 2ns/DIV

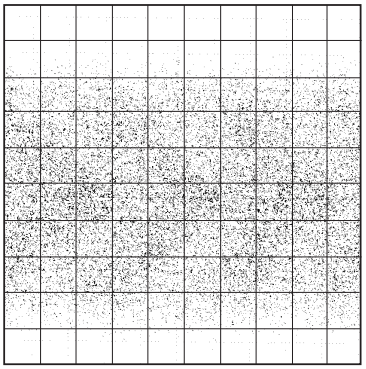
ATM-155

NRZ Transmit Output (TX±)



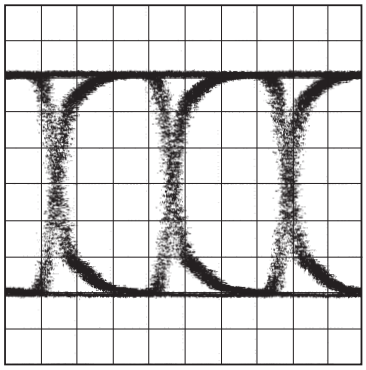
D 0 Meter UTP-5 Cable
200mV/DIV, 2ns/DIV

Receiver Input (RX±)



E 100 Meter UTP-5 Cable
100mV/DIV, 2ns/DIV

NRZ Receiver Output (RD±)



F 100 Meter UTP-5 Cable
200mV/DIV, 2ns/DIV

NOTES

All jitter measurements shown are peak values resulting from combination of transmit, receive and cable contributions. In MLT3 mode, the transmit eye pattern has a 3.5 ns rise-time, overshoot <3% and transmit jitter <1 ns. As a result of this, the receiver eye pattern has < 2 ns of jitter at 100 m UTP-5 cable. In NRZ mode, the transmit eye pattern has a rise time of 3 ns, <5% overshoot and transmit jitter <1 ns . As a result, the receiver jitter at 100 m UTP-5 cable is < 1.6 ns.

There is a general performance trade-off involved here. A faster rise time will reduce jitter and result in lower Bit Error Rate (BER). However, a faster rise time can also result in excessive signal overshoot and EMI emissions when signal encounters impedance mismatches in cable or punch down blocks. The application circuit shown should result in optimum waveform parameters.

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	MIN	Typical	MAX	Units
Supply Voltage	Vcc	0	—	6.0	V
Input Voltage	V_I	GND - 0.3	—	Vcc + 0.3	V
Lead Solder Temp/Time	—	—	—	240/10	°C/s

Recommended Operating Conditions

Supply Voltage	Vcc	4.75	5.0	5.25	V
Supply Current	Is	—	170	200	mA
Operating Temperature	T_A	0	25	70	°C
Storage Temperature	Ts	-40	—	+125	°C

Transmitter Characteristics

PECL High Level Input	TD+/-V_{IH}	Vcc—1170	—	Vcc—720	mV
PECL Low Level Input	TD+/-V_{IL}	Vcc—1950	—	Vcc—1440	mV
Transmit Output Current at TXP/N with R(txref) = 1K(1)	Iout	38.8	40	41.2	mA
Rise/Fall Time(2)	Tr/Tf	—	—	2.0	ns
Total Peak-to-Peak Jitter	—	—	0.5	1.0	ns

Receiver Characteristics

Differential input signal at RXP/N - PE-95000	—	—	2	2.5	V
PE-95010	—	—	1	1.5	V
Common Mode input voltage at RXP/N	—	3.0	3.5	4.0	V
PECL High Level Output at RDP/N(3)	RD+/-V_{OH}	Vcc—1220	—	Vcc—720	mV
PECL Low Level Output at RDP/N(3)	RD+/-V_{OL}	Vcc—1950	—	Vcc—1600	mV
PECL Output Voltage Swing	V_{OH}-V_{OL}	600	—	—	mV
Rise Time at RDP/N (10%-90%)	T_R	0.3	0.7	1.2	ns
Fall Time at RDP/N (90%-10%)	T_F	0.3	0.7	1.2	ns
Total Peak-to-Peak Jitter Binary Mode(4) (PE-95010)	—	—	1.0	2.0	ns
Total Peak-to-Peak Jitter MLT3 Mode(4) (PE-95000)	—	—	1.5	2.5	ns

Signal Detect Characteristics

PECL High Level Output	SD+ V_{OH}	Vcc-1220	—	Vcc-720	mV
PECL Low Level Output	SD+ V_{OL}	Vcc—1950	—	Vcc—1600	mV
Assert Time (Max)	—	—	—	1000	µs
Deassert Time (Max)	—	—	—	350	µs

Control Signals

Input high level output at ENCSEL to select Binary Mode	4.0	—	—	V
Input low level output at ENCSEL to select MLT3 Mode	—	—	0.8	V

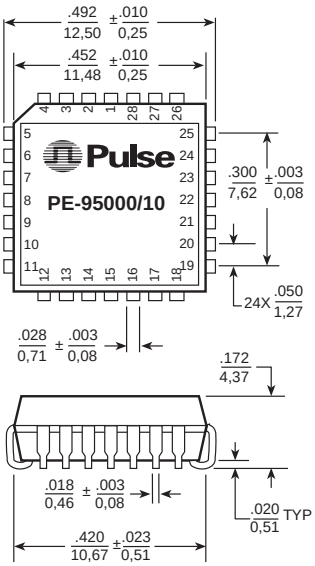
NOTES

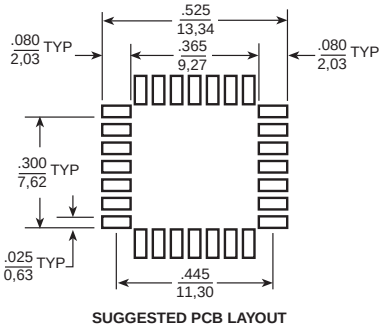
1. I_{OUT} is set by resistor at TXREF. I_{OUT} = 40/R(TXREF).
2. Rise/Fall Time can be controlled by external capacitor. See application circuit.
3. Measured with standard PECL load, 50 Ω to Vcc-2 V.
4. Includes jitter from the transmitter, cable and receiver in the systems shown in the application diagrams.
5. Refer to data sheets for detailed specifications of magnetic modules: PE-68517L (H303) and PE-69016 (H305).

Pulse
A TECHNITROL COMPANY

Mechanicals & Schematics

PE-95000/10

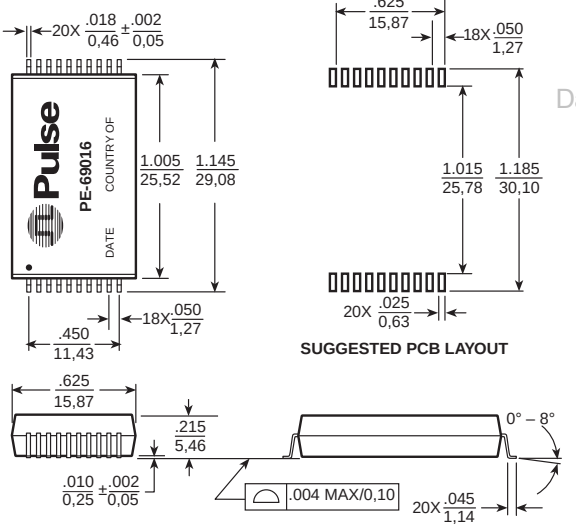




SUGGESTED PCB LAYOUT

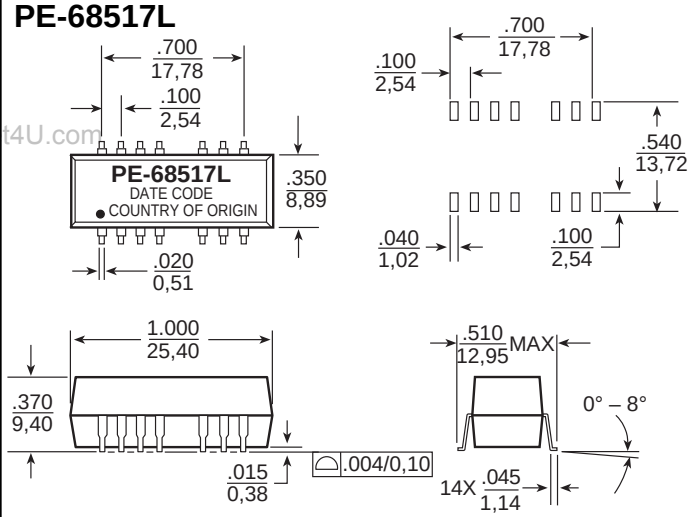
Part Number	Weight (Grams)	Tube	Tape & Reel
PE-9000/10	1.2	—	500
PE-69016	4.5	30	250
PE-68517L	3.8	20	160

PE-69016

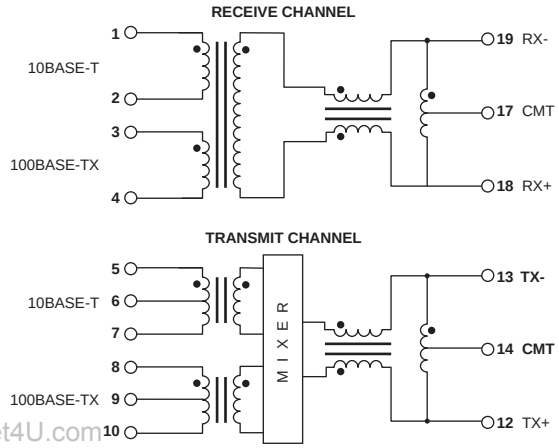


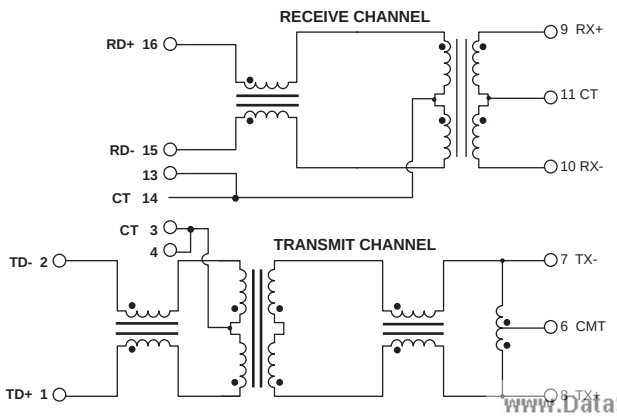
SUGGESTED PCB LAYOUT

PE-68517L



Dimensions: Inches / mm Unless otherwise specified, all tolerances are ± .005 0,13





EMC Considerations

TP-FDDI/100Base-TX uses MLT3 line coding (fundamental frequency = 31.25 MHz) to shift 90% of spectral energy to below 40 MHz. ATM 155 (fundamental frequency = 77.5 MHz) uses NRZ coding with 1 V_{PP} amplitude to reduce EMI emissions.

The *MediaCAT* transceiver kit has been designed to minimize EMI emissions and noise susceptibility. Some of the key measures which help to achieve this are as follows:

Edge-rate control on PE-95000/10 internal signals/transceiver output.

Excellent CMRR and PSRR (power supply rejection ratio) of transmit/receive amplifiers.

High performance balanced magnetics — tuned to transceiver silicon.

Dual common mode choke architecture. The PE-68517L employs a single high performance choke on receiver chip-side to boost immunity. However, for transmit channel, there are two complimentary chokes employed — one on chip-side and one on line-side. These are to minimize common mode emissions. The transmit autoformer allows for effective common mode termination, since a transformer center tap's effectiveness here would be reduced by the intervening choke impedance.

It is crucial to employ good high speed PCB design rules in laying out the board.

1. Use multi-layer PCB with dedicated ground and power layers for best high frequency and EMC performance. At least four layers are recommended with outside layers for signal routing and inner layers for supply planes.
2. Use of ground plane partitions as indicated in the layout guide is recommended. The chassis ground is generally connected to backplate directly. The ground plane area under the magnetic module is left void for optimum noise separation.
3. Use of shielded RJ45 (UTP-5) or DB9 (STP) is recommended with galvanic contact to backplate for chassis ground continuity.
4. Termination of unused cable pairs is recommended. The unused pairs are terminated in their common mode impedance (to chassis ground) to minimize cable reflections and common mode standing waves. The application circuits shown indicate one termination scheme, but there are other options. Refer to the PMD standards for additional information.
5. Decoupling of RX/TX transformer center-taps (Pin 3 and 14) to ground, as shown in application circuit, reduces common mode impedance and consequently improves common mode rejection.
6. The PE-68517L allows a further option to terminate line side common mode noise. In receive channel this can be done by connecting pin 11 to chassis ground through the existing unused pair RC network (75 Ω/0.1 µF). In transmit channel, pin 6 can similarly be connected to same RC network.

It should however be noted that EMC performance is a system measurement and highly implementation specific.

Appendix 1: Physical ControllerChipsets

Standard	Vendor	Device
TP-FDDI/100TX	AMD	AM79865/AM79866
TP-FDDI/100TX	National Semiconductor	DP83222/83257
ATM	PMC	SUNI Series
ATM	Fujitsu	ITC Series
ATM	Texas Instruments	TDC1500
ATM	AMCC	S30XX

NOTES

1. **Further Pulse Products:** The *FASTPULSE* series includes further transceiver products in more integrated platforms:

   High Speed LAN Transceivers, a series of 9-pin transceivers which are drop-in replacements for standard Fiber Optic transceivers. Available for ATM, 100Base-TX and TP-FDDI.

   MediaDrive is a compact surface mount module which integrates the *MediaCAT* transceiver IC and magnetic module to yield a single chip solution. Available for ATM and 100Base-TX/TP-FDDI.

   Contact Pulse Engineering for more information on these and other latest developments.

2. Pulse Engineering has other magnetic modules which can be used with *MediaCAT* transceiver IC (Datasheet H303, H305 and H316). Please contact Pulse for information on these and Pulse's catalog of high speed LAN magnetic modules.

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