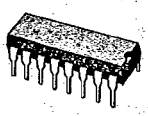
SGS-THOMSON MICROELECTRONICS

T74LS190
T74LS191

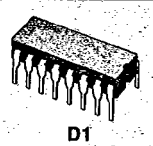
LS190 - PRESETTABLE BCD/DECADE UP/DOWN COUNTERS
LS191 - PRESETTABLE 4-BIT BINARY UP/DOWN COUNTERS

T-45-23-09

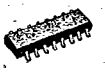
- LOW POWER 90 mW TYPICAL DISSIPATION
- SYNCHRONOUS COUNTING
- INDIVIDUAL PRESET INPUTS
- CASCADABLE
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- HIGH SPEED 35 MHz TYPICAL COUNT FREQUENCY
- ASYNCHRONOUS PARALLEL LOAD
- COUNT ENABLE AND UP/DOWN CONTROL INPUT
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)



M1
(Micro Package)

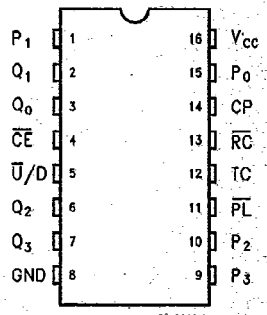
C1
(Plastic Chip Carrier)

ORDER CODES :

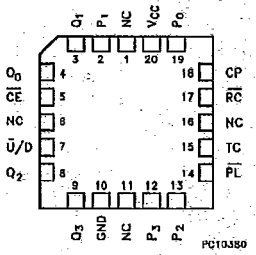
T74LSXXX D1	T74LSXXX C1
T74LSXXX B1	T74LSXXX M1

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

DESCRIPTION

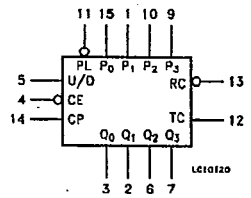
The T74LS190 is a synchronous UP/DOWN BCD Decade (8421) Counter and the T74LS191 is a synchronous UP/DOWN Modulo-16 Binary Counter. State changes of the counters are synchronous with the LOW to HIGH transition of the Clock Pulse input.

An asynchronous Parallel Load ($\overline{PL}$) input overrides counting and loads the data present on the P_n inputs into the flip-flops, which makes it possible to use the circuits as programmable counters.

A Count Enable ($\overline{CE}$) input serves as the carry/borrow input in multi-stage counters. An Up/Down Count Control ($\overline{U}$/D) input determines whether a circuit count up or down. A Terminal Count (TC) output and a Ripple Clock ($\overline{RC}$) output provide overflow/underflow indication and make possible a variety of methods for generating carry/borrow signal in multi-stage counter applications.

LOGIC SYMBOL AND STATE DIAGRAM

T-45-23-09



LS190

UP : $TC = \overline{Q_0} \cdot \overline{Q_3} \cdot (\overline{U/D})$

DOWN : $TC = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (U/D)$

LS191

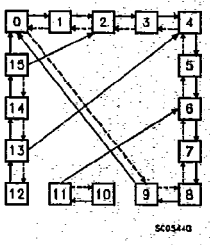
UP : $TC = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (\overline{U/D})$

DOWN : $TC = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (U/D)$

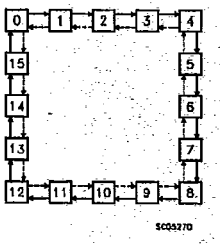
COUNT UP ⟶

COUNT DOWN ⟶

LS190



LS191



MODE SELECT TABLE

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U/D}$	CP	
H	L	L	⌐	Count Up
H	L	H	⌐	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

RC TRUTH TABLE

INPUTS			$\overline{RC}$ OUTPUT
$\overline{CE}$	TC *	CP	
L	H	⌐	⌐
H	X	X	H
X	L	X	H

* TC is generated internally

L = LOW Voltage Level, H = HIGH Voltage Level, X = Don't Care, ⌐ = LOW to HIGH transition, ⌐⌐ = LOW Pulse

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to 7	V
V_I	Input Voltage, Applied to Input	− 0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, into Inputs	− 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

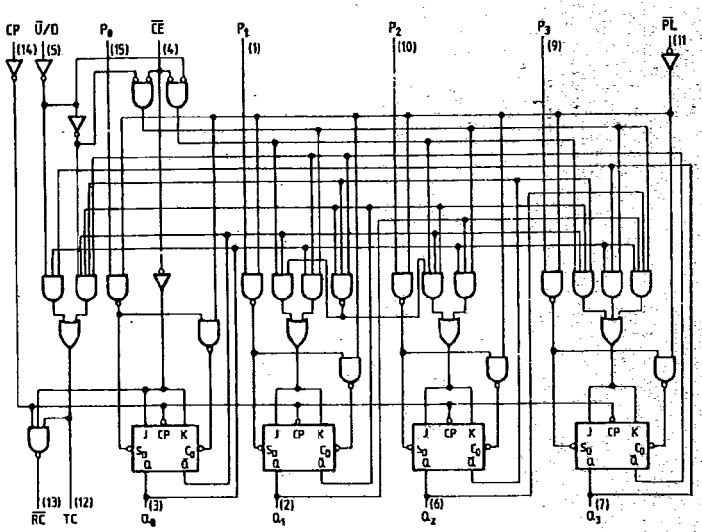
GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS190/191XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

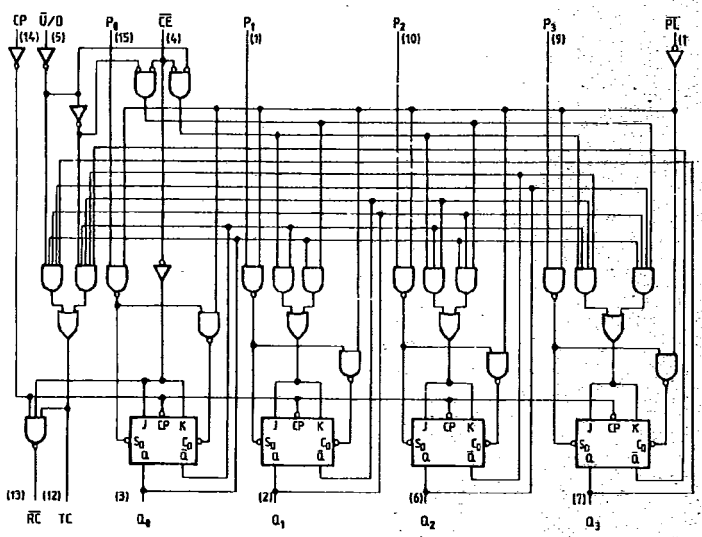
LOGIC DIAGRAMS

T-45-23-09

DECADE COUNTER
LS190



BINARY COUNTER
LS191



Vcc = Pin 16
GND = Pin 8
( ) = Pin numbers

FUNCTIONAL DESCRIPTION

The LS190 is a synchronous Up/Down BCD Decade Counter and the LS191 is a synchronous Up/Down 4-Bit Binary Counter. The operating modes of the LS190 decade counter and the LS191binary counterare identical, with the only difference being the count sequences as noted in the state diagrams. Each circuit contains four master slave flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has a n asynchronous parallel loas capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Data inputs (P_0-P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibit counting. When $\overline{CE}$ is LOW, internal state changes are initiaded synchronously by thee LOW to HIGH transition of the clock input.. The direction of counting is determined by the $\overline{U}$/D input signal, as indicate in the Mode Select Table. When counting is to be enabled, the $\overline{CE}$ signal can be made LOW when the clock is in either state.

However, when counting is to be inhibited, the LOW to HIGH $\overline{CE}$ transition must occur only while the clock is HIGH. Similary, the $\overline{U}$/D signal should only be changed when either $\overline{CE}$ or the clock is HIGH.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or raches maximum (9 for LS190, 15 for the LS191) in the count-up mode. The TC output will then remain HIGH until a stage changeoccurs, wheter by counting or presetting or until U/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to be enable the Rpple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, the $\overline{RC}$ output will go LOW when the clock next goes HIGH again. This feature simplifies the design of multistage counters, as indicated in Figures a and b. In Figure a, each $\overline{RC}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage,since a HIGH signals on $\overline{CE}$ inhibit the $\overline{RC}$ output pulse, as indicated in the $\overline{RC}$ Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages.

This represent the cumulative delay of the clock as it ripples through the preceding stages. A method of causing state changes to occur simultaneously in all stages is shown in Figure b. All Clock inputs are driven in parallel and the RC output propagate the carry/borrow signals ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative going edge of the of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{RC}$ output of any package goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure c avoids ripple delays and their associated restrictions. The $\overline{CE}$ input signal for a given stage is formad by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figure a and b doesn't apply, because the TC output of a given stage is not affect by its own $\overline{CE}$.

Fig. a: n-stage counter using ripple clock

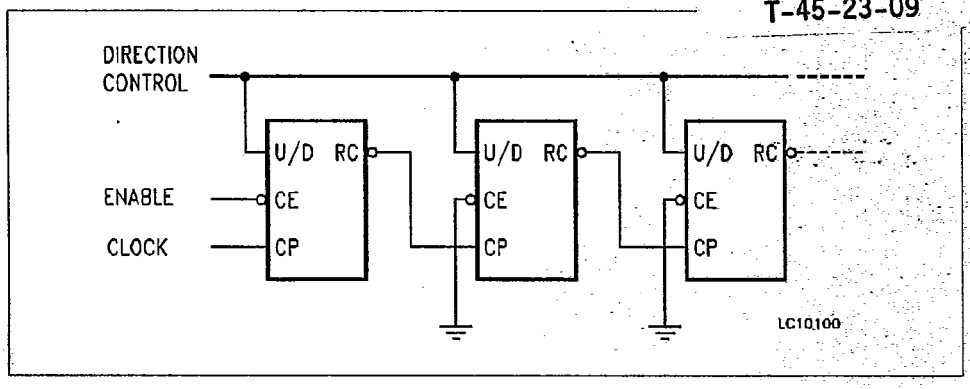


Fig.b: Synchronous n-stage counter using ripple carry/borrow

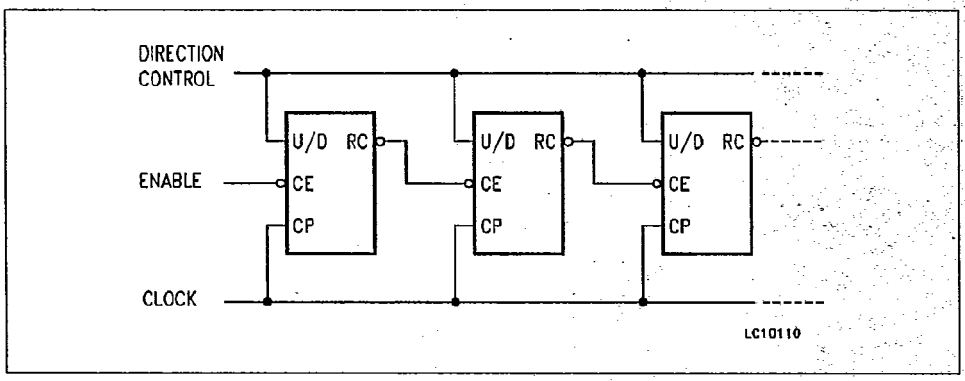
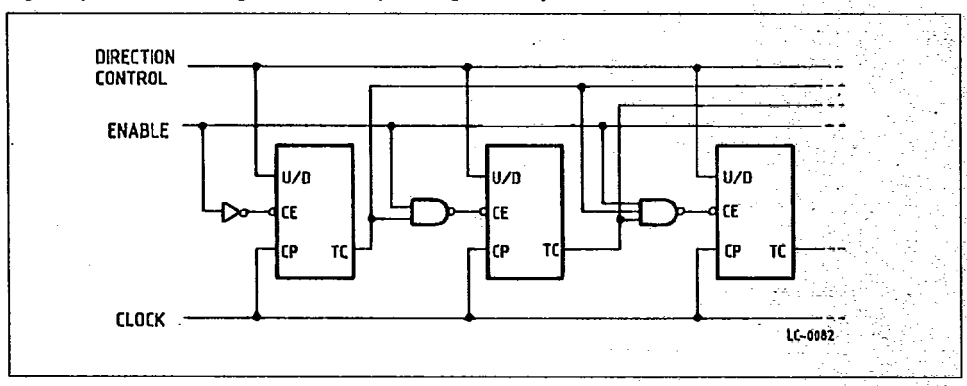


Fig. c: Synchronous n-stage counter with parallel gated carry/borrow



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current $\overline{P_0}$, $\overline{PL}$, CP, U/D $\overline{CE}$			20 60	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	$\overline{P_0}$, $\overline{PL}$, CP, U/D $\overline{CE}$			0.1 0.3	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current $\overline{P_0}$, $\overline{PL}$, CP, U/D $\overline{CE}$			- 0.4 - 1.08	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		20	35	V_{CC} = MAX, All Inputs 0V		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Note more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
f_{MAX}	Max Input Count Frequency	20	25		Figures 1	V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Propagation Delay, CP Input to Q Outputs		16 24	24 36	Figures 1		ns
t_{PLH} t_{PHL}	Propagation Delay, CP Input to $\overline{RC}$ Outputs		13 16	20 24	Figures 2		ns
t_{PLH} t_{PHL}	Propagation Delay, CP Input to TC Outputs		28 37	42 52	Figures 1		ns
t_{PLH} * t_{PHL} *	Propagation Delay, U/D Input to $\overline{RC}$ Outputs		30 30	45 45	Figures 7		ns
t_{PLH} t_{PHL} *	Propagation Delay, U/D Input to TC Outputs		21 22	33 33	Figures 7		ns
t_{PLH} t_{PHL}	Propagation Delay, P0-P_3 Inputs to Q_0-Q_3 Outputs		20 27	32 40	Figures 3		ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{PL}$ Input to Any Output		22 33	33 50	Figures 4		ns
t_{PLH} * t_{PHL}	Propagation Delay, $\overline{CE}$ Input to $\overline{RC}$ Output		21 22	33 33	Figures 2		ns

* It is possible to get these timing relationship, but they should not occur during normal operation since the CP would be HIGH.

AC SET-UP REQUIREMENTS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_w	CP Pulse Width	25			Figure 1	V_{CC} = 5.0 V	ns
t_w	PL Pulse Width	35			Figure 4		ns
t_sL	Set-Up Time LOW, Data to PL	30					ns
t_hL	Hold Time LOW, Data to PL	5			Figure 6		ns
t_sH	Set-Up Time HIGH, Data to PL	30					ns
t_hH	Hold Time HIGH, Data to PL	5					ns
t_{rec}	Recovery Time, PL to CP	40			Figure 5		ns
t_sL	Set-Up Time LOW, CE to Clock	30			Figure 8		ns
t_hL	Hold Time LOW, CE to Clock	5					ns

DEFINITION OF TERMS:

SET-UP TIME (t_s): is defined as the minimum time required for the corret logic level to be present at the loglo input prior the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h): is defined as the minimum time following the clock transition from LOW to HIGH at which the logiclevel must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be relased prior to the clock transitio from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) : is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORM

Fig 1.

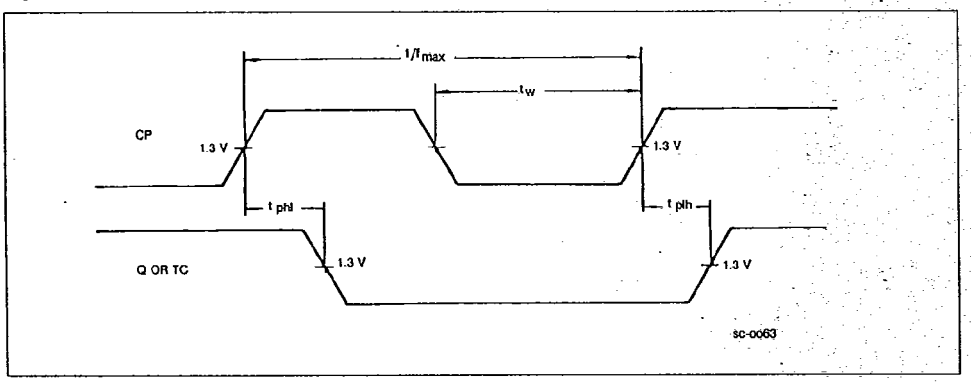


Fig 2.

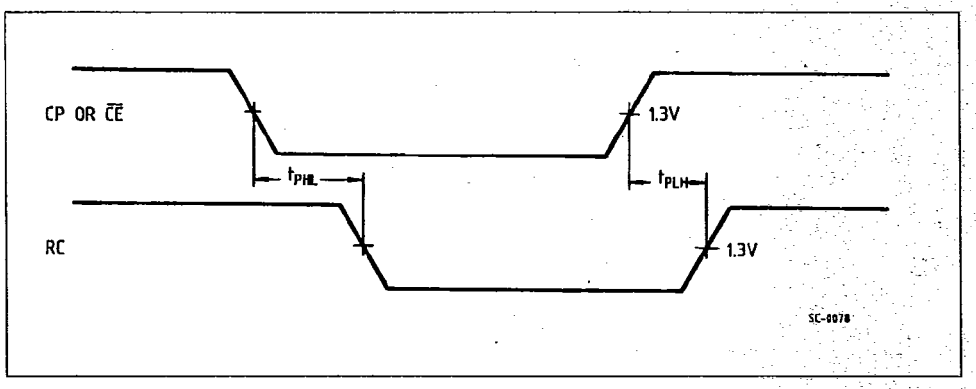


Fig 3.

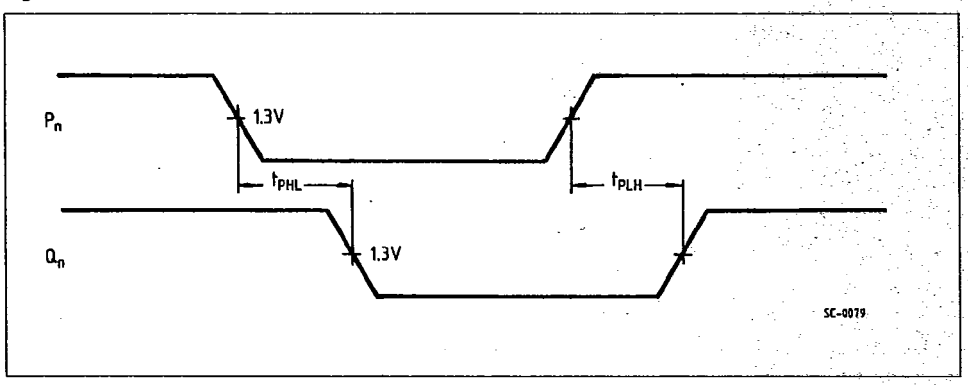
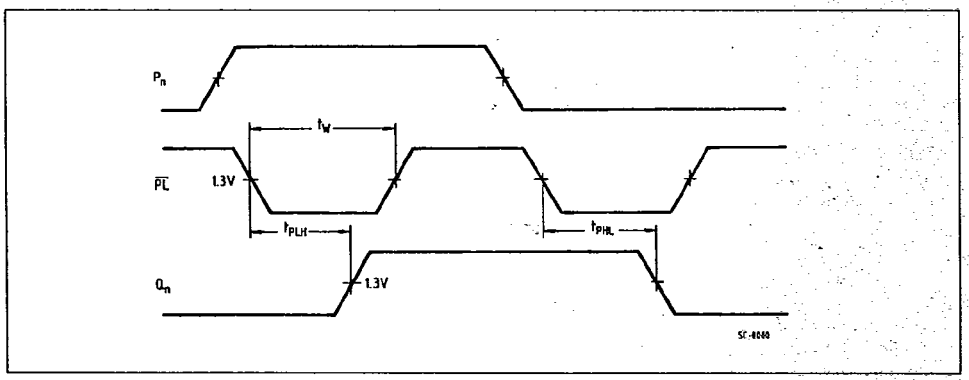


Fig 4.



42E D 7929237 0033472 4 SGTH

Fig 5.

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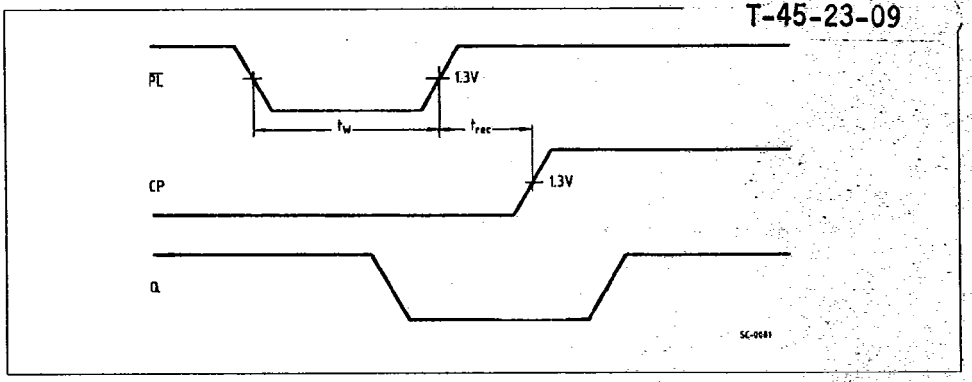
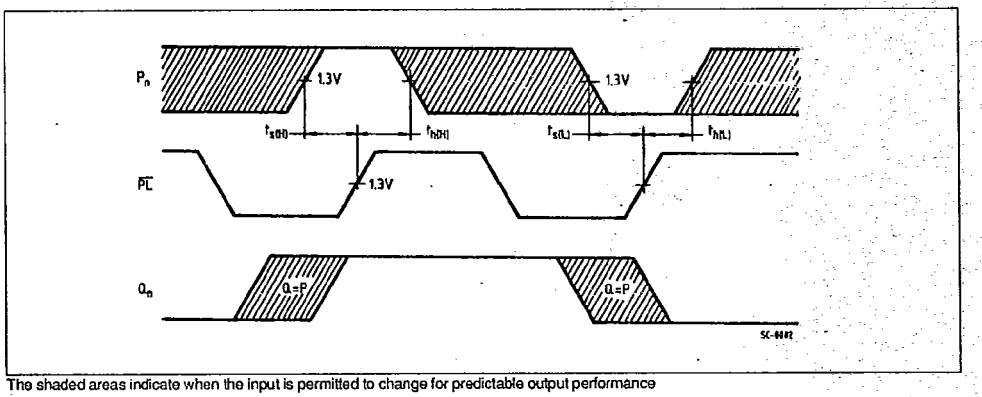


Fig 6.



The shaded areas indicate when the input is permitted to change for predictable output performance

Fig 7.

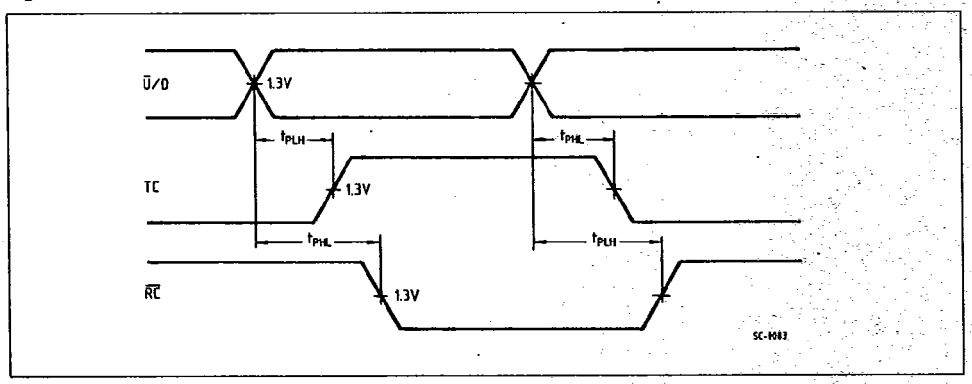


Fig 8. 42E D 7929237 0033473 6 SGTH