

RoHS Compliant Product

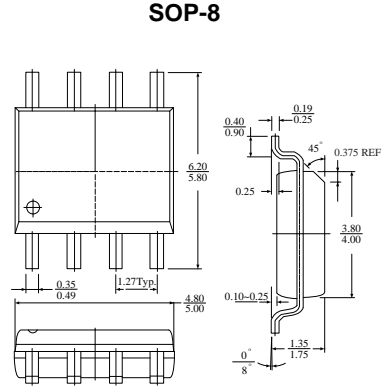
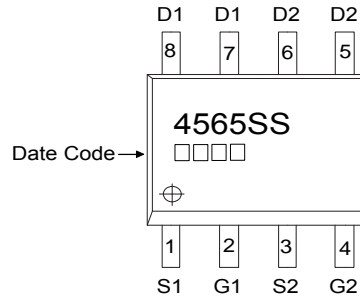
### Description

The SSG4565 provide the designer with the best combination of fast switching, ruggedized device design, Ultra low on-resistance and cost-effectiveness.

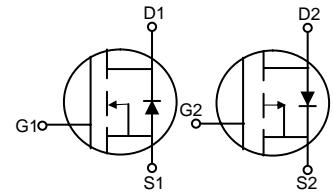
The SOP-8 package is universally preferred for all commercial industrial surface mount application and suited for low voltage applications such as DC/DC converters.

### Features

- \* Simple Drive Requirement
- \* Lower On-resistance
- \* Fast Switching Performance



Dimensions in millimeters



### Absolute Maximum Ratings

Parameter	Symbol	Ratings		Unit
		N-Channel	P-Channel	
Drain-Source Voltage	V <sub>DS</sub>	40	-40	V
Gate-Source Voltage	V <sub>GS</sub>	±20	±20	V
Continuous Drain Current <sup>3</sup>	I <sub>D</sub> @T <sub>A</sub> =25 °C	7.6	-6.5	A
Continuous Drain Current <sup>3</sup>	I <sub>D</sub> @T <sub>A</sub> =70 °C	6	-5.2	A
Pulsed Drain Current <sup>1</sup>	I <sub>DM</sub>	30	-30	A
Total Power Dissipation	P <sub>D</sub> @T <sub>A</sub> =25 °C	2		W
Linear Derating Factor		0.016		W/°C
Operating Junction and Storage Temperature Range	T <sub>j</sub> , T <sub>stg</sub>	-55~+150		°C

### Thermal Data

Parameter	Symbol	Ratings	Unit
Thermal Resistance Junction-ambient <sup>3</sup>	R <sub>thj-a</sub>	62.5	°C/W

### Electrical Characteristics N-Channel ( $T_j=25^\circ\text{C}$ Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain-Source Breakdown Voltage	$BV_{DSS}$	40	-	-	V	$V_{GS}=0V, I_D=250\mu A$
Breakdown Voltage Temp. Coefficient	$\Delta BV_{DSS}/\Delta T_j$	-	0.03	-	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D=1mA$
Gate Threshold Voltage	$V_{GS(th)}$	1.0	-	3.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Gate-Source Leakage Current	$I_{GSS}$	-	-	$\pm 100$	nA	$V_{GS}=\pm 20V$
Drain-Source Leakage Current ( $T_j=25^\circ\text{C}$ )	$I_{DSS}$	-	-	1	$\mu A$	$V_{DS}=40V, V_{GS}=0$
Drain-Source Leakage Current ( $T_j=70^\circ\text{C}$ )		-	-	25	$\mu A$	$V_{DS}=32V, V_{GS}=0$
Static Drain-Source On-Resistance <sup>2</sup>	$R_{DS(ON)}$	-	-	25	m $\Omega$	$V_{GS}=10V, I_D=7A$
		-	-	32		$V_{GS}=4.5V, I_D=5A$
Total Gate Charge <sup>2</sup>	$Q_g$	-	17	27	nC	$I_D=7A$ $V_{DS}=32V$ $V_{GS}=4.5V$
Gate-Source Charge	$Q_{gs}$	-	4	-		
Gate-Drain ("Miller") Charge	$Q_{gd}$	-	10	-		
Turn-on Delay Time <sup>2</sup>	$T_{d(ON)}$	-	11	-	nS	$V_{DD}=20V$ $I_D=1A$ $V_{GS}=10V$ $R_G=3.3\Omega$ $R_D=20\Omega$
Rise Time	$T_r$	-	8	-		
Turn-off Delay Time	$T_{d(OFF)}$	-	30	-		
Fall Time	$T_f$	-	11	-		
Input Capacitance	$C_{iss}$	-	1400	2400	pF	$V_{GS}=0V$ $V_{DS}=25V$ $f=1.0MHz$
Output Capacitance	$C_{oss}$	-	250	-		
Reverse Transfer Capacitance	$C_{rss}$	-	170	-		
Forward Transconductance	$G_{fs}$	-	12	-	S	$V_{DS}=10V, I_D=7A$

### Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Forward On Voltage <sup>2</sup>	$V_{SD}$	-	-	1.2	V	$I_S=1.7A, V_{GS}=0V.$
Reverse Recovery Time <sup>2</sup>	$T_{rr}$	-	26	-	ns	$I_S=7A, V_{GS}=0V$ $di/dt=100A/\mu s$
Reverse Recovery Charge	$Q_{rr}$	-	21	-	nC	

Notes: 1.Pulse width limited by Max. junction temperature.

2.Pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .

3.Surface mounted on 1 inch<sup>2</sup> copper pad of FR4 board; 270 $^\circ\text{C}/W$  when mounted on min. copper pad.

# SSG4565

N Channel 7.6A, 40V,  $R_{DS(ON)}$  25m $\Omega$

P Channel 6.5A, 40V,  $R_{DS(ON)}$  33m $\Omega$

## Enhancement Mode Power Mos.FET

### Electrical Characteristics P-Channel( $T_j=25^\circ\text{C}$ Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain-Source Breakdown Voltage	$BV_{DSS}$	-40	-	-	V	$V_{GS}=0V, I_D=-250\mu A$
Breakdown Voltage Temp. Coefficient	$\Delta BV_{DS}/\Delta T_j$	-	-0.03	-	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D=-1mA$
Gate Threshold Voltage	$V_{GS(th)}$	-1.0	-	-3.0	V	$V_{DS}=V_{GS}, I_D=-250\mu A$
Gate-Source Leakage Current	$I_{GSS}$	-	-	$\pm 100$	nA	$V_{GS}=\pm 20V$
Drain-Source Leakage Current ( $T_j=25^\circ\text{C}$ )	$I_{DSS}$	-	-	-1	$\mu A$	$V_{DS}=-40V, V_{GS}=0$
Drain-Source Leakage Current ( $T_j=70^\circ\text{C}$ )		-	-	-25	$\mu A$	$V_{DS}=-32V, V_{GS}=0$
Static Drain-Source On-Resistance <sup>2</sup>	$R_{DS(ON)}$	-	-	33	m $\Omega$	$V_{GS}=-10V, I_D=-6A$
		-	-	42		$V_{GS}=-4.5V, I_D=-4A$
Total Gate Charge <sup>2</sup>	$Q_g$	-	20	32	nC	$I_D=-6A$ $V_{DS}=-32V$ $V_{GS}=-4.5V$
Gate-Source Charge	$Q_{gs}$	-	4	-		
Gate-Drain ("Miller") Charge	$Q_{gd}$	-	10	-		
Turn-on Delay Time <sup>2</sup>	$T_{d(ON)}$	-	11	-	nS	$V_{DS}=-20V$ $I_D=-1A$ $V_{GS}=-10V$ $R_G=3.3\Omega$ $R_D=20\Omega$
Rise Time	$T_r$	-	7	-		
Turn-off Delay Time	$T_{d(OFF)}$	-	67	-		
Fall Time	$T_f$	-	43	-		
Input Capacitance	$C_{iss}$	-	1440	2300	pF	$V_{GS}=0V$ $V_{DS}=-25V$ $f=1.0MHz$
Output Capacitance	$C_{oss}$	-	250	-		
Reverse Transfer Capacitance	$C_{rss}$	-	190	-		
Forward Transconductance	$G_{fs}$	-	10	-	S	$V_{DS}=-10V, I_D=-6A$

### Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Forward On Voltage <sup>2</sup>	$V_{SD}$	-	-	-1.2	V	$I_S=-1.7A, V_{GS}=0V.$
Reverse Recovery Time <sup>2</sup>	$T_{rr}$	-	27	-	ns	$I_S=-6A, V_{GS}=0V$ $di/dt=100A/\mu s$
Reverse Recovery Charge	$Q_{rr}$	-	23	-	nC	

Notes: 1.Pulse width limited by Max. junction temperature.

2.Pulse width  $\leq 300\mu s$ , dutycycle  $\leq 2\%$ .

3.Surface mounted on 1 inch<sup>2</sup> copper pad of FR4 board; 270 $^\circ\text{C}/\text{W}$  when mounted on min. copper pad.

#### Characteristics Curve N-Channel

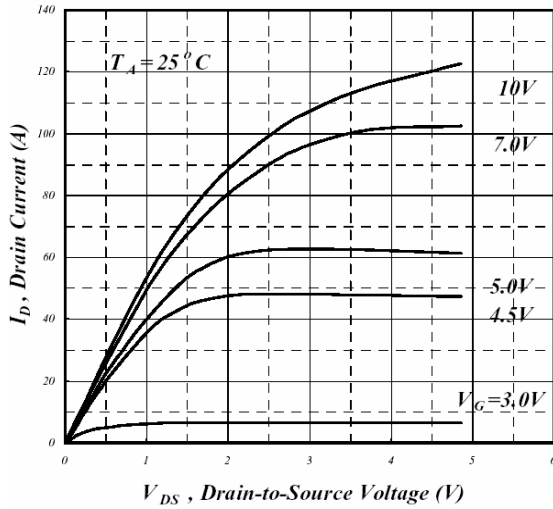


Fig 1. Typical Output Characteristics

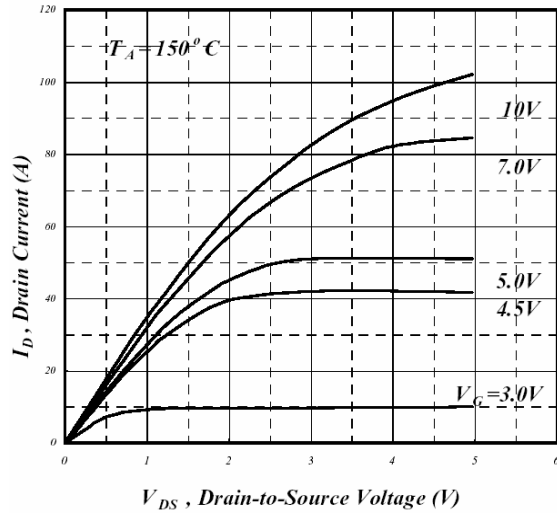


Fig 2. Typical Output Characteristics

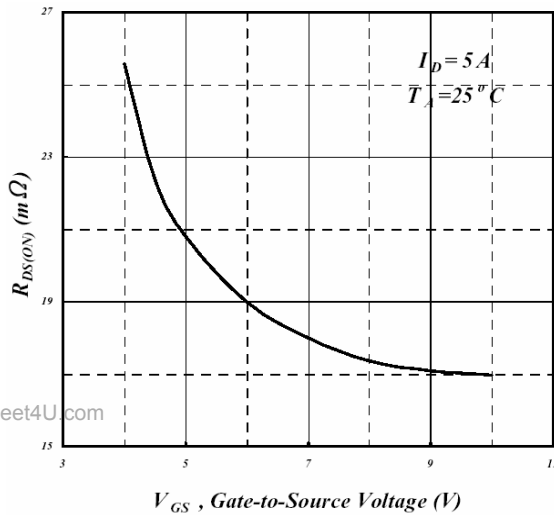


Fig 3. On-Resistance v.s. Gate Voltage

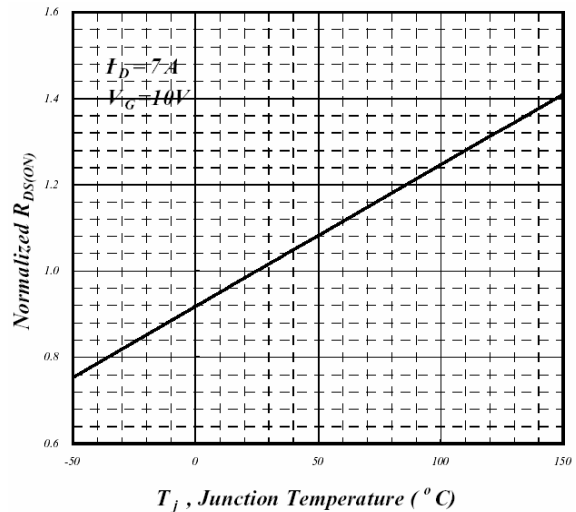


Fig 4. Normalized On-Resistance v.s. Junction Temperature

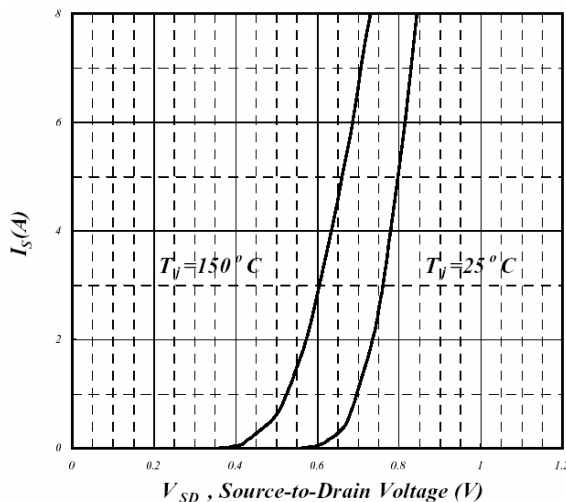


Fig 5. Forward Characteristics of Reverse Diode

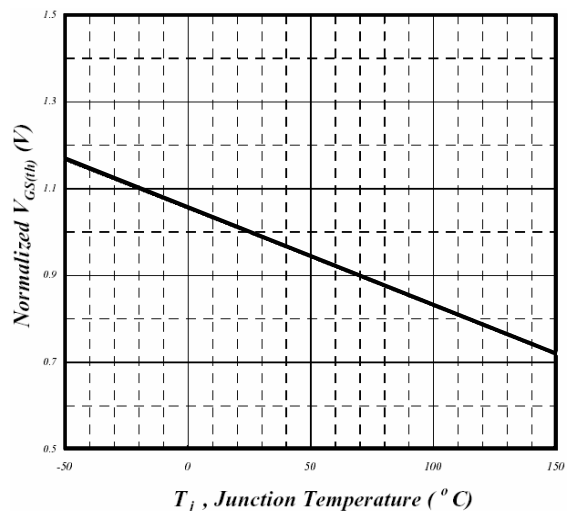


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

#### N-Channel

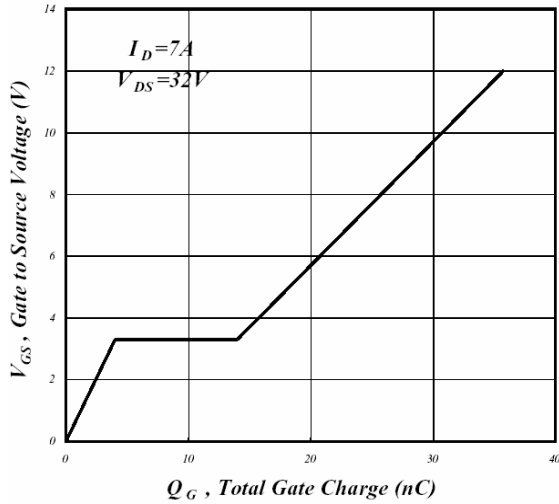


Fig 7. Gate Charge Characteristics

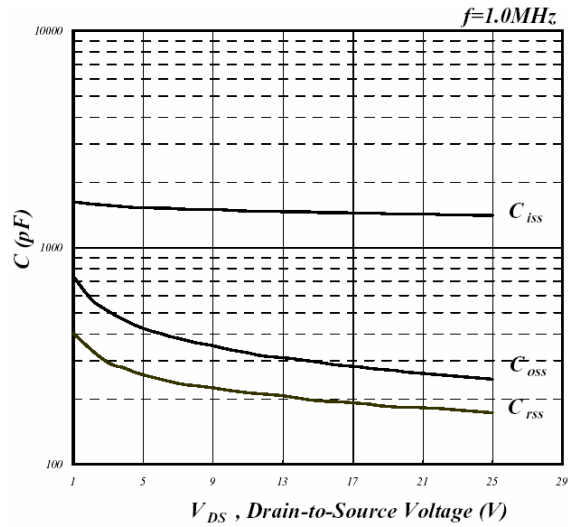


Fig 8. Typical Capacitance Characteristics

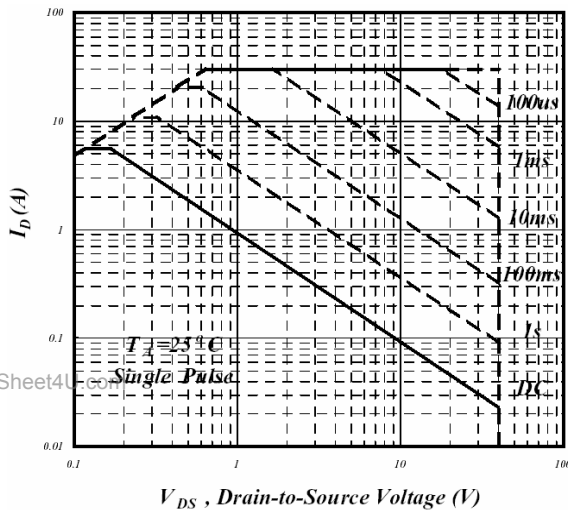


Fig 9. Maximum Safe Operating Area

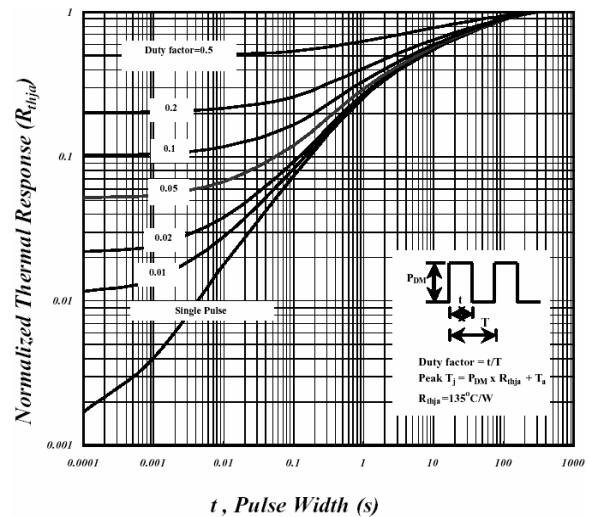


Fig 10. Effective Transient Thermal Impedance

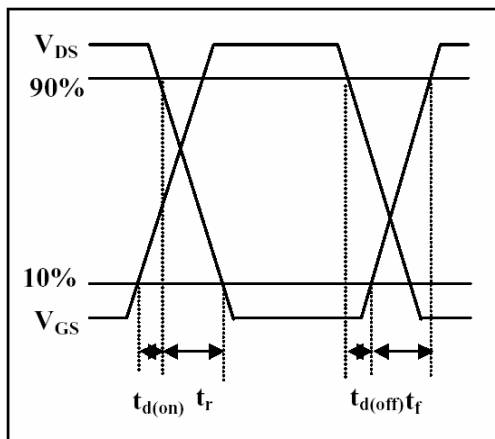


Fig 11. Switching Time Waveform

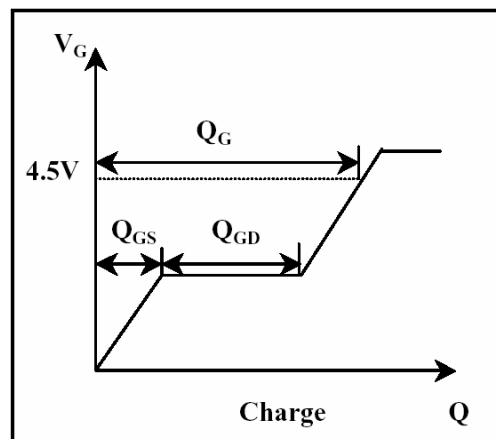


Fig 12. Gate Charge Waveform

#### P-Channel

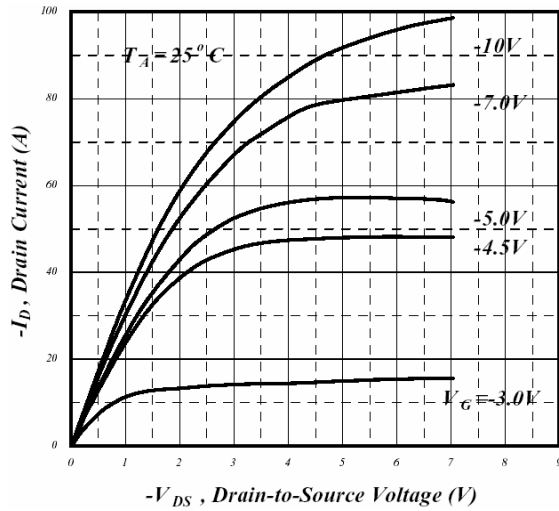


Fig 1. Typical Output Characteristics

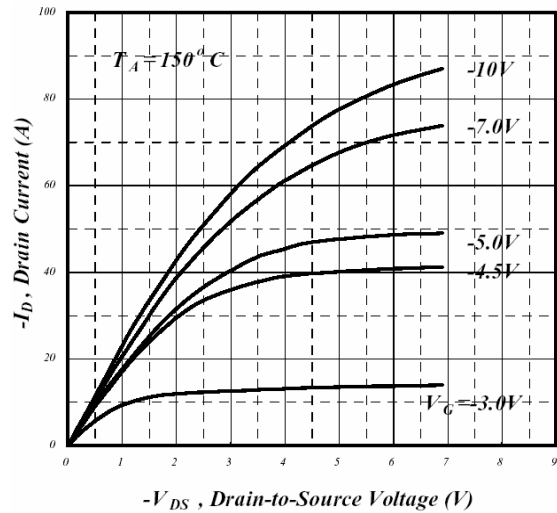


Fig 2. Typical Output Characteristics

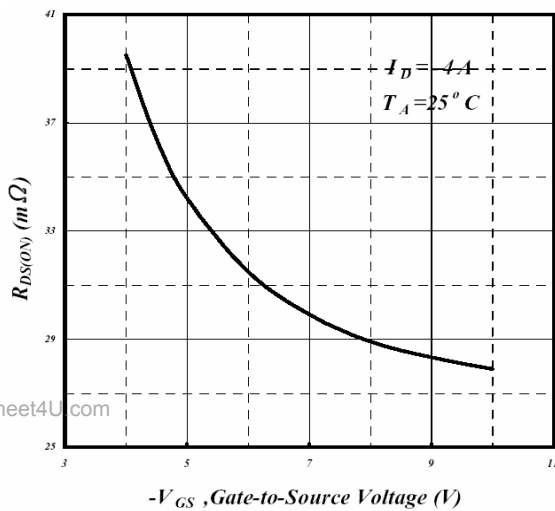


Fig 3. On-Resistance v.s. Gate Voltage

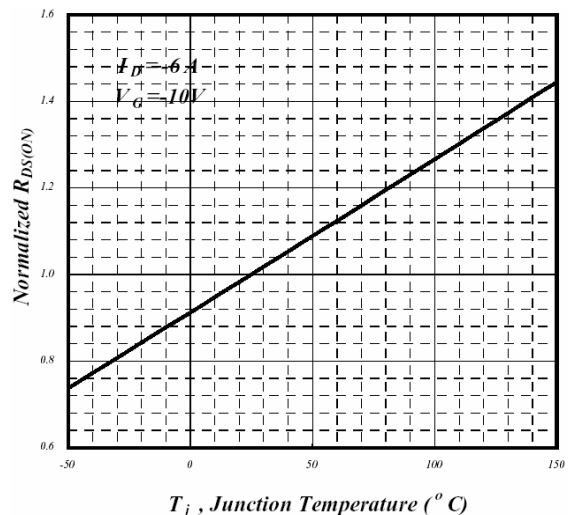


Fig 4. Normalized On-Resistance v.s. Junction Temperature

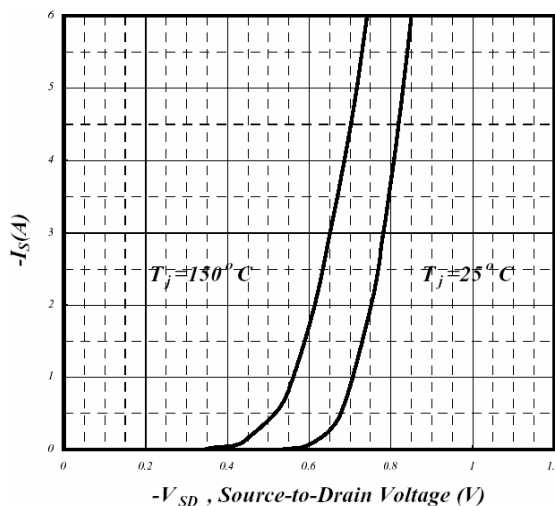


Fig 5. Forward Characteristics of Reverse Diode

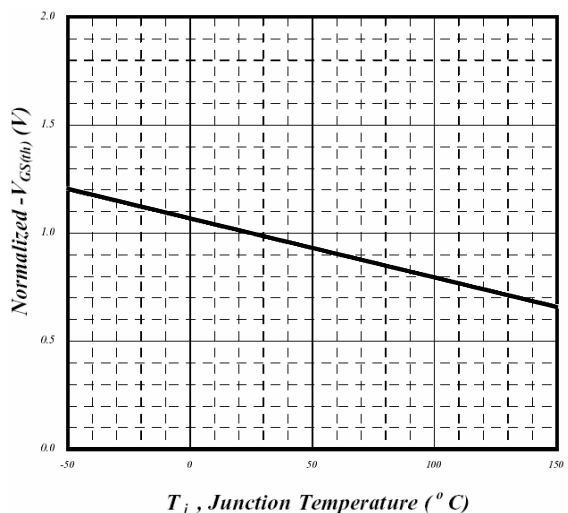


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

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#### P-Channel

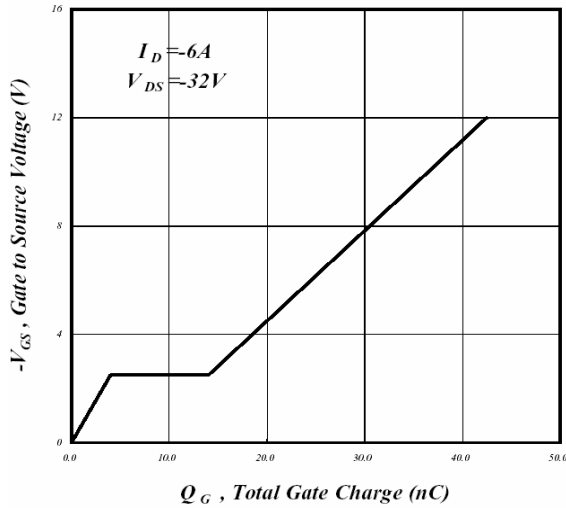


Fig 7. Gate Charge Characteristics

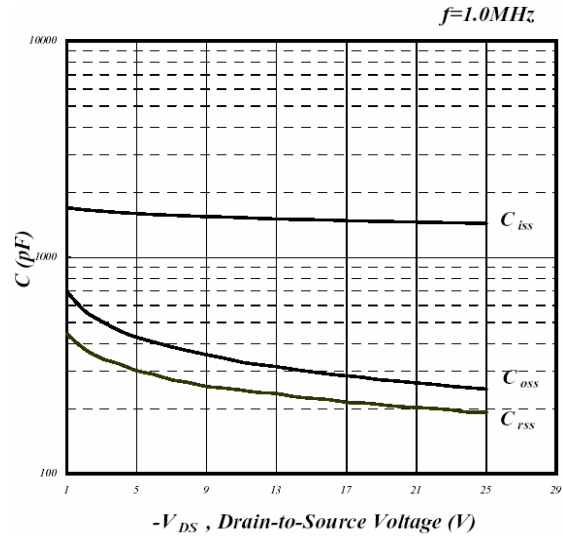


Fig 8. Typical Capacitance Characteristics

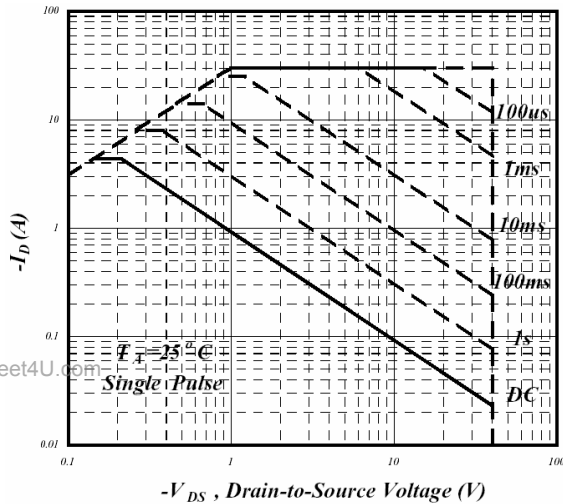


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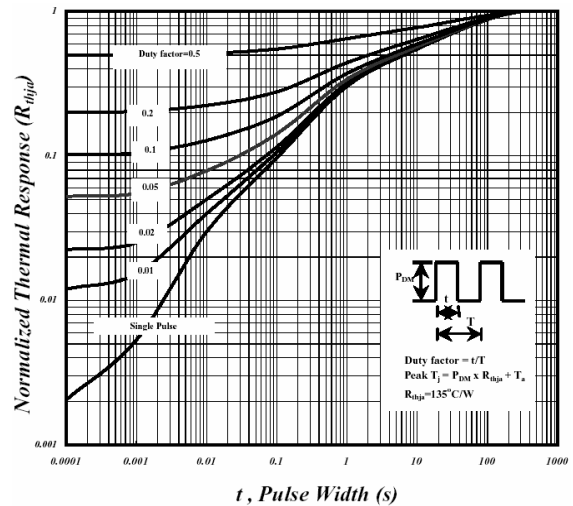


Fig 10. Effective Transient Thermal Impedance

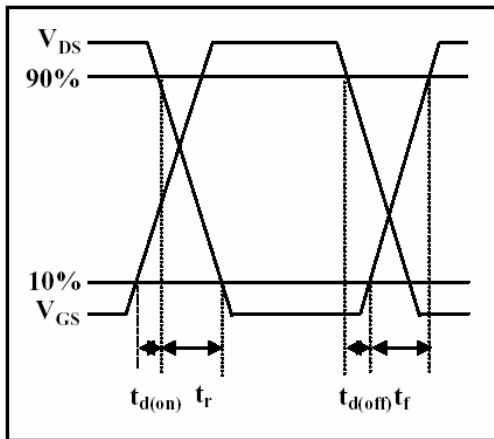


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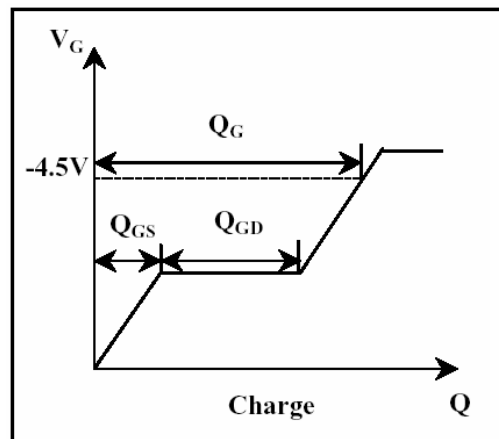


Fig 12. Gate Charge Waveform