# Silan Microelectronics

SC23M28

8K-BIT MEMORY CARD IC

DESCRIPTION

SC23M28 is a smart card module utilizing CMOS EEPROM technology. 1024 bytes main memory with write-protect function and programmable security code. And the periphery interface is compatible with ISO7816 agreement (synchronous propagation).

FEATURES

* 1024 X 8 bit EEPROM
* Byte addressing
* Permanent write-protect for each byte
* 1024 X 1bit memory protection
* Serial three buses interface
* More than 100,000 times write endurance cycles
* Data retention of more than 10 years
* Contact definition and serial interface comply to ISO7816 specification (synchronous propagation)
* 2Byte programmable security code PSC(Programmable Security Code), and the data can be changed only when pass the PSC authentication
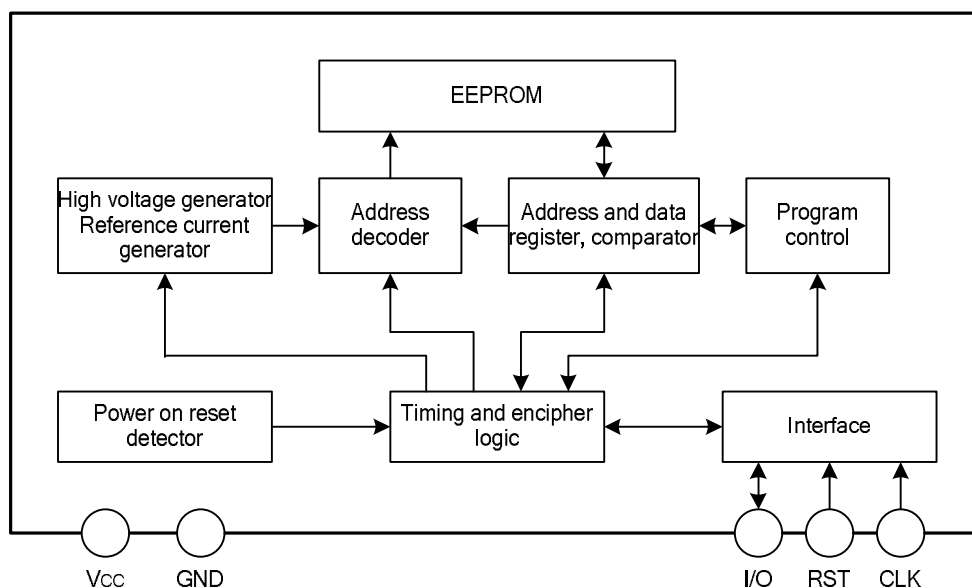* Compatible with SLE4428

APPLICATIONS

* Used for various IC cards.

P8-12   FPC-1
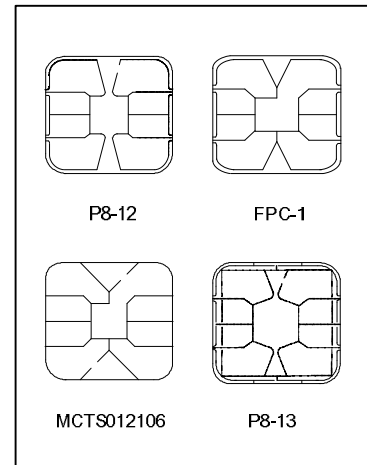
MCTS012106   P8-13

ORDERING INFORMATION

Device	Package
SC23M28A	P8-13
SC23M28B	MCTS012106
SC23M28C	P8-12
SC23M28D	FPC-1

BLOCK DIAGRAM

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ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Ratings	Unit
Power Supply Voltage	Vcc	-0.3~6	V
Input Voltage	VI	-0.3~6	V
Storage Temperature	Tstg	-40~125	°C
Power Dissipation	Ptot	60	mW

DC ELECTRICAL CHARACTERISTICS (Vcc=5V, Tamb =25°C)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc		2.4	--	5.5	V
Supply Current	Icc		--	2	10	mA
H Input Voltage(I/O, CLK, RST)	VIH		3.0	--	Vcc	V
L Input Voltage(I/O, CLK, RST)	VIL		0	--	1.2	V
H Input Current (I/O, CLK, RST)	IH		--	3	5	μA
L Output Current (VL=0.4V, Open-drain)	IOL		0.5	1.0	--	mA
H Leakage Current (VH=Vcc, Open-drain)	IOH		--	--	1	μA
Input Capacitance	Ci		--	--	10	pF
Operating Frequency	F		--	20	--	kHz

AC ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Vcc=5.0V, Tamb=25°C, and testing frequency is 20kHz)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset Time	tRE		9	--	--	μs
CLK (High Level)	tH		10	--	--	μs
CLK (Low Level)	tL		10	--	--	μs
Write Time	tW		5	--	--	ms
Erase Time	tE		5	--	--	ms
Set Up Time(D/CLK)	td1		4	--	--	μs
Set Up Time (CLK/RST)	td3		4	--	--	μs
Set Up Time (RST/CLK)	td4		4	--	--	μs
Hold Time(D/CLK)	td5		4	--	--	μs
Delay Time(CLK/D)	td2		6	--	--	μs
Rise Time(I/O, CLK, RST)	tR		--	--	1	μs
Fall Time(I/O, CLK, RST)	tF		--	--	1	μs

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PIN CONFIGURATION

```
        ┌─────────────────┐
        │                 │
   Vcc ─┤ 1           8 ├─ GND
        │                 │
   RST ─┤ 2           7 ├─ NC
        │                 │
   CLK ─┤ 3           6 ├─ I/O
        │                 │
    NC ─┤ 4           5 ├─ NC
        │                 │
        │                 │
        │ (Contact of the card) │
        └─────────────────┘
```
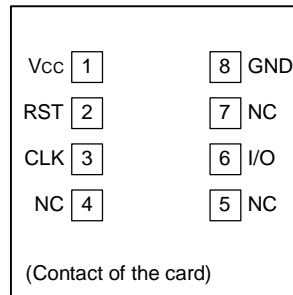
PIN DESCRIPTIONS

| Pin No.	Symbol	I/O	Description
1	VCC	--	Power supply voltage is 5V
2	RST	I	Reset signal
3	CLK	I	Clock signal
4	NC	--	No connect
5	GND	--	Ground
6	NC	--	No connect
7	I/O	I/O	Data bus(open-drain output)
8	NC	--	No connect

FUNCTION DESCRIPTIONS

SC23M28 provides 1024×8 bits EEPROM memory units with write-protect for each bit. Except PSC (Programmable Security Code) memory unit, all units are readable. The unit can be erased and written before the write-protect is active, or else the unit is only readable. The bit with write-protection can be programmed only once, and cannot be erased. The chip has one 8-bit error register which provides 8 times continuous PSC authentication, after 8 times the chip cannot be erased and written.

1. Reset and reset acknowledge

The chip enters the power on reset state when it is power on, and this state will end by the reset signal. The reset signal begins when RST changed from "0" to "1", and end when CLK changed from "0" to"1". The reset signal can stop any active instruction. Read operation must be carried out first after power on reset, then the other operations.

The reset acknowledge complies to ISO7816-3 synchronous propagation. The address counter is set to "0" automatically and will send the first data to the I/O port. As the clock signal, the address data can be read serially. The details refer to the figure 1.

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Figure 1 Reset and reset acknowledge
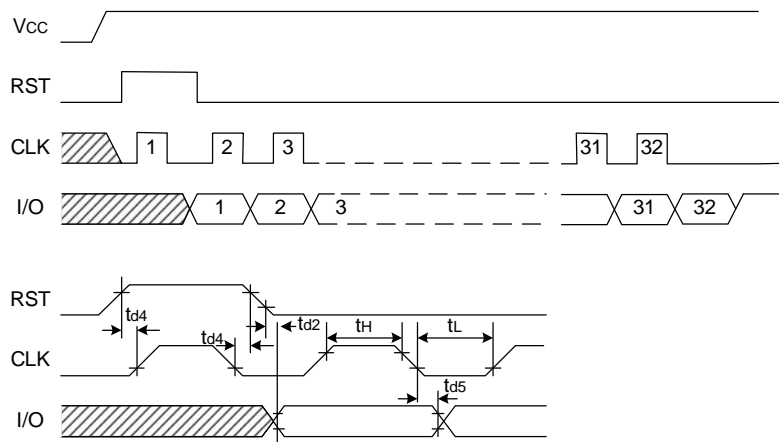
2. Instruction format

The chip inputs and outputs the data by I/O ports, and the RST signal will control the direction of the data;

RST=1, I/O is instruction input;

RST=0, I/O is data output.

Instruction table

Byte1			Byte2	Byte3	Operation
S0 S1	S2 S3 S4 S5	A8 A9	A0-A7	D0-D7	
1 0	0 0 1 1	Address bit 8, 9	Address bit 0-7	Input data	With bit-protect erasure or write
1 1	0 0 1 1			Input data	Without bit-protect erasure or write
0 0	0 0 1 1			Comparative data	Write protect bit with data comparison
0 0	1 1 0 0			Invalid	With bit-protect read
0 1	1 1 0 0			Invalid	Without bit-protect read
0 1	0 0 1 1	1 1	253	Bit mask code	Write error counter
1 0	1 1 0 0		254	PSC code 1	Authentication PSC code 1
1 0	1 1 0 0		255	PSC code 2	Authentication PSC code 2

Figure 2 Command input time sequence

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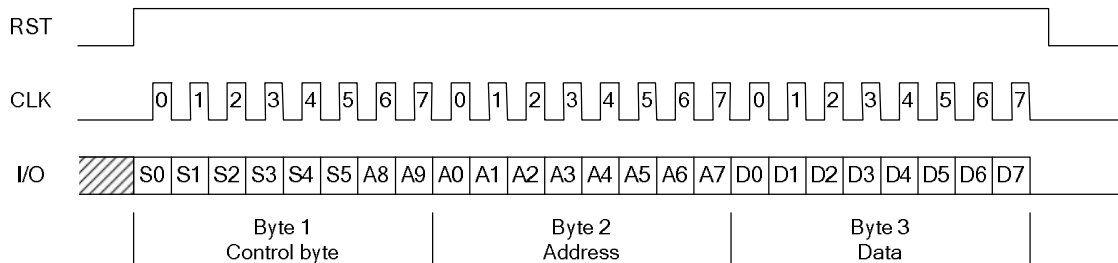
3. Instruction description

3.1 Erase/write operation

1) Erase or write with protect bit

The write protect bit is active as long as you write the data, and this unit is only readable.

2) Erase or write without protect bit.

Write the data but not set the protect bit, so this unit can still be erased and written.

3) Write protect bit with data comparison

When the command is executed, it will compare the data and the content of the destination address unit, if the contents are the same, then write "0" to the corresponding address unit; if the contents are different, do nothing.

The chip can execute 3 erase and write operation:

Erase and write (Last 203 clock cycles) (Figure3);

Only Write: used for some bits of 1 byte data change from "1" to "0"(Last 103 clock cycles)(Figure4);

Only Erase: data is FF (Last 103 clock cycles) (Figure4).

If error occurs when erase or write data, I/O port will change from high level to low level at the raising edge of the third clock cycle. (Figure5).

Figure3 Erase and write time sequence

Figure4 Only Erase or only Write time sequence

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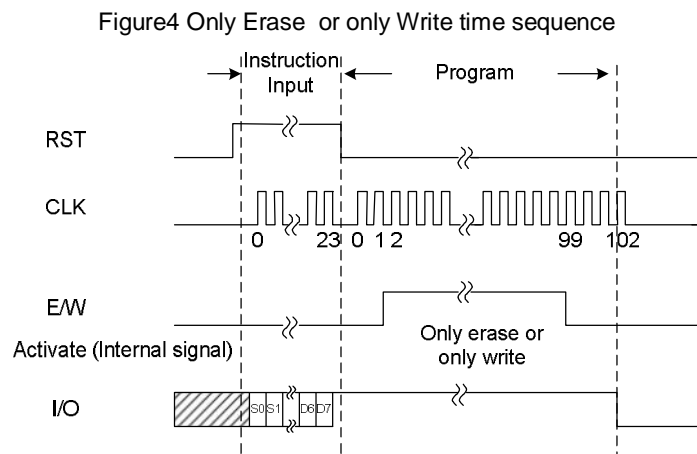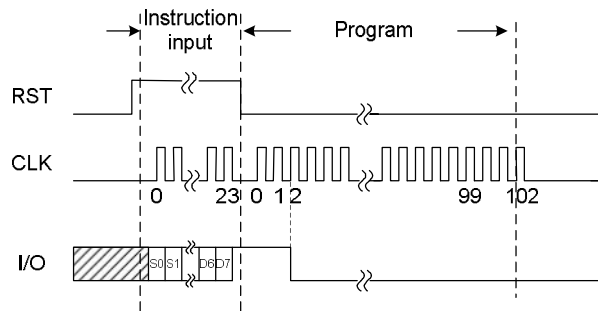Microelectronics
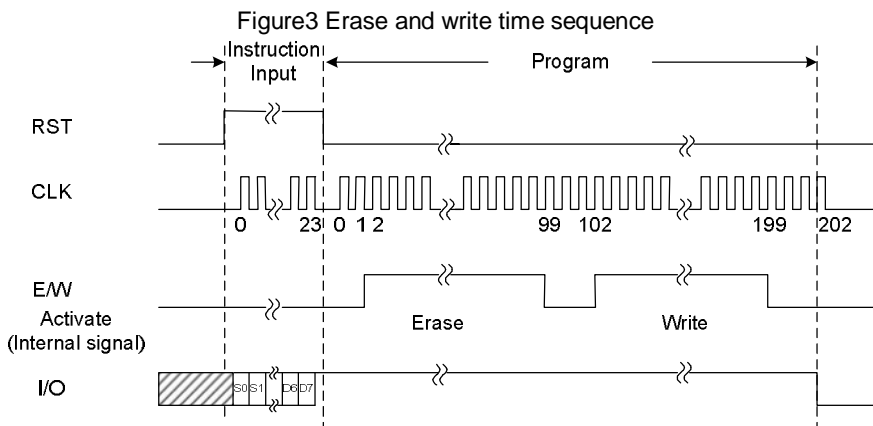
Figure5 Time sequence of erase or write error

3.2   Read operation

1) Read with protect bit

This command will read the content of the destination address unit and the corresponding protect bit together, 9 bits in total (Figure6). After 9 clock cycles, the address increases by 1 automatically.

2) Read without protect bit

This command will only read the content of the destination address unit（Figure6）. After 8 clock cycles, the address increases by 1 automatically.

When RST changes from "0" to"1", read operation stops.

Figure6 Read operation time sequence
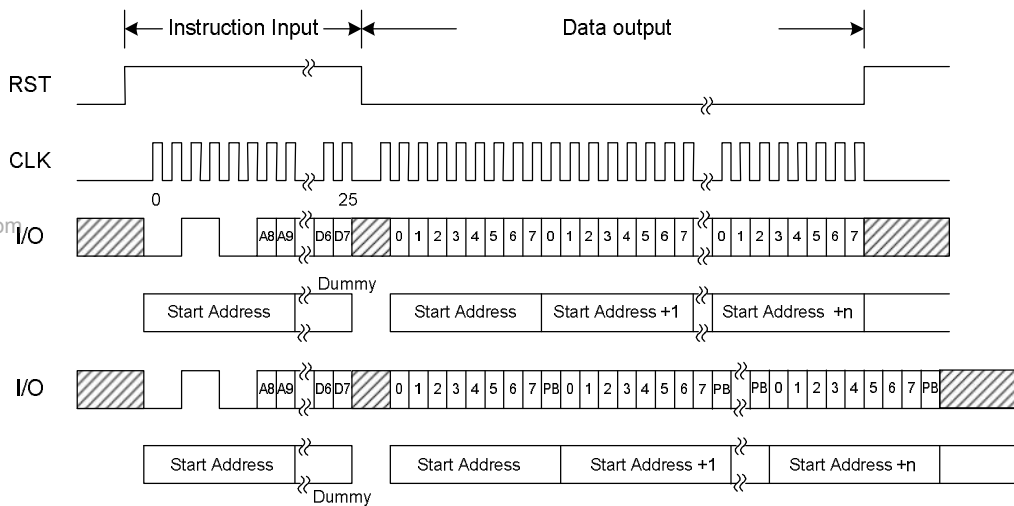
3.3   Password authentication

The SC23M28 is only readable without PSC authentication. The content of PSC cannot be read, if you try to read PSC, you will get "00".

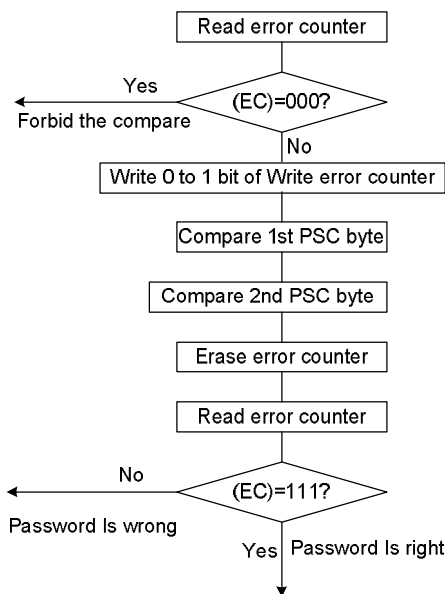The authentication steps are as follows:

--Write one to not written error counter (EC) bit and the EC address is"1021";

--Input the first byte data of PSC code, and the address is"1022";

--Input the second byte data of PSC code, and the address is "1023";

--If pass the authentication, EC can be erased.

Figure7 Time sequence of write error counter and PSC code authentication
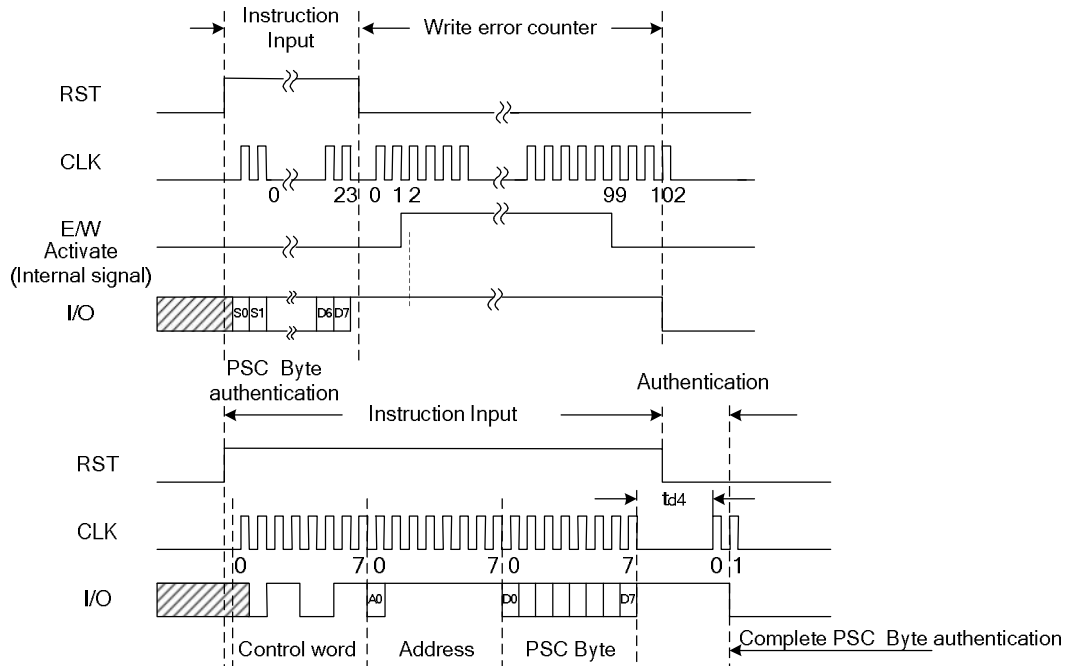
If the initial value of the error counter is "00", the error counter cannot be written, and also cannot go through the password authentication. After the PSC authentication, I/O port will change from "1" to "0" at the raising edge of the second clock no matter pass the authentication or not. When RST changes from "0"to"1", I/O port returns to "1". The flow chart is as follows:
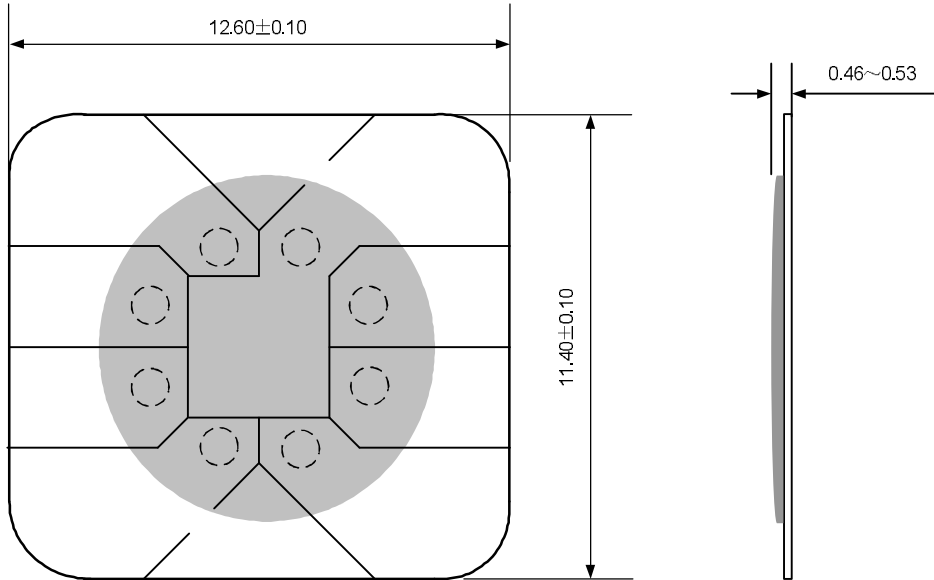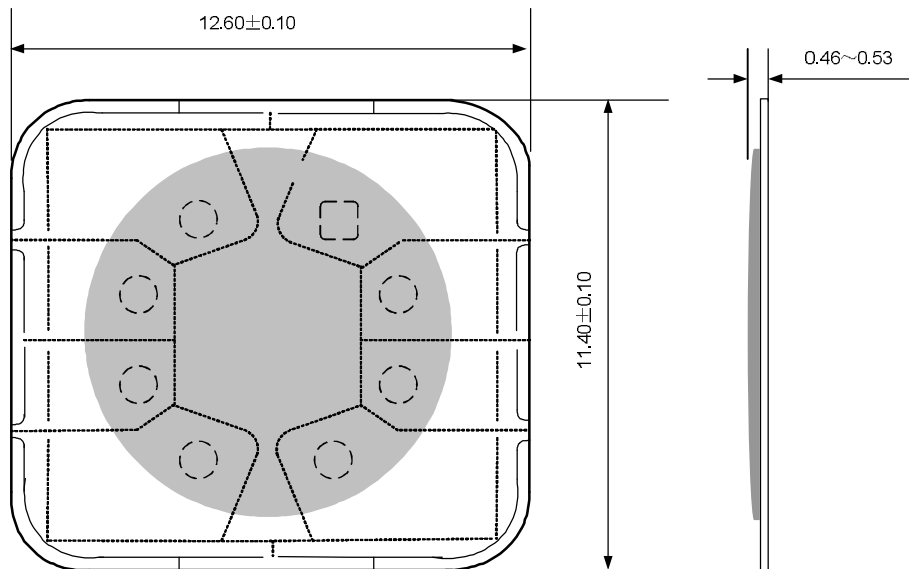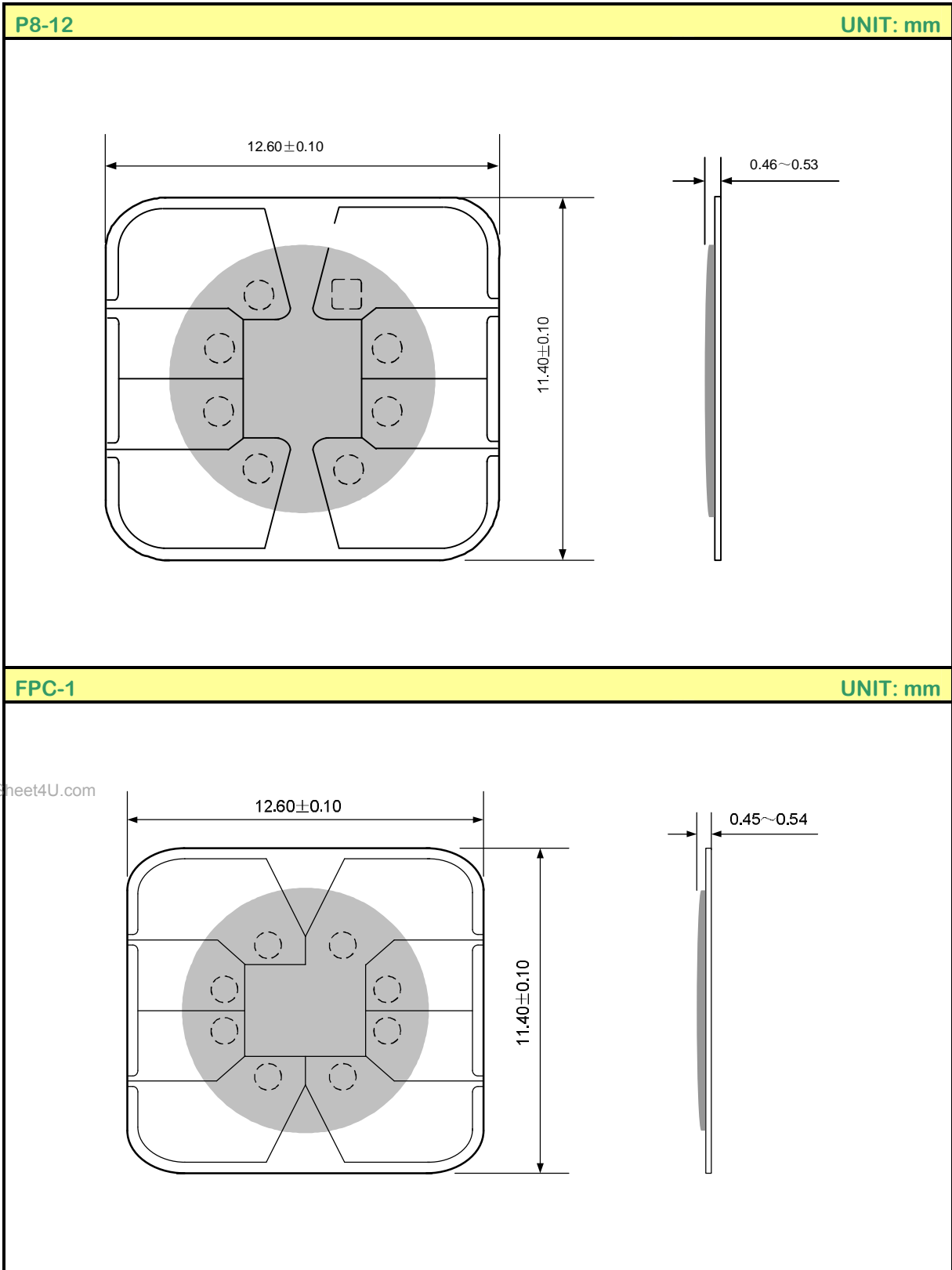
Figure8 PSC authentication flow chart

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PACKAGE OUTLINE

MCTS012106 UNIT: mm

12.60±0.10

11.40±0.10

0.46～0.53

P8-13 UNIT: mm

12.60±0.10

11.40±0.10

0.46～0.53

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PACKAGE OUTLINE

P8-12   UNIT: mm

12.60±0.10

11.40±0.10

0.46～0.53

FPC-1   UNIT: mm

12.60±0.10

11.40±0.10

0.45～0.54

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REV:1.0   2006.07.21

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CAUTION
ELECTROSTATIC
SENSITIVE DEVICE
DO NOT OPEN OR HANDLE
EXPECT AT A STATIC-FREE
WORKSTATION

HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.

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