Data Sheet, Rev. 1.73, Aug. 2005

HYB18H512321AF–12/14/16/20
HYB18H512321AFL14/16/20

512-Mbit GDDR3 Graphics RAM

RoHS compliant

Memory Products

Never stop thinking.

Edition 2005-08

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HYB18H512321AF–12/14/16/20, HYB18H512321AFL14/16/20

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Previous Revision:	Rev. 1.60	
Page	Subjects (major changes since last revision)	
75	figure 61: changed DQ setting	

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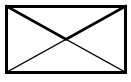

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1 Overview

1.1 Features

- 2.0 V V_{DDQ} IO voltage HYB18H512321AF–12/14/16/20
- 2.0 V V_{DD} core voltage HYB18H512321AF–12/14/16/20
- 1.8 V V_{DDQ} IO voltage HYB18H512321AFL14/16/20
- 1.8 V V_{DD} core voltage HYB18H512321AFL14/16/20
- Organization: 2048K $\times$ 32 $\times$ 8 banks
- 4096 rows and 512 columns (128 burst start locations) per bank
- Differential clock inputs (CLK and $\overline{CLK}$)
- CAS latencies of 7, 8, 9, 10, 11
- Write latencies of 3, 4
- Burst sequence with length of 4, 8.
- 4n prefetch
- Short RAS to CAS timing for Writes
- t_{RAS} Lockout support
- t_{WR} programmable for Writes with Auto-Precharge
- Data mask for write commands
- Single ended READ strobe (RDQS) per byte. RDQS edge-aligned with READ data
- Single ended WRITE strobe (WDQS) per byte. WDQS center-aligned with WRITE data
- DLL aligns RDQS and DQ transitions with Clock
- Programmable IO interface including on chip termination (ODT)
- Autoprecharge option with concurrent autoprecharge support
- 8k Refresh (32ms)
- Autorefresh and Self Refresh
- PG-TFBGA 136 package (11mm $\times$ 14mm)
- Calibrated output drive. Active termination support
- RoHS Compliant Product[1)]

1)RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

Table 1 Ordering Information

Part Number[1)]	Organisation	Clock (MHz)	Package
HYB18H512321AF–12/14/16/20	×32	800/700/600/500	PG-TFBGA 136
HYB18H512321AFL14/16/20		700/600/500	

1) HYB: designator for memory components
18H: V_{DDQ} = 1.8 V
512: 512-Mbit density
32: Organization
A: Product revision
F: Lead- and Halogen-Free
L: Low power product

1.2 Description

The Infineon 512-Mbit GDDR3 Graphics RAM is a high speed memory device, designed for high bandwidth intensive applications like PC graphics systems. The chip's 8 bank architecture is optimized for high speed.

HYB18H512321AF uses a double data rate interface and a 4n-prefetch architecture. The GDDR3 interface transfers two 32 bit wide data words per clock cycle to/from the I/O pins. Corresponding to the 4n-prefetch a single write or read access consists of a 128 bit wide, one-clock-cycle data transfer at the internal memory core and four corresponding 32 bit wide, one-half-clock-cycle data transfers at the I/O pins.

Single-ended unidirectional Read and Write Data strobes are transmitted simultaneously with Read and Write data respectively in order to capture data properly at the receivers of both the Graphics SDRAM and the controller. Data strobes are organized per byte of the 32 bit wide interface. For read commands the RDQS are edge-aligned with data, and the WDQS are center-aligned with data for write commands.

The HYB18H512321AF operates from a differential clock (CLK and $\overline{\text{CLK}}$). Commands (addresses and control signals) are registered at every positive edge of CLK. Input data is registered on both edges of WDQS, and output data is referenced to both edges of RDQS.

In this document references to 'the positive edge of CLK' imply the crossing of the positive edge of CLK and the negative edge of $\overline{\text{CLK}}$. Similarly, the 'negative edge of CLK' refers to the crossing of the negative edge of CLK and the positive edge of $\overline{\text{CLK}}$. References to RDQS are to be interpreted as any or all RDQS<3:0>. WDQS, DM and DQ should be interpreted in a similar fashion.

Read and write accesses to the HYB18H512321AF are burst oriented. The burst length is fixed to 4 and 8 and the two least significant bits of the burst address are 'Don't Care' and internally set to LOW. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the column location for the burst access. Each of the 8 banks consists of 4096 row locations and 512 column locations. An AUTO PRECHARGE function can be combined with READ and WRITE to provide a self-timed row precharge that is initiated at the end of the burst access. The pipelined, multibank architecture of the HYB18H512321AF allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

The "On Die Termination" interface (ODT) is optimized for high frequency digital data transfers and is internally controlled. The termination resistor value can be set using an external ZQ resistor or disabled through the Extended Mode Register.

The output driver impedance can be set using the Extended Mode Register. It can either be set to ZQ / 6 (autocalibration) or to 35, 40 or 45 Ohms.

Auto Refresh and Power Down with Self Refresh operations are supported.

A standard JEDEC PG-TFBGA 136 package is used which enables ultra high speed data transfer rates and a simple upgrade path from former DDR Graphics SDRAM products.

2 Pin Configuration

1	2	3	4	5	6	7	8	9	10	11	12
V_{DDQ}	V_{DD}	V_{SS}	ZQ		A			MF	V_{SS}	V_{DD}	V_{DDQ}
V_{SSQ}	DQ0	DQ1	V_{SSQ}		B			V_{SSQ}	DQ9	DQ8	V_{SSQ}
V_{DDQ}	DQ2	DQ3	V_{DDQ}		C			V_{DDQ}	DQ11	DQ10	V_{DDQ}
V_{SSQ}	WDQS0	RDQS0	V_{SSQ}		D			V_{SSQ}	RDQS1	WDQS1	V_{SSQ}
V_{DDQ}	DQ4	DM0	V_{DDQ}		E			V_{DDQ}	DM1	DQ12	V_{DDQ}
V_{DD}	DQ6	DQ5	$\overline{CAS}$		F			$\overline{CS}$	DQ13	DQ14	V_{DD}
V_{SS}	V_{SSQ}	DQ7	BA0		G			BA1	DQ15	V_{SSQ}	V_{SS}
V_{REF}	A1	$\overline{RAS}$	CKE		H			$\overline{WE}$	BA2	A5	V_{REF}
V_{SSA}	RFU	RFU	V_{DDQ}		J			V_{DDQ}	$\overline{CK}$	CK	V_{SSA}
V_{DDA}	A10	A2	A0		K			A4	A6	A8/AP	V_{DDA}
V_{SS}	V_{SSQ}	DQ25	A11		L			A7	DQ17	V_{SSQ}	V_{SS}
V_{DD}	DQ24	DQ27	A3		M			A9	DQ19	DQ16	V_{DD}
V_{DDQ}	DQ26	DM3	V_{DDQ}		N			V_{DDQ}	DM2	DQ18	V_{DDQ}
V_{SSQ}	WDQS3	RDQS3	V_{SSQ}		P			V_{SSQ}	RDQS2	WDQS2	V_{SSQ}
V_{DDQ}	DQ28	DQ29	V_{DDQ}		R			V_{DDQ}	DQ21	DQ20	V_{DDQ}
V_{SSQ}	DQ30	DQ31	V_{SSQ}		T			V_{SSQ}	DQ23	DQ22	V_{SSQ}
V_{DDQ}	V_{DD}	V_{SS}	SEN		V			RESET	V_{SS}	V_{DD}	V_{DDQ}

Figure 1 Ballout 512Mbit GDDR3 Graphics RAM [Top View, MF = Low]

2.1 Ball Definition and Description

Table 2 Ball Description

Ball	Type	Detailed Function
CLK, $\overline{CLK}$	Input	**Clock:** CLK and $\overline{CLK}$ are differential clock inputs. Address and command inputs are latched on the positive edge of CLK. Graphics SDRAM outputs (RDQS, DQs) are referenced to CLK. CLK and $\overline{CLK}$ are not internally terminated.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates the internal clock and input buffers. Taking CKE LOW provides Power Down. If all banks are precharged, this mode is called Precharge Power Down and Self Refresh mode is entered if a Auto Refresh command is issued. If at least one bank is open, Active Power Down mode is entered and no Self Refresh is allowed. All input receivers except CLK, $\overline{CLK}$ and CKE are disabled during Power Down. In Self Refresh mode the clock receivers are disabled too. Self Refresh Exit is performed by setting CKE asynchronously HIGH. Exit of Power Down without Self Refresh is accomplished by setting CKE HIGH with a positive edge of CLK. The value of CKE is latched asynchronously by Reset during Power On to determine the value of the termination resistor of the address and command inputs. CKE is not allowed to go LOW during a RD, a WR or a snoop burst.
$\overline{CS}$	Input	**Chip Select:** $\overline{CS}$ enables the command decoder when low and disables it when high. When the command decoder is disabled, new commands with the exeption of DTERDIS are ignored, but internal operations continue. $\overline{CS}$ is one of the four command balls.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** Sampled at the positive edge of CLK, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define (together with $\overline{CS}$) the command to be executed.
DQ<0:31>	I/O	**Data Input/Output:** The DQ signals form the 32 bit data bus. During READs the balls are outputs and during WRITEs they are inputs. Data is transferred at both edges of RDQS.
DM<0:3>	Input	**Input Data Mask:** The DM signals are input mask signals for WRITE data. Data is masked when DM is sampled HIGH with the WRITE data. DM is sampled on both edges of WDQS. DM0 is for DQ<0:7>, DM1 is for DQ<8:15>, DM2 is for DQ<16:23> and DM3 is for DQ<24:31>. Although DM balls are input-only, their loading is designed to match the DQ and WDQS balls.
RDQS<0:3>	Output	**Read Data Strobes:** RDQSx are unidirectional strobe signals. During READs the RDQSx are transmitted by the Graphics SDRAM and edge-aligned with data. RDQS have preamble and postamble requirements. RDQS0 is for DQ<0:7>, RDQS1 for DQ<8:15>, RDQS2 for DQ<16:23> and RDQS3 for DQ<24:31>.
WDQS<0:3>	Input	**Write Data Strobes:** WDQS are unidirectional strobe signals. During WRITEs the WDQS are generated by the controller and center aligned with data. WDQS have preamble and postamble requirements. WDQS0 is for DQ<0:7>, WDQS1 for DQ<8:15>, WDQS2 for DQ<16:23> and WDQS3 for DQ<24:31>.
BA<0:2>	Input	**Bank Address Inputs:** BA select to which internal bank an ACTIVATE, READ, WRITE or PRECHARGE command is being applied. BA are also used to distinguish between the MODE REGISTER SET and EXTENDED MODE REGISTER SET commands.
A<0:11>	Input	**Address Inputs:** During ACTIVATE, A0-A11 defines the row address. For READ/WRITE, A2-A7 and A9 defines the column address, and A8 defines the auto precharge bit. If A8 is HIGH, the accessed bank is precharged after execution of the column access. If A8 is LOW, AUTO PRECHARGE is disabled and the bank remains active. Sampled with PRECHARGE, A8 determines whether one bank is precharged (selected by BA<0:2>, A8 LOW) or all 8 banks are precharged (A8 HIGH). During (EXTENDED) MODE REGISTER SET the address inputs define the register settings. A<0:11> are sampled with the positive edge of CLK.

Table 2 Ball Description

Ball	Type	Detailed Function
ZQ	-	**ODT Impedance Reference:** The ZQ ball is used to control the ODT impedance.
RES	Input	**Reset pin:** The RES pin is a V_{DDQ} CMOS input. RES is not internally terminated. When RES is at LOW state the chip goes into full reset. The chip stays in full reset until RES goes to HIGH state. The Low to High transition of the RES signal is used to latch the CKE value to set the value of the termination resistors of the address and command inputs. After exiting the full reset a complete initialization is required since the full reset set the internal settings to default.
MF	Input	**Mirror function pin:** The MF pin is a V_{DDQ} CMOS input. This pin must be hardwired on board either to a power or to a ground plane. With MF set to HIGH, the command and address pins are reassigned in order to allow for an easier routing on board for a back to back memory arrangement.
SEN	Input	Enables **Boundary Scan** Functionality. If Boundary Scan is not used PIN should be constantly connected to GND.
V_{REF}	Supply	**Voltage Reference:** V_{REF} is the reference voltage input.
V_{DD}, V_{SS}, V_{DDA}, V_{SSA}	Supply	**Power Supply:** Power and Ground for the internal logic. V_{DD} and V_{DDA} must be provided by the same power rail. Shorted in the package.
V_{DDQ}, V_{SSQ}	Supply	**I/O Power Supply:** Isolated Power and Ground for the output buffers to provide improved noise immunity.
NC, RFU	-	Please do not connect No Connect and Reserved for Future Use balls.

2.2 Mirror Function

The GDDR3 Graphics RAM provides a ball mirroring feature that is enabled by applying a logic HIGH on ball MF. This function allows for efficient routing in a clam shell configuration.

Depending of the logic state applied on MF, the command and address signals will be assigned to different balls. The default ball configuration (see **Figure 1**) correponds to MF = LOW.

The DC level (HIGH or LOW) must be applied on the MF pin at power up and is not allowed to change after that.

Table 3 shows the ball assignment as a function of the logic state applied on MF.

Table 3 Ball Assignment with Mirror

MF Logic State		Signal
LOW	**HIGH**	
H3	H10	$\overline{RAS}$
F4	F9	$\overline{CAS}$
H9	H4	$\overline{WE}$
F9	F4	$\overline{CS}$
H4	H9	CKE
K4	K9	A0
H2	H11	A1
K3	K10	A2
M4	M9	A3
K9	K4	A4
H11	H2	A5
K10	K3	A6

Table 3 Ball Assignment with Mirror (cont'd)

MF Logic State		Signal
LOW	**HIGH**	
L9	L4	A7
K11	K2	A8
M9	M4	A9
K2	K11	A10
L4	L9	A11
G4	G9	BA0
G9	G4	BA1
H10	H3	BA2

2.3 Functional Block Diagram

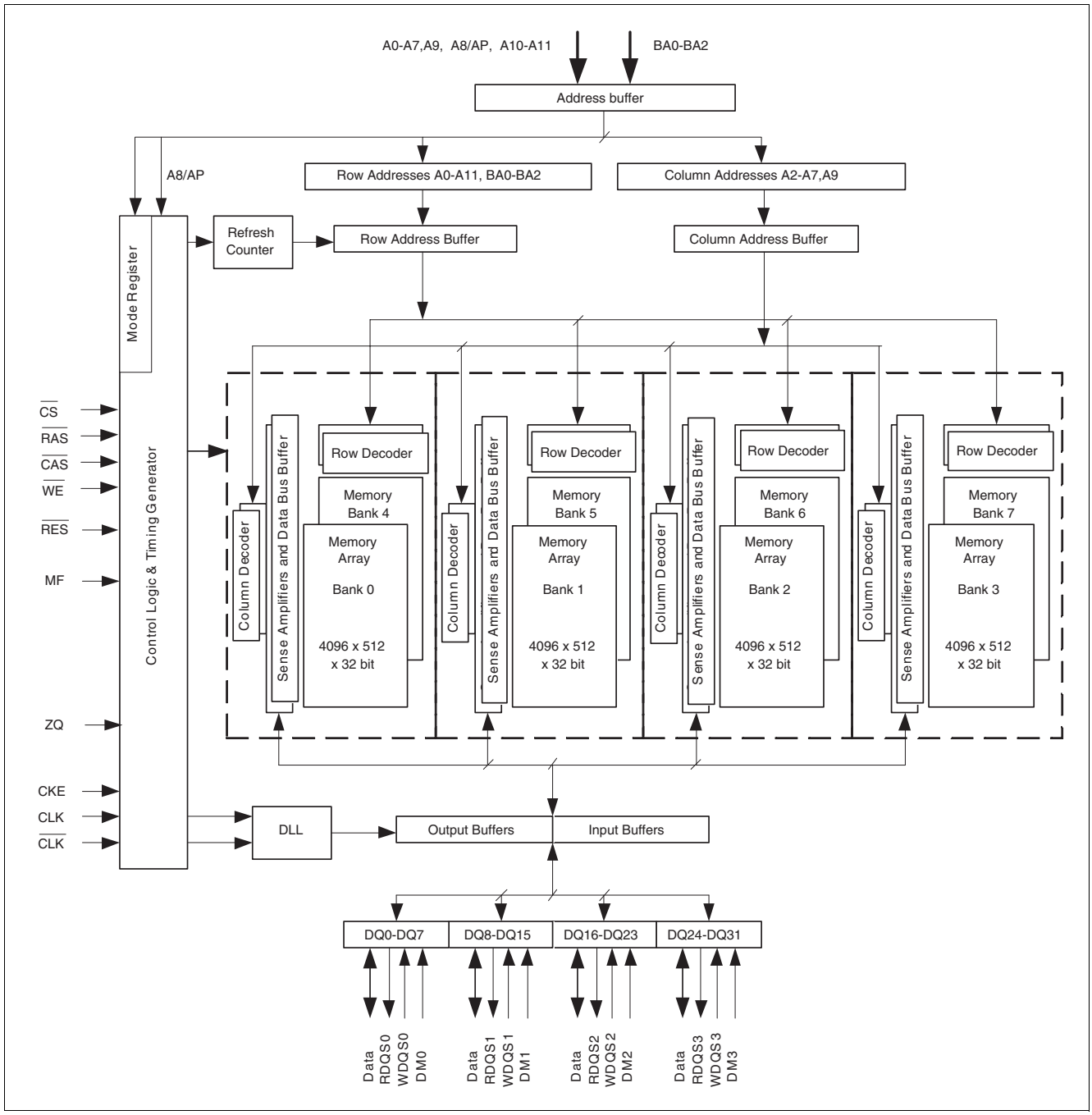

Figure 2 Functional Block Diagram

2.4 Commands

2.4.1 Command Table

In the following table CKEn refers to the positive edge of CLK corresponding to the clock cycle when the command is given to the Graphics SDRAM. CKEn-1 refers to the previous positive edge of CLK. For all command and address inputs CKEn is implied.

All input states or sequences not shown are illegal or reserved.

Table 4 Command Overview

Operation	Code	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0	BA1	BA2	A8	A2-7 A9-11	Note
Device Deselect	DESEL	H	H	H L X H	X X H	X L H	X		X	X	X		1)
Data Terminator Disable	DTERDIS	H	H	H	H	L	H	X	X	X	X	X	1)2)
No Operation	NOP	H	H	L	H	H	H	X	X	X	X	X	
Mode Register Set	MRS	H	H	L	L	L	L	0	0	0	OPCODE		
Extended Mode Register Set	EMRS	H	H	L	L	L	L	1	0	0	OPCODE		
Bank Activate	ACT	H	H	L	L	H	H	BA	BA	BA	Row Address		1)3)
Read	RD	H	H	L	H	L	H	BA	BA	BA	L	Col.	1)4)
Read w/ Autoprecharge	RD/A	H	H	L	H	L	H	BA	BA	BA	H	Col.	1)4)
Write	WR	H	H	L	H	L	L	BA	BA	BA	L	Col.	1)4)
Write w/ Autoprecharge	WR/A	H	H	L	H	L	L	BA	BA	BA	H	Col.	1)4)
Precharge	PRE	H	H	L	L	H	L	BA	BA	BA	L	X	1)
Precharge All	PREALL	H	H	L	L	H	L	X	X	X	H	X	1)
Auto Refresh	AREF	H	H	L	L	L	H	X	X	X	X	X	1)5)
Power Down Mode Entry	PWDNEN	H	L	H L	X H	X H	X H	X	X	X	X	X	1)6)
Power Down Mode Exit	PWDNEX	L	H	X	X	X	X	X	X	X	X	X	1)7)
Self Refresh Entry	SREFEN	H	L	L	L	L	H	X	X	X	X	X	1)8)
Self Refresh Exit	SREFEX	L	H	X	X	X	X	X	X	X	X	X	1)9)

1) X represents “Don’t Care”.
2) This command is invoked when a Read is issued on another DRAM rank placed on the same command bus. Cannot be in power-down or self-refresh state. The Read command will cause the data termination to be disabled. Refer to **Figure 14** for timing.
3) BA0 - BA2 provide bank address, A0 - A11 provide the row address.
4) BA0 - BA2 provide bank address, A2- A7, A9 provide the column address, A8/AP controls Auto Precharge.
5) Auto Refresh and Self Refresh Entry differ only by the state of CKE.
6) PWDNEN is selected by issuing a DESEL or NOP at the first positive CLK edge following the HIGH to LOW transition of CKE.
7) First possible valid command after t_{XPN}. During t_{XPN} only NOP or DESEL commands are allowed.
8) Self Refresh is selected by issuing AREF at the first positive CLK edge following the HIGH to LOW transition of CKE.
9) First possible valid command after t_{XSC}. During t_{XSC} only NOP or DESEL commands are allowed.

Abbreviations: BA: Bank Adress; Col.: Column Adress

2.4.2 Description of Commands

Table 5 Description of Commands

Command	Description
DESEL	The DESEL function prevents new commands from being executed by the Graphics SDRAM. The Graphics SDRAM is effectively deselected. Operations in progress are not affected.
NOP	The NOP command is used to perform a no operation to the Graphics SDRAM, which is selected ($\overline{CS}$ is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.
MRS	The Mode Register is loaded via address inputs A0 - A11. For more details see **"Mode Register Set Command (MRS)" on Page 40** . The MRS command can only be issued when all banks are idle and no bursts are in progress. A subsequent executable command cannot be issued until t_{MRD} is met.
EMRS	The Extended Mode Register is loaded via address inputs A0 - A11. For more details see section **"Extended Mode Register Set Command (EMRS)" on Page 37**. The EMRS command can only be issued when all banks are idle and no bursts are in progress. A subsequent executable command cannot be issued until t_{MRD} is met.
ACT	The ACT command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0 - BA2 inputs selects the bank, and the address provided in inputs A0 - A11 selects the row. This row remains active (or open) for accesses until a precharge (PRE, RD/A, or WR/A command) is issued to that bank. A precharge must be issued before opening a different row in the same bank.
RD	The RD command is used to initiate a burst read access to an active row. The value on the BA0 - BA2 inputs selects the bank, and the address provided on inputs A2-A7, A9 selects the column location. The row will remain open for subsequent accesses. For RD commands the value on A8 is set LOW.
RD/A	The RD/A command is used to initiate a burst read access to an active row. The value on the BA0 - BA2 inputs selects the bank, and the address provided on inputs A2-A7, A9 selects the column location. The value on input A8 is set HIGH. The row being accessed will be precharged at the end of the read burst. The same individual-bank precharge function is performed like it is described for the PRE command. Auto precharge ensures that the precharge is initiated at the earliest valid stage within the burst. The user must not issue a new ACT command to the same bank until the precharge time (t_{RP}) is completed. This time is determined as if an explicit PRE command was issued at the earliest possible time as described in section **"Reads (RD)" on Page 55**.
WR	The WR command is used to initiate a burst write access to an active row. The value on the BA0 - BA2 inputs selects the bank, and the address provided on inputs A2-A7, A9 selects the column location. The row will remain open for subsequent accesses. For WR commands the value on A8 is set LOW. Input data appearing on the DQs is written to the memory array depending on the value on the DM input appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to the memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a write will not be executed for that byte / column location.

Table 5 Description of Commands

Command	Description
WR/A	The WR/A command is used to initiate a burst write access to an active row. The value on the BA0, BA1 and BA2 inputs selects the bank, and the address provided on inputs A2-A7, A9 selects the column location. The value on input A8 is set HIGH. The row being accessed will be precharged at the end of the write burst. The same individual-bank precharge function is performed which is described for the PRE command. Auto precharge ensures that the precharge is initiated at the earliest valid stage within the burst. The user is not allowed to issue a new ACT to the same bank until the precharge time (t_{RP}) is completed. This time is determined as if an explicit PRE command was issued at the earliest possible time as described in section **"Writes (WR)" on Page 45**. Input data appearing on the DQs is written to the memory array depending on the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to the memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a write will not be executed to that byte / column location.
PRE	The PRE command is used to deactivate the open row in a particular bank. The bank will be available for a subsequent row access a specified time (t_{RP}) after the PRE command is issued. Inputs BA0 - BA2 select the bank to be precharged. A8/AP is set to LOW. Once a bank has been precharged, it is in the idle state and must be activated again prior to any RD or WR commands being issued to that bank. A PRE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.
PREALL	The PREALL command is used to deactivate all open rows in the memory device. The banks will be available for a subsequent row access a specified time (t_{RP}) after the PREALL command is issued. Once the banks have been precharged, they are in the idle state and must be activated prior to any read or write commands being issued. The PREALL command will be treated as a NOP for those banks where there is no open row, or if a previously open row is already in the process of precharging. PREALL is issued by a PRE command with A8/AP set to HIGH.
AREF	The AREF is used during normal operation of the GDDR3 Graphics RAM to refresh the memory content. The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AREF command. The HYB18H512321AF requires AREF cycles at an average periodic interval of t_{REFI}(max). To improve efficiency a maximum number of eight AREF commands can be posted to one memory device (with t_{RFC} from AREF to AREF) as described in section **"Auto Refresh Command (AREF)" on Page 70**. This means that the maximum absolute interval between any AREF command is 8 x t_{REFI}(max). This maximum absolute interval is to allow the GDDR3 Graphics RAM output drivers and internal terminators to recalibrate, compensating for voltage and temperature changes. All banks must be in the idle state before issuing the AREF command. They will be simultaneously refreshed and return to the idle state after AREF is completed. t_{RFC} is the minimum required time between an AREF command and a following ACT/AREF command.
SREFEN	The Self Refresh function can be used to retain data in the GDDR3 Graphics RAM even if the rest of the system is powered down. When entering the Self Refresh mode by issuing the SREFEN command, the GDDR3 Graphics RAM retains data without external clocking. The SREFEN command is initiated like an AREF command except CKE is disabled (LOW). The DLL is automatically disabled upon entering Self Refresh mode and automatically enabled and reset upon exiting Self Refresh. (1000 cycles must then occur before a RD command can be issued) The active terminations remain enabled during Self Refresh. Input signals except CKE are "Don't Care". If two GDDR3 Graphics RAMs share the same Command and Address bus, Self Refresh may be entered only for the two devices at the same time.

Table 5 Description of Commands

Command	Description
SREFEX	The SREFEX command is used to exit the Self Refresh mode. The DLL is automatically enabled and resetted upon exiting. The procedure for exiting Self Refresh requires a sequence of commands. First CLK and $\overline{CLK}$ must be stable prior to CKE going from LOW to HIGH. Once CKE is HIGH, the GDDR3 Graphics RAM must receive only NOP/DESEL commands until t_{XSNR} is satisfied. This time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh, DLL requirements and output calibration is to apply NOPs for 1000 cycles before applying any other command to allow the DLL to lock and the output drivers to recalibrate.
PWDNEN	The PWDNEN command enables the power down mode. It is entered when CKE is set low together with a NOP/DESEL. The CKE signal is sampled at the rising edge of the clock. Once the power down mode is initiated, all of the receiver circuits except CLK and CKE are gated off to reduce power consumption. The DLL remains active (unless disabled before with EMRS). All banks can be set to idle state or stay active. During Power Down Mode, refresh operations cannot be performed; therefore the refresh conditions of the chip have to be considered and if necessary Power Down state has to be left to perform an Auto Refresh cycle. If two GDDR3 Graphics RAMs share the same Command and Address bus, Power down may be entered only for the two devices at the same time.
PWDNEX	A CKE HIGH value sampled at a low to high transition of CLK is required to exit power down mode. Once CKE is HIGH, the GDDR3 Graphics RAM must receive only NOP/DESEL commands until t_{XPN} is satisfied. After t_{XPN} any command can be issued, but it has to comply with the state in which the power down mode was entered.
DTERDIS	Data Termination Disable (Bus snooping for RD commands) : The Data Termination Disable Command is detected by the device by snooping the bus for RD commands excluding $\overline{CS}$. The GDDR3 Graphics RAM will disable its Data terminators when a RD command is detected. The terminators are disabled starting at CL - 1 clocks after the RD command is detected and the duration is 4 clocks. In a two rank system, both DRAM devices will snoop the bus for RD commands to either device and both will disable their terminators if a RD command is detected. The command and address terminators are always enabled. See **Figure 14** for an example of when the data terminators are disabled during a RD command.

Table 6 Minimum delay from RD/A and WR/A to any other command (to another bank) with concurrent Autoprecharge

From Command	To Command	Minimum delay to another bank (with concurrent autoprecharge)	Note
WR/A	RD or RD/A	$(WL + 2) \times t_{CK} + t_{WTR}$	
	WR or WR/A	$2 \times t_{CK}$	
	PRE	t_{CK}	
	ACT	t_{CK}	
RD/A	RD or RD/A	$2 \times t_{CK}$	
	WR or WR/A	$(CL + 4 - WL) \times t_{CK}$	
	PRE	t_{CK}	
	ACT	t_{CK}	

2.5 State Diagram and Truth Tables

2.5.1 State Diagram for One Activated Bank

The following diagram shows all possible states and transitions for one activated bank. The other 7 banks of the Graphics SDRAM are assumed to be in idle state.

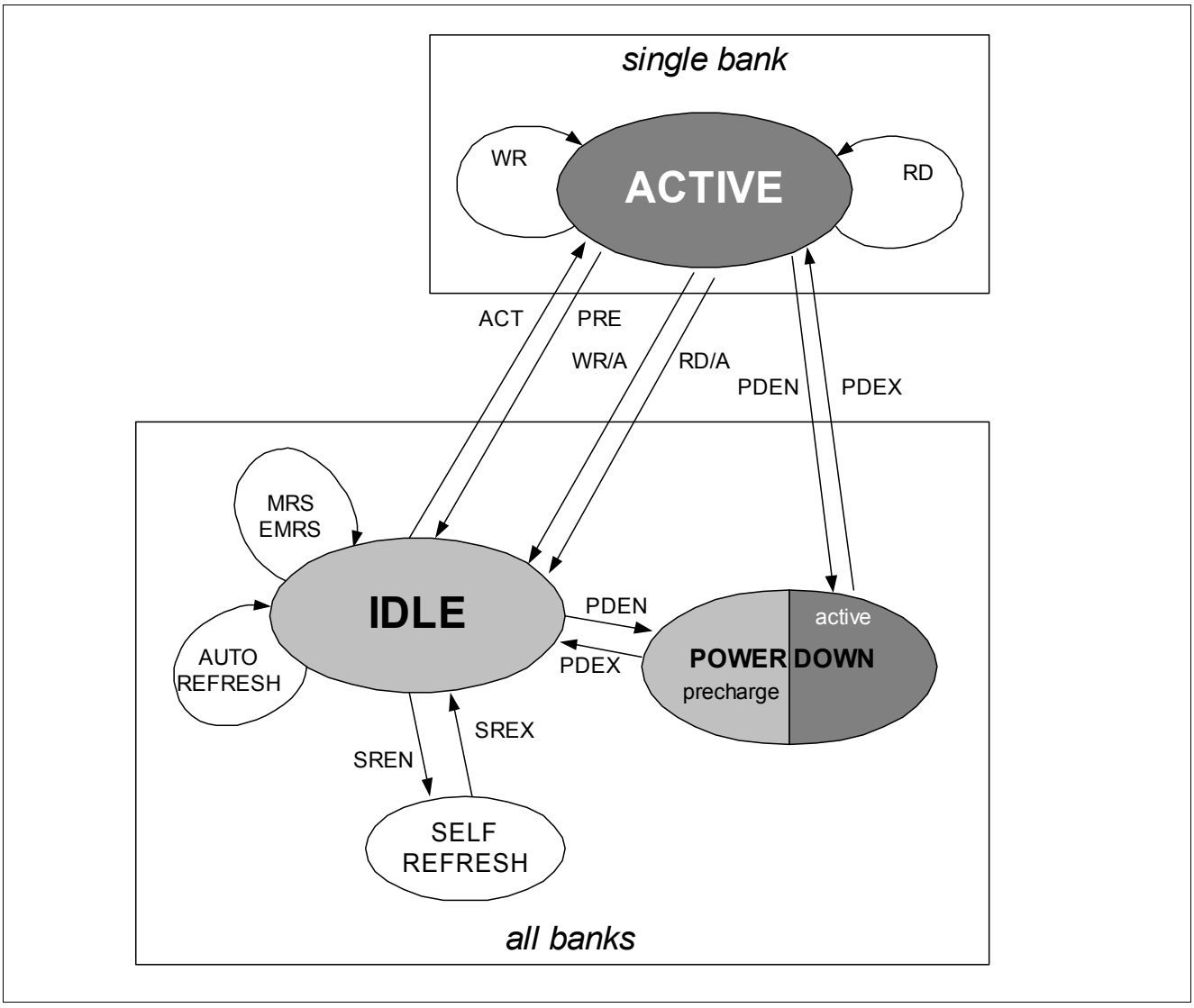

Figure 3 State diagram for one bank

Note: MRS, EMRS, AUTO REFRESH, SELF REFRESH and precharge POWER DOWN are only allowed if all 8 banks are idle.

2.5.2 Function Truth Table for more than one Activated Bank

If there is more than one bank activated in the Graphics SDRAM, some commands can be performed in parallel due to the chip's multibank architecture. The following table defines for which commands such a scheme is possible. All other transitions are illegal. Notes 1-11 define the start and end of the actions belonging to a submitted command. This table is based on the assumption that there are no other actions ongoing on bank n or bank m. If there are any actions ongoing on a third bank t_{RRD}, t_{RTW} and t_{WTR} have to be taken always into account.

Table 7 Function Truth Table I

Current State	ongoing action on bank n	possible action in parallel on bank m
ACTIVE	ACTIVATE 1)	ACT, PRE, WRITE, WRITE/A, READ, READ/A 2)
	WRITE 3)	ACT, PRE, WRITE, WRITE/A, READ, READ/A4)
	WRITE/A 5)	ACT, PRE, WRITE, WRITE/A, READ 6)
	READ 7)	ACT, PRE, WRITE, WRITE/A, READ, READ/A8)
	READ/A 9)	ACT, PRE, WRITE, WRITE/A, READ, READ/A 8)
	PRECHARGE 10)	ACT, PRE, WRITE, WRITE/A, READ, READ/A 11)
	PRECHARGE ALL 10)	-
	POWER DOWN ENTRY 12)	-
IDLE	ACTIVATE 1)	ACT
	POWER DOWN ENTRY 12)	-
	AUTO REFRESH 13)	-
	SELF REFRESH ENTRY 12)	-
	MODE REGISTER SET (MRS)14)	-
	EXTENDED MRS 14)	-
POWER DOWN	POWER DOWN EXIT 15)	-
SELF REFRESH	SELF REFRESH EXIT 16)	-

1) Action ACTIVATE starts with issuing the command and ends after t_{RCD}.
2) During action ACTIVATE an ACT command on another bank is allowed considering t_{RRD}, a PRE command on another bank is allowed any time. WR, WR/A, RD and RD/A are always allowed.
3) Action WRITE starts with issuing the command and ends tWR after the first pos. edge of CLK following the last falling WDQS edge.
4) during action WRITE an ACT or a PRE command on another bank is allowed any time. A new WR or WR/A command on another bank must be separated by at least one NOP from the ongoing WRITE. RD or RD/A are not allowed before t_{WTR} is met.
5) Action WRITE/A starts with issuing the command and ends tWR after the first positive edge of CLK following the last falling WDQS edge.
6) during action WRITE/A an ACT or a PRE command on another bank is allowed any time. A new WR or WR/A command on another bank has to be separated by at least one NOP from the ongoing command. RD is not allowed before tWTR is met. RD/A is not allowed during an ongoing WRITE/A action.
7) Action READ starts with issuing the command and ends with the first positive edge of CLK following the last falling edge of RDQS.
8) during action READ and READ/A an ACT or a PRE command on another bank is allowed any time. A new RD or RD/A command on another bank has to be separated by at least one NOP from the ongoing command. A WR or WR/A command on another bank has to meet t_{RTW}.
9) Action READ/A starts with issuing the command and ends with the first positive edge of CLK following the last falling edge of RDQS.
10) Action PRECHARGE and PRECHARGE ALL start with issuing the command and ends after t_{RP}.
11) During Action ACTIVE an ACT command on another banks is allowed considering t_{RRD}. A PRE command on another bank is allowed any time. WR, WR/A, RD and RD/A are always allowed.
12) During POWER DOWN and SELF REFRESH only the EXIT commands are allowed.

13) AUTO REFRESH starts with issuing the command and ends after t_{RFC}.
14) Actions MODE REGISTER SET and EXTENDED MODE REGISTER SET start with issuing the command and ends after t_{MRD}.
15) Action POWER DOWN EXIT starts with issuing the command and ends after t_{XPN}.
16) Action SELF REFRESH EXIT starts with issuing the command and ends after t_{XSC}.

2.6 Function Truth Table for CKE

Table 8 Function Truth Table II (CKE Table)

CKE n-1	CKE n	CURRENT STATE	COMMAND	ACTION
L	L	Power Down	X	stay in Power Down
		Self Refresh	X	stay in Self Refresh
L	H	Power Down	DESEL or NOP	Exit Power Down
		Self Refresh	DESEL or NOP	Exit Self Refresh [5]
H	L	All Banks Idle	DESEL or NOP	Entry Precharge Power Down
		Bank(s) Active	DESEL or NOP	Entry Active Power Down
		All Banks Idle	Auto Refresh	Entry Self Refresh

Note:

1. *CKEn is the logic step at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.*
2. *Current state is the state of the GDDR3 Graphics RAM immediatly prior to clock edge n.*
3. *COMMAND is the command registered at clock edge n, and ACTION is a result of COMMAND.*
4. *All states and sequences not shown are illegal or reserved.*
5. *DESEL or NOP commands should be issued on any clock edges occuring during the t_{XSR} period. A minimum of 1000 clock cycles is required before applying any other valid command.*

3 Boundary Scan

3.1 General Description

The 512Mb GDDR3 incorporates a modified boundary scan test mode. This mode doesn't operate in accordance with IEEE Standard 1149.1-1990. To save the current GDDR3 ball-out, this mode will scan the parallel data input and output the scanned data through the WDQS0 pin controlled by SEN.

3.2 Disabling the scan feature

It is possible to operate the 512Mb GDDR3 without using the boundary scan feature. SEN (at U-4 of 136- ball package) should be tied LOW(VSS) to prevent the device from entering the boundary scan mode. The other pins which are used for scan mode, RES, MF, WDQS0 and $\overline{CS}$ will be operating at normal GDDR3 functionalities when SEN is deasserted.

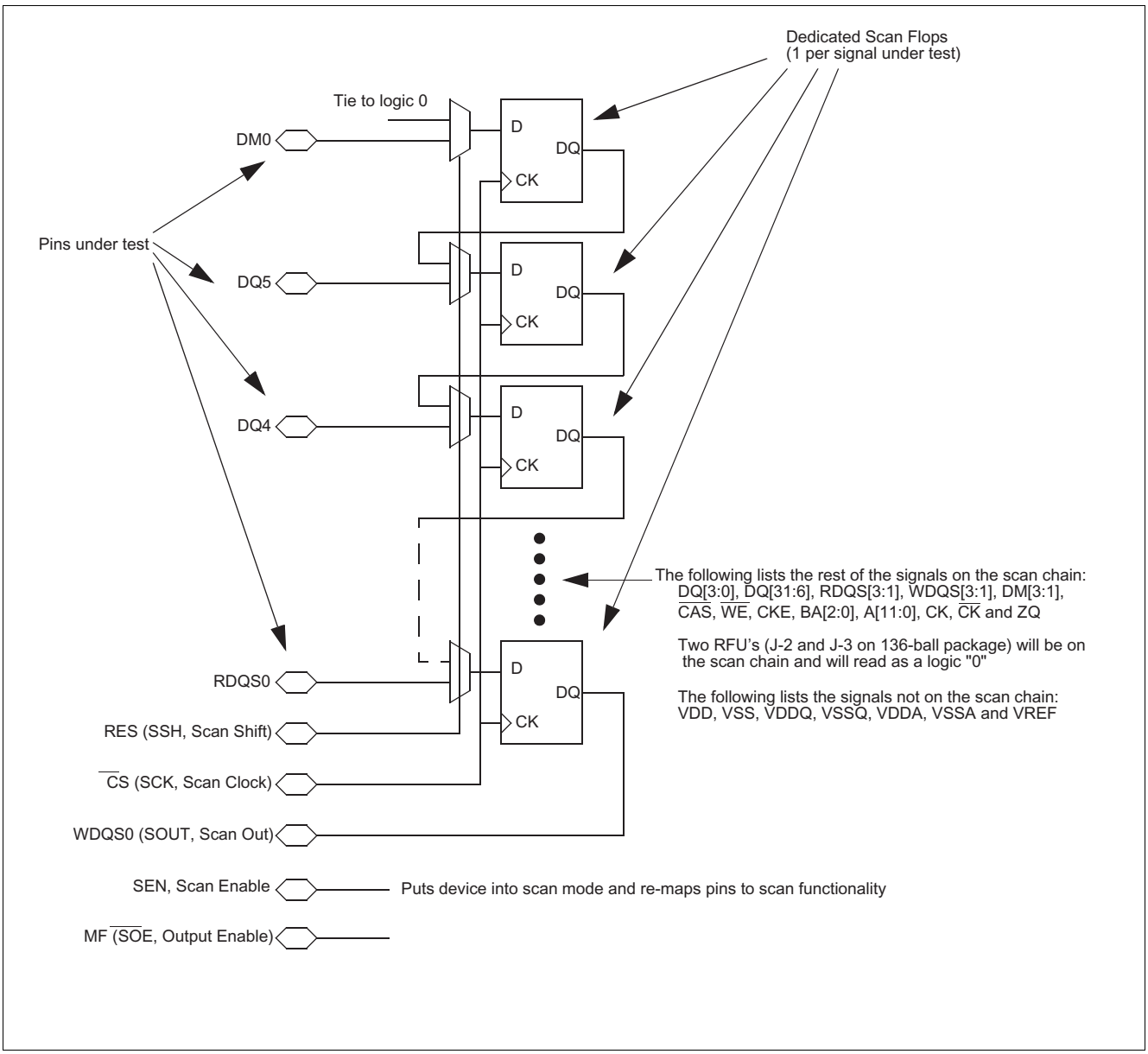

Figure 4 Internal Block Diagram (Reference only)

Table 9 Boundary Scan Exit) Order

BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL
1	D-3	13	E-10	25	K-11	37	R-10	49	L-3	61	G-4
2	C-2	14	F-10	26	K-10	38	T-11	50	M-2	62	F-4
3	C-3	15	E-11	27	K-9	39	T-10	51	M-4	63	F-2
4	B-2	16	G-10	28	M-9	40	T-3	52	K-4	64	G-3
5	B-3	17	F-11	29	M-11	41	T-2	53	K-3	65	E-2
6	A-4	18	G-9	30	L-10	42	R-3	54	K-2	66	F-3
7	B-10	19	H-9	31	N-11	43	R-2	55	L-4	67	E-3
8	B-11	20	H-10	32	M-10	44	P-3	56	J-3		
9	C-10	21	H-11	33	N-10	45	P-2	57	J-2		
10	C-11	22	J-11	34	P-11	46	N-3	58	H-2		
11	D-10	23	J-10	35	P-10	47	M-3	59	H-3		
12	D-11	24	L-9	36	R-11	48	N-2	60	H-4		

Notes

1. *When the device is in scan mode, the mirror function will be disabled and none of the pins are remapped.*
2. *Since the other input of the MUX for DM0 tied to GND, the device will output the continuous zeros after scanning a bit #67, if the chip stays in scan shift mode.*
3. *Two RFU balls (#56 and #57) in the scan order, will read as a logic“0”.*

Table 10 Scan Pin Description

PACKAGE BALL	SYMBOL	NORMAL FUNCTION	TYPE	DESCRIPTION
V-9	SSH	RES	Input	**Scan Shift:** Capture the data input from the pad at logic LOW and shift the data on the chain at logic HIGH.
F-9	SCK	$\overline{CS}$	Input	**Scan Clock:** Not a true clock, could be a single pulse or series of pulses. All scan inputs will be referenced to rising edge of the scan clock
D-2	SOUT	WDQS0	Output	**Scan Output**
V-4	SEN	SEN	Input	**Scan Enable:** Logic HIGH enables the device into scan mode and will be disabled at logic LOW. Must be tied to GND when not in use.
A-9	$\overline{SOE}$	MF	Input	**Scan Output Enable:** Enables (registered LOW) and disables (registered HIGH) SOUT data. This pin will be tied to V_{DD} or GND through a resistor (typically 1KΩ for normal operation. Tester needs to overdrive this pin to guarantee the required input logic level in scan mode.

Notes

1. *When SEN is asserted, no commands are to be executed by the GDDR3. This applies both to user commands and manufacturing commands which may exist while RES is deasserted.*
2. *The Scan Function can be used right after bringing up V_{DD} / V_{DDQ} of the device. No initialization sequence of the device is required. After leaving the Scan Function it is required to run through the complete initialization sequence.*
3. *In Scan Mode all terminations for CMD/ADD and DQ, DM, RDQS and WDQS are switched off.*
4. *In a double-load clam-shell configuration, SEN will be asserted to both devices. Separate two $\overline{SOE}$'s should be provided to top and bottom devices to access the scanned output. When either of the devices is in scan mode, $\overline{SOE}$ for the other device which is not in a scan will be disabled.*

Table 11 Scan DC Electrical Characteristics and Operating Conditions

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	V_{IH}(DC)	V_{REF}+0.15	—		1)2)
Input Low (Logic 0) Voltage -	V_{IL}(DC)	—	V_{REF}-0.15 V		1) 2)

1) The parameter applies only when SEN is asserted.
2) All voltages referenced to GND.

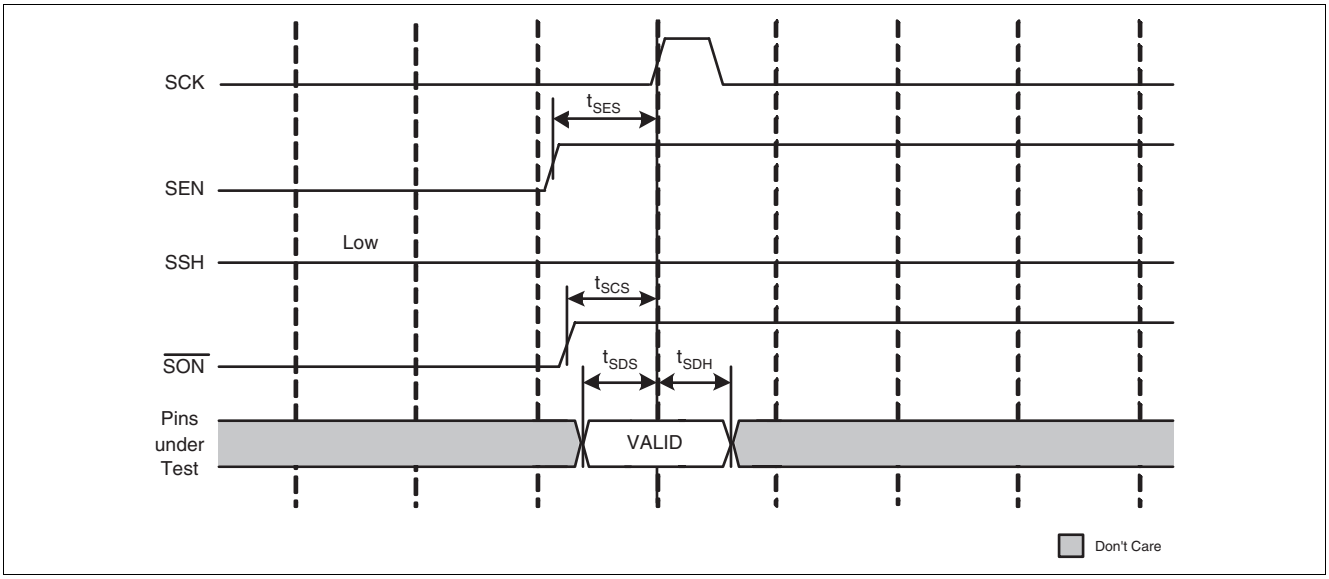

Figure 5 Scan Capture Timing

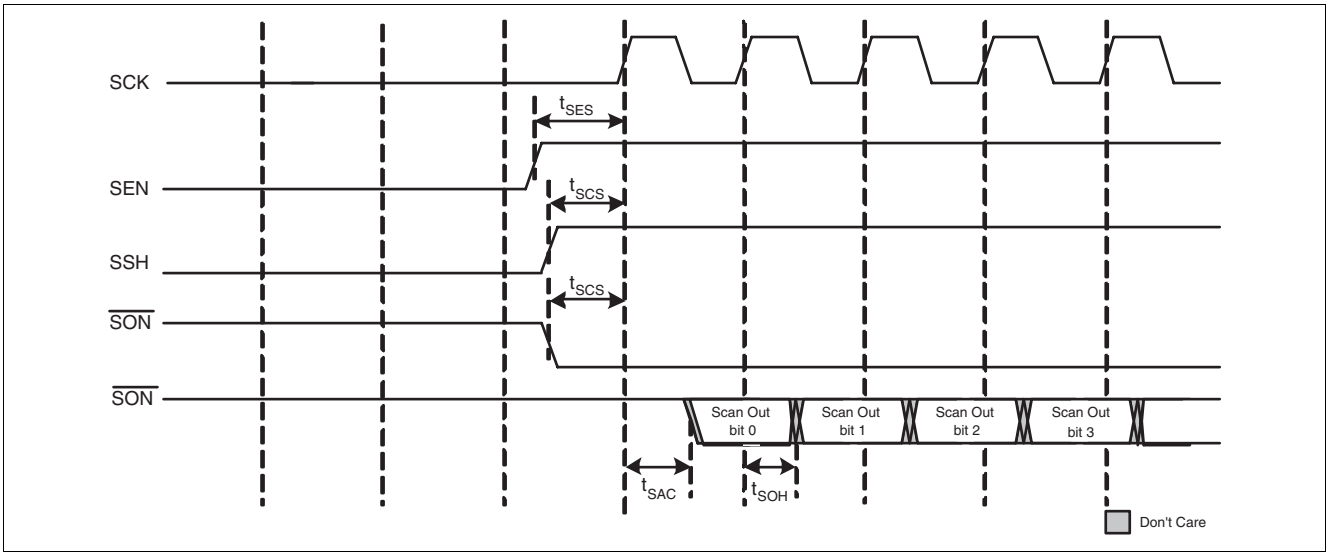

Figure 6 Scan Shift Timing

Table 12 Scan AC Electrical Characteristics

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Clock					
Clock cycle time	t_{SCK}	40	—	ns	1
Scan Command Time					
Scan enable setup time	t_{SES}	20	—	ns	1)2
Scan enable hold time	t_{SEH}	20	—	ns	1
Scan command setup time for SSH, $\overline{SOE}$ and SOUT	t_{SCS}	14	—	ns	1
$\overline{Scan\ command\ hold\ time\ for\ SSH, SOE\ and\ SOUT}$	t_{SCH}	14	—	ns	1
Scan Capture Time					
Scan capture setup time	t_{SDS}	10	—	ns	1
Scan capture hold time	t_{SDH}	10	—	ns	1

Table 12 Scan AC Electrical Characteristics

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Scan Shift Time					
Scan clock to valid scan output	t_{SAC}	—	—	ns	1
Scan clock to scan output hold	t_{SOH}	1.5	—	ns	1

Notes

1. *The parameter applies only when SEN is asserted.*
2. *Scan Enable should be issued earlier than other Scan Commands by 6 ns.*

3.3 Scan Initilization

The initilization sequence for the boundary scan functionality depends on the intended SGRAM operation mode. There are two modes to distinguish. The first mode is the Stand-Alone mode. In the Stand-Alone mode the SGRAM is supposed to support the Boundary Scan functionality only, the user does not intend to operate the DRAM in its ordinary functionality after or prior to the entering of the Boundary Scan functionality. The purpose of the Stand-Alone mode could be a connectivity test at the manufacturing site.

The second mode is the regular SGRAM functionality. With this common mode the boundary scan functionality can be enabled after the SGRAM has been initialized by the regular power-up and SGRAM initilization sequence. When the boundary scan functionality is left the regular SGRAM initialization sequence has to be re-iterated.

3.3.1 Scan initilization for Stand-Alone Mode

The SGRAM needs to follow the given sequence to support the boundary scan functionality in the Stand-Alone mode. There is no external clock for the whole sequence needed.

Sequence Flow:

1.) external Voltages (VDD/VDDQ/VREF) need to be stable for 200us, SEN has to be kept low

2.) bring SEN up to high state to enter boundary scan functionality

3.) operate boundary scan functionality according to the scan features given in **Chapter 3.2**

4.) boundary scan can be exited by bringing SEN low or simply by switching power off

The Scan initialization sequence for the Stand-Alone Mode is shown in Figure 7.

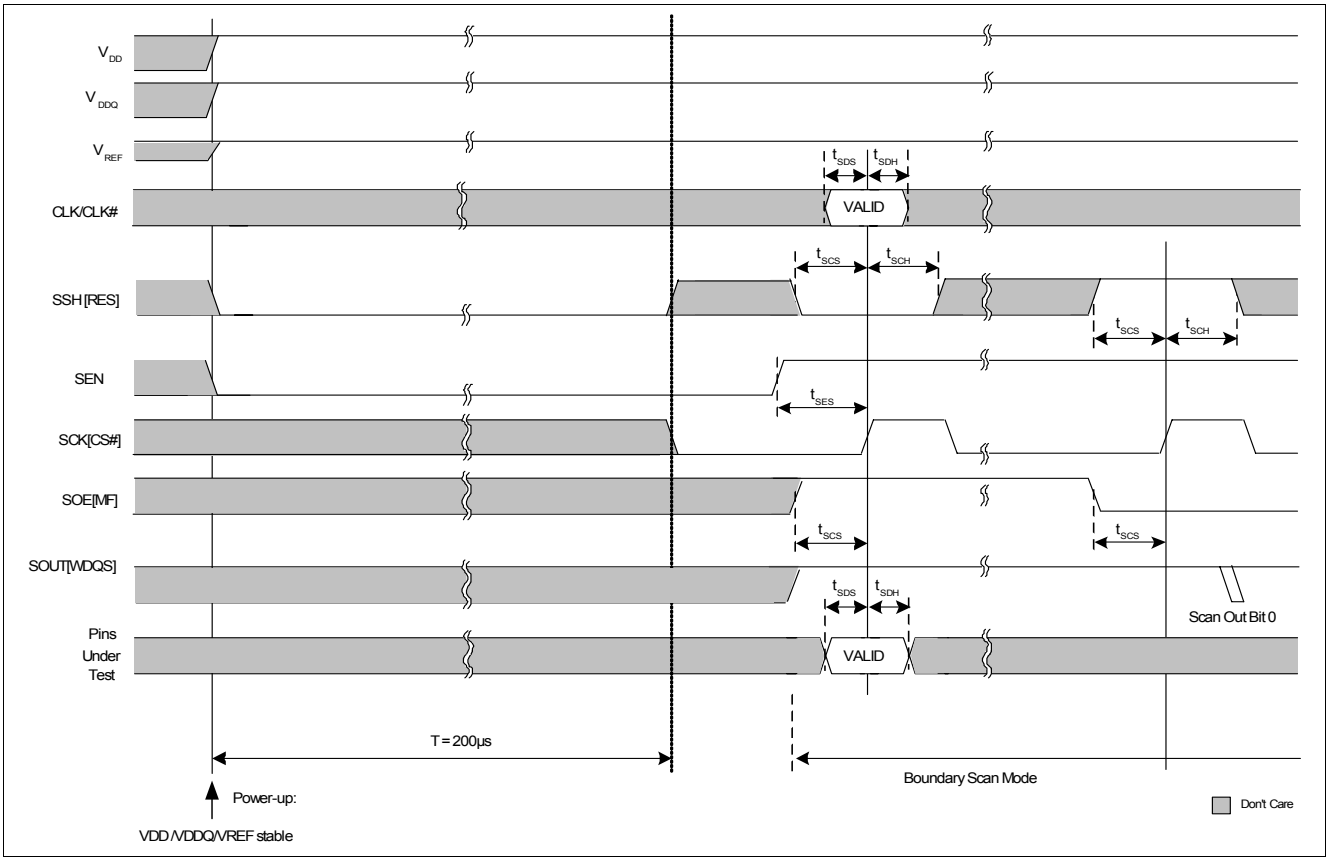

Figure 7 Scan Initialization for Stand-Alone mode

3.3.2 Scan initilization in regular SGRAM operation

The initilization sequence of the boundary scan functionality in regular SGRAM operation has to follow the given sequence.

Sequence Flow:

1.) external Voltages (VDD/VDDQ/VREF) need to be stable for 200us, RES has to be kept low, external clock has to be stable prior to RES goes high

2.) bring RES high and keep clock stable for 700tcks, CKE will be latched by rising RES edge, keep tATH/tATS

3.) bring SEN up to high state to enter boundary scan functionality

4.) operate boundary scan functionality accordingly to the scan features given in **Chapter 3.2**

5.) boundary scan can be exited by bringing SEN low

6.) wait t_{SN} for bringing up RES, prior to bringing RES to high state external has to be stable

7.) after RES is at high state wait 700tck

8.) continue with regular initilization sequence (PRE-ALL, EMRS, MRS)

The steps 1 and 2 are necessary to enable the termination for the command/address pins. They are part of the regular SGRAM initilization. They are required if the user wants to issue commands between to entering of the boundary scan functionality and the power-up sequence. The entering of the boundary scan mode is resetting the command/address termination values and all EMRS/MRS settings. Therefore they have to be initilized again after the boundary scan functionary has been left. **Figure 8** shows the scan initilization sequence for regular SGRAM operation.

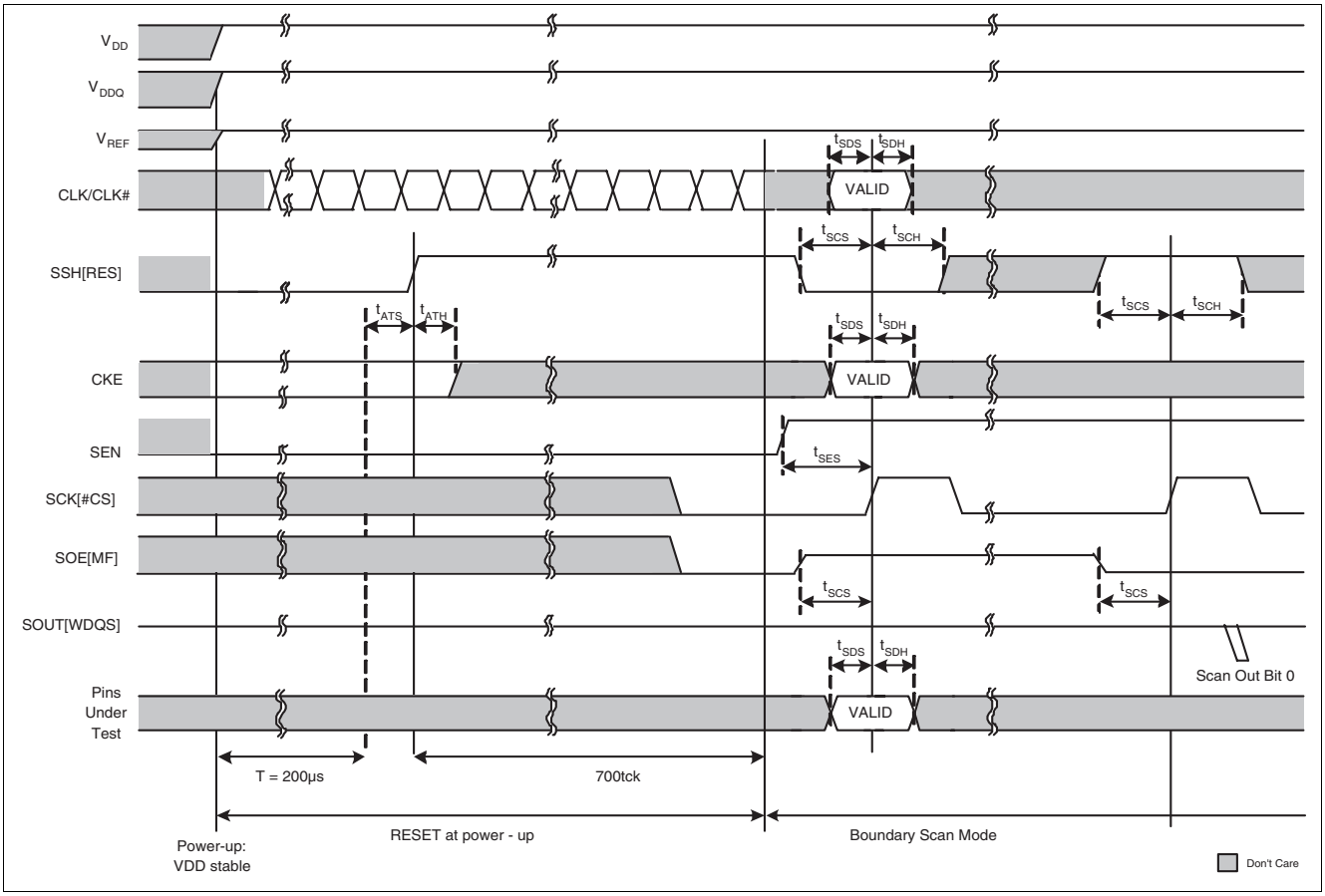

Figure 8 Scan Initialization Sequence within regular SGRAM Mode

3.3.3 Scan Exit Sequence

Figure 9 shows the Scan exit Sequence. This figure show the exiting of the boundary scan functionality in conjugation with the appended regular SGRAM initilization sequence to bring the SGRAM again in a well defined state.

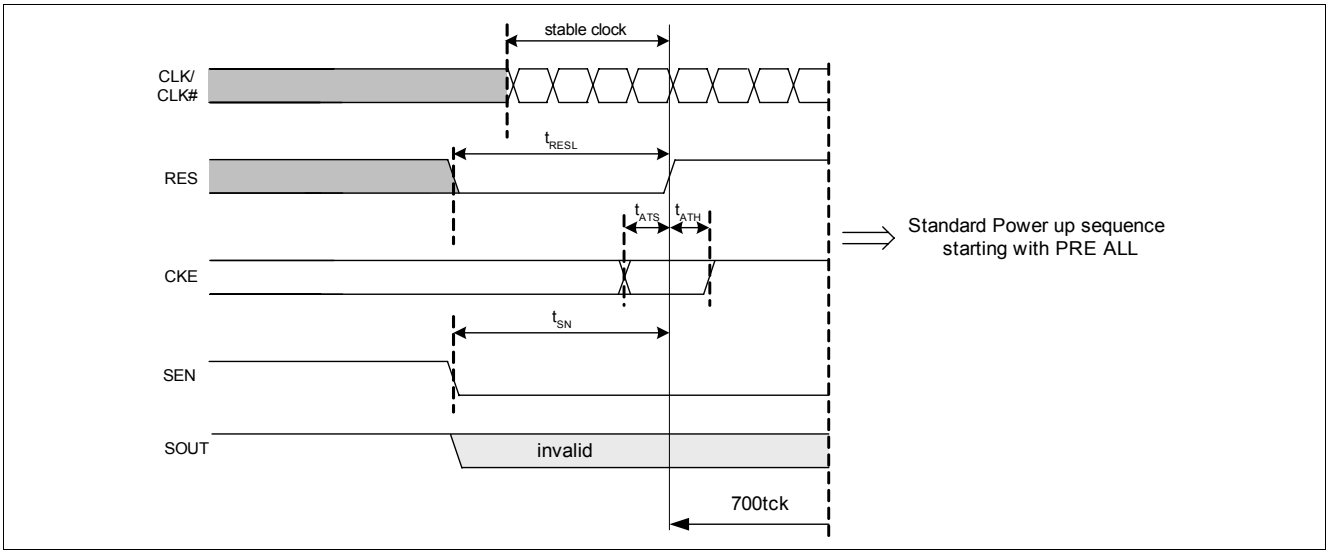

Figure 9 Boundary Scan Exit Sequence

Table 13 Scan AC Electrical Parameters

Parameter	CAS latency	Symbol	Limit Values		Unit	Notes
			min	max		
t_{RESL}		t_{RESL}	20	-	*ns*	
t_{SN}		t_{SN}	20	-	*ns*	

4 Functional Description

4.1 Initialization

The HYB18H512321AF must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation or permanent damage to the device.
The following sequence is highly recommended for Power-Up:

1. Apply power (V_{DD}, V_{DDA}, V_{DDQ}, V_{REF}). Apply V_{DD} before or at the same time as V_{DDQ}, apply V_{DDQ} before or at the same time as V_{REF}. Maintain RES=L and CS=H to ensure that all the DQ ouputs will be in HiZ state, all active terminations off and the DLL off. All other pins may be undefined.
2. Maintain stable conditions for 200 µs minimum for the to power up.
3. After clock is stable, set CKE to High or Low. After t_{ATS} minimum set RES to high. On the rising edge of RES, the CKE value is latched to determine the address and command bus termination value. If CKE is sampled LOW the address termination value is set to ZQ / 2. If CKE is sampled HIGH, the address and command bus termination is set to ZQ.
4. After tATH minimum, set CKE to high.
5. Wait a minimum of 700 cycles to calibrate and update the address and command termination impedances. Issue DESELECT on the command bus during these 700 cycles.
6. Apply a PRECHARGE ALL command, followed by an Extended Mode Register command after t_{RP} is met and activate the DLL.
7. Issue an Mode Register Set command after t_{MRD} is met to reset the DLL and define the operating parameters.
8. Wait 1000 cycles of clock input to lock the DLL. No Read command can be applied during this time. Since the impedance calibration is already completed, the DLL mimic circuitry can use the actual programmed driver impedance value.
9. Issue a PRECHARGE ALL command or issue 8 single bank PRECHARGE commands, one to each of the 8 banks to place the chip in an idle state.
10. Issue two or more AUTO REFRESH commands.

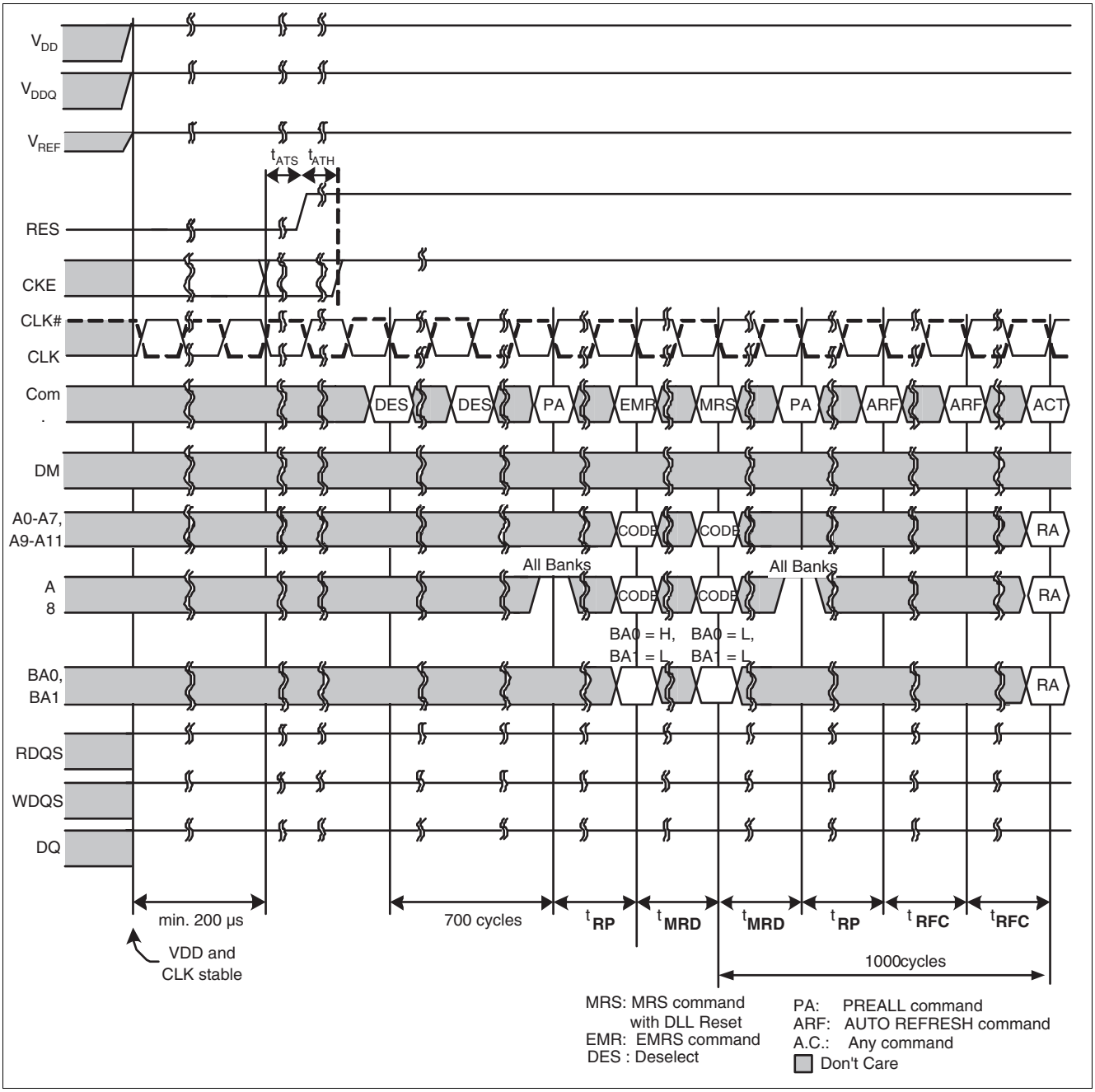

Figure 10 Power Up Sequence

4.2 Programmable impedance output drivers and active terminations

4.2.1 GDDR3 IO Driver and Termination

The is equipped with programmable impedance output buffers and active terminations. This allows the user to match the driver impedance to the system impedance.

To adjust the impedance of DQ<0:31> and RDQS<0:3> , an external precision resistor (ZQ) is connected between the ZQ pin and VSS. The value of the resistor must be six times the value of the desired impedance. For example, a 240 Ω resistor is required for an output impedance of 40 Ω. The range of ZQ is 210 Ω to 270 Ω, giving an output impedance range of 35 Ω to 45 Ω (one sixth the value of ZQ within 10%).

The value of ZQ is used to calibrate the internal DQ termination resistors of DQ<0:31>, WDQS<0:3> and DM<0:3>. The two termination values that are selectable using EMRS[3:2] are ZQ / 4 and ZQ / 2.

The value of ZQ is also used to calibrate the internal address command termination resistors. The inputs terminated in this manner are A<0:11>, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$. The two termination values that are selectable upon power up (CKE latched LOW to HIGH transition of RES) are ZQ/2 and ZQ.

RES, MF, CLK and $\overline{CLK}$ are not internally terminated.

If no resistance is connected to ZQ, an internal default value of 240 Ω will be used. In this case, no calibration will be performed.

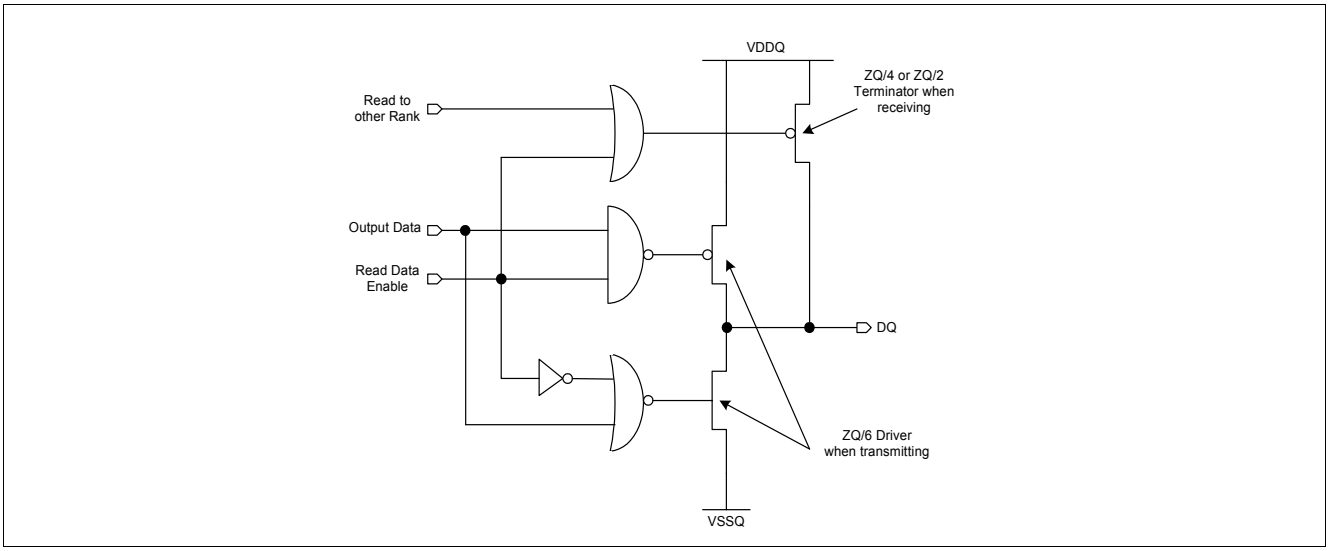

Figure 11 Output Driver simplified schematic

Table 14 Range of external resistance ZQ

Parameter	Symbol	min	nom	max	Units	Notes
External resistance value	ZQ	210	240	270	Ω	

Table 15 Termination Types and Activation

Ball	Termination type	Termination activation
CLK, $\overline{CLK}$, RDQS<0:3>, ZQ, RES, MF	No termination	
CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0 - BA2, A<0:11>	Add / CMDs	Always ON
DM<0:3>, WDQS<0:3>,	DQ	Always ON
DQ<0:31>	DQ	CMD bus snooping

4.2.2 Self Calibration for Driver and Termination

The ouput impedance is updated during all AREF commands. These updates are used to compensate for variations in supply voltage and temperature. Impedance updates do not affect device operation. No activity on the Address, command and data bus is allowed during a minimum Keep Out time t_{KO} after the Autorefresh command has been issued.

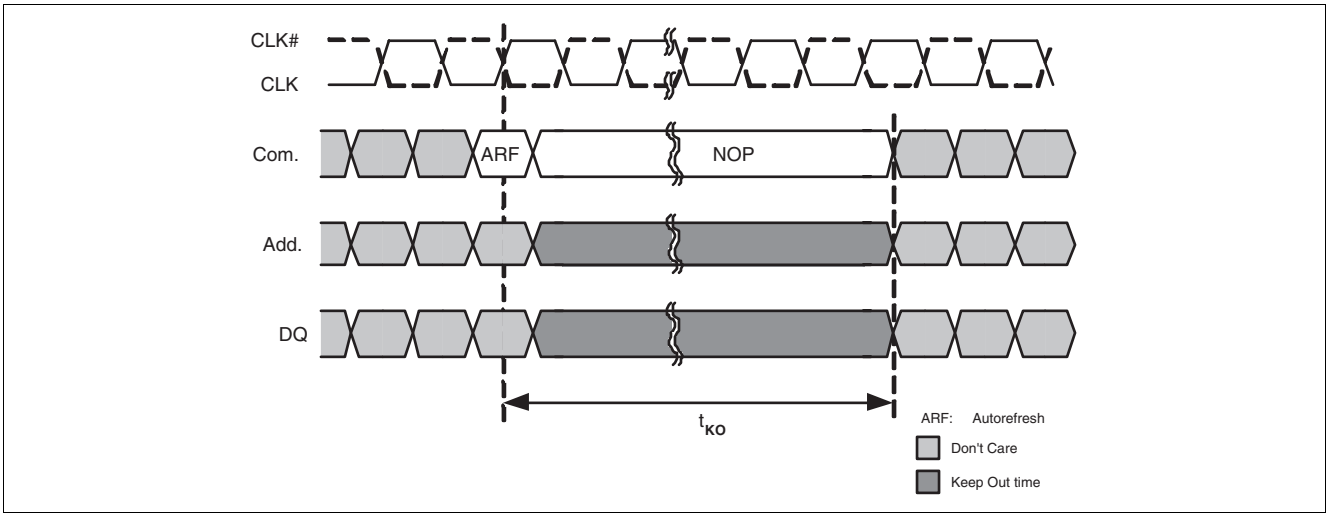

Figure 12 Termination update Keep Out time after Autorefresh command

To guarantee optimum driver impedance after power-up, the needs 700 cycles after the clock is applied and stable to calibrate the impedance upon power-up. The user can operate the part with fewer than 700 cycles, but optimal output impedance will not be guaranteed.

The GDDR3 Graphics RAM proceeds in the following manner for Self Calibration:

The PMOS device is calibrated against the external ZQ resistor value. First one PMOS leg is calibrated against ZQ. The number of legs used for the terminators (DQ and ADD/CMD) and the PMOS driver is represented in **Table 16**. Next, one NMOS leg is calibrated against the already calibrated PMOS leg. The NMOS driver uses 6 NMOS legs.

Table 16 Number of Legs used for Terminator and Driver Self Calibration

			Termination	Number of Legs	Notes
		CKE (at RES)			
Terminator	ADD / CMD	0	ZQ/2	2	
		1	ZQ	1	
		EMRS[3:2]			
	DQ	00	Disabled	0	1)
		10	ZQ/4	4	
		11	ZQ/2	2	
Driver	PMOS		ZQ/6	6	
	NMOS		ZQ/6	6	

1) EMRS[3:2] = 00 disables the ADD and CMD terminations as well.

Figure 13 represents a simplified schematic of the calibration circuits. First, the strength control bits are adjusted in such a way that the VDDQ voltage is divided equaly between the PMOS device and the ZQ resistor. The best bit pattern will cause the comparator to switch the PMOS Match signal output value. In a second step, the NFET is calibrated against the already calibrated PFET. In the same manner, the best control bit combination will cause the comparator to switch the NMOS Match signal output value.

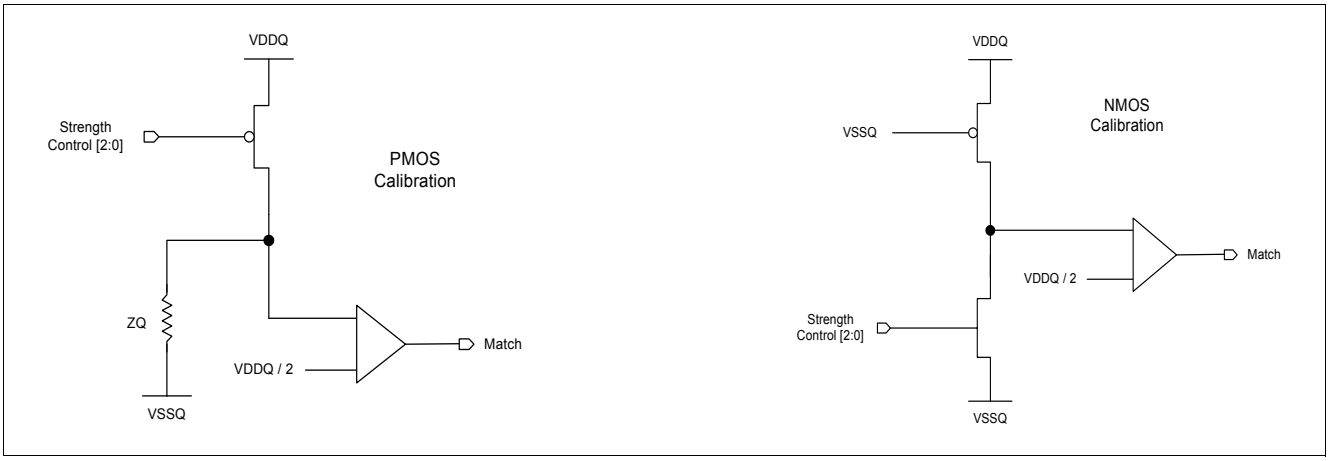

Figure 13 Self Calibration of PMOS and NMOS Legs

4.2.3 Dynamic Switching of DQ terminations

The GDDR3 Graphics RAM will disable its data terminators when a READ or DTERDIS command is detected. The terminators are disabled starting at CL - 1 Clocks after the READ / DTERDIS command is detected and the duration is 4 clocks. In a two rank system, both devices will snoop the bus for a READ / DTERDIS command to either device and both will disable their terminators if a READ / DTERDIS command is detected. The address and command terminators are always enabled.

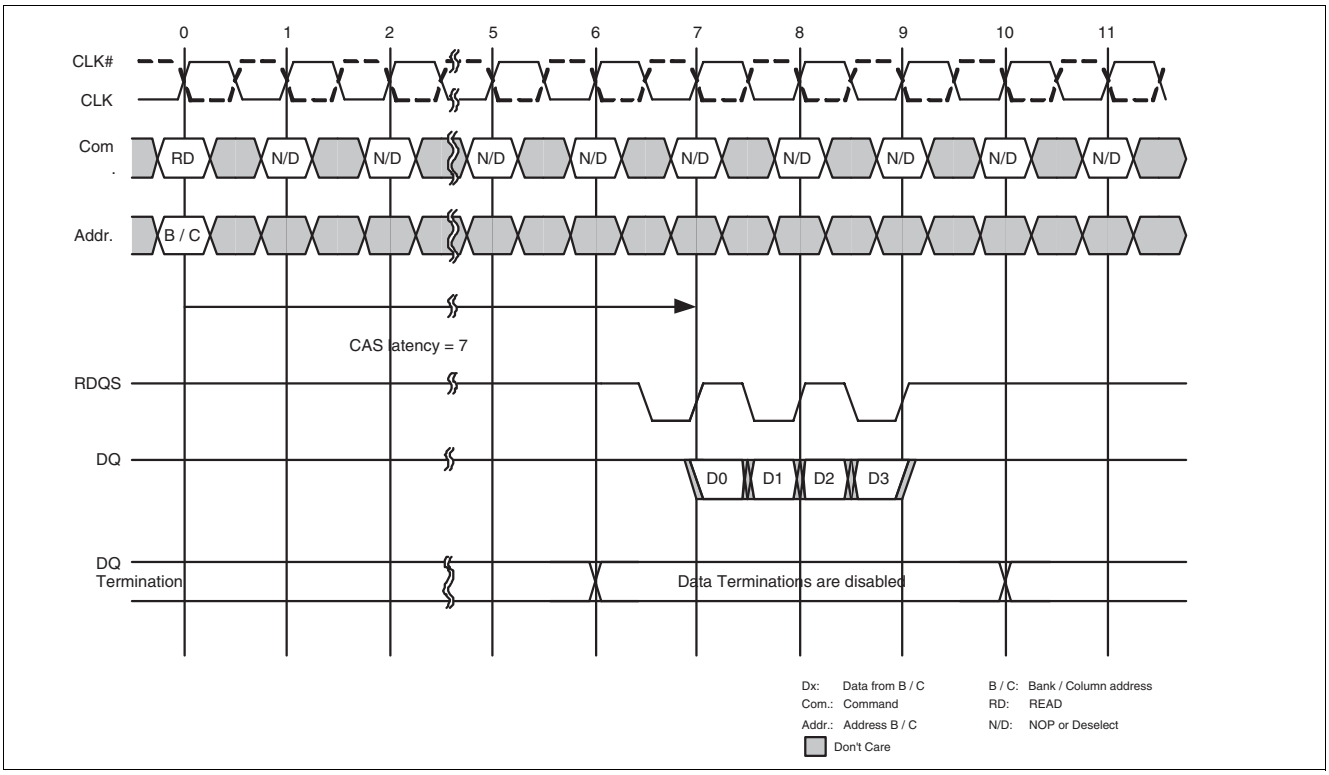

Figure 14 ODT Disable Timing during a READ command

4.2.4 Output impedance and Termination DC Electrical Characteristics

The Driver and Termination impedances are determined by applying $V_{DDQ/2}$ nominal at the corresponding input / output and by measuring the current flowing into or out of the device. V_{DDQ} is set to the nominal value.

I_{OH} is the current flowing out of DQ when the Pull-Up transistor is activated and the DQ termination disabled.

I_{O}Lis the current flowing into DQ when the Pull-Down transistor is activated and the DQ termination disabled.

$I_{TCAH(ZQ)}$ is the current flowing out of the Termination of Commands and Addresses for a ZQ termination value.

Table 17 DC Electrical Characteristics

Parameter		Nom.		Unit	Notes
	ZQ Value	**240**		Ω	
		min	**max**		
I_{OH}	ZQ/6	20.5	25.0	mA	1)
I_{OL}	ZQ/6	20.5	25.0	mA	1)
$I_{TCAH(ZQ)}$	ZQ	3.4	4.2	mA	1)

1) Measurement performed with V_{DDQ} (nominal) and by applying $V_{DDQ/2}$ at the corresponding Input / Output. 0 °C ≤ Tc ≤ 85

4.3 Extended Mode Register Set Command (EMRS)

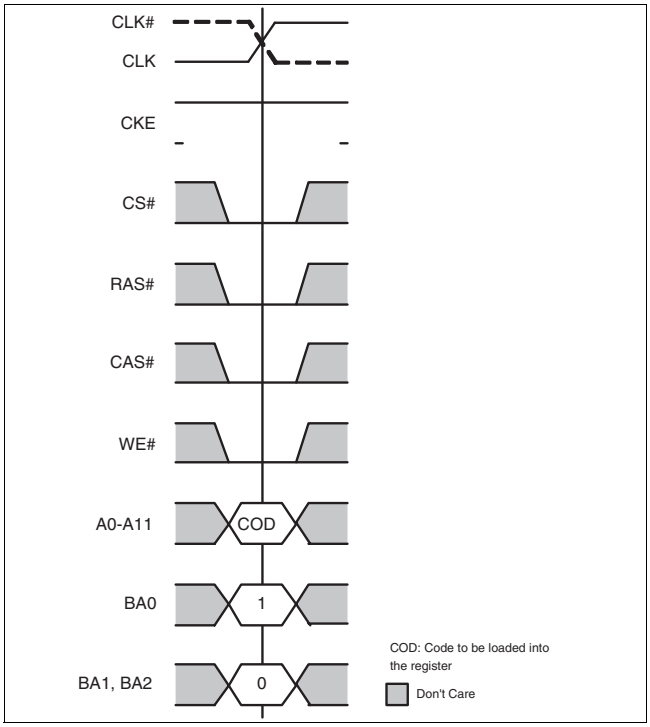

Figure 15 Extended Mode Register Set Command

The Extended Mode Register is used to set the output driver impedance value, the termination impedance value, the Write Recovery time value for Write with Autoprecharge. It is used as well to enable/disable the DLL, to issue the Vendor ID and to enable/disable the Low Power mode. There is no default value for the Extended Mode Register. Therefore it must be written after power up to operate the GDDR3 Graphics RAM. The Extended Mode Register can be programmed by performing a normal Mode Register Set operation and setting the BA0 bit to HIGH. All other bits of the EMR register are reserved and should be set to LOW.

The Extended Mode Register must be loaded when all banks are idle and no burst are in progress. The controller must wait the specified time t_{MRD} before initiating any subsequent operation (**Figure 16**).

The timing of the EMRS command operation is equivalent to the timing of the MRS command operation.

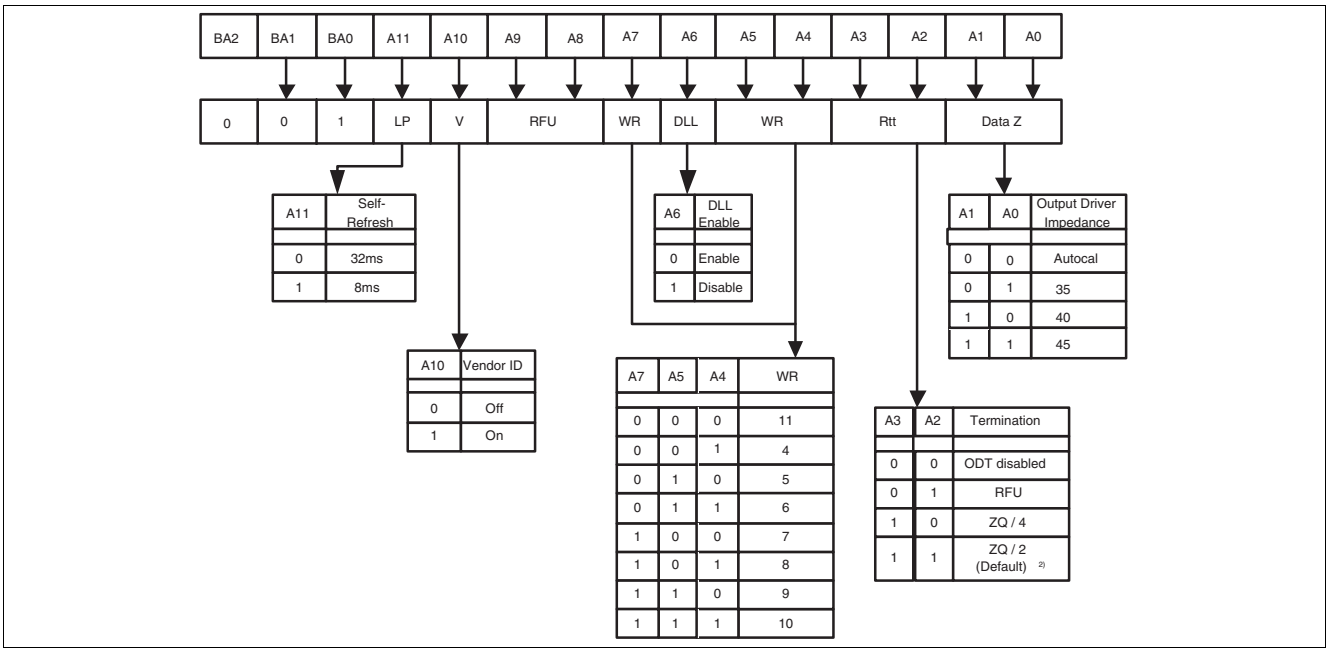

Figure 16 Extended Mode Register Bitmap

1. *These settings are for debugging purposes only.*
2. *Default termination values at Power Up.*
3. *The ODT disable function disables all terminators on the device.*
4. *If the user activates bits in the extended mode register in an optional field, either the optional field is activated (if option implemented in the device) or no action is taken by the device (if option not implemented).*
5. *WR (write recovery time for autoprecharge) in clock cycles is calculated by dividing t_{WR} (in ns) and rounding up to the next integer (WR[cycles] = t_{WR}[ns] / t_{CK}[ns]). The mode register must be programmed to this value.*

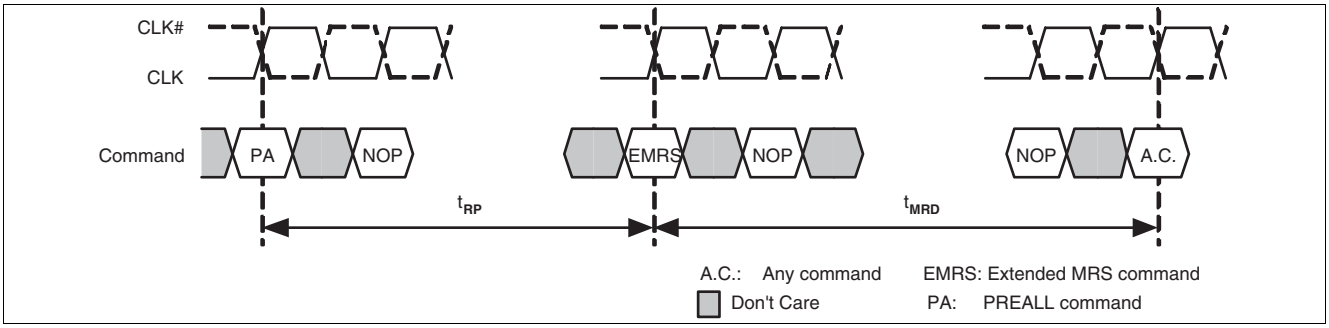

Figure 17 Extended Mode Register Set Timing

4.3.1 DLL enable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL. (When the device exits self-refresh mode, the DLL is enabled automatically). Anytime the DLL is enabled, 1000 cycles must occur before a READ command can be issued.

4.3.2 WR

The WR parameter is programmed using the register bits A4, A5 and A7. This integer parameter defines as a number of clock cycles the Write Recovery time in a Write with Autoprecharge operation.

The following inequality has to be complied with : WR * $t_{CK} \geq t_{WR}$, where t_{CK} is the clock cycle time.

4.3.3 Termination Rtt

The data termination, Rtt, is used to set the value of the internal termination resistors. The GDDR3 DRAM supports ZQ / 4 and ZQ / 2 termination values. The termination may also be disabled for testing and other purposes.

4.3.4 Output Driver Impedance

The Output Driver Impedance extended mode register is used to set the value of the data output driver impedance. When the autocalibration is used, the output driver impedance is set nominally to ZQ / 6.

4.3.5 Low Power

When the Low Power extended mode register is set, the device changes its internal self-refresh rate from 32 ms to 8 ms. This allows self-refresh operation at higher temperatures for mobile applications.

4.3.6 Vendor Code and Revision Identification

The Manufacturer Vendor Code is selected by issuing an Extended Mode Register Set command with bit A10 set to 1 and bits A0-A9 and A11 set to the desired value. When the Vendor Code function is enabled the GDDR3 DRAM will provide the Infineon vendor code on DQ[3:0] and the revision identification on DQ[7:4]. The code will be driven onto the DQ bus after tRIDon following the EMRS command that sets A10 to 1. The Vendor Code and Revision ID will be driven on DQ[7:0] until a new EMRS command is issued with A10 set back to 0. After tRDoff following the second EMRS command, the data bus is driven back to HIGH. This second EMRS command must be issued before initiating any subsequent operation. Violating this requirement will result in unspecified operation.

Table 18 Revision ID and Vendor Code

Revision Identification	Infineon Vendor Code
DQ[7:4]	DQ[3:0]
0000	0010

Note: Please refer to Revision Release Note for Revision ID value

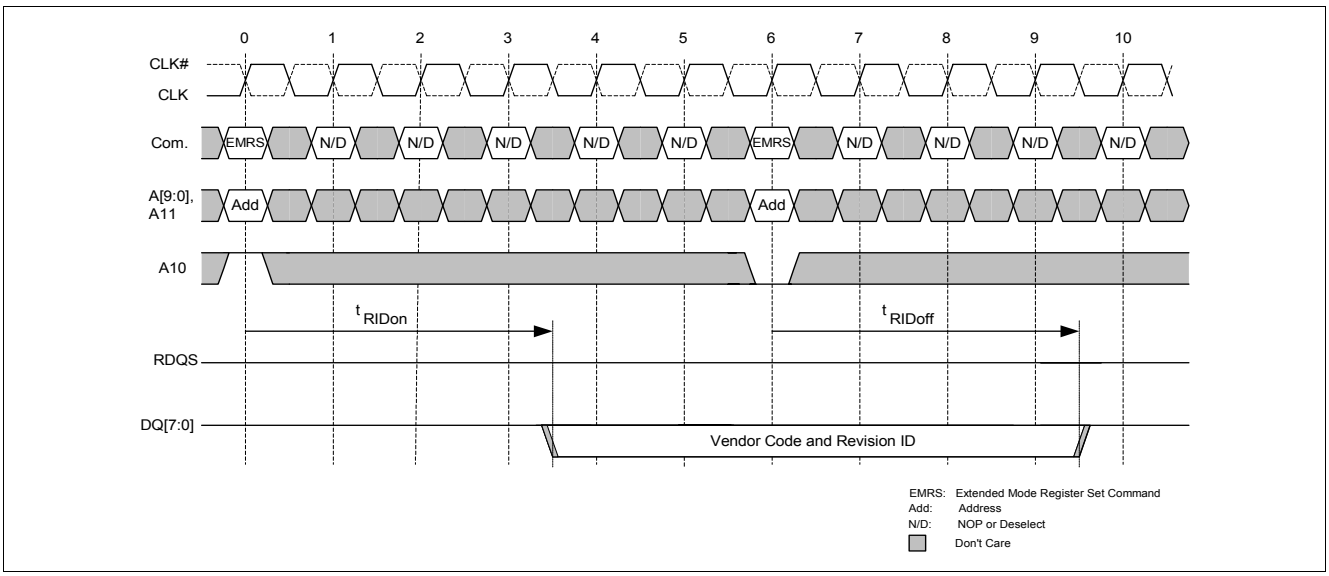

Figure 18 Timing of Vendor Code and Revision ID Generation on DQ[7:0]

4.4 Mode Register Set Command (MRS)

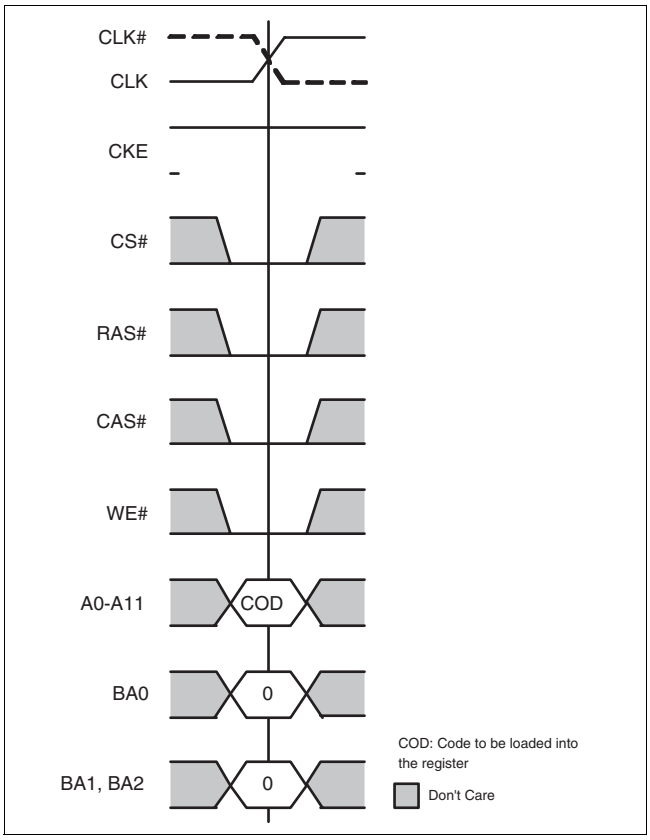

Figure 19 Mode Register Set Command

The mode register stores the data for controlling the operating modes of the memory. It programs CAS latency, test mode, DLL Reset and the value of the write latency. There is no default value for the mode register; therefore it must be written after power up to operate the . During a Mode Register Set command the address inputs are sampled and stored in the mode register.

t_{MRD} must be met before any command can be issued to the Graphics SDRAM. The Mode Register contents can only be set or changed when the Graphics SDRAM is in idle state.

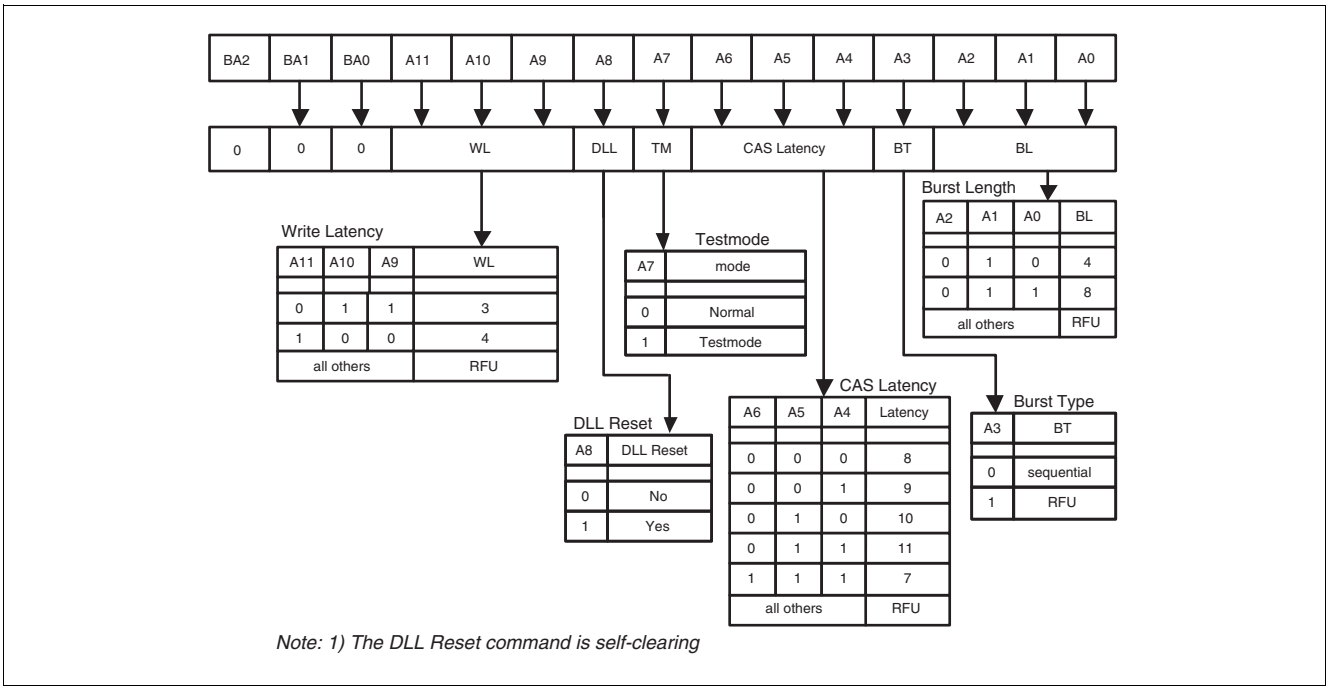

Figure 20 Mode Register Bitmap

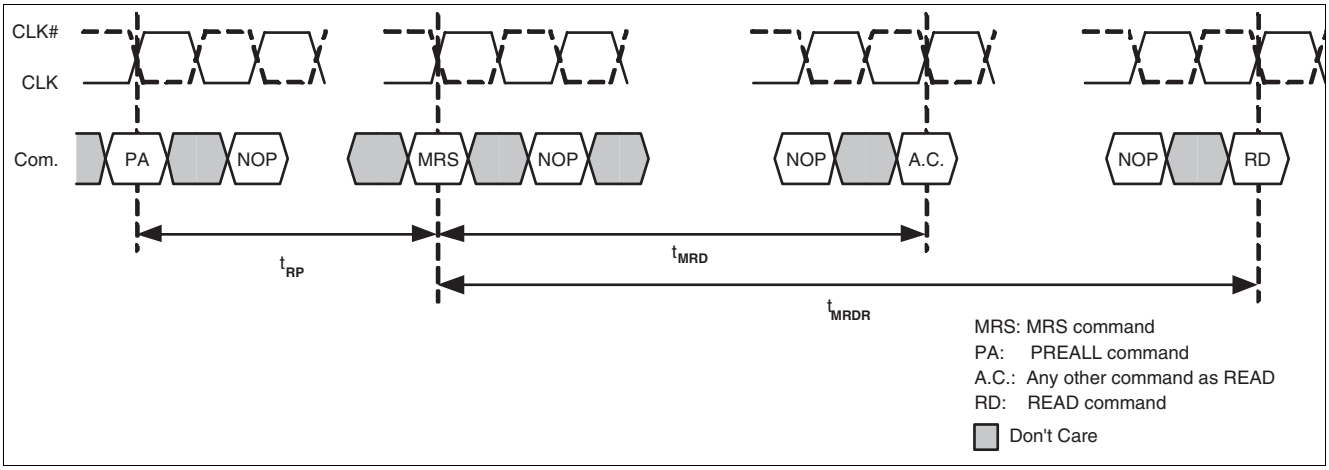

Figure 21 Mode Register Set Timing

4.4.1 Burst length

Read and Write accesses to the GDDR3 Graphics RAM are burst oriented with burst length of 4 and 8. This value must be programmed using the Mode Register Set command (A0 .. A2). The burst length determines the number of column locations that can be accessed for a given READ or WRITE command.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block if a boundary is reached. The starting location within this block is determined by the two least significant bits A0 and A1 which are set internally to the fixed value of zero each.

Reserved states should not be used, as unknow operation or incompatibility with future versions may result.

4.4.2 Burst type

Accesses within a given bank must be programmed to be sequential. This is done using the Mode Register Set command (A3) . This device does not support the burst interleave mode.

Table 19 Burst Definition

Burst Length	Starting Column Adress			Order of Accesses within a Burst (Type = sequential)
	A2	A1	A0	
4	—	X	X	0-1-2-3
8	0	X	X	0-1-2-3-4-5-6-7
	1	X	X	4-5-6-7-0-1-2-3

The value applied at the balls A0 and A1 for the column address is “Don’t care”

4.4.3 CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data as shown on **Figure 38**.

If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available nominally coincident with clock edge n+m.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

4.4.4 Write Latency

The WRITE latency, WL, is the delay, in clock cycles, between the registration of a WRITE command and the availability of the first bit of input data as shown in **Figure 28**.

4.4.5 Test mode

The normal operating mode is selected by issuing a Mode Register Set command with bit A7 set to zero and bits A0-A6 and A8-A11 set to the desired value.

4.4.6 DLL Reset

The normal operating mode is selected by issuing a Mode Register Set command with bit A8 set to zero and bits A0-A7 and A9-A11 set to the desired values. A DLL Reset is initiated by issuing a Mode Register Set command with bit A8 set to one and bits A0-A7 and A9-A11 set to the desired values. The GDDR3 Graphics RAM returns automatically in the normal mode of operations once the DLL reset is completed.

4.5 Bank / Row Activation (ACT)

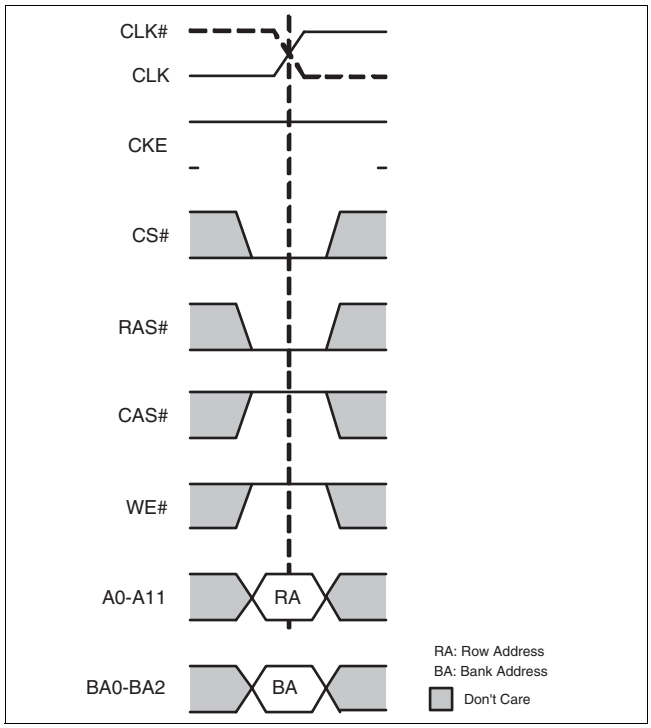

Figure 22 Activating a specific row

Before a READ or WRITE command can be issued to a bank, a row in that bank must be opened.

This is accomplished via the ACT command, which selects both the bank and the row to be activated.

After opening a row by issuing an ACT command, a READ or WRITE command may be issued after t_{RCD} to that row.

A subsequent ACT command to a different row in the same bank can only be issued after the previous active row has been closed (precharged). The minimum time interval between successive ACT commands to the same bank is defined by t_{RC}.

A subsequent ACT command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACT commands to different banks is defined by t_{RRD}.

There is a minimum time t_{RAS} between opening and closing a row.

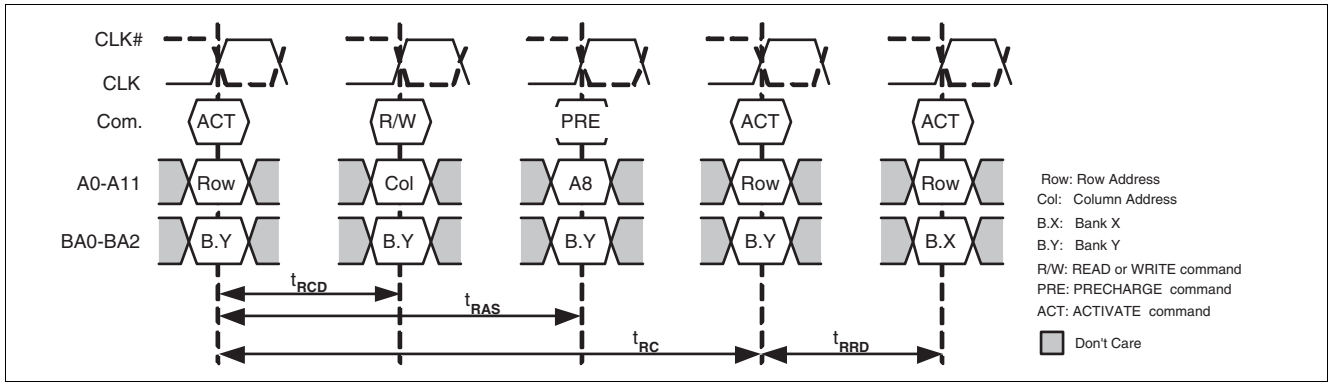

Figure 23 Bank Activating Timing

For eight bank GDDR3 devices, there may be a need to limit the number of activates in a rolling window to ensure that the instantaneous current supplying capability of the devices is not exceeded. To reflect the true capability of the DRAM instantaneous current supply, the parameter t_{FAW} (four activate window) is defined. No more than 4 banks may be activated in a rolling t_{FAW} window. Converting to clocks is done by dividing t_{FAW} (ns) by t_{CK} (ns) and rounding up the next integer value. As an example of the rolling window, if (t_{FAW} / t_{CK}) rounds up to 10 clocks, and an activate command is issued in clock n, no more than three further activate commands may be issued in clocks n+1 through n+9.

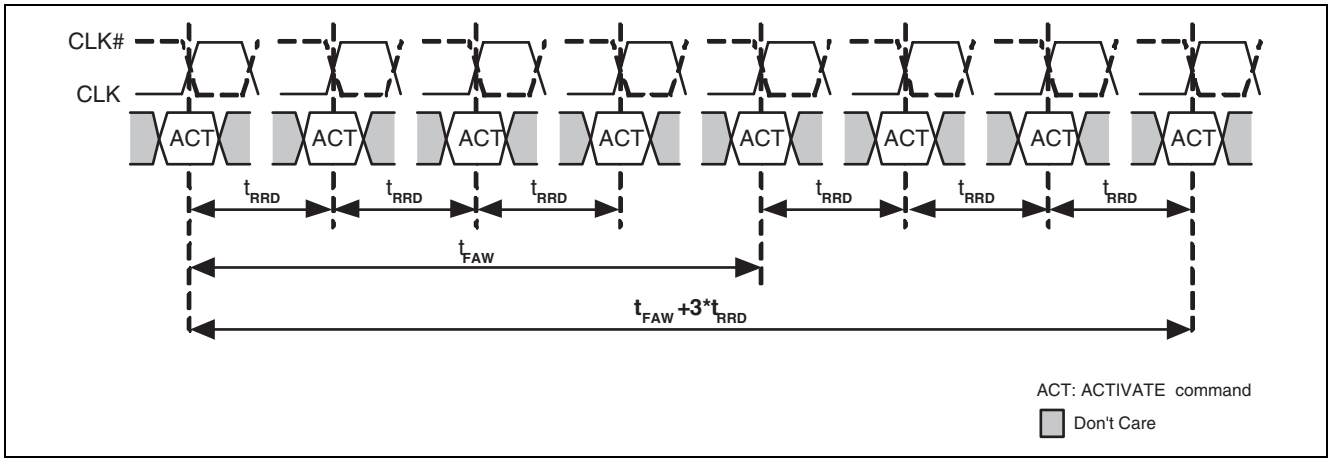

Figure 24 Four Window Active t_{FAW}

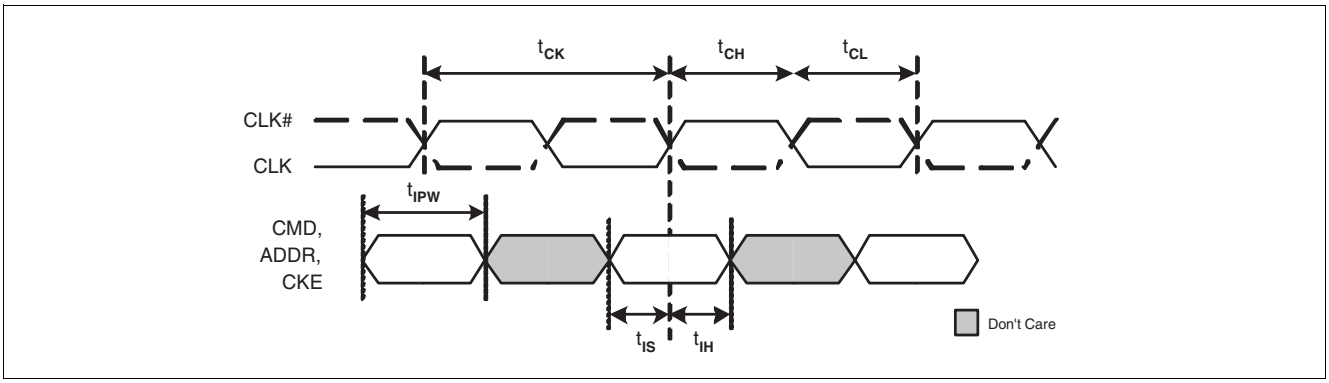

Figure 25 Clock, CKE and Command/Address Timings

Setup and Hold Timing for CKE is equal to CMD and ADDR Setup and Hold Timing.

4.6 Writes (WR)

4.6.1 Write - Basic Information

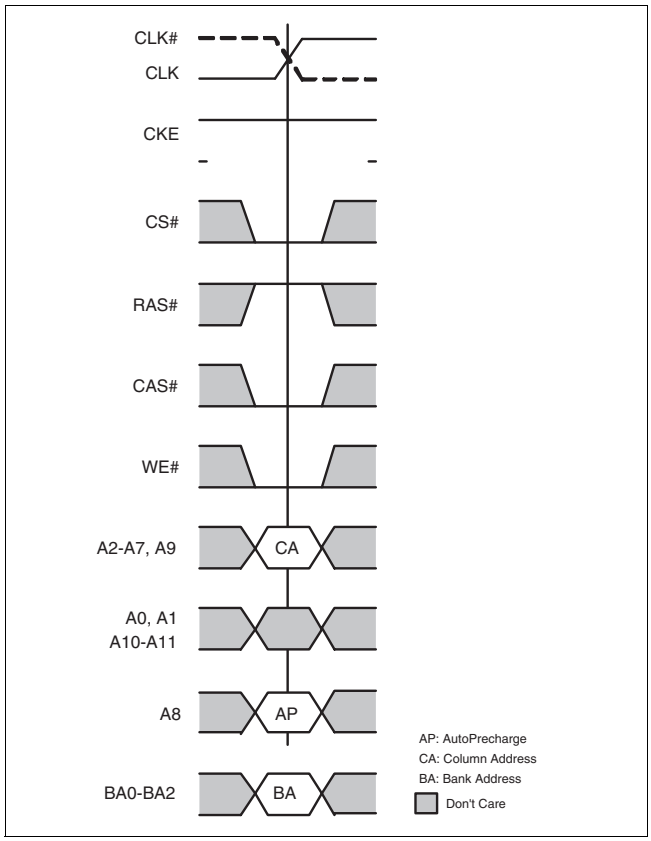

Figure 26 Write Command

Write bursts are initiated with a WR command, as shown in **Figure 26**. The column and bank addresses are provided with the WR command, and Auto Precharge is either enabled or disabled for that access. The length of the burst initiated with a WR command is four or eight depending on the mode register setting. There is no interruption of WR bursts. The two least significant address bits A0 and A1 are 'Don't Care'.

For WR commands with Autoprecharge the row being accessed is precharged $t_{WR/A}$ after the completion of the burst. If t_{RAS}(min) is violated the begin of the internal Autoprecharge will be performed one cycle after t_{RAS}(min) is met. WR, the write recovery time for write with Autoprecharge can be programmed in the Mode Register. Choosing high values for WR will prevent the chip to delay the internal Autoprecharge in order to meet t_{RAS}(min).

During WR bursts data will be registered with the edges of WDQS. The write latency can be programmed during Extended Mode Register Set. The first valid data is registered with the first valid rising edge of WDQS following the WR command. The externally provided WDQS must switch from HIGH to LOW at the beginning of the preamble. There is also a postamble requirement before the WDQS returns to HIGH. The WDQS signal can only transition when data is applied at the chip input and during pre- and postambles.

t_{DQSS} is the time between WR command and first valid rising edge of WDQS. Nominal case is when WDQS edges are aligned with edges of external CLK. Minimum and maximum values of t_{DQSS} define early and late WDQS operation. Any input data will be ignored before the first valid rising WDQS transition. t_{DQSL} and t_{DQSH} define the width of low and high phase of WDQS. The sum of t_{DQSL} and t_{DQSH} has to be t_{CK}.

Back to back WR commands are possible and produce a continuous flow of input data. There must be one NOP cycle between two back to back WR commands.

Any WR burst may be followed by a subsequent RD command. **Figure 32** shows the timing requirements for a WR followed by a RD. A WR may also be followed by a PRE command to the same bank. t_{WR} has to be met as shown in **Figure 35**.

Setup and hold time for incoming DQs and DMs relative to the WDQS edges are specified as t_{DS} and t_{DH}. DQ and DM input pulse width for each input is defined as t_{DIPW}. The input data is masked if the corresponding DM signal is high.

All timing parameters are defined with graphics DRAM terminations on.

Table 20 Mapping of WDQS and DM Signals

WDQS	Data mask signal	Controlled DQs
WDQS0	DM0	DQ0 - DQ7
WDQS1	DM1	DQ8 - DQ15
WDQS2	DM2	DQ16 - DQ23
WDQS3	DM3	DQ24 - DQ31

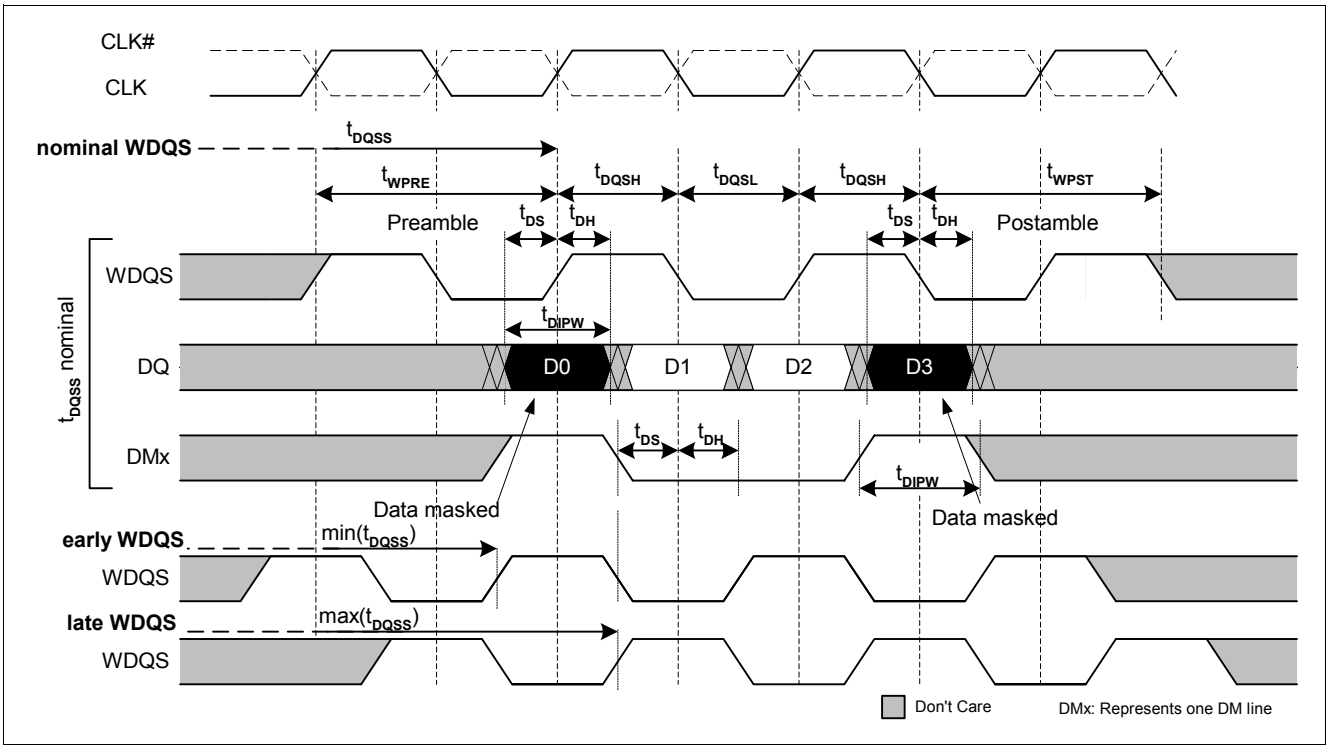

Figure 27 Basic Write Burst / DM Timing

Note: WDQS can only transition when data is applied at the chip input and during pre- and postambles.

4.6.2 Write - Basic Sequence

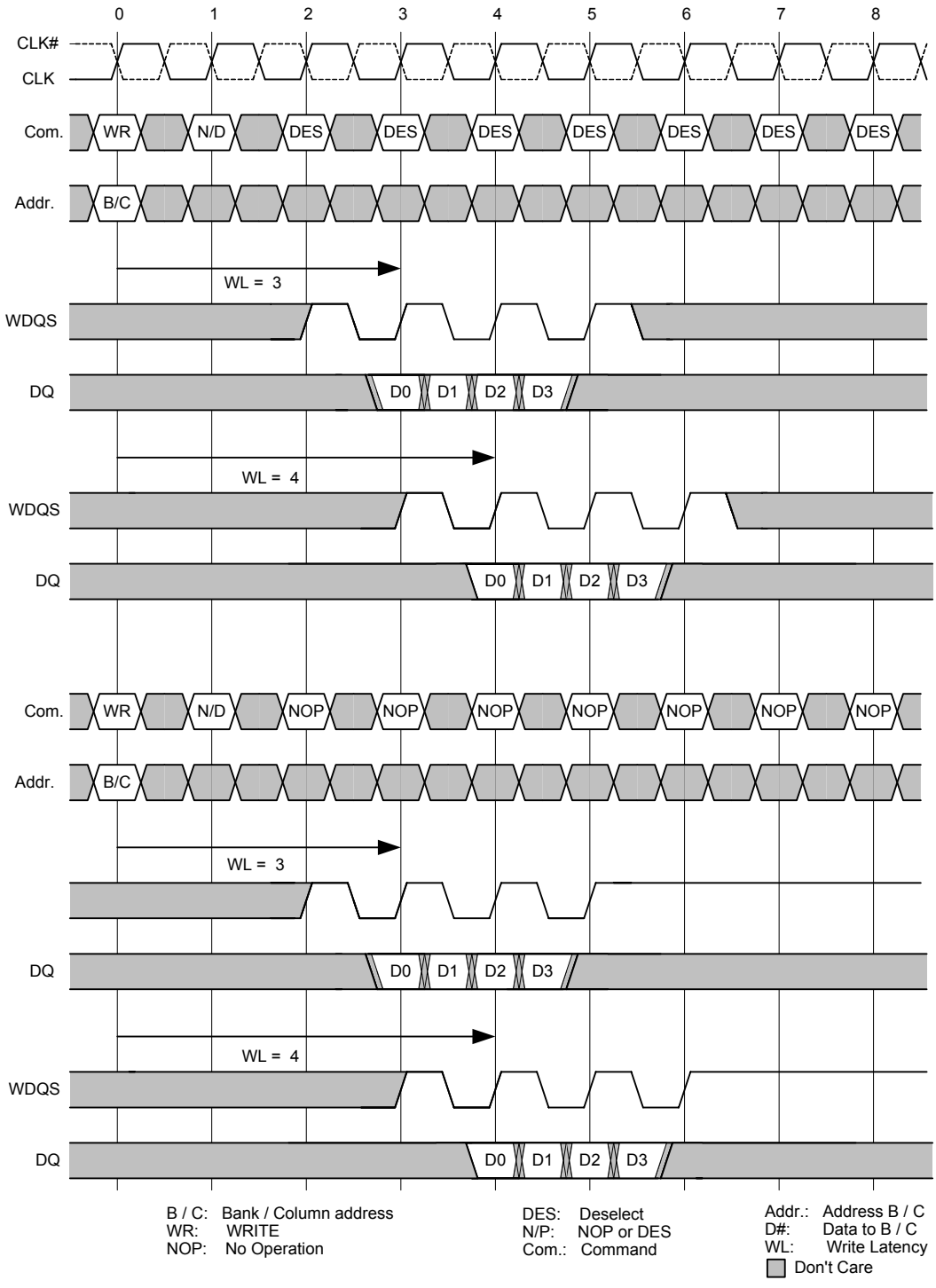

Figure 28 Write Basic Sequence

1. *Shown with nominal value of t_{DQSS}.*
2. *WDQS can only transition when data is applied at the chip input and during pre- and postambles.*
3. *When NOPs are applied on the command bus, the WDQS and the DQ busses remain stable High.*
4. *When DESs are applied on the command bus, the status of the WDQS and DQ busses is unknown.*

4.6.3 Write - Consecutive Bursts

4.6.3.1 Gapless Bursts

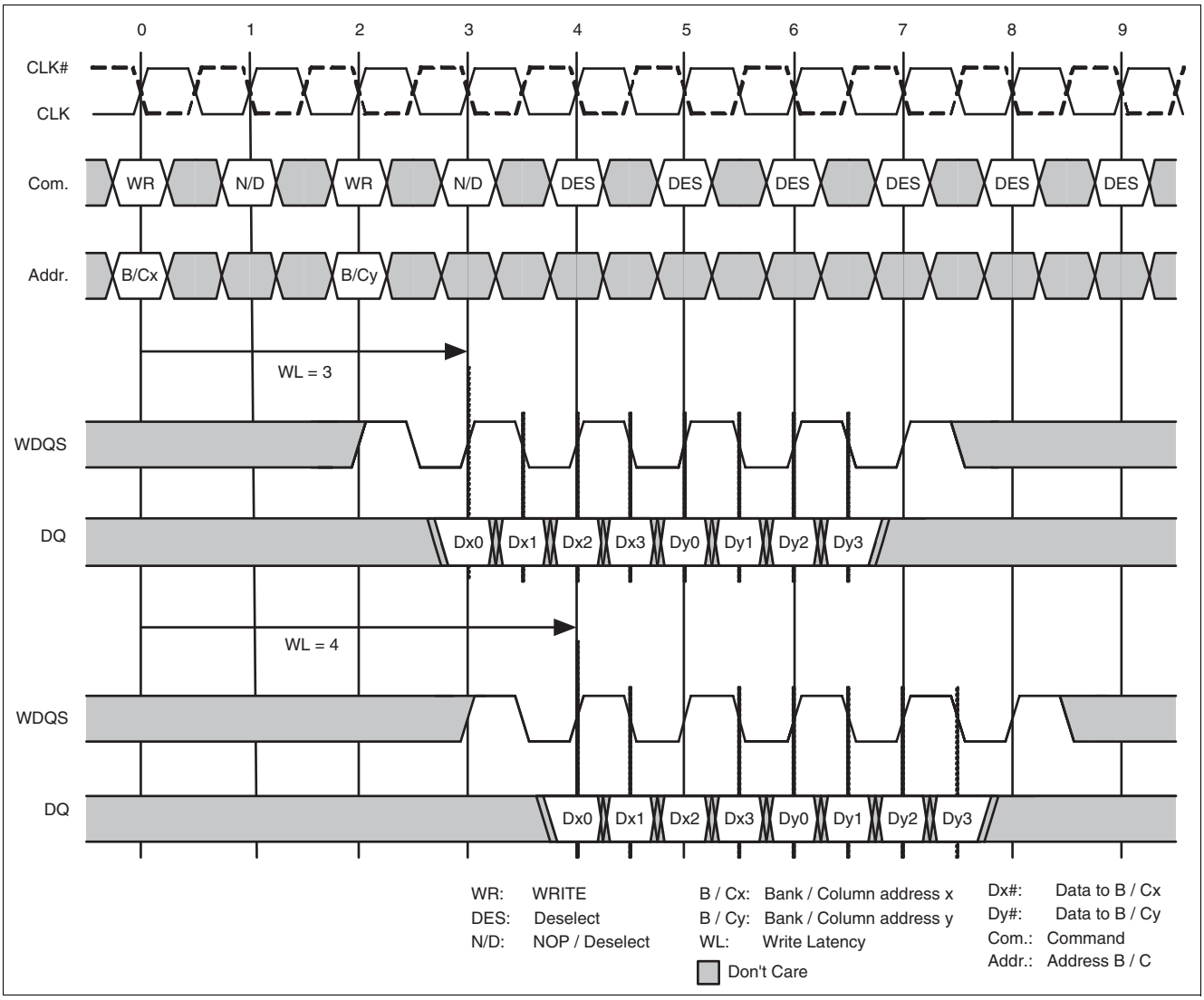

Figure 29 Gapless Write Bursts

1. *Shown with nominal value of t_{DQSS}.*
2. *The second WR command may be either for the same bank or another bank.*
3. *WDQS can only transition when data is applied at the chip input and during pre- and postambles.*

4.6.3.2 Bursts with Gaps

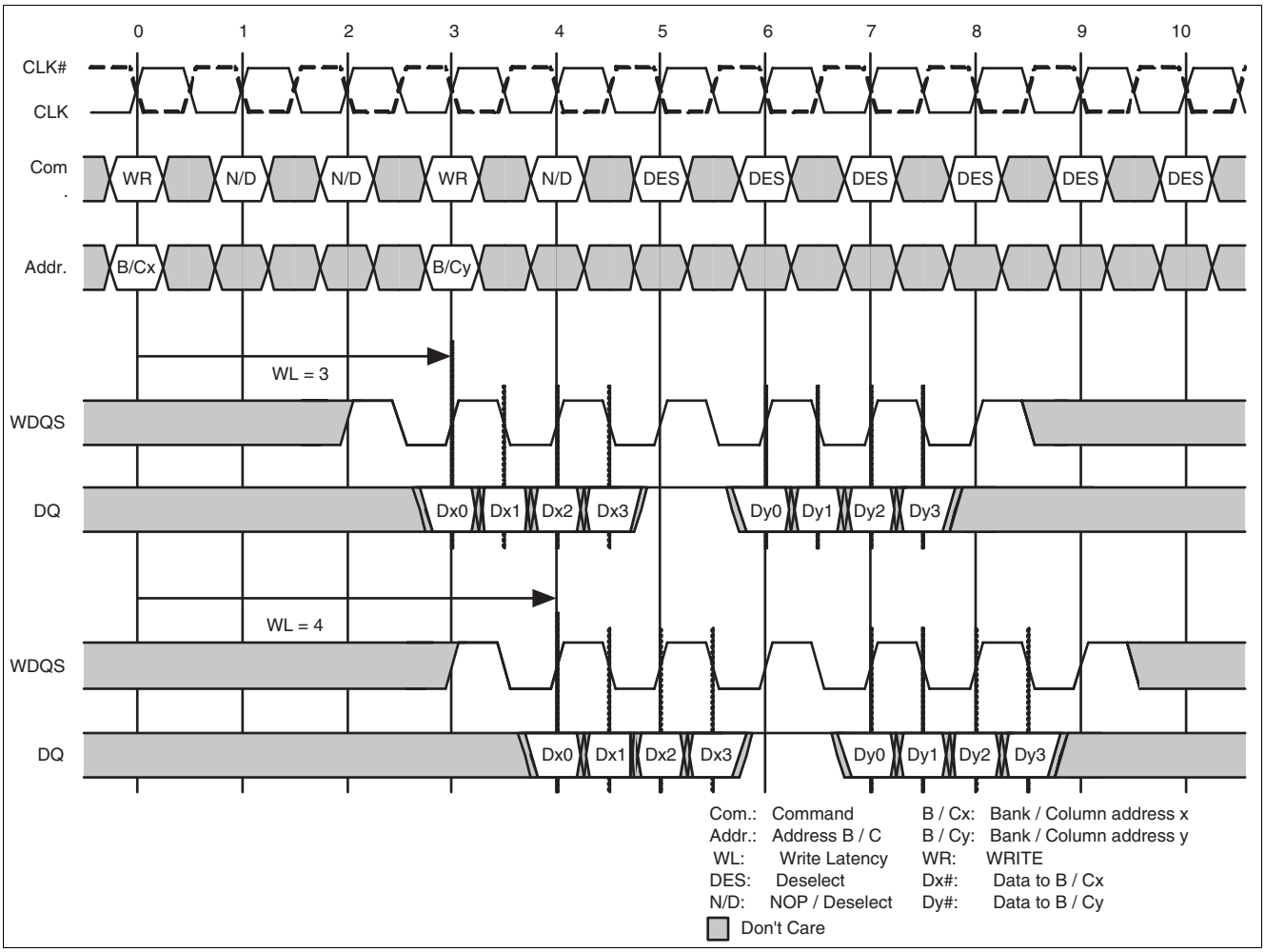

Figure 30 Consecutive Write Bursts with Gaps

1. *Shown with nominal value of t_{DQSS}.*
2. *The second WR command may be either for the same bank or another bank.*
3. *WDQS can only transition when data is applied at the chip input and during pre- and postambles.*

4.6.4 Write with Autoprecharge

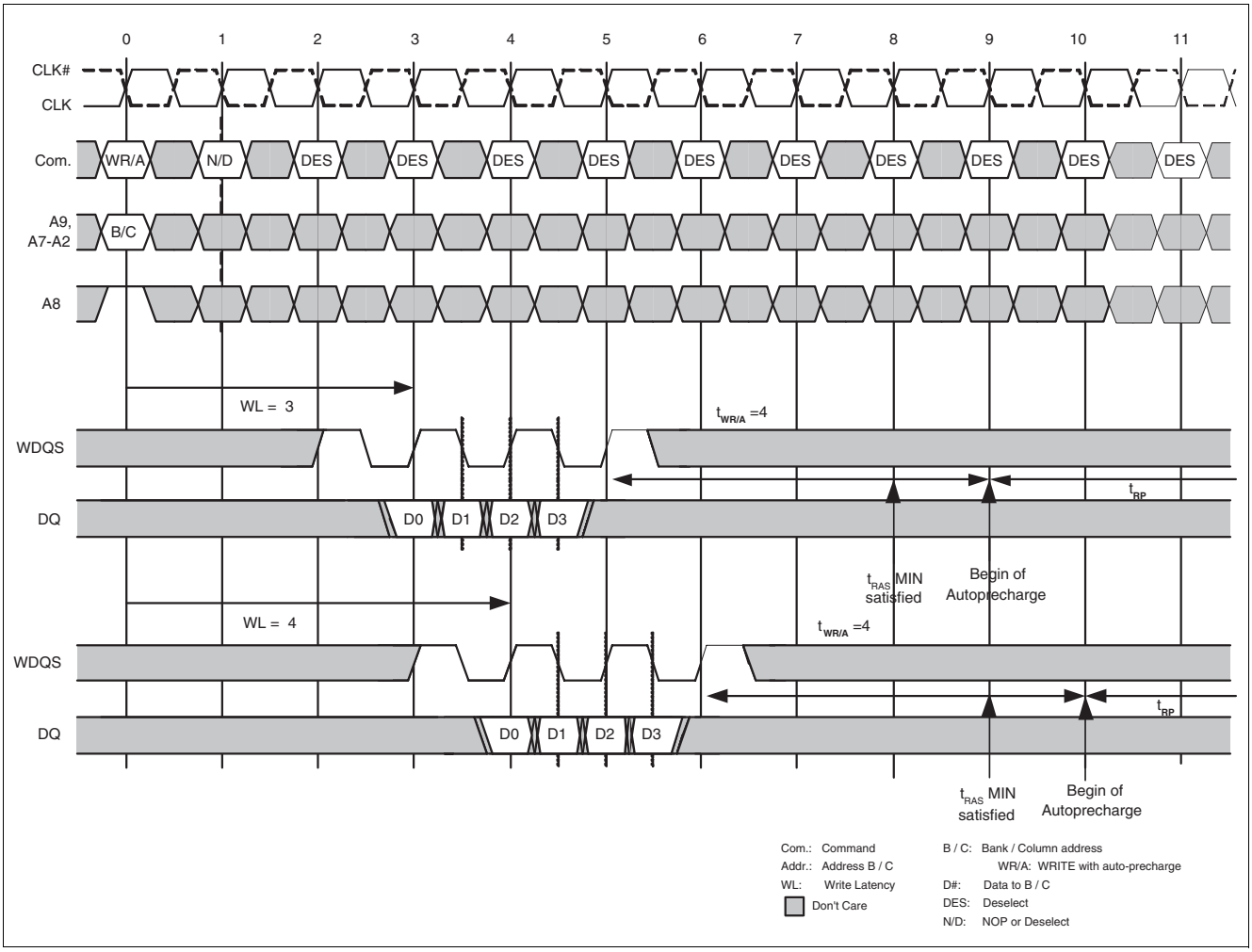

Figure 31 Write with Autoprecharge

1. *Shown with nominal value of t_{DQSS}.*
2. *$t_{WR/A}$ starts at the first rising edge of CLK after the last valid edge of WDQS.*
3. *t_{RP} starts after $t_{WR/A}$ has been expired.*
4. *When issuing a WR/A command please consider that the t_{RAS} requirement also must be met at the beginning of t_{RP}.*
5. *$t_{WR/A} * t_{CYC} \geq t_{WR}$.*
6. *WDQS can only transition when data is applied at the chip input and during pre- and postambles.*

4.6.5 Write followed by Read

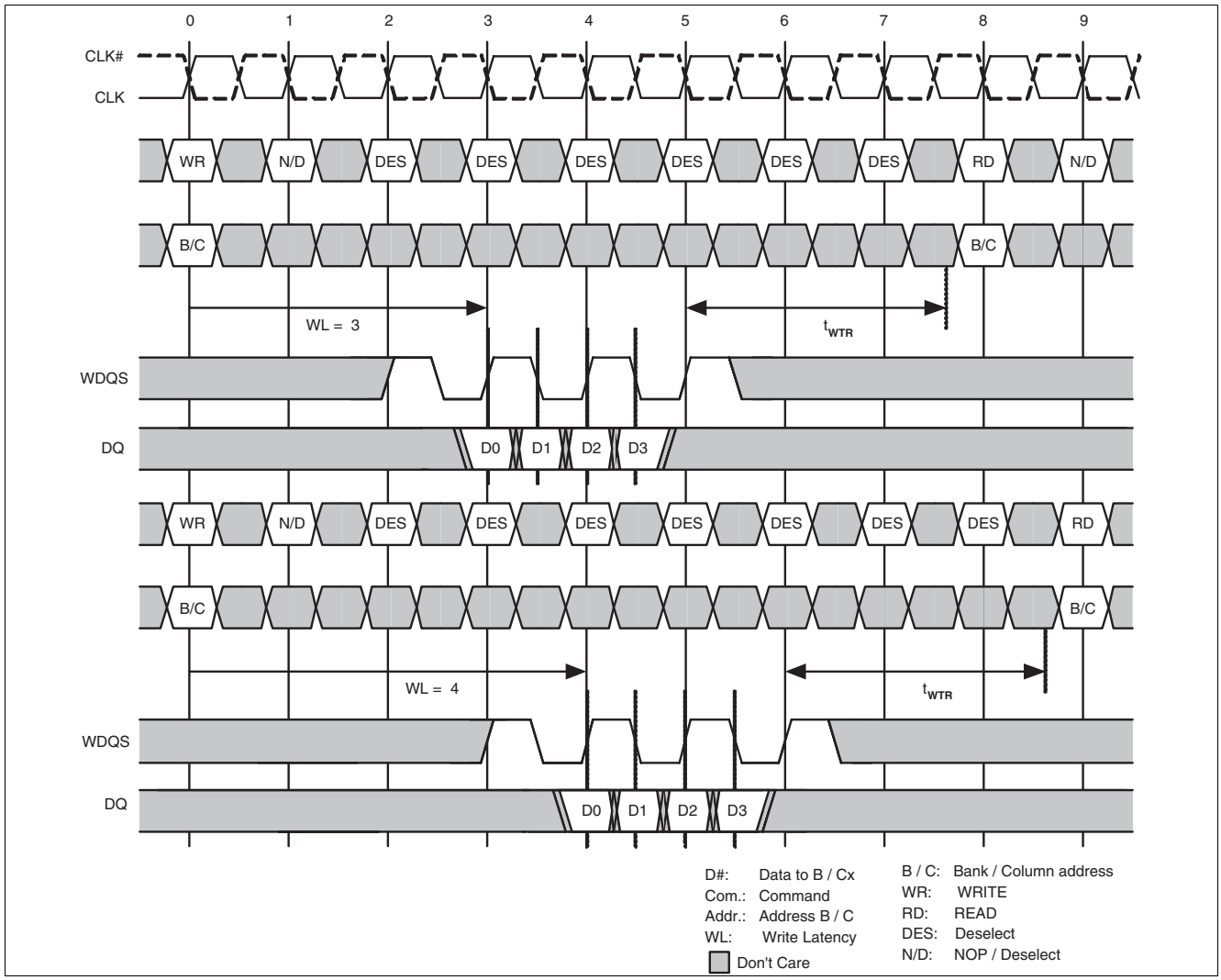

Figure 32 Write followed by Read

1. *Shown with nominal value of t_{DQSS}.*
2. *The RD command may be either for the same bank or another bank.*
3. *WDQS can only transition when data is applied at the chip input and during pre- and postambles.*

4.6.6 Write followed by DTERDIS

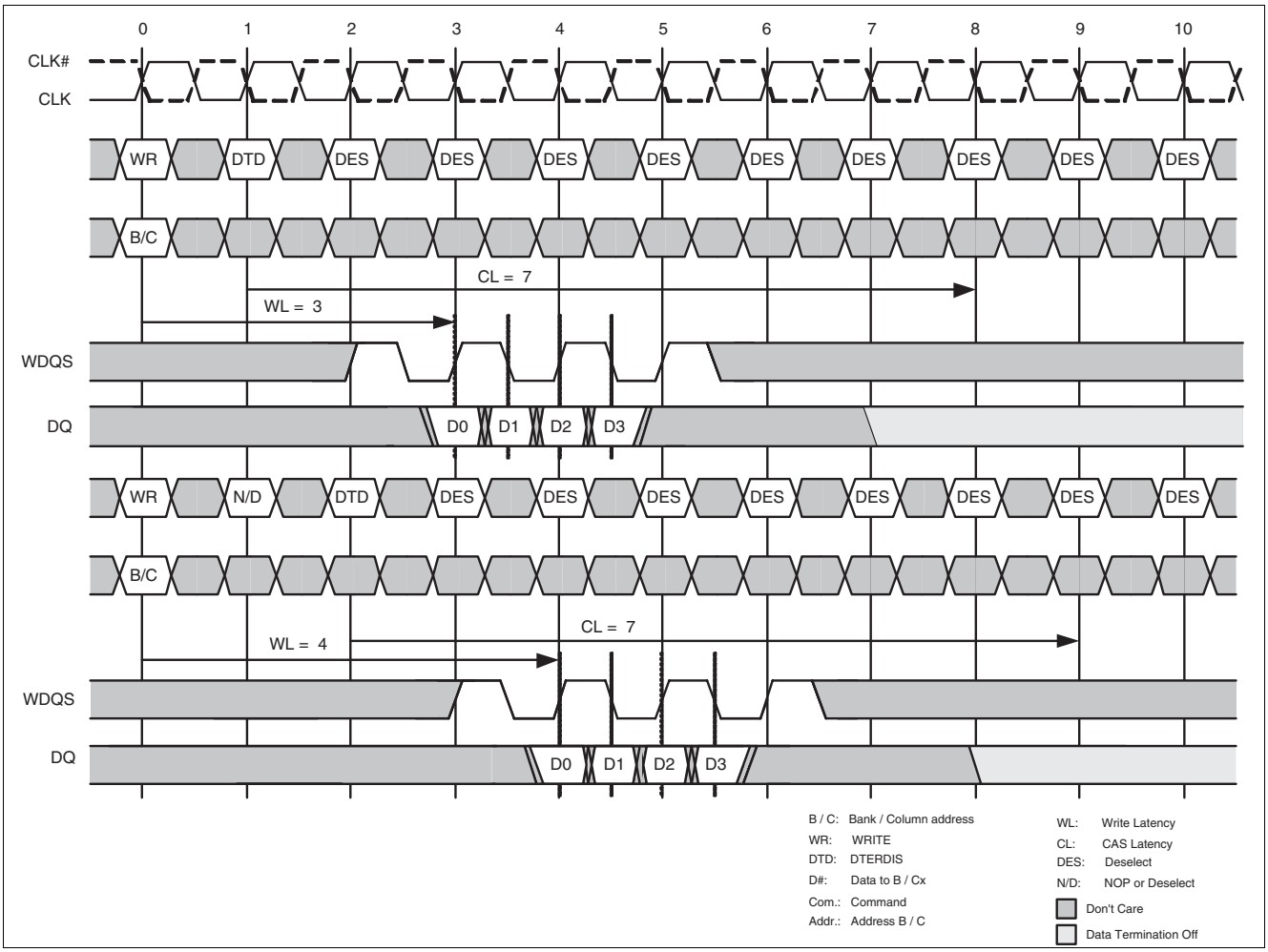

Figure 33 Write Command followed by DTERDIS

1. *Shown with nominal value of t_{DQSS}.*
2. *WDQS can only transition when data is applied at the chip input and during pre- and postambles.*
3. *A margin of one clock has been introduced in order to make sure that the data termination are still on when the last Write data reaches the memory.*
4. *The minimum distance between Write and DTERDIS is one clock.*

4.6.7 Write with Autoprecharge followed by Read / Read with Autoprecharge

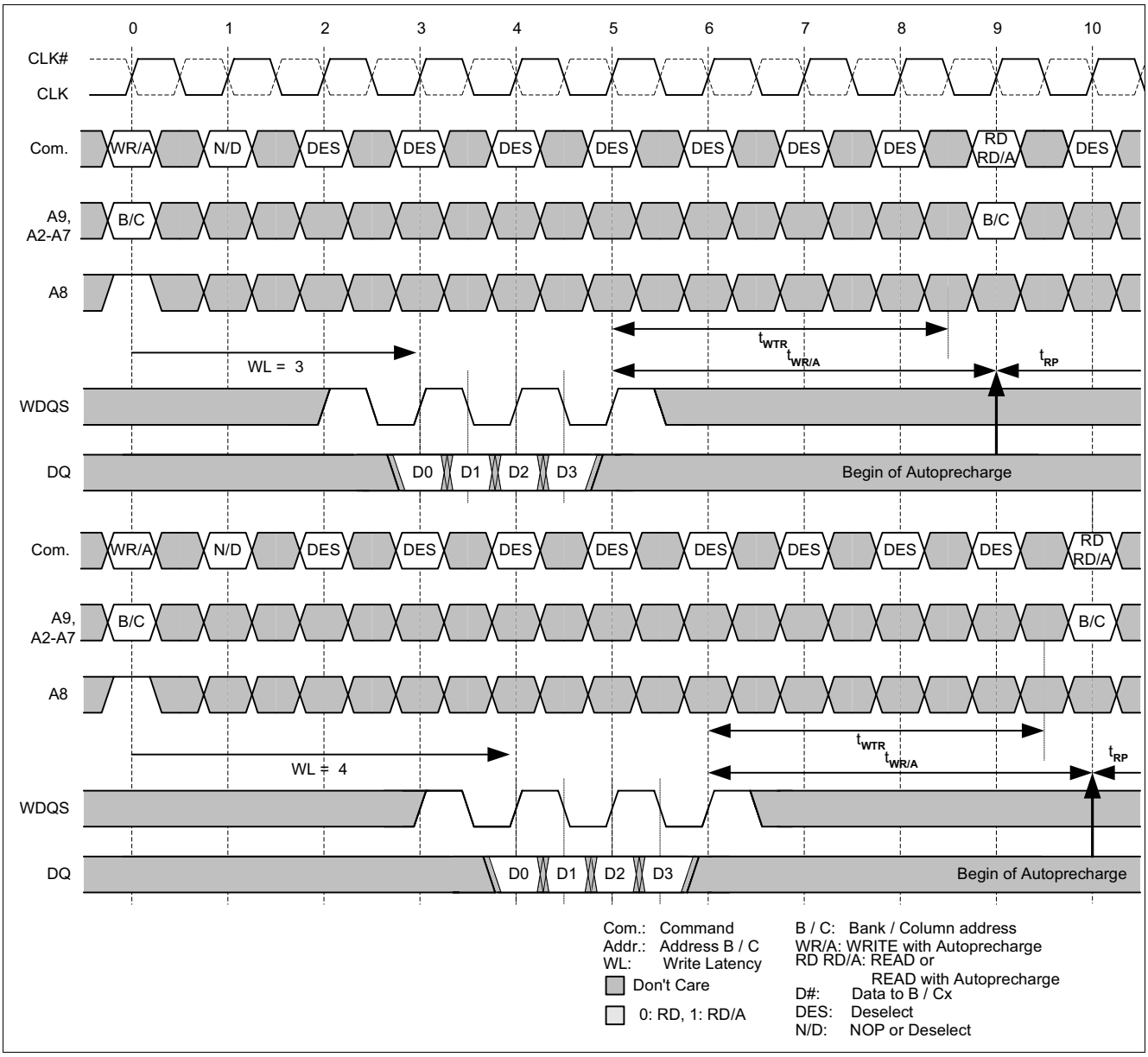

Figure 34 Write with Autoprecharge followed by Read or Read with Autoprecharge on another bank.

1. *Shown with nominal value of t_{DQSS}.*
2. *The RD command is only allowed for another activated bank.*
3. *$t_{WR/A}$ is set to 4 in this example.*
4. *WDQS can only transition when data is applied at the chip input and during pre- and postambles.*

4.6.8 Write followed by Precharge on same bank.

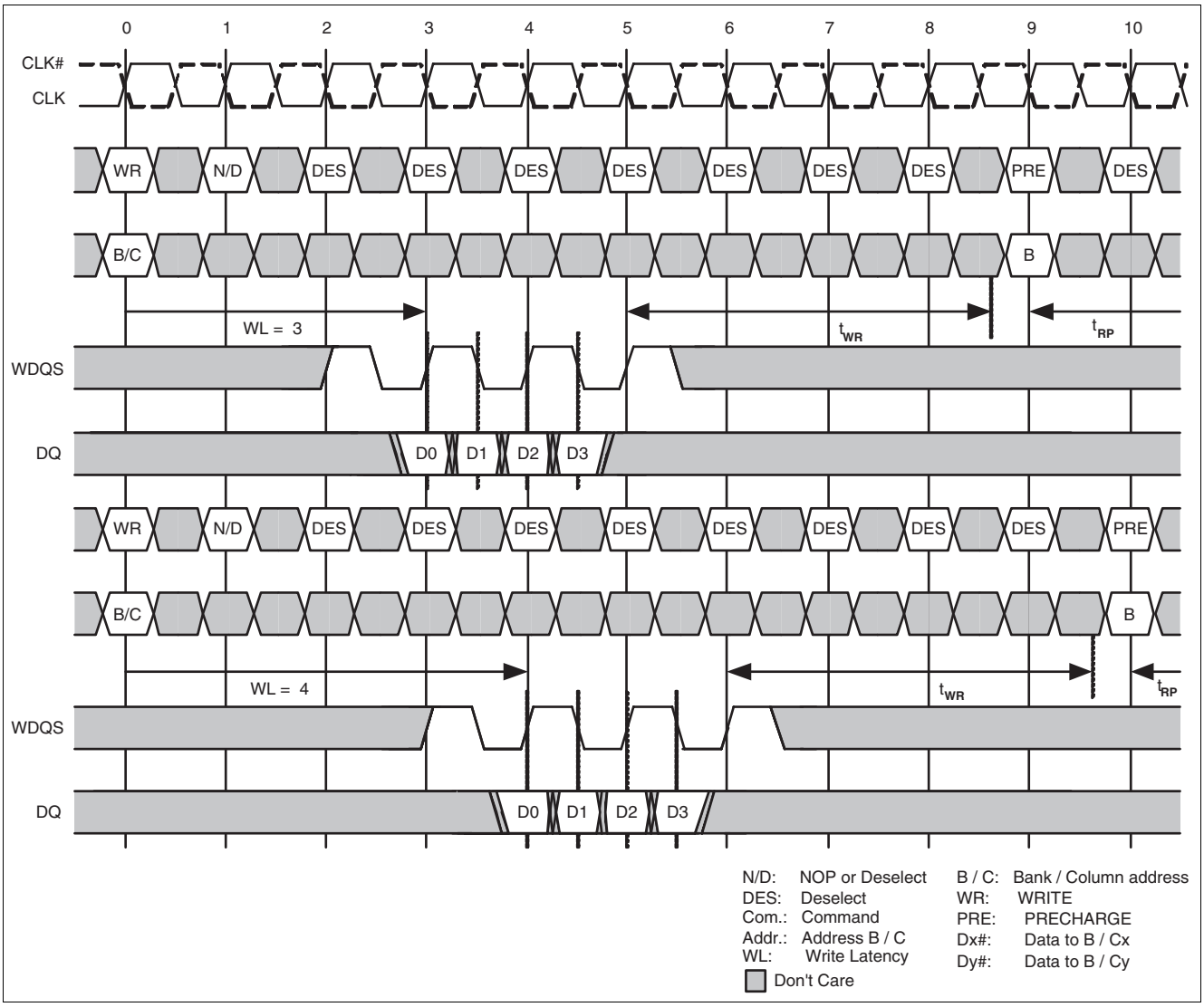

Figure 35 Write followed by Precharge on same Bank

1. *Shown with nominal value of t_{DQSS}.*
2. *WR and PRE commands are to same bank.*
3. *t_{RAS} requirement must also be met before issuing PRE command.*
4. *WDQS can only transition when data is applied at the chip input and during pre- and postambles.*

4.7 Reads (RD)

4.7.1 Read - Basic Information

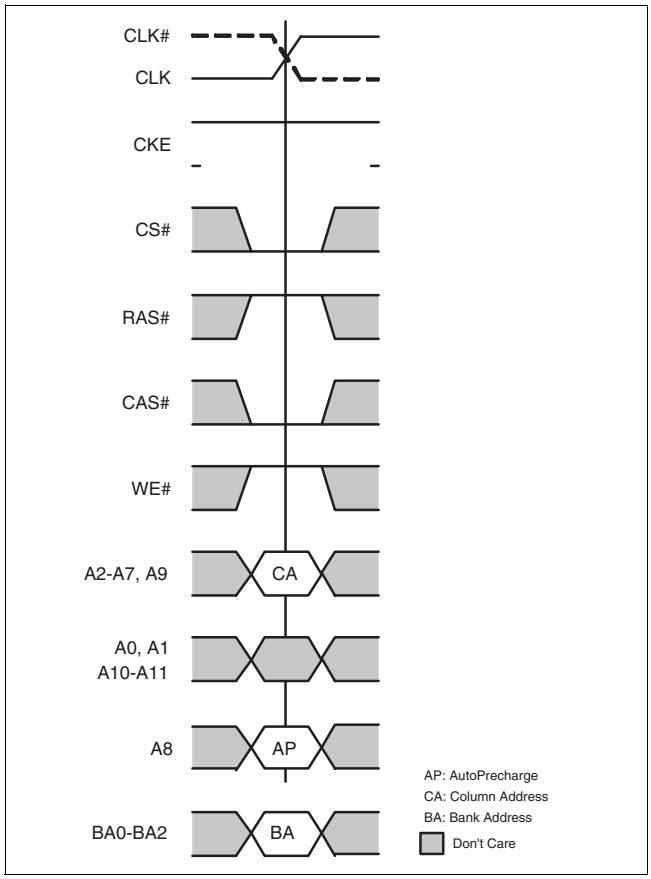

Figure 36 Read Command

Read bursts are initiated with a RD command, as shown in **Figure 36**. The column and bank addresses are provided with the RD command and Autoprecharge is either enabled or disabled for that access. The length of the burst initiated with a RD command is 4 or 8. There is no interruption of RD bursts. The two least significant start address bits are 'Don't Care'.

If Autoprecharge is enabled, the row being accessed will start precharge at the completion of the burst. The begin of the internal Autoprecharge will always be one cycle after $t_{RAS(min)}$ is met.

During RD bursts the memory device drives the read data edge aligned with the RDQS signal which is also driven by the memory. After a programmable CAS latency of 7, 8. 9 or 10 the data is driven to the controller. RDQS leaves HIGH state one cycle before its first rising edge (RD preamble t_{RPRE}). After the last falling edge of RDQS a postamble of t_{RPST} is performed.

t_{AC} is the time between the positive edge of CLK and the appearance of the corresponding driven read data. The skew between RDQS and the crossing point of CLK/$\overline{CLK}$ is specified as t_{DQSCK}. t_{AC} and t_{DQSCK} are defined relatively to the positive edge of CLK. t_{DQSQ} is the skew between a RDQS edge and the last valid data edge belonging to the RDQS edge. t_{DQSQ} is derived at each RDQS edge and begins with RDQS transition and ends with the last valid transition of DQs. t_{QHS} is the data hold skew factor and t_{QH} is the time from the first valid rising edge of RDQS to the first conforming DQ going non-valid and it depends on tHP and t_{QHS}. tHP is the minimum of t_{CL} and t_{CH}. t_{QHS} is effectively the time from the first data transition (before RDQS) to the RDQS transition. The data valid window is derived for each RDQS transition and is defined as t_{QH} minus t_{DQSQ}.

After completion of a burst, assuming no other commands have been initiated, data will go HIGH and RDQS will go HIGH. Back to back RD commands are possible producing a continuous flow of output data. There has to be one NOP cycle between back to back RD commands.

Any RD burst may be followed by a subsequent WR command. The minimum required number of NOP commands between the RD command and the WR command (t_{RTW}) depends on the programmed Read latency and the programmed Write latency

t_{RTW}(min)= (CL+4-WL).

Chapter 4.7.7 shows the timing requirements for RD followed by a WR with some combinations of CL and WL.

A RD may also be followed by a PRE command. Since no interruption of bursts is allowed the minimum time between a RD command and a PRE is two clock cycles as shown in **Chapter 4.7.8**.

All timing parameters are defined with controller terminations on.

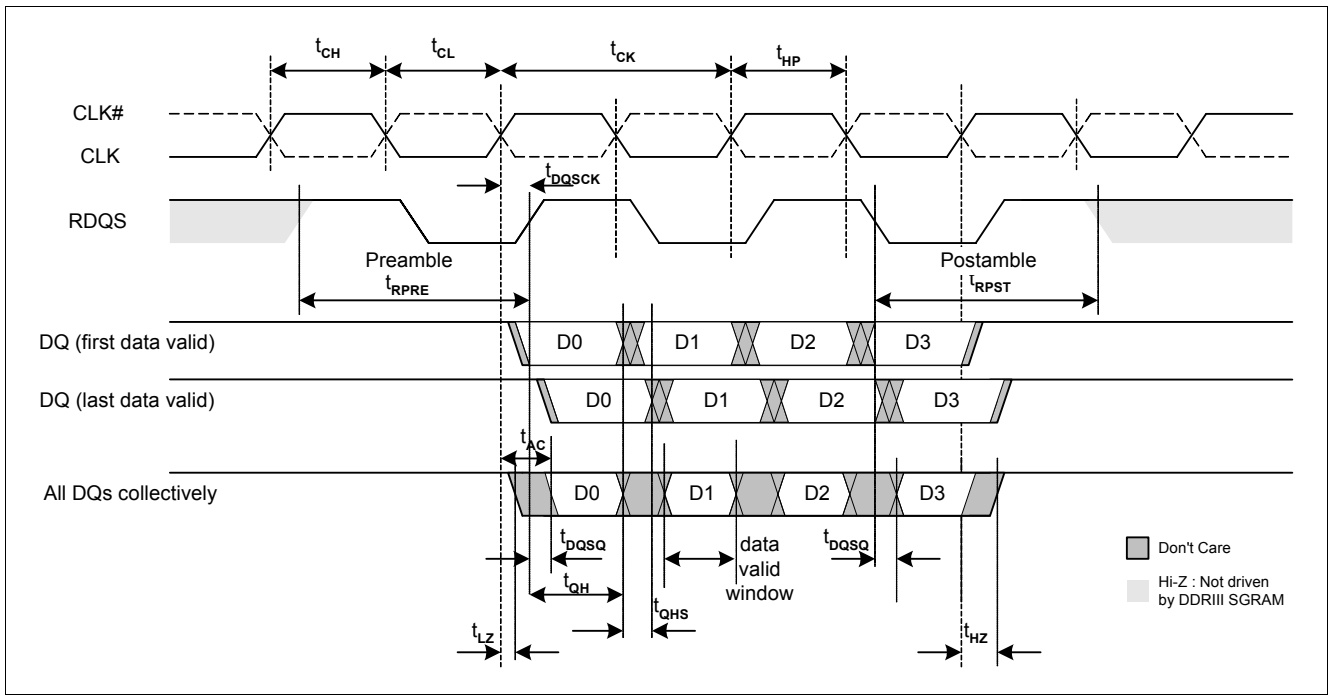

Figure 37 Basic Read Burst Timing

1. *The GDDR3 SGRAM switches off the DQ terminations one cycle before data appears on the bus and drives the data bus HIGH.*
2. *The GDDR3 SGRAM drives the data bus HIGH one cycle after the last data driven on the bus before switching the termination on again.*

4.7.2 Read - Basic Sequence

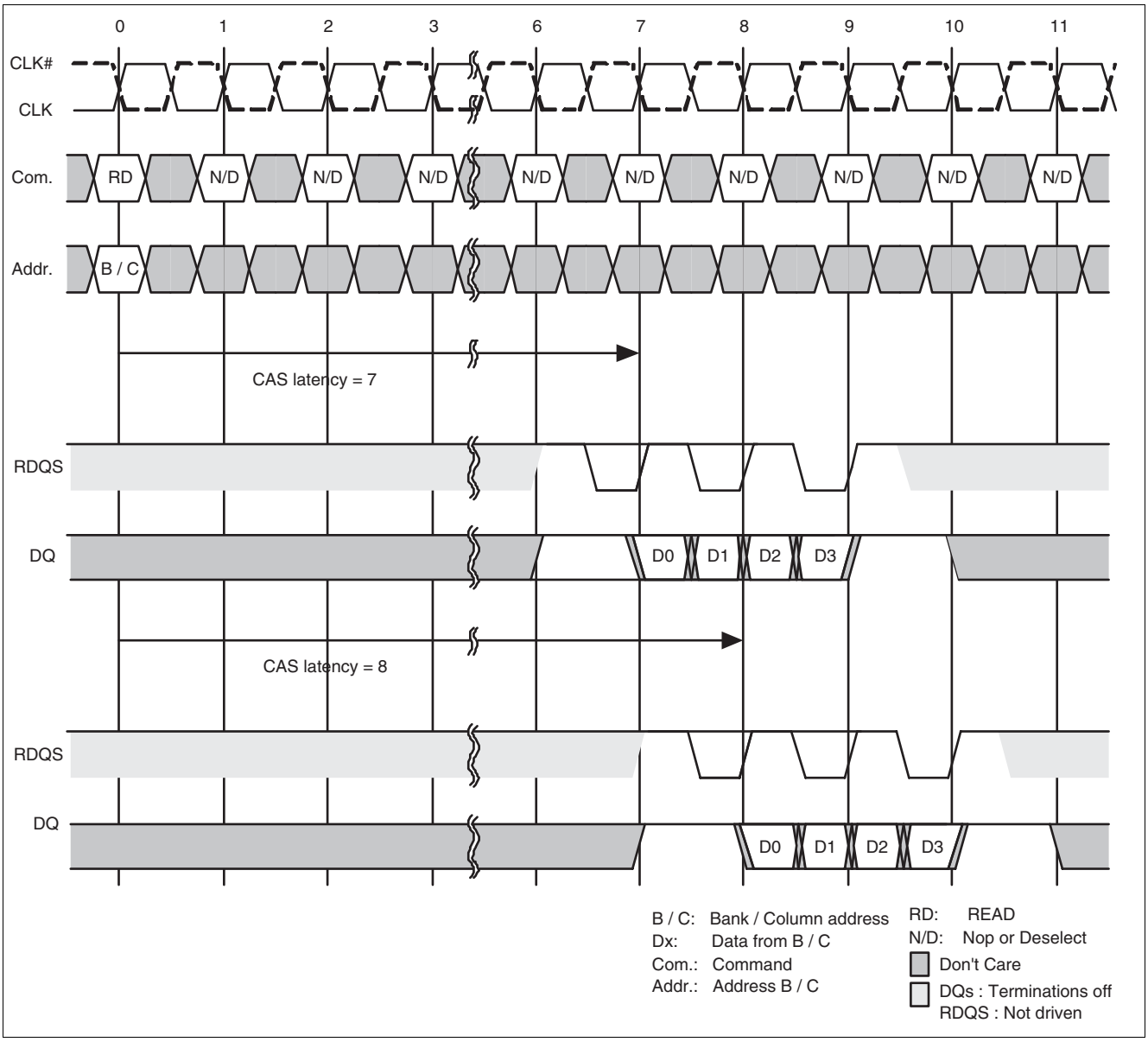

Figure 38 Read Burst

1. *Shown with nominal t_{AC} and t_{DQSQ}.*
2. *RDQS will start driving high 1/2 cycle prior to the first falling edge and stop 1/2 cycle after the last rising edge of RDQS.*
3. *The DQ terminations are switched off 1 cycle before the first Read Data and on again 1 cycle after the last Read data.*

4.7.3 Consecutive Read Bursts

4.7.3.1 Gapless Bursts

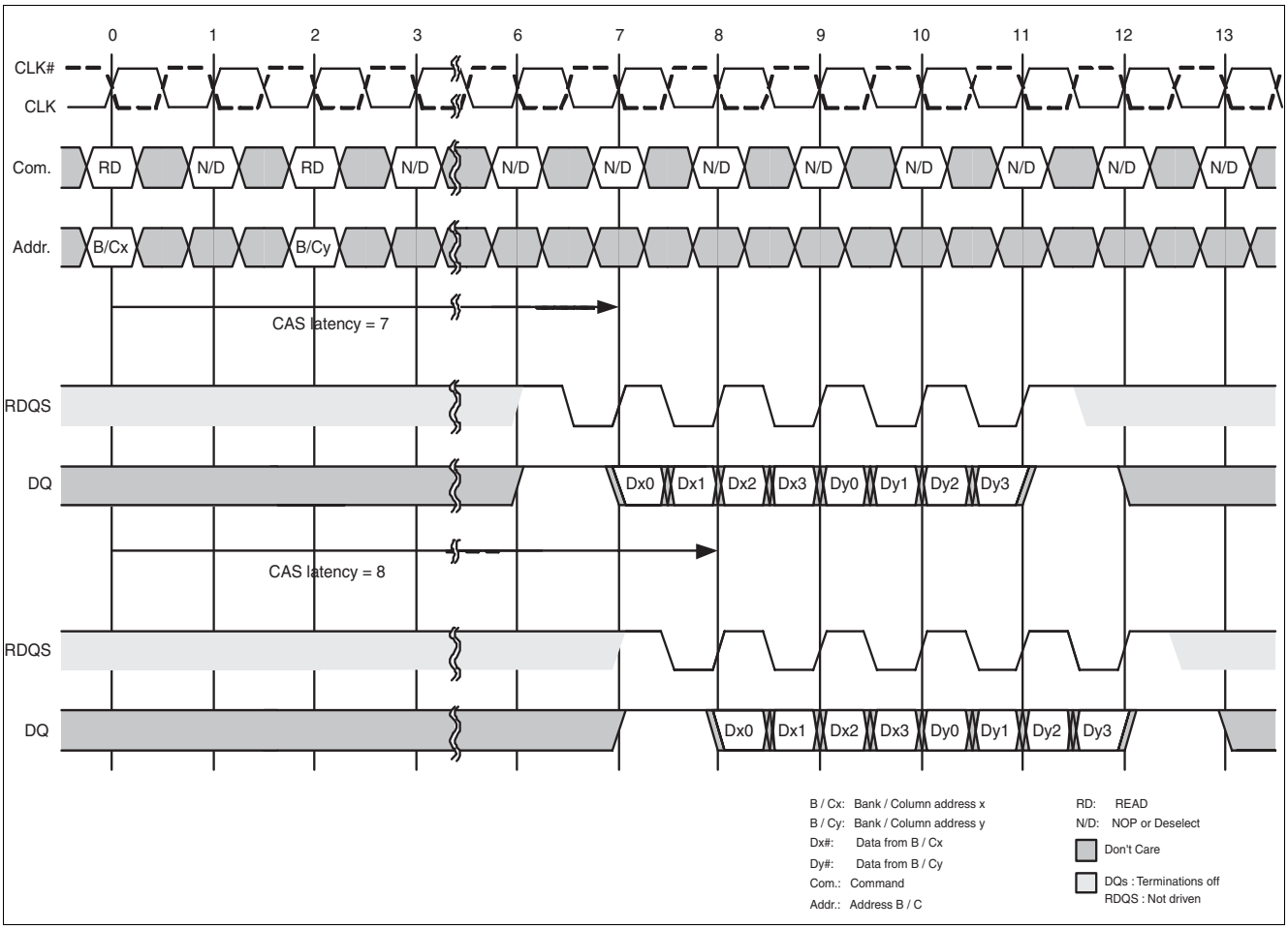

Figure 39 Gapless Consecutive Read Bursts

1. *The second RD command may be either for the same bank or another bank.*
2. *Shown with nominal t_{AC} and t_{DQSQ}.*
3. *Example applies only when READ commands are issued to same device.*
4. *RDQS will start driving high 1/2 cycle prior to the first falling edge and stop 1/2 cycle after the last rising edge of RDQS.*
5. *The DQ terminations are switched off 1 cycle before the first Read Data and on again 1 cycle after the last Read data.*

4.7.4 Bursts with Gaps

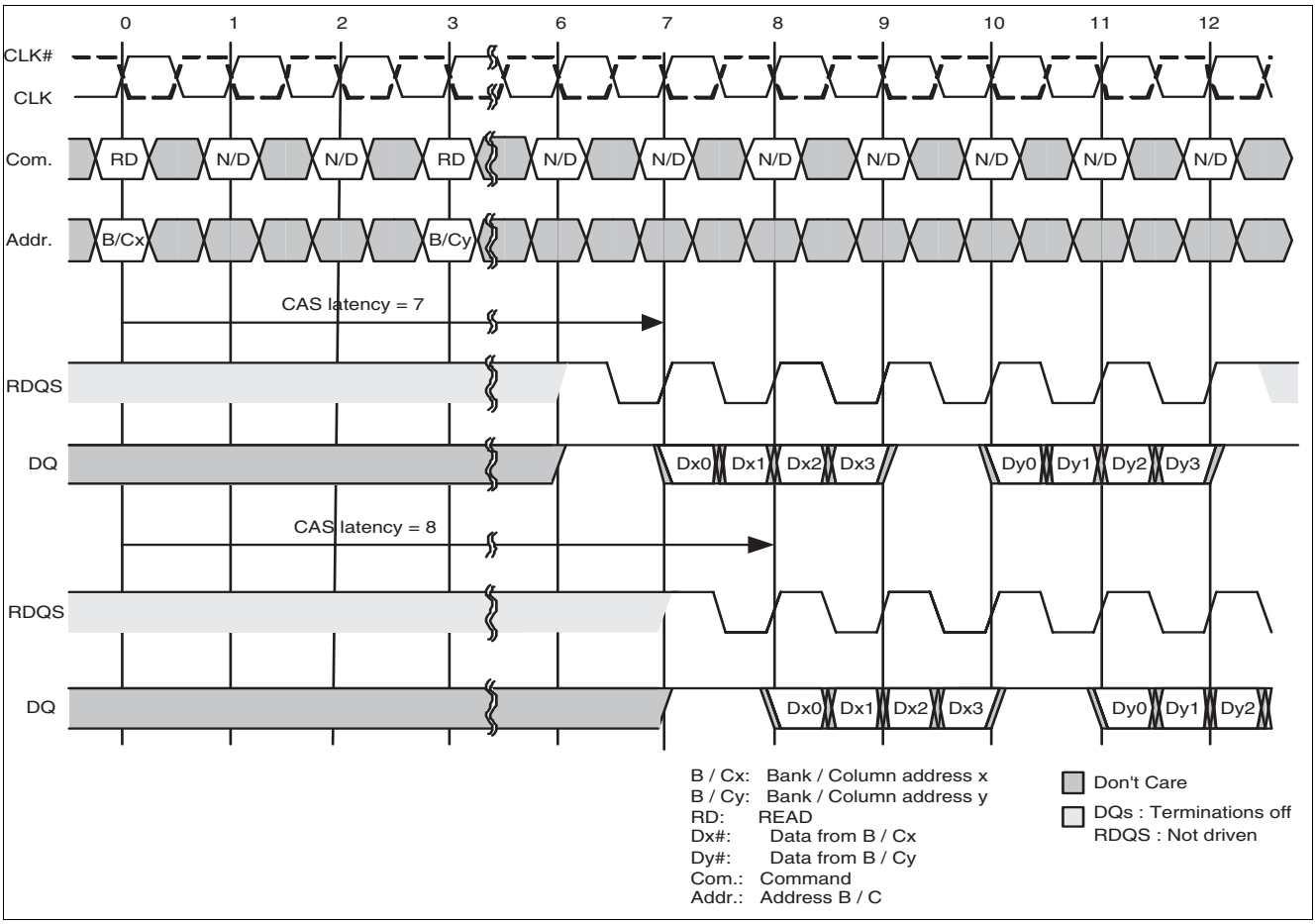

Figure 40 Consecutive Read Bursts with Gaps

1. *The second RD command may be either for the same bank or another bank.*
2. *RDQS will start driving high 1/2 cycle prior to the first falling edge and stop 1/2 cycle after the last rising edge of RDQS.*
3. *The DQ terminations are switched off 1 cycle before the first Read Data and on again 1 cycle after the last Read data.*

4.7.5 Read followed by DTERDIS

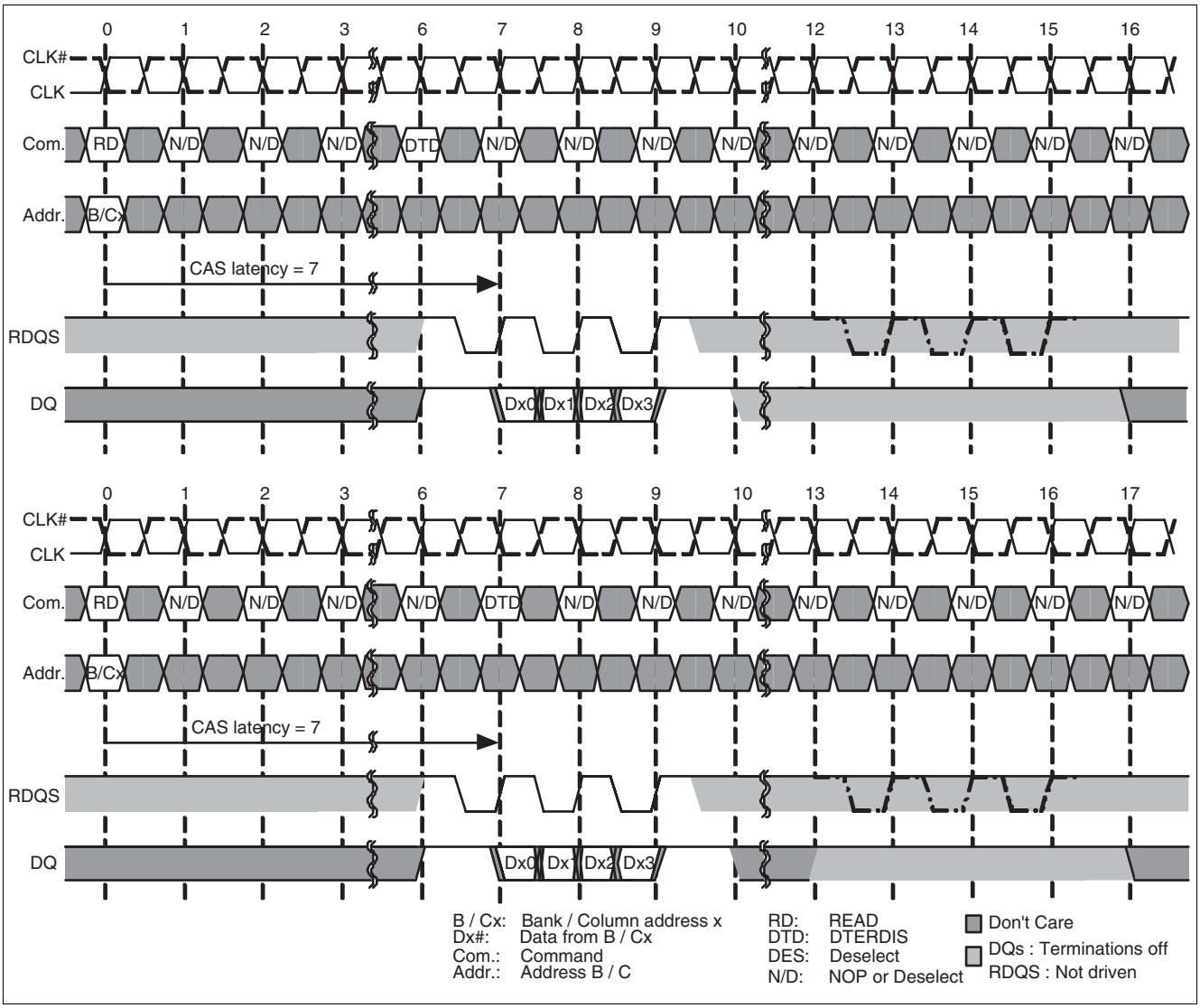

Figure 41 Read Command followed by DTERDIS

1. *At least 3 NOPs are required between a READ command and a DTERDIS command in order to avoid contention on the RDQS bus in a 2 rank system.*
2. *CAS Latency 7 is used as an example.*
3. *The DQ terminations are switched off (CL-1) clock periods after the DTERDIS command for a duration of 4 clocks.*
4. *The dashed lines (RDQS bus) describe the RDQS behavior in the case where the DTERDIS command corresponds to a Read command applied to the second Graphics DRAM in a 2 rank system. In this case, RDQS would be driven by the second Graphics DRAM.*

4.7.6 Read with Autoprecharge

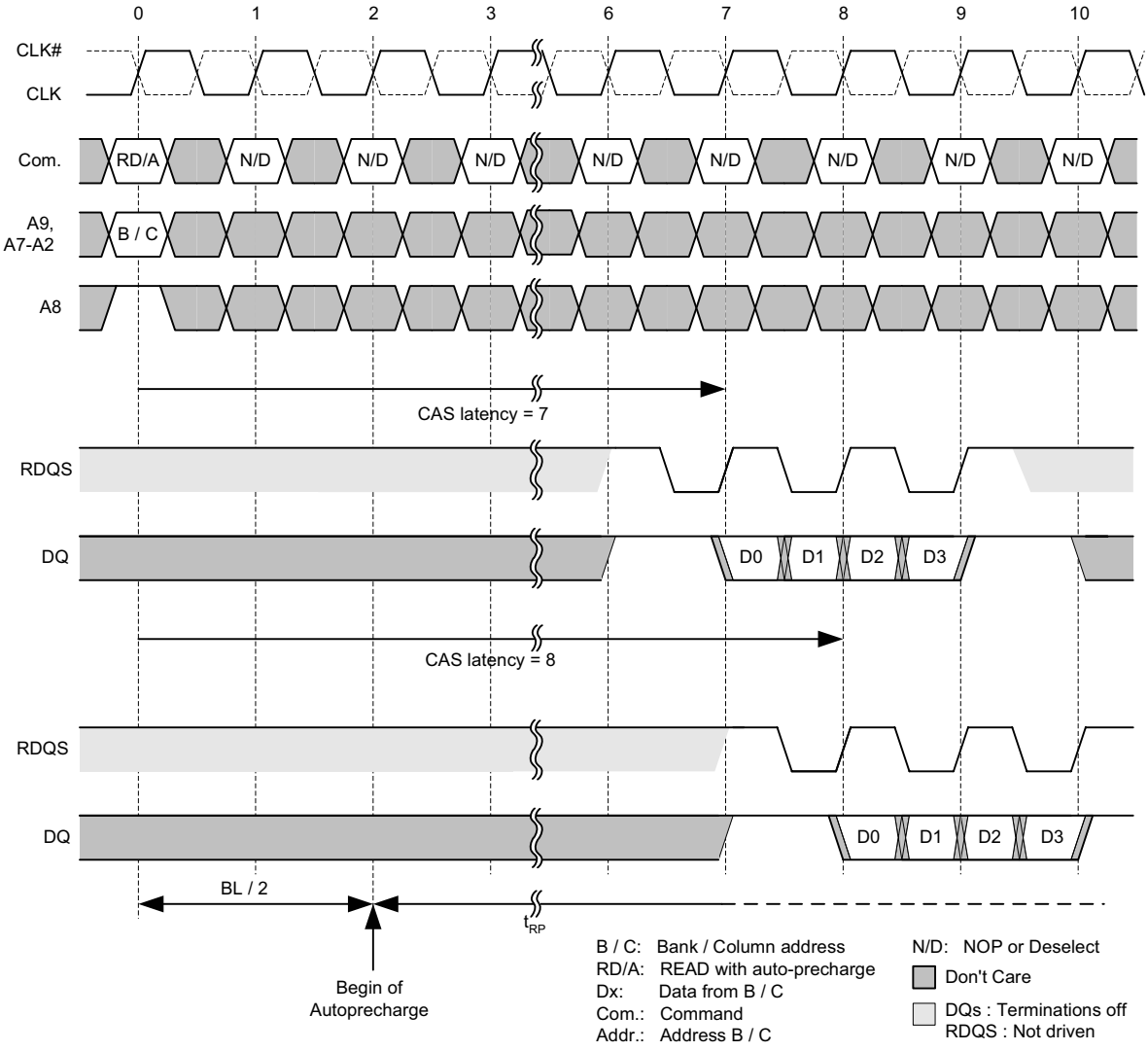

Figure 42 Read with Autoprecharge

1. *When issuing a RD/A command , the t_{RAS} requirement must be met at the beginning of Autoprecharge*
2. *Shown with nominal t_{AC} and t_{DQSQ}*
3. *RDQS will start driving high 1/2 cycle prior to the first falling edge and stop 1/2 cycle after the last rising edge of RDQS.*
4. *The DQ terminations are switched off 1 cycle before the first Read Data and on again 1 cycle after the last Read data.*
5. *t_{RAS} Lockout support.*

4.7.7 Read followed by Write

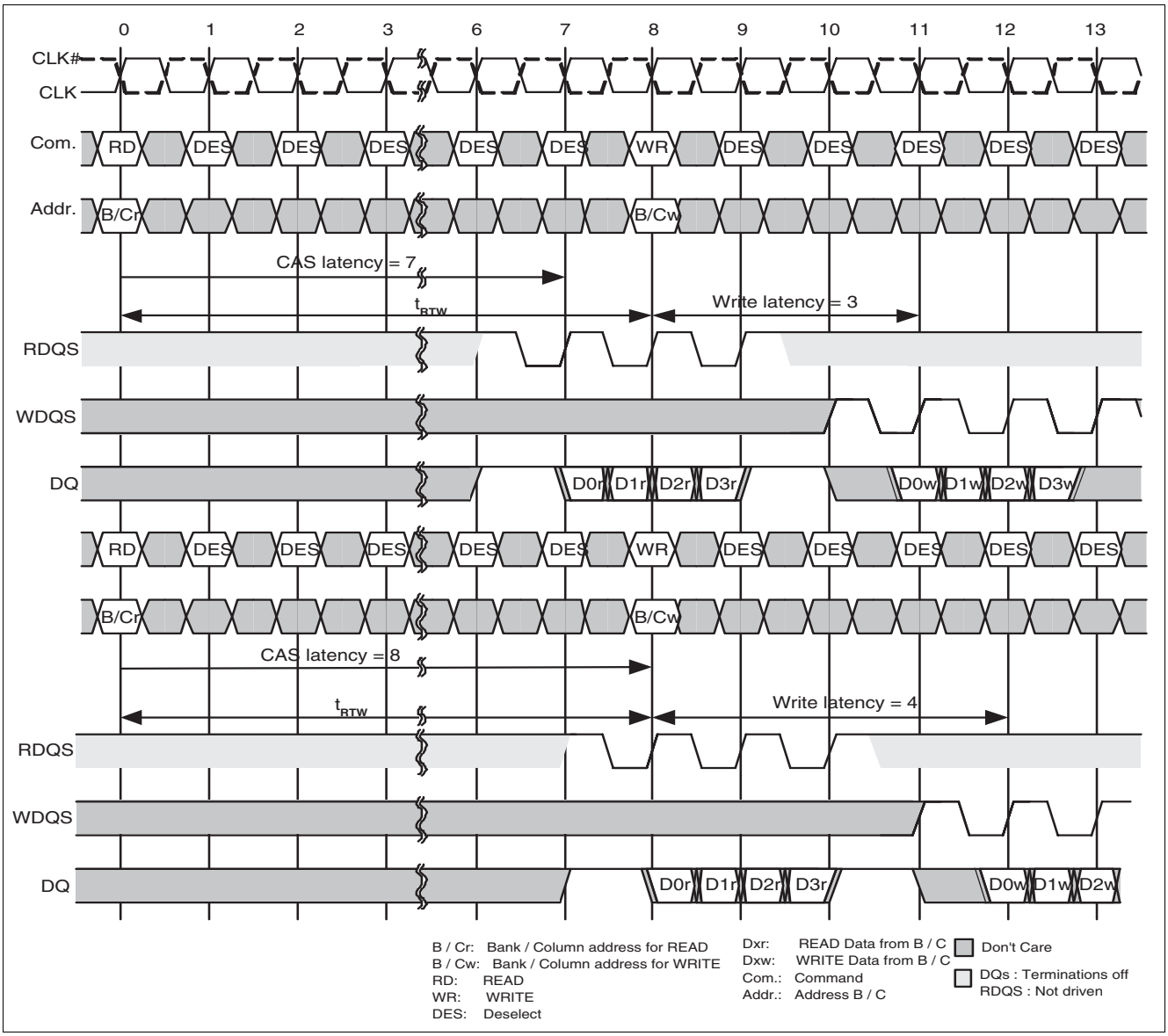

Figure 43 Read followed by Write

1. *Shown with nominal t_{AC}, t_{DQSQ} and t_{DQSS}*
2. *RDQS will start driving high 1/2 cycle prior to the first falling edge and stop 1/2 cycle after the last rising edge of RDQS.*
3. *The DQ terminations are switched off 1 cycle before the first Read Data and on again 1 cycle after the last Read data*
4. *WDQS can only transition when data is applied at the chip input and during pre- and postambles.*
5. *The Write command may be either on the same bank or on another bank.*

4.7.8 Read followed by Precharge on the same Bank

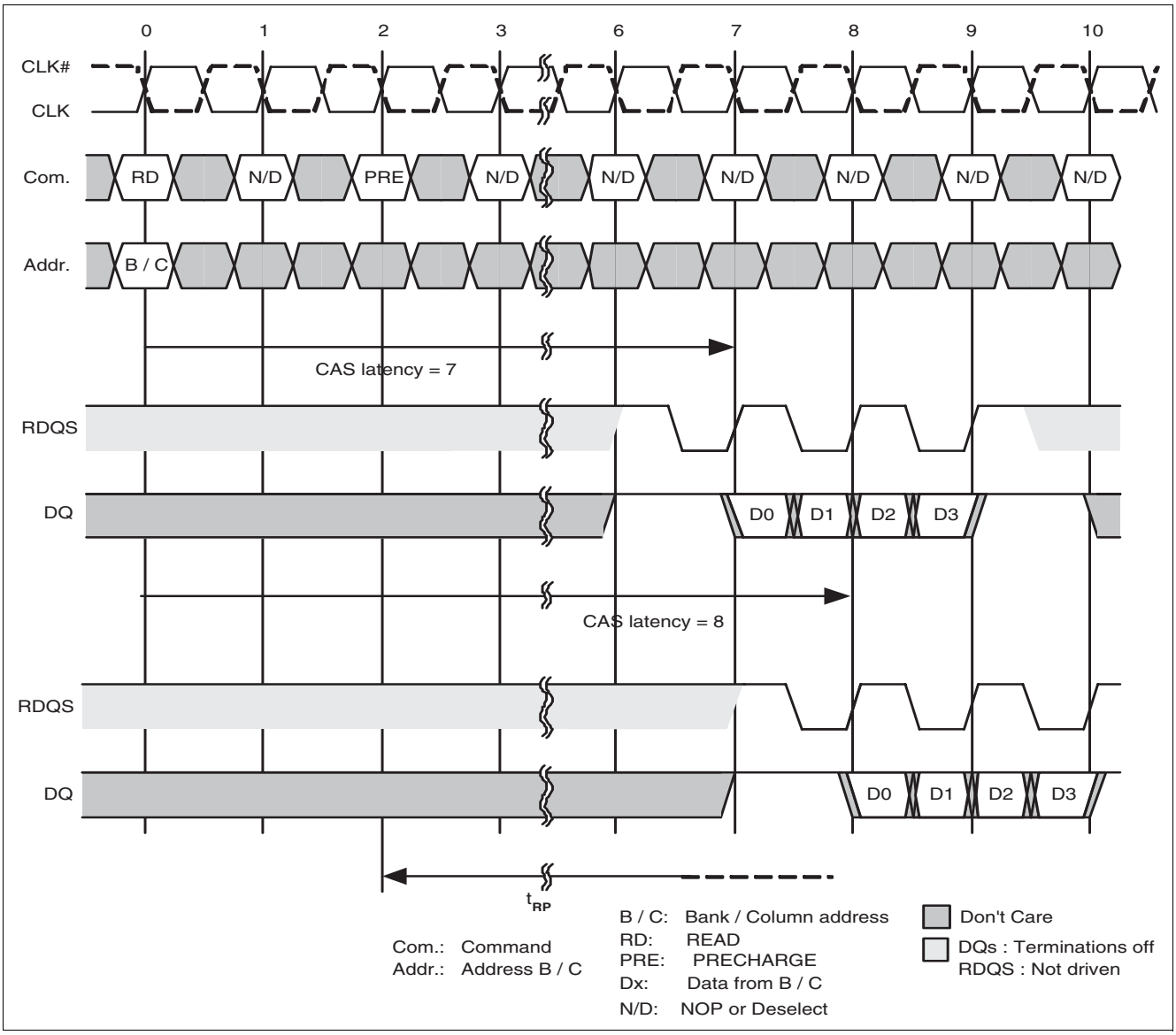

Figure 44 Read followed by Precharge on the same bank

1. *t_{RAS} requirement must also be met before issuing PRE command*
2. *RD and PRE commands are applied to the same bank.*
3. *Shown with nominal t_{AC} and t_{DQSQ}*
4. *RDQS will start driving high 1/2 cycle prior to the first falling edge and stop 1/2 cycle after the last rising edge of RDQS.*

4.8 Data Termination Disable (DTERDIS)

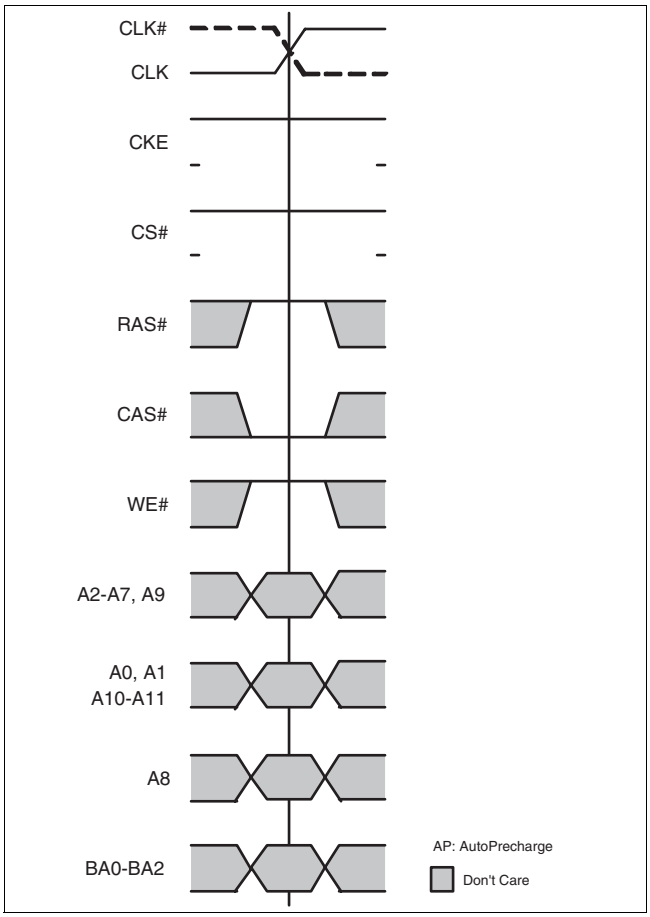

Figure 45 Data Terminal Disable Command

The Data Termination Disable command is detected by the device by snooping the bus for Read commands when $\overline{CS}$ is high. The terminators are disabled starting at CL - 1 clocks after the DTERDIS command is detected and the duration is 4 clocks. The command and address terminators are always enabled.

DTERDIS may only be applied to the GDDR3 Graphics memory if it is not in the Power Down or in the Self Refresh state.

The timing relationship between DTERDIS and other commands is defined by the constraint to avoid contention on the RDQS bus (i.e Read to DTERDIS transistion) or the necessity to have a defined termination on the data bus during Write (i.e. Write to DTERDIS transition). ACT and PRE/PREALL may be applied at any time before or after a DTERDIS command.

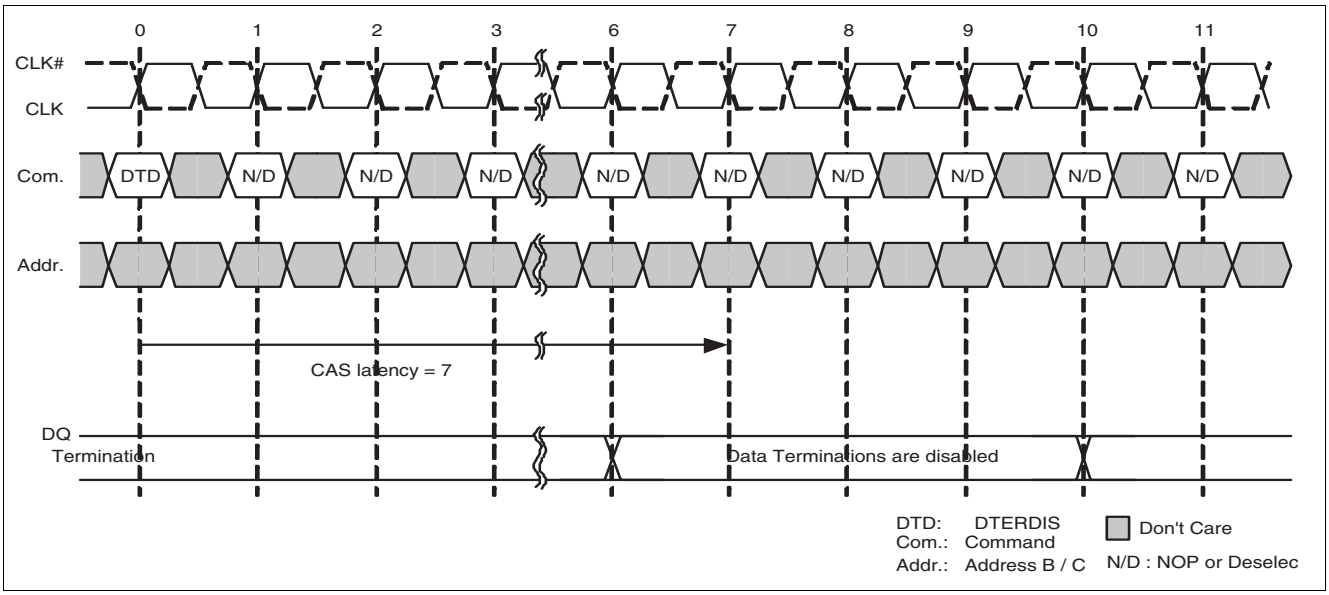

Figure 46 DTERDIS Timing

4.8.1 DTERDIS followed by DTERDIS

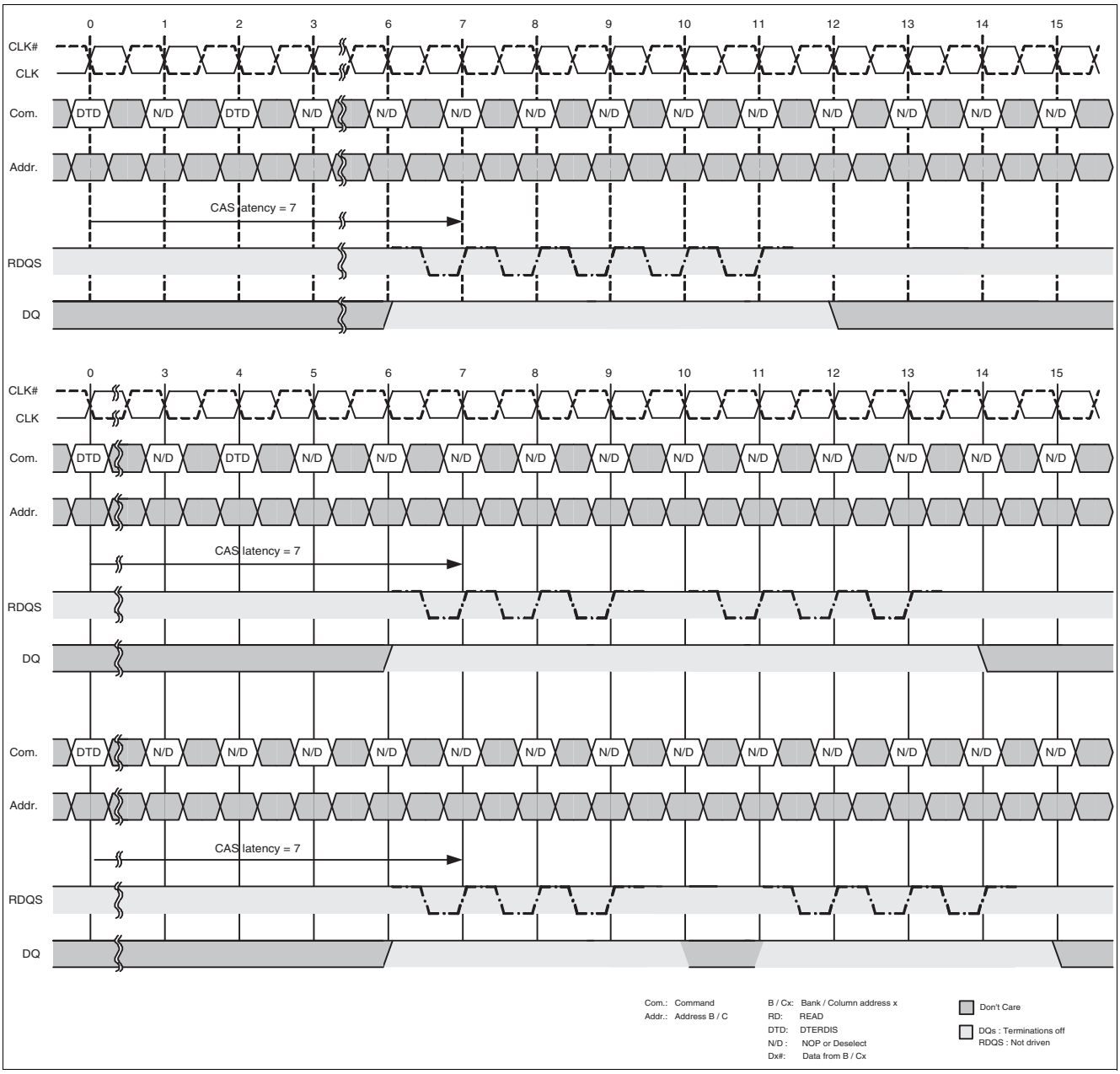

Figure 47 DTERDIS Command followed by DTERDIS

1. *At least 1NOP is required between 2 DTERDIS commands. This correspond to a Read to Read transistion on the other memory in a 2 rank system.*
2. *CAS Latency 7 is used as an example.*
3. *The DQ terminations are switched off (CL-1) clock periods after the DTERDIS command for a duration of 4 clocks.*
4. *The dashed lines (RDQS bus) describe the RDQS behavior in the case where the DTERDIS command corresponds to a Read command applied to the second Graphics DRAM in a 2 rank system. In this case, RDQS would be driven by the second Graphics DRAM.*

4.8.2 DTERDIS followed by READ

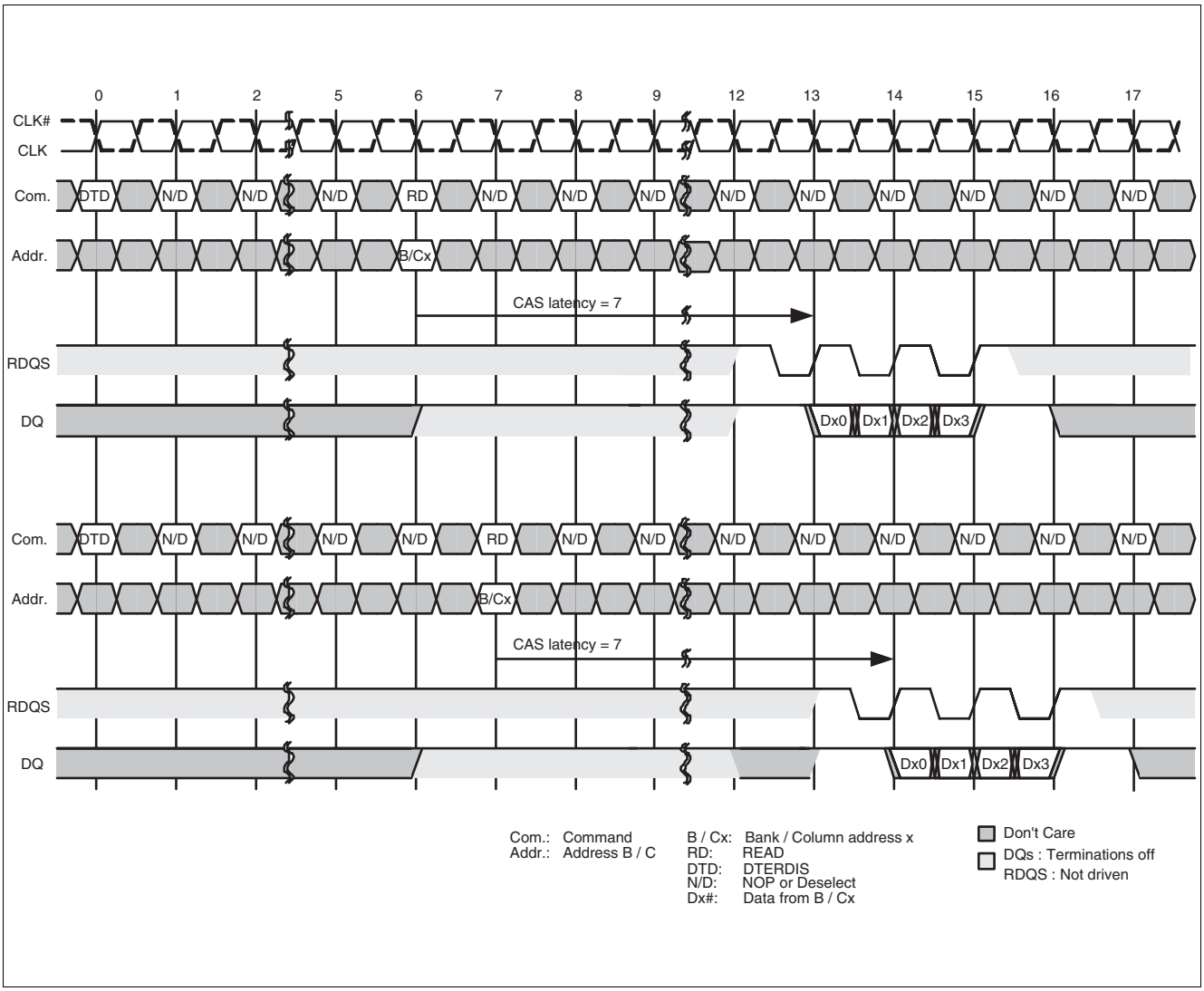

Figure 48 DTERDIS Command followed by READ

1. *At least 3 NOPs are required between a DTERDIS command and a READ command in order to avoid contention on the RDQS bus in a 2 rank system.*
2. *CAS Latency 7 is used as an example.*
3. *The DQ terminations are switched off (CL-1) clock periods after the DTERDIS command for a duration of 4 clocks.*

4.8.3 DTERDIS followed by Write

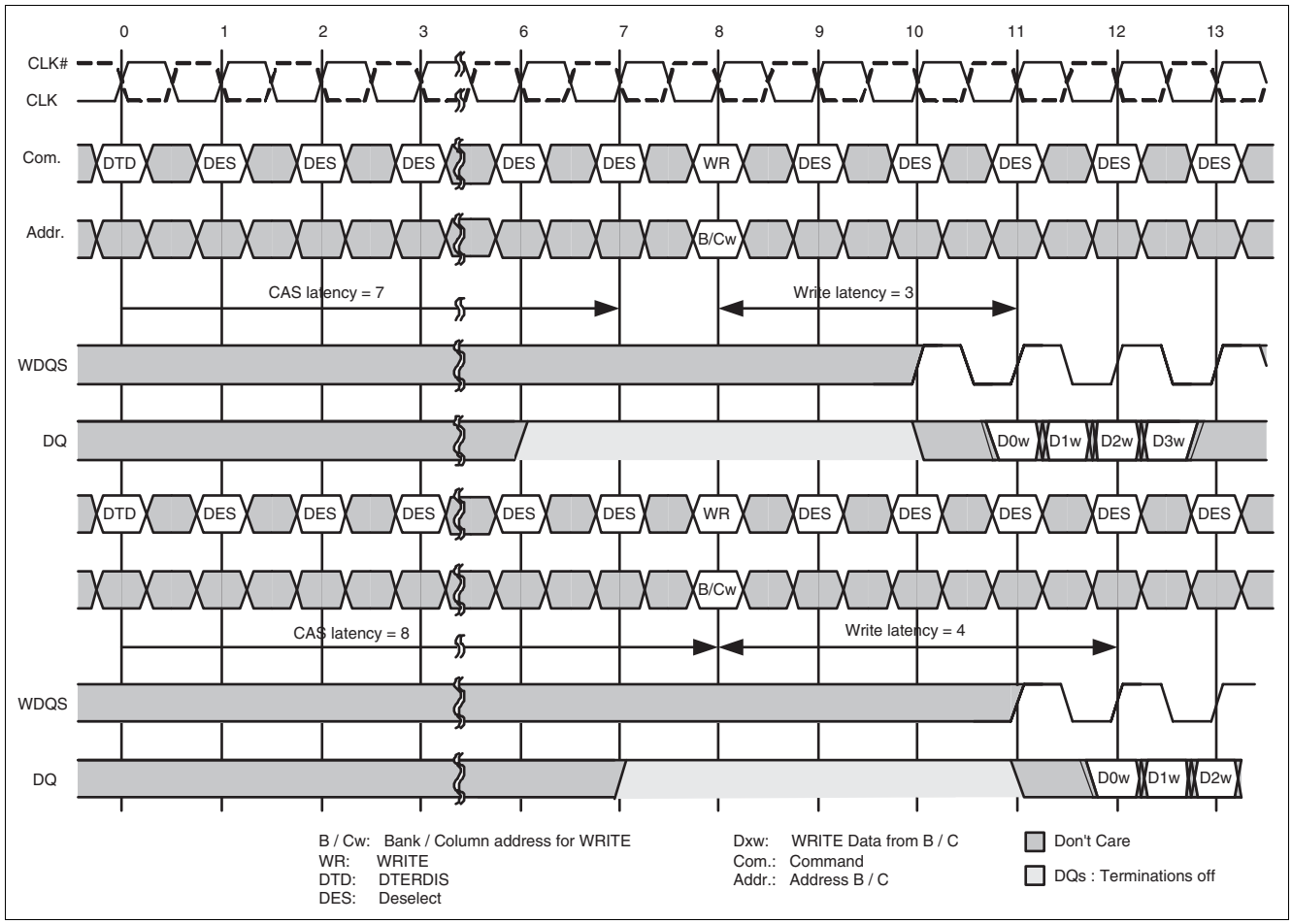

Figure 49 DTERDIS Command followed by Write

1. *Write shown with nominal value of t_{DQSS}.*
2. *WDQS can only transition when data is applied at the chip input and during pre- and postambles*
3. *The minimum distance between DTERDIS and Write is (CL - WL + BL/2 +2) clocks.*

4.9 Precharge (PRE/PREALL)

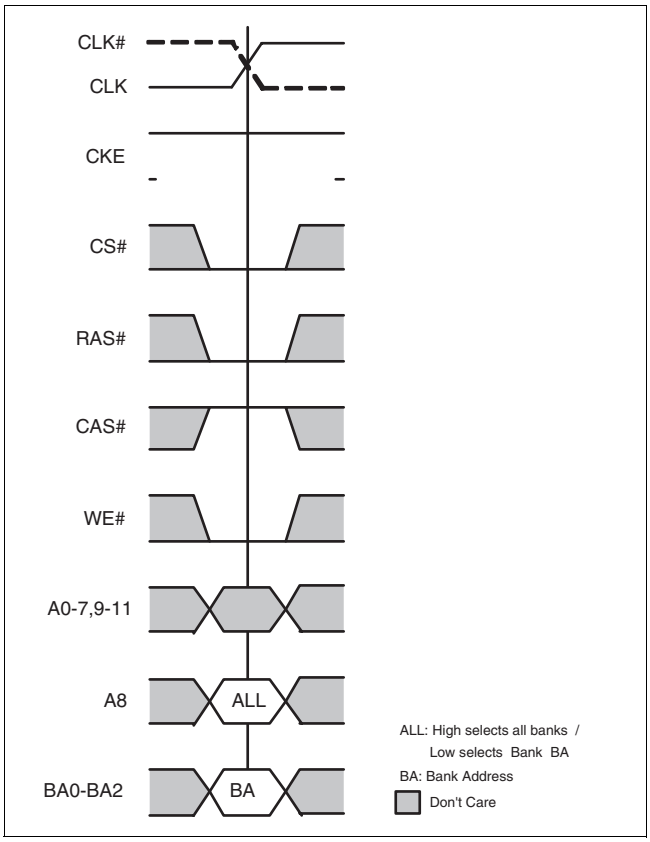

Figure 50 Precharge Command

The Precharge command is used to deactivate the open row in a particular bank (PRE) or the open rows in all banks (PREALL). The bank(s) will enter the idle state and be available again for a new row access after the time t_{RP}. A8/AP sampled with the PRE command determines whether one or all banks are to be precharged. For PRE commands BA0, BA1 and BA2 select the bank. For PREALL inputs BA0, BA1 and BA2 are “Don’t Care”. The PRE/PREALL command may not be given unless the t_{RAS} requirement is met for the selected bank (PRE), or for all banks (PREALL).

Table 21 BA02, BA1 and BA0 precharge bank selection

A8 / AP	BA2	BA1	BA0	precharged bank(s)
0	0	0	0	Bank 0 only
0	0	0	1	Bank 1 only
0	0	1	0	Bank 2 only
0	0	1	1	Bank 3 only
0	1	0	0	Bank 4 only
0	1	0	1	Bank 5 only
0	1	1	0	Bank 6 only
0	1	1	1	Bank 7 only
1	X	X	X	All banks

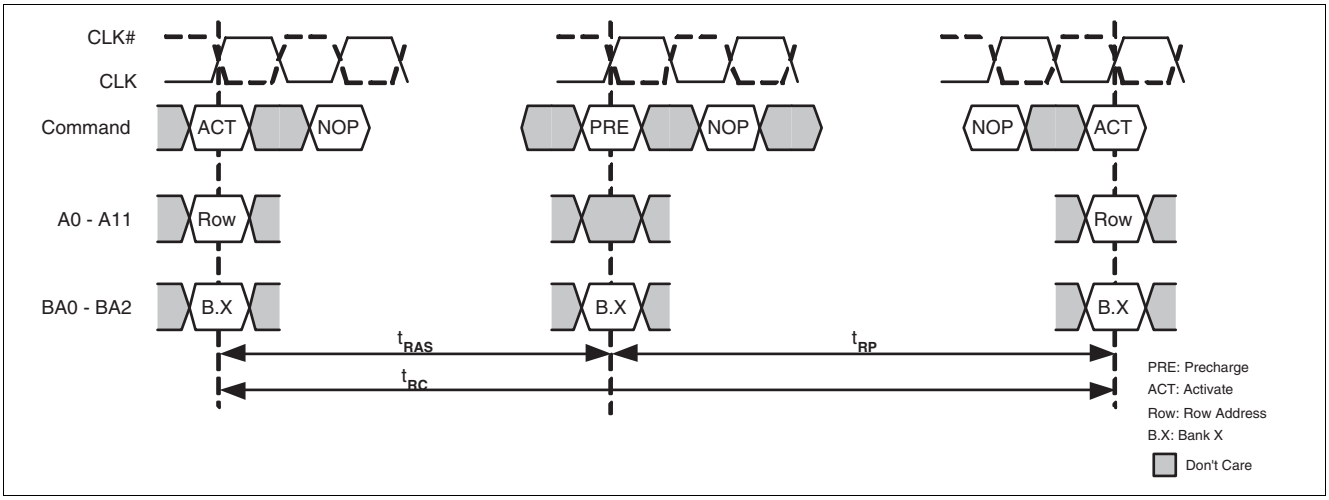

Figure 51 Precharge Timing

4.10 Auto Refresh Command (AREF)

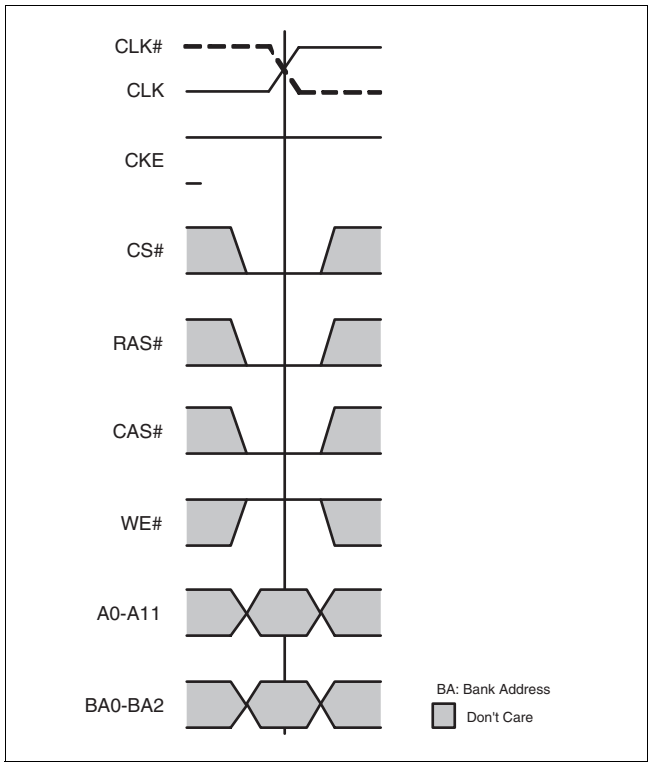

Figure 52 Auto Refresh Command

AREF is used to do a refresh cycle on one row in each bank. The addresses are generated by an internal refresh controller; external address pins are “DON’T CARE”. All banks must be idle before the AREF command can be applied. The delay between the AREF command and the next ACT or subsequent AREF must be at least t_{RFC}(min). The refresh period starts when the AREF command is entered and ends t_{RFC} later at which time all banks will be in the idle state.

Within a period of t_{REF} the whole memory has to be refreshed. The average periodic interval time from AREF to AREF is then t_{REFI}.

To improve efficiency bursts of AREF commands can be used. Such bursts may consist of maximum 8 AREF commands. t_{RFC}(min) is the minimum required time between two AREF commands inside of one AREF burst. According to the number of AREF commands in one burst the average required time from one AREF burst to the next can be increased. Example: If the AREF bursts consists of 8 AREF commands, the average time from one AREF burst to the next is 8* t_{REFI}.

The AREF command generates an update of the OCD output impedance and of the addresses, commands and DQ terminations. The timing parameter t_{KO} (see **Chapter 4.2.2** must be met.

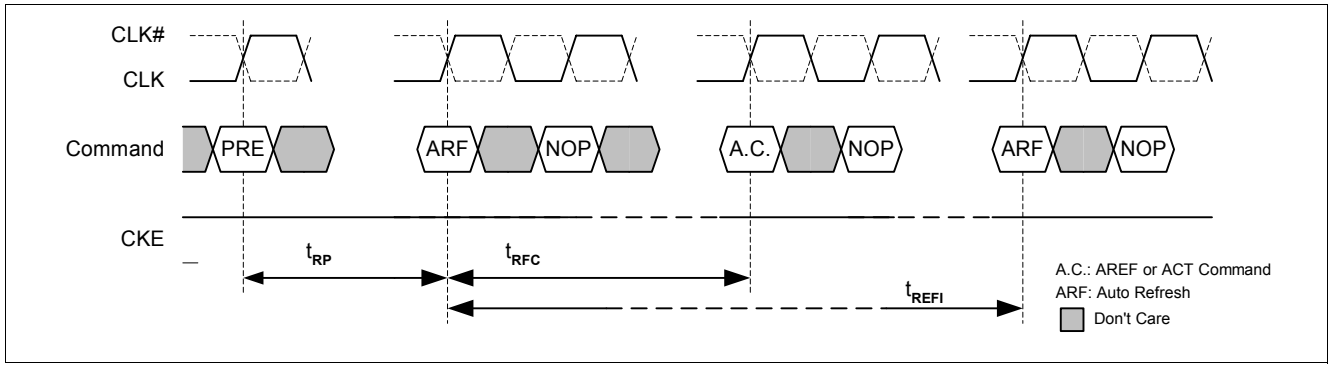

Figure 53 Auto Refresh Cycle

4.11 Self-Refresh

4.11.1 Self-Refresh Entry (SREFEN)

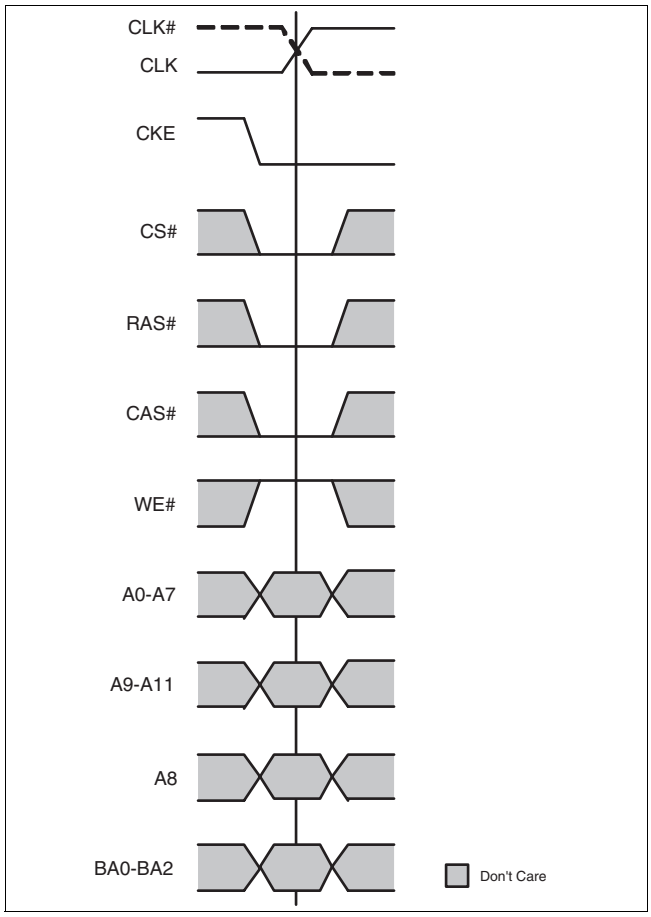

Figure 54 Self-Refresh Entry Command

The Self-Refresh mode can be used to retain data in the GDDR3 Graphics RAM even if the rest of the system is powered down. When in the Self-Refresh mode, the GDDR3 Graphics RAM retains data without external clocking. The Self-Refresh command is initiated like an Auto-Refresh command except CKE is disabled (LOW). Self Refresh Entry is only possible if all banks are precharged and t_{RP} is met.

The GDDR3 Graphics RAM has a build-in timer to accomodate Self-Refresh operation. The Self-Refresh command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. Once the command is registered, CKE must be held LOW to keep the device in Self-Refresh mode. When the has entered the Self-Refresh mode, all external control signals, except CKE are disabled. The address, command and data terminators remain on. The DLL and the clock are internally disabled to save power. The user may halt the external clock while the device is in Self-Refresh mode the next clock after Self-Refresh entry, however the clock must be restarted before the device can exit Self-Refresh operation.

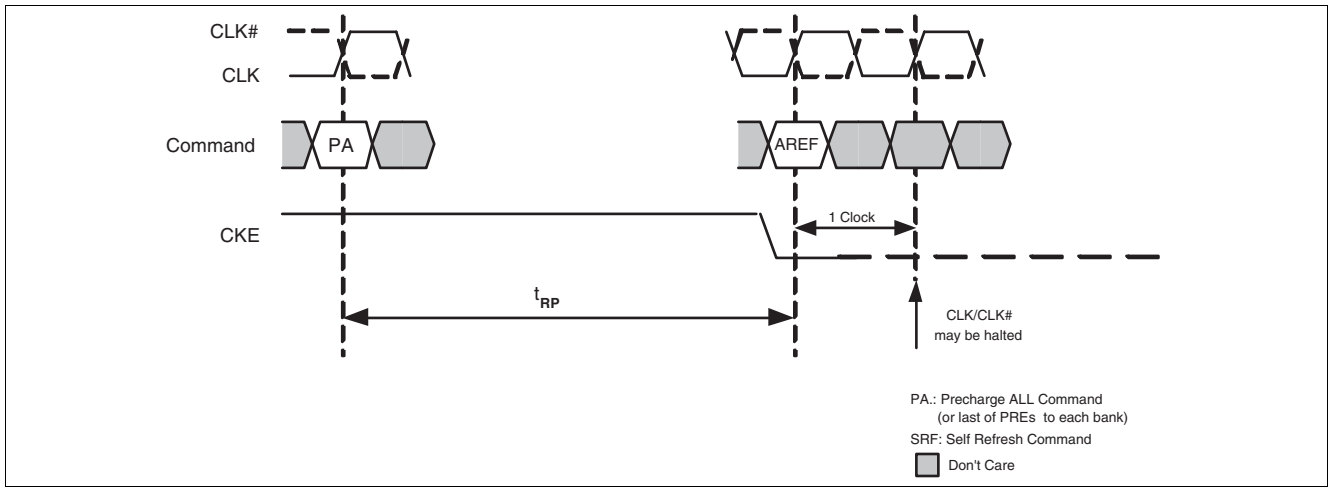

Figure 55 Self Refresh Entry

4.12 Self-Refresh Exit (SREFEX)

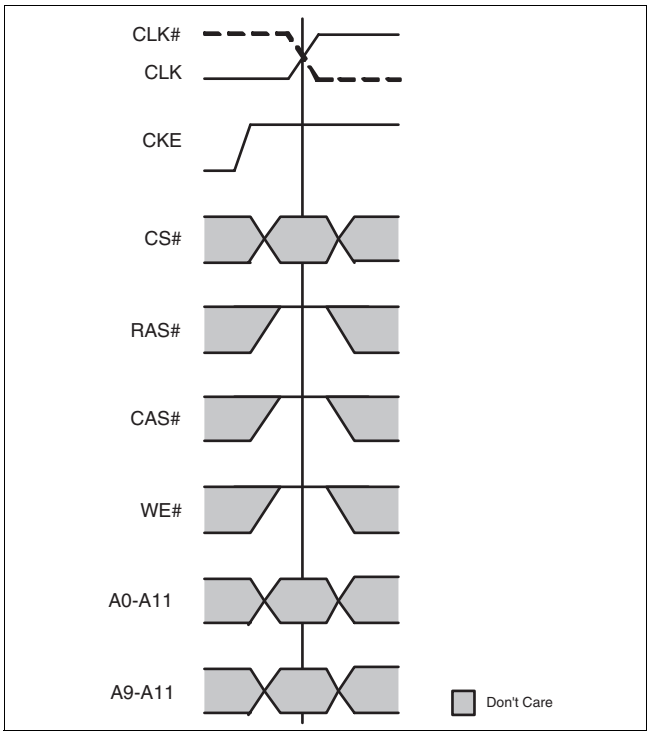

Figure 56 Self Refresh Exit Command

To exit the Self Refresh Mode, a stable external clock is needed before setting CKE high asynchronously. Once the Self-Refresh Exit command is registered, a delay equal or longer than t_{XSC} must be satisfied before any command can be applied. During this time, the DLL is automatically enabled, reset and calibrated.

CKE must remain HIGH for the entire Self-Refresh exit period and commands must be gated off with $\overline{CS}$ held HIGH. Alternately, NOP commands may be registered on each positive clock edge during the Self Refresh exit interval.

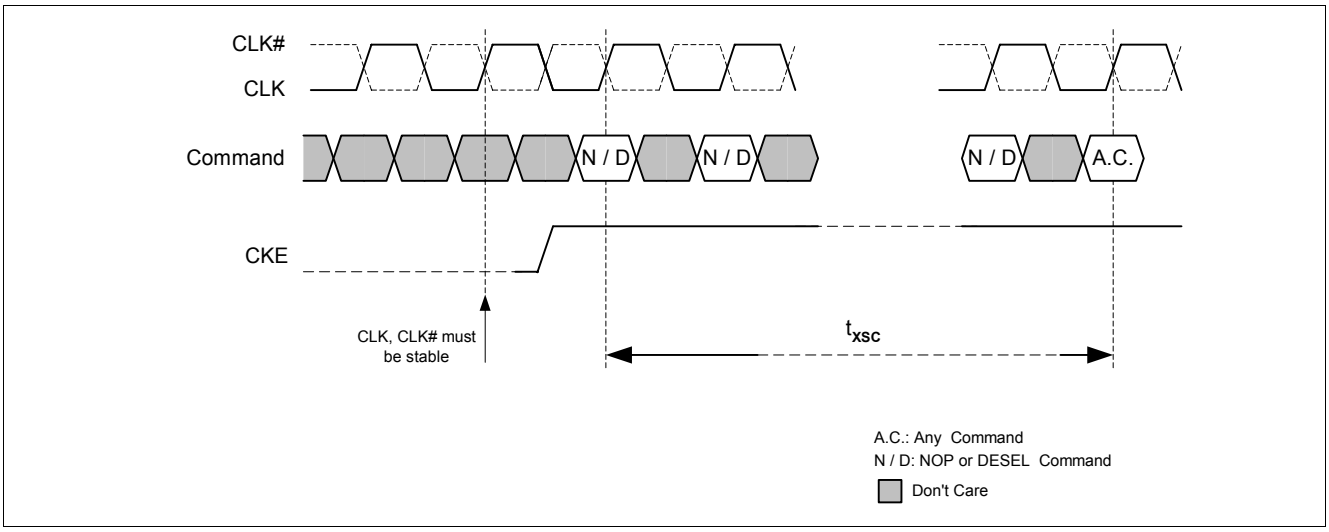

Figure 57 Self Refresh Exit

4.13 Power-Down

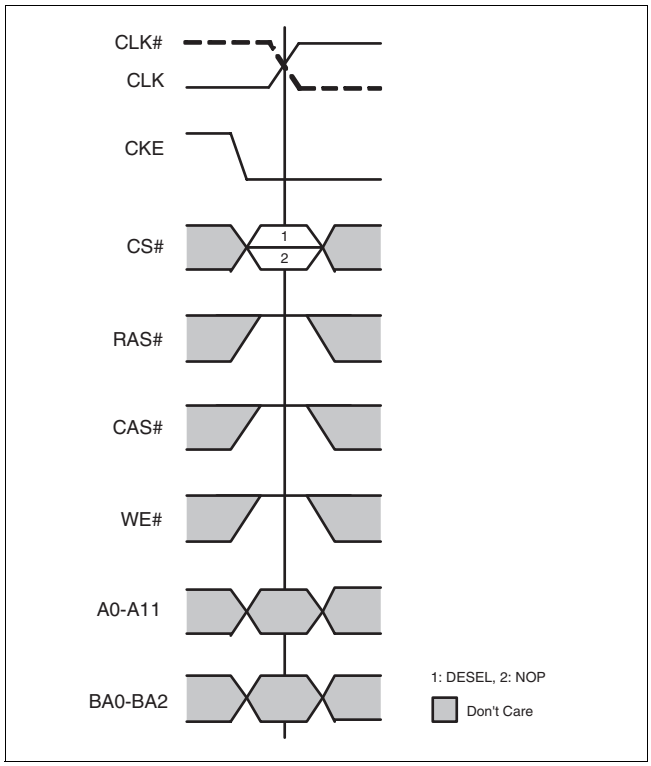

Figure 58 Power Down Command

The requires CKE to be active at all times an access is in progress : From the issuing of a READ or WRITE command until completion of the burst. For READs, a burst completion is defined after the rising edge of the Read Postamble. For Writes, a burst completion is defined one clock after the rising edge of the Write Postamble.

For Read with Autoprecharge and Write with Autoprecharge, the internal Autoprecharge must be completed before entering Power-Down.

Power-Down is entered when CKE is registered LOW. (No access can be in progress. "Access" means as well READ or WRITE to a second memory sharing the data bus in a dual rank system.) If Power-Down occurs when all banks are idle, this mode is referred to as Precharge Power-Down; if Power-Down occurs when there is a row active in any bank, this mode is referred to as Active Power-Down. Entering power-down deactivates the input and output buffers, excluding CLK, $\overline{CLK}$ and CKE. For maximum power saving, the user has the option of disabling the DLL prior to entering power-down. In that case the DLL must be enabled and reset after exiting power-down, and 1000 cycles must occur before a READ command can be issued.

In Power-Down mode, CKE low and a stable clock signal must be maintained at the inputs of the GDDR3 Graphics RAM, all the other input signals are “Don’t Care”. Power down duration is limited by the refresh requirements of the device.

The Power-Down state is synchronously exited when CKE is registered HIGH (along with a NOP or DESEL command). A valid executable command may be applied t_{XPN} later.

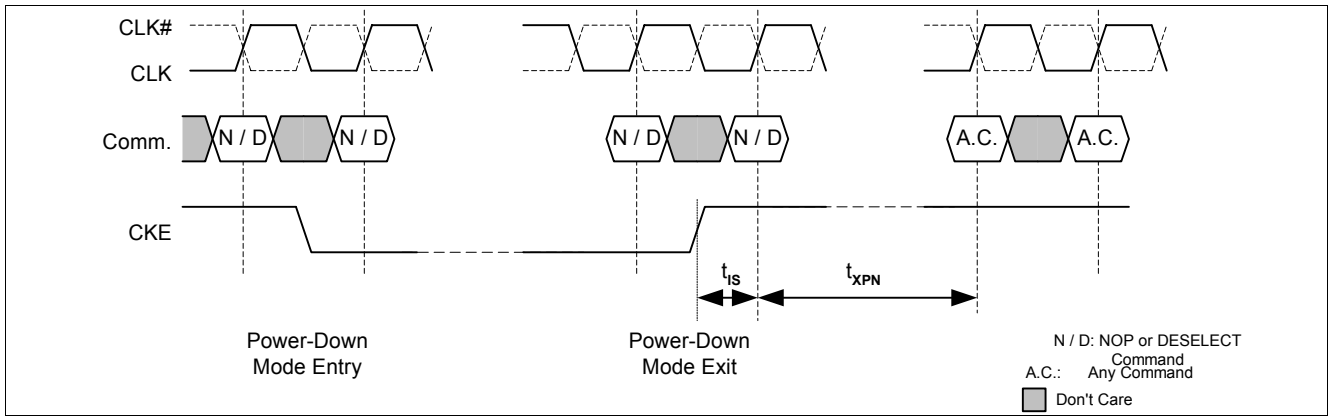

Figure 59 Power-Down Mode

4.14 DLL Off Mode

For very low frequency operations between 100 MHz and 350 MHz the DLL off mode is supported. Entering this mode requires an Extended Mode Register Set command disabling the DLL by setting A0 to 1. For 350 MHz clock speed and faster DLL on mode operation is recommended.

Most of the commands and timings described in **Chapter 4.5** to **Chapter 4.13** are also applicable for DLL off mode. Differences exist for the frequency range, the initialization and the timing of WR command and RD command.

4.14.1 Frequency range in DLL off mode

Operations in DLL off mode are limited to the frequencies between 100 MHz and 350 MHz.

Table 22 DLL off: General Timing Parameter for –16 and –20 speed sorts

Parameter	Read Latency	Symbol	Limit Values				Unit	Note
			-16		-20			
			min	max	min	max		
Clock DLL off mode								
System Frequency	9	f_{CK9}	100	350	100	350	MHz	
	8	f_{CK8}	100	350	100	350	MHz	
	7	f_{CK7}	100	350	100	350	MHz	

4.14.2 Initialization in DLL off mode

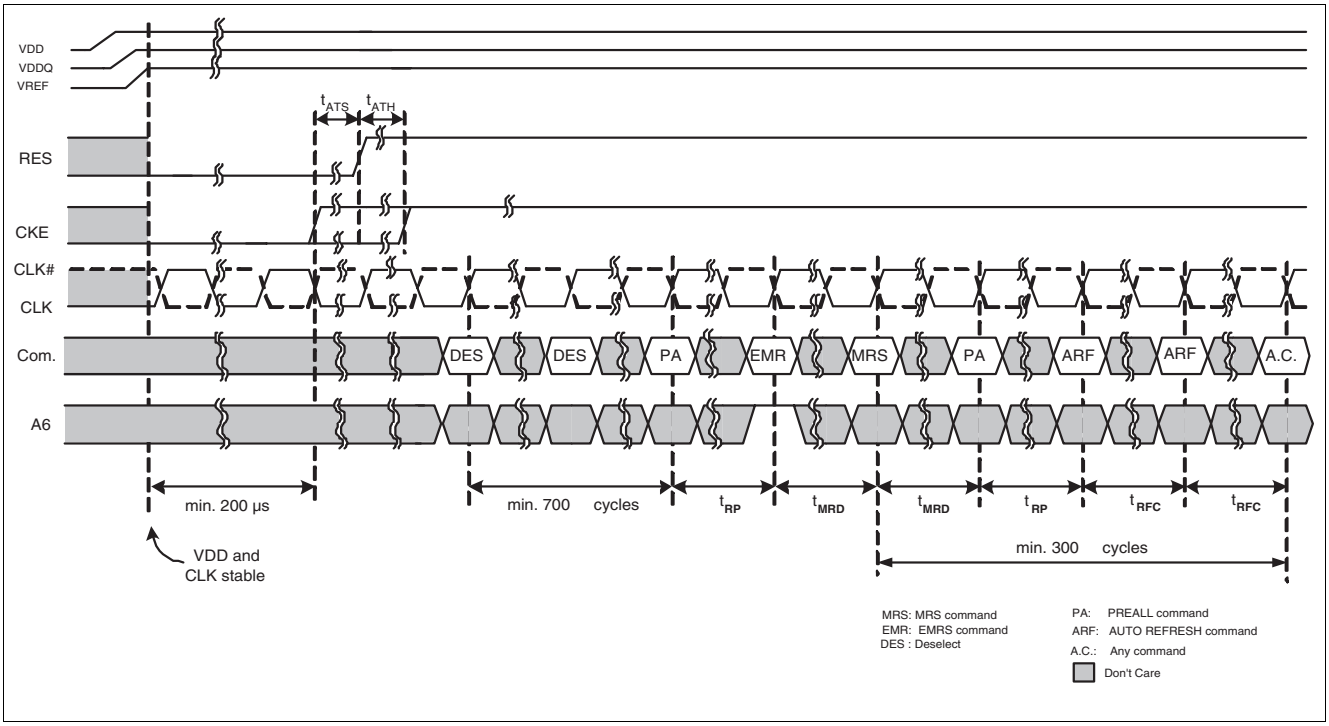

Figure 60 DLL off: Power Up Sequence

4.14.3 Writes (WR) in DLL off mode

Table 23 General Timing Parameter

Parameter	Symbol	Limit Values				Unit
		-16		-20		
		min	max	min	max	
Write comm. to the first DQS latching transition	t_{DQSS}	(WL*t_{CK}) - 0.5	(WL*t_{CK}) + 0.5	(WL*t_{CK}) - 0.5	(WL*t_{CK}) + 0.5	ns
Data-in and DM input pulse width (each input)	t_{DIPW}	0.77	—	0.88	—	ns
DQS Write Preamble Time	t_{WPRE}	0.55	—	0.63	—	ns
DQS Write Postamble Time	t_{WPST}	0.88	1.32	1.0	1.5	ns
Write to Read	t_{WTR}	8	—	8	—	ns
Write to Precharge	t_{WR}	14	—	14	—	ns

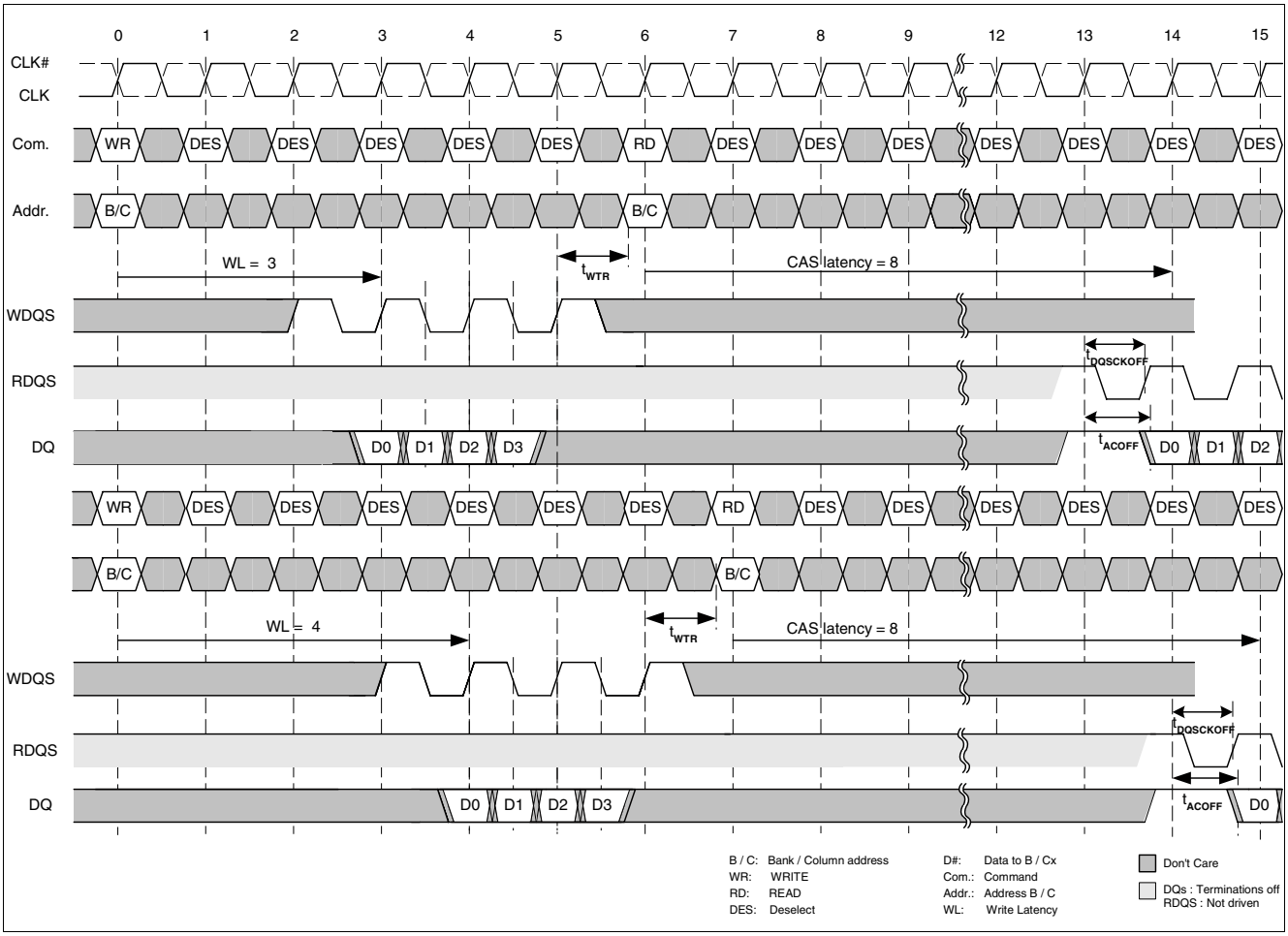

Figure 61 DLL off: Write followed by Read

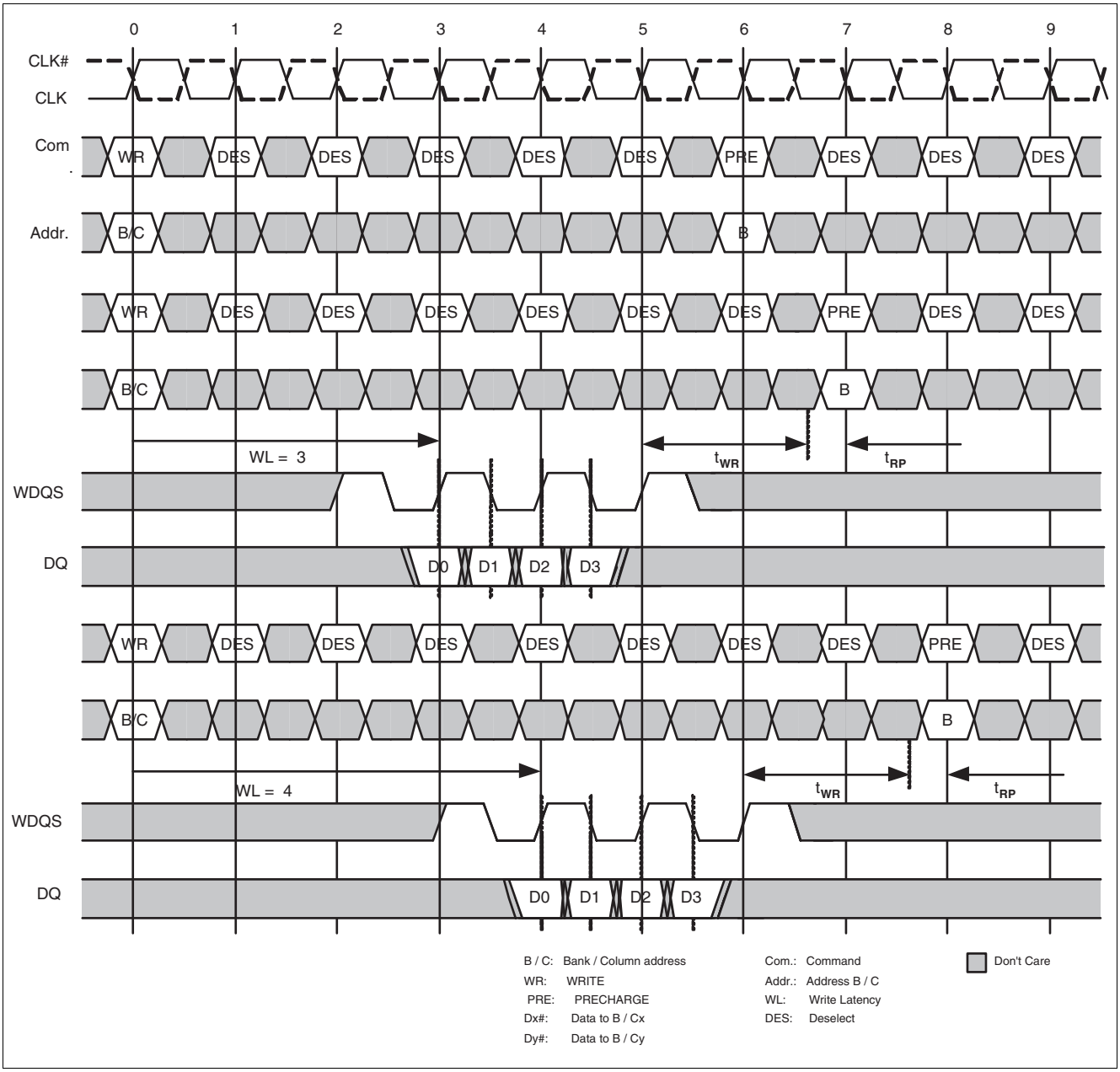

Figure 62 Write followed by Precharge

4.14.4 Reads (RD) in DLL off mode

Definition of read latency in DLL off mode is different from DLL on mode. Since in DLL off mode the read data is not synchronized to the CLK, the internal access time to the memory array becomes visible. Read data in DLL off mode appears on the I/O balls after (CL - 1) + t_{AC}. CL is the value for the read latency which is set in the Mode Register.

Table 24 Read Timing Parameter

Parameter	Read Latency	Symbol	Limit Values				Unit	Note
			-16		-20			
			min	max	min	max		
Read to Write command delay		t_{RTW}	$t_{RTW(min)}$ = (CL+4-WL)				t_{CK}	
Read Cycle Timing Parameters for Data and Data Strobe								
Data Access Time from Clock in DLL off mode		t_{ACOFF}	2.4	6.2	2.4	6.2	ns	
DQS edge to Clock edge skew in DLL off mode		t_{DQSCK}	2.4	6.2	2.4	6.2	ns	

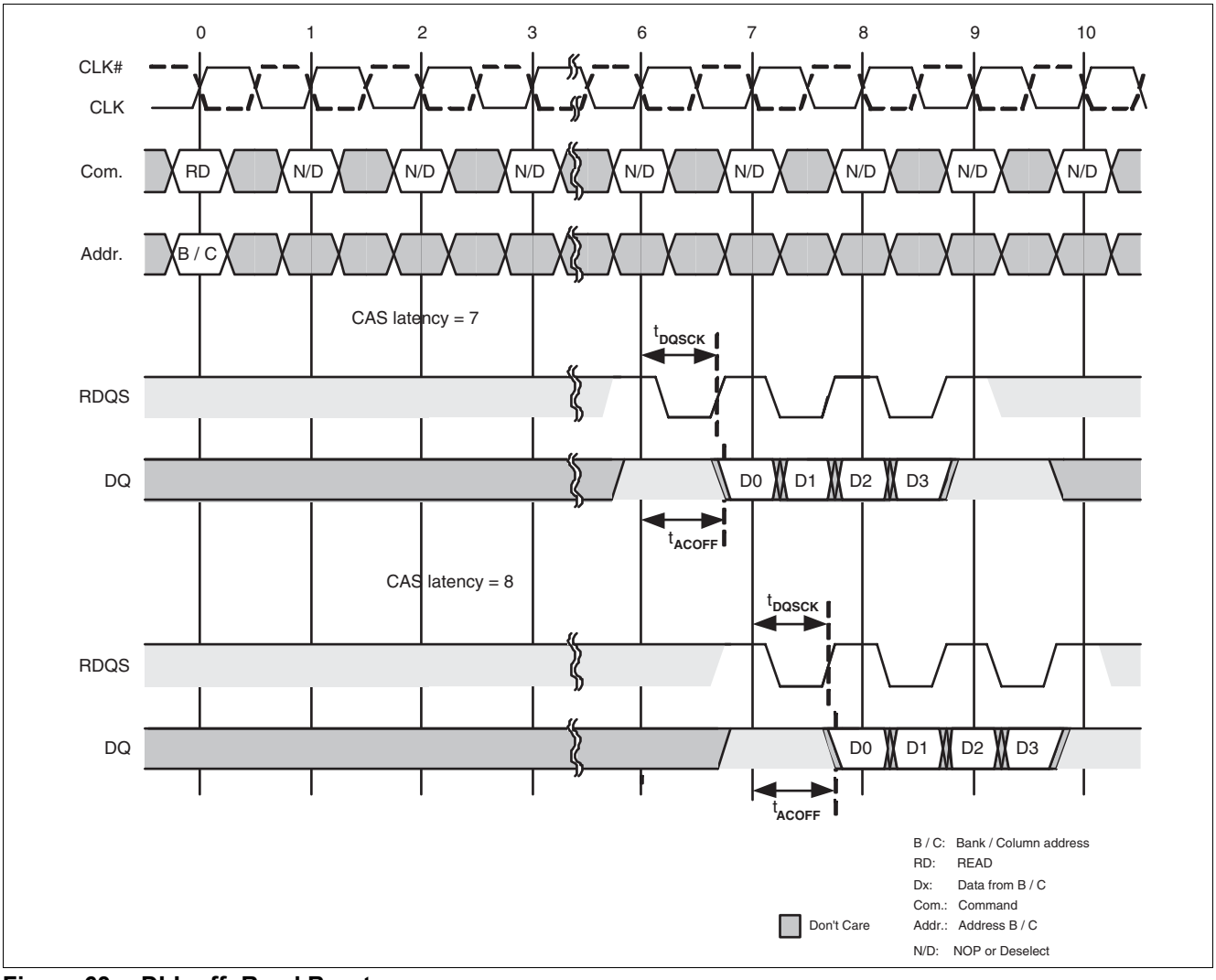

Figure 63 DLL off: Read Burst

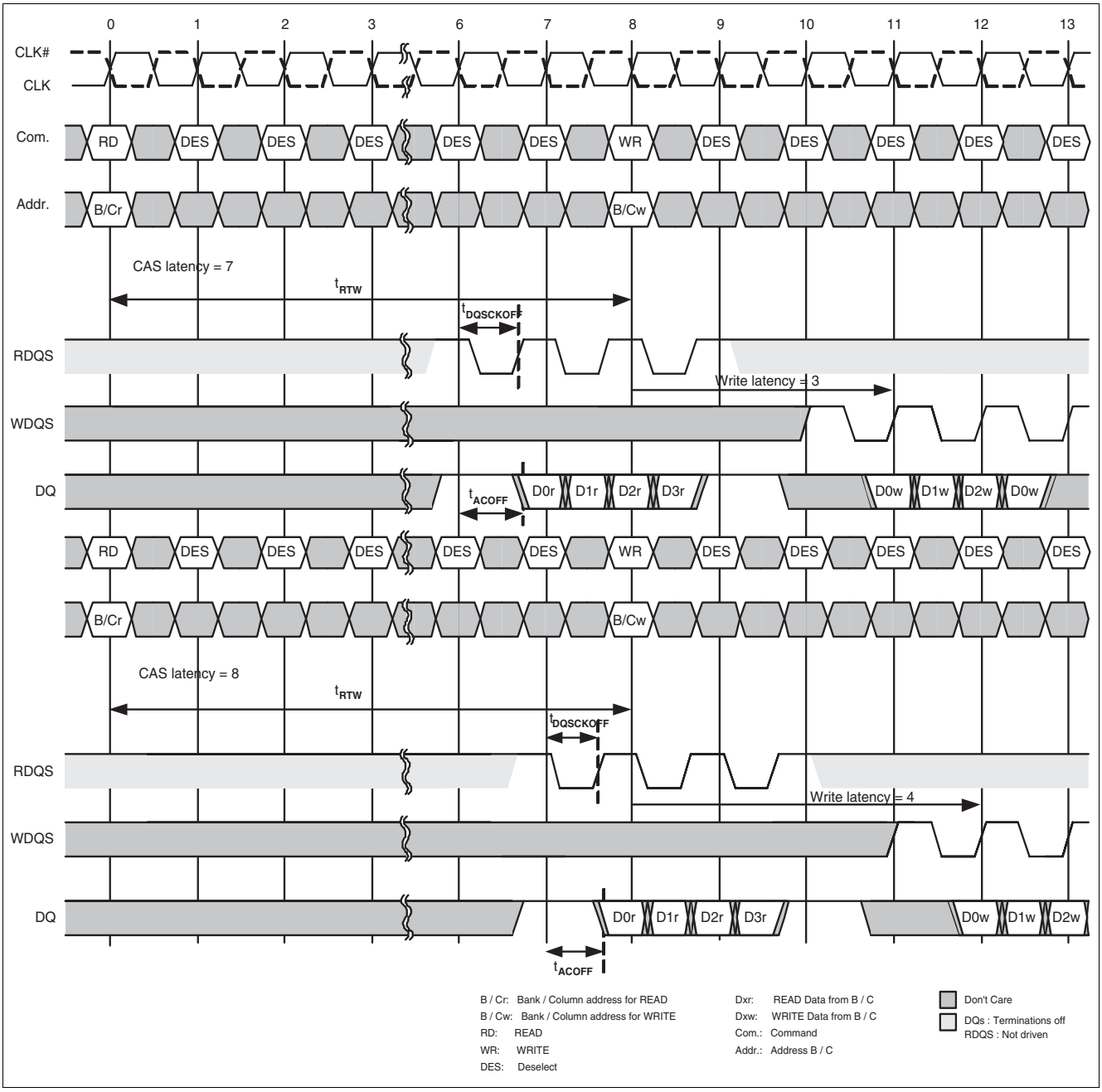

Figure 64 DLL off: Read followed by Write

4.14.5 Self Refresh in DLL off mode

Self Refresh in DLL off mode is basically the same like in DLL on mode.

Table 25 Self Refresh Exit Timing Parameter

Parameter	Read Latency	Symbol	Limit Values				Unit	Note
			-16		-20			
			min	max	min	max		
Self Refresh Exit Time		t_{XSC}	700	—	700	—	t_{CK}	

5 Electrical Characteristics

5.1 Absolute Maximum Ratings and Operation Conditions

Table 26 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit
		min.	max.	
Power Supply Voltage	V_{DD}	-0.5	2.5	V
Power Supply Voltage for Output Buffer	V_{DDQ}	-0.5	2.5	V
Input Voltage	V_{IN}	-0.5	2.5	V
Output Voltage	V_{OUT}	-0.5	2.5	V
Storage Temperature	T_{STG}	-55	+150	°C
Junction Temperature	T_J		+125	°C
Short Circuit Output Current	I_{OUT}	—	50	mA

Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.2 DC Operation Conditions

5.2.1 Recommended Power & DC Operation Conditions.

Table 27 Power & DC Operation Conditions.(0 °C ≤ T_c ≤ 85 °C)

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Power Supply Voltage	V_{DD}, V_{DDA}	1.9	2.0	2.1	V	1)2)
Power Supply Voltage for I/O Buffer	V_{DDQ}	1.9	2.0	2.1	V	1)2)
Power Supply Voltage	V_{DD}, V_{DDA}	1.7	1.8	1.9	V	1)3)
Power Supply Voltage for I/O Buffer	V_{DDQ}	1.7	1.8	1.9	V	1)3)
Reference Voltage	V_{REF}	0.69*V_{DDQ}	—	0.71*V_{DDQ}	V	4)
Output Low Voltage	$V_{OL(DC)}$	—	—	0.8	V	
Input leakage current	I_{IL}	–5.0	—	+5.0	µA	5)
CLK Input leakage current	I_{ILC}	–5.0	—	+5.0	µA	
Output leakage current	I_{OL}	–5.0	—	+5.0	µA	5)

1) V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
2) HYB18H512321AF–12/14/16/20
3) HYB18H512321AFL14/16/20
4) V_{REF} is expected to equal 70% of V_{DDQ} for the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ±2% V_{REF} (DC). Thus, from 70% of V_{DDQ}, V_{REF} is allowed ± 19mV for DC error and an additionnal ± 27mV for AC noise.
5) I_{IL} and I_{OL} are measured with ODT disabled.

5.3 DC & AC Logic Input Levels

5.4 Differential Clock DC and AC Levels

Table 28 DC & AC Logic Input Levels (0 °C ≤ T_c ≤ 85 °C)

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input logic high voltage, DC	V_{IH}(DC)	V_{REF} + 0.15	—	V	1)
Input logic low voltage, DC	V_{IL}(DC)	—	V_{REF} -0.15	V	1)
Input logic high voltage, AC	V_{IH}(AC)	V_{REF} + 0.25	—	V	2),3)
Input logic low voltage, AC	V_{IL}(AC)	—	V_{REF} - 0.25	V	2),3)
Input logic high, DC, RESET pin	V_{IHR}(DC)	0.65.V_{DDQ}	V_{DDQ} + 0.3	V	
Input logic low, DC, RESET pin	V_{ILR}(DC)	-0.3	0.35.V_{DDQ}	V	
Input Logic High, DC, MF pin	V_{IHMF}(DC)	V_{DD}	V_{DD} + 0.3	V	4)
Input Logic Low,DC, MF pin	V_{ILMF}(DC)	–0.3	0	V	

1) The DC values define where the input slew rate requirements are imposed, and the input signal must not violate these levels in order to maintain a valid level.
2) Input slew rate = 3V/ns. If the input slew rate is less than 3V/ns, input timing may be compromised. All slew rates are measured between V_{IL}(DC) and V_{IH}(DC).
3) V_{IH} overshoot : V_{IH}(max) = V_{DDQ}+0.5V for a pulse width ≤ 500ps and the pulse width cannot be greater than 1/3 of the cycle rate. V_{IL} undershoot: V_{IL}(min) = 0V for a pulse width ≤ 500ps and the pulse width cannot be greater than 1/3 of the cycle rate.
4) The MF pin must be hard-wired on board to either V_{DD} or V_{SS}.

Table 29 Differential Clock DC and AC Input conditions (0 °C ≤ T_c ≤ 85 °C)

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Clock Input Mid-Point Voltage, CLK and $\overline{CLK}$	$V_{MP(DC)}$	0.7 × V_{DDQ} – 0.10	0.7 × V_{DDQ} + 0.10	V	1)
Clock Input Voltage Level, CLK and $\overline{CLK}$	$V_{IN(DC)}$	0.42	V_{DDQ} + 0.3	V	1)
Clock DC Input Differential Voltage, CLK and $\overline{CLK}$	$V_{ID(DC)}$	0.3	V_{DDQ}	V	1)
Clock AC Input Differential Voltage, CLK and $\overline{CLK}$	$V_{ID(AC)}$	0.5	V_{DDQ} + 0.5	V	1)2)
AC Differential Crossing Point Input Voltage	$V_{IX(AC)}$	0.7 × V_{DDQ} – 0.15	0.7 × V_{DDQ} + 0.15	V	1)3)

1) All voltages referenced to V_{SS}.
2) V_{ID} is the magnitude of the difference between the input level on CLK and the input level on $\overline{CLK}$.
3) The value of V_{IX} is expected to equal 0.7 × V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

5.5 Output Test Conditions

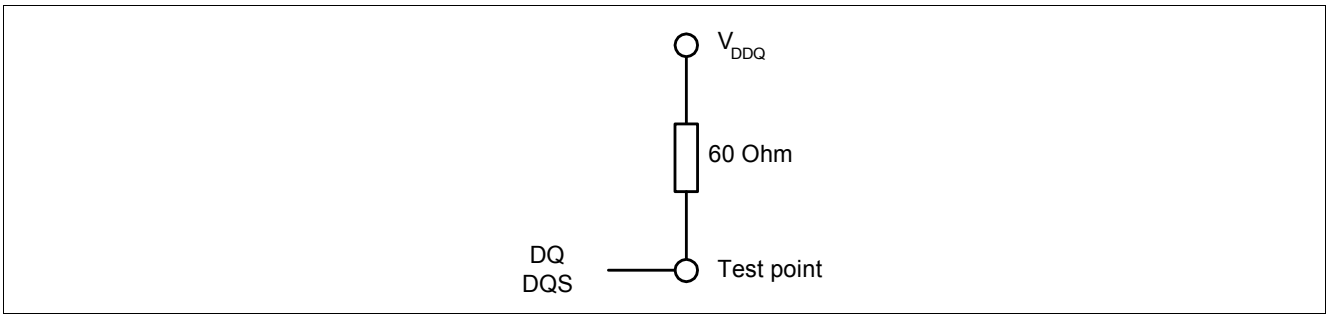

Figure 65 Output Test Circuit

5.6 Pin Capacitances

Table 30 Pin Capacitances (VDDQ = 1.8V, TA = 25°C, f= 1MHz)

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance: A0-A11, BA0-2,CKE, $\overline{CS}$, $\overline{CAS}$, $\overline{RAS}$, $\overline{WE}$, CKE, RES,CLK,CLK	CI,CCK	1.5	2.5	pF	
Input capacitance: DQ0-DQ31, RDQS0-RDQS3, WDQS0-WDQS3, DM0-DM3	CIO	2.5	3.5	pF	

5.7 Driver current characteristics

5.7.1 Driver IV characteristics at 40 Ohms

Figure 66 represents the driver Pull-Down and Pull-Up IV characteristics under process, voltage and temperature best and worst case conditions. The actual Driver Pull-Down and Pull-Up current must lie between these two bounding curves. The value of the external ZQ resistor is 240 Ω, setting the nominal driver output impedance to 40 Ω.

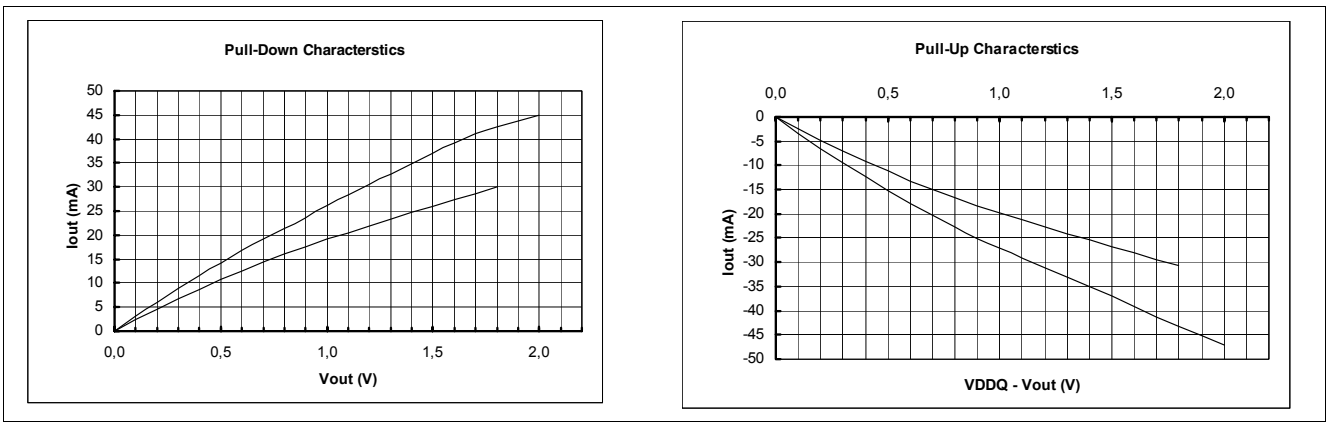

Figure 66 40 Ohm Driver Pull-Down and Pull-Up characteristics

Table 31 lists the numerical values of the minimum and maximum allowed values of the output driver Pull-Down and Pull-Up IV characteristics.

Table 31 Programmed Driver IV Characterisitcs at 40 Ohm

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Minimum	Maximum	Minimum	Maximum
0.1	2.32	3.04	-2.44	-3.27
0.2	4.56	5.98	-4.79	-6.42
0.3	6.69	8.82	-7.03	-9.45
0.4	8.74	11.56	-9.18	-12.37
0.5	10.70	14.19	-11.23	-15.17
0.6	12.56	16.72	-13.17	-17.83
0.7	14.34	19.14	-15.01	-20.37
0.8	16.01	21.44	-16.74	-22.78
0.9	17.61	23.61	-18.37	-25.04
1.0	19.11	26.10	-19.90	-27.17
1.1	20.53	28.45	.21.34	-29.17
1.2	21.92	30.45	-22.72	-31.25
1.3	23.29	32.73	-24.07	-33.00
1.4	24.65	34.95	-25.40	-35.00
1.5	26.00	37.10	-26.73	-37.00
1.6	27.35	39.15	-28.06	-39.14
1.7	28.70	41.01	-29.37	-41.25
1.8	30.08	42.53	-30.66	-43.29
1.9	—	43.71	—	-45.23
2.0	—	44.89	—	-47.07

5.7.2 Termination IV Characteristic at 60 Ohms

Figure 67 represents the DQ termination Pull-Up IV characteristic under process, voltage and temperature best and worst case conditions. The actual DQ termination Pull-Up current must lie between these two bounding curves. The value of the external ZQ resistor is 240 Ω, setting the nominal DQ termination impedance to 60 Ω. (Extended Mode Register programmed to ZQ/4).

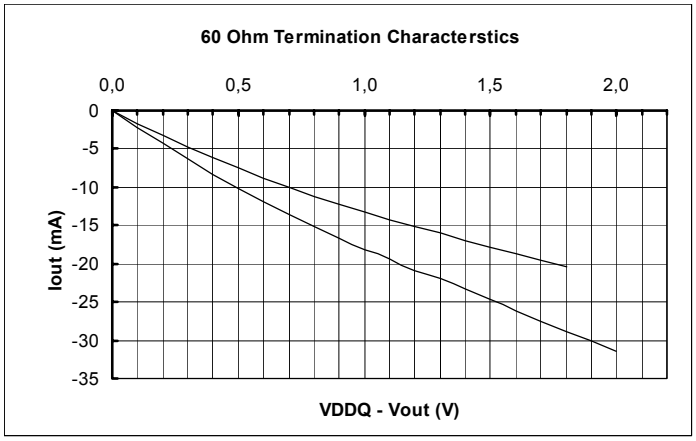

Figure 67 60 Ohm Active Termination Characteristic

Table 32 lists the numerical values of the minimum and maximum allowed values of the output driver termination IV characteristic.

Table 32 Programmed Terminator Characteristics at 60 Ohm

Voltage (V)	Terminator Pull-Up Current (mA)		Voltage (V)	Terminator Pull-Up Current (mA)	
	Minimum	Maximum		Minimum	Maximum
0.1	-1.63	-2.18	1.1	-14.23	-19.45
0.2	-3.19	-4.28	1.2	-15.14	-20.83
0.3	-4.69	-6.30	1.3	-16.04	-22.00
0.4	-6.12	-8.25	1.4	-16.94	-23.33
0.5	-7.49	-10.11	1.5	-17.82	-24.67
0.6	-8.78	-11.89	1.6	-18.70	-26.09
0.7	-10.01	-13.58	1.7	-19.58	-27.50
0.8	-11.16	-15.19	1.8	-20.44	-28.86
0.9	-12.25	-16.69	1.9	—	-30.15
1.0	-13.27	-18.11	2.0	—	-31.38

5.8 Termination IV Characteristic at 120 Ohms

Figure 68 represents the DQ or ADD/CMD termination Pull-Up IV characteristic under process, voltage and temperature best and worst case conditions. The actual termination Pull-Up current must lie between these two bounding curves. The value of the external ZQ resistor is 240 Ω, setting the nominal termination impedance to 120 Ω. (Extended Mode Register programmed to ZQ/2 for DQ terminations or CKE = 0 at the RES transition during Power-Up for ADD/CMD terminations).

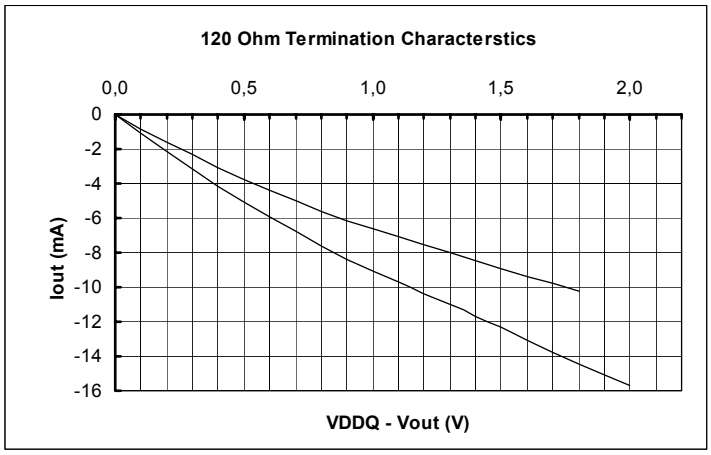

Figure 68 120 Ohm Active Termination Characteristics

Table 33 lists the numerical values of the minimum and maximum allowed values of the termination IV characteristic.

Table 33 Programmed Terminator Characteristics af 120 Ohm

Voltage (V)	Terminator Pull-Up Current (mA)			Voltage (V)	Terminator Pull-Up Current (mA)	
	Minimum	Maximum			Minimum	Maximum
0.1	-0.81	-1.09		1.1	-7.11	-9.72
0.2	-1.60	-2.14		1.2	-7.57	-10.42
0.3	-2.34	-3.15		1.3	-8.02	-11.00
0.4	-3.06	-4.12		1.4	-8.47	-11.67
0.5	-3.74	-5.06		1.5	-8.91	-12.33
0.6	-4.39	-5.94		1.6	-9.35	-13.05
0.7	-5.00	-6.79		1.7	-9.79	-13.75
0.8	-5.58	-7.59		1.8	-10.22	-14.43
0.9	-6.12	-8.35		1.9	—	-15.08
1.0	-6.63	-9.06		2.0	—	-15.69

5.9 Termination IV Characteristic at 240 Ohms

Figure 69 represents the ADD/CMD termination Pull-Up IV characteristic under process, voltage and temperature best and worst case conditions. The actual ADD/CMD termination Pull-Up current must lie between these two bounding curves. The value of the external ZQ resistor is 240 Ω, setting the nominal termination impedance to 240 Ω. (CKE = 1at the RES transition during Power-Up for ADD/CMD terminations).

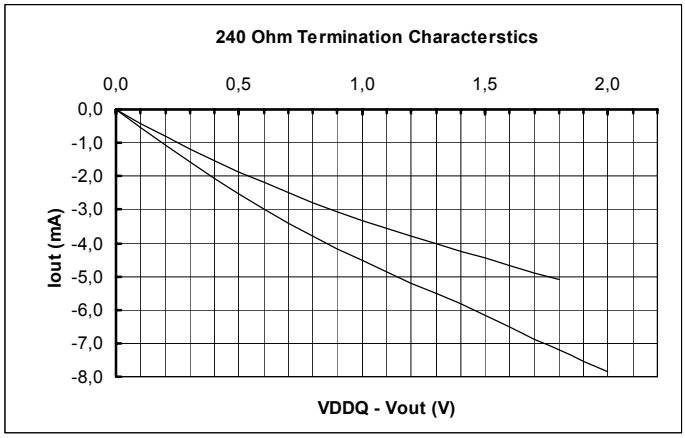

Figure 69 240 Ohm Active Termination Characteristic

Table 34 lists the numerical values of the minimum and maximum allowed values of the ADD/CMD termination IV characteristic.

Table 34 Programmed Terminator Characteristic at 240 Ohm

Voltage (V)	Terminator Pull-Up Current (mA)			Voltage (V)	Terminator Pull-Up Current (mA)	
	Minimum	Maximum			Minimum	Maximum
0.1	-0.41	-0.55		1.1	-3.56	-4.86
0.2	-0.80	-1.07		1.2	-3.79	-5.21
0.3	-1.17	-1.58		1.3	-4.01	-5.50
0.4	-1.53	-2.06		1.4	-4.23	-5.83
0.5	-1.87	-2.53		1.5	-4.46	-6.17
0.6	-2.20	-2.97		1.6	-4.68	-6.52
0.7	-2.50	-3.40		1.7	-4.90	-6.88
0.8	-2.79	-3.80		1.8	-5.11	-7.21
0.9	-3.06	-4.17		1.9	—	-7.54
1.0	-3.32	-4.53		2.0	—	-7.85

5.10 Operating Currents

5.10.1 Operating Current Ratings (HYB18H512321AF–12/14/16/20)

Table 35 Operating Current Ratings (0 °C ≤ Tc ≤ 85 °C)

Parameter	Symbol	Values				Unit	Notes
		–12	–14	–16	–20		
		typ.	typ.	typ.	typ.		
Operating Current	I_{DD0}	498	453	406	362	mA	1),2),3)
Operating Current	I_{DD1}	463	425	383	348	mA	1),2),3)
Precharge Power-Down Standby Current	I_{DD2P}	271	243	215	186	mA	1),2),3)
Precharge Floating Standby Current	I_{DD2F}	352	316	280	243	mA	1),2),3)
Precharge Quiet Standby Current	I_{DD2Q}	319	287	254	221	mA	1),2),3)
Active Power-Down Standy Current	I_{DD3P}	272	244	216	187	mA	1),2),3)
Active Standby Current	I_{DD3N}	456	411	364	317	mA	1),2),3)
Operating Current Burst Read	I_{DD4R}	805	725	642	558	mA	1),2),3)
Operating Current Burst Write	I_{DD4W}	641	581	511	445	mA	1),2),3)
Auto-Refresh Current (t_{RC}=min(t_{RFC}))	I_{DD5B}	587	548	500	409	mA	1),2),3)
Auto-Refresh Current at t_{REFI}	I_{DD5D}	408	366	324	281	mA	1),2),3)
Self Refresh Current	I_{DD6}	8	8	8	8	mA	1),2),3),4)
Operating Current	I_{DD7}	733	703	671	641	mA	1),2),3)

1) IDD specifications are tested after the device is properly initialized.
2) Input slew rate = 3V/ns.
3) Measured with Output open and On Die termination off.
4) Enables on-chip refresh and address counter.

5.10.2 Operating Current Ratings (HYB18H512321AFL14/16/20)

Table 36 Operating Current Ratings (0 °C ≤ Tc ≤ 85 °C)

Parameter	Symbol	Values			Unit	Notes
		–14	–16	–20		
		typ.	typ.	typ.		
Operating Current	I_{DD0}	406	367	328	mA	1),2),3)
Operating Current	I_{DD1}	384	346	315	mA	1),2),3)
Precharge Power-Down Standby Current	I_{DD2P}	218	192	167	mA	1),2),3)
Precharge Floating Standby Current	I_{DD2F}	283	250	218	mA	1),2),3)
Precharge Quiet Standby Current	I_{DD2Q}	257	228	199	mA	1),2),3)
Active Power-Down Standy Current	I_{DD3P}	220	195	169	mA	1),2),3)
Active Standby Current	I_{DD3N}	369	328	286	mA	1),2),3)
Operating Current Burst Read	I_{DD4R}	648	610	501	mA	1),2),3)
Operating Current Burst Write	I_{DD4W}	521	466	403	mA	1),2),3)
Auto-Refresh Current (t_{RC}=min(t_{RFC}))	I_{DD5B}	514	472	386	mA	1),2),3)
Auto-Refresh Current at t_{REFI}	I_{DD5D}	328	290	252	mA	1),2),3)
Self Refresh Current	I_{DD6}	8	8	8	mA	1),2),3),4)
Operating Current	I_{DD7}	654	627	600	mA	1),2),3)

1) IDD specifications are tested after the device is properly initialized.
2) Input slew rate = 3V/ns.
3) Measured with Output open and On Die termination off.
4) Enables on-chip refresh and address counter.

5.11 Operating Current Measurement Conditions

Table 37 Operating Current Measurement Conditions

Symbol	Parameter/Condition
I_{DD0}	Operating Current - One bank, Activate - Precharge t_{CK}=min(t_{CK}), t_{RC}=min(t_{RC}) Databus inputs are SWITCHING; Address and control inputs are SWITCHING, $\overline{CS}$ = HIGH between valid commands.
I_{DD1}	Operating Current - One bank, Activate - Read - Precharge One bank is accessed with t_{CK}=min(t_{CK}), t_{RC}=min(t_{RC}), CL = CL(min), Address and control inputs are SWITCHING; $\overline{CS}$ = HIGH between valid commands. I_{out}=0mA
I_{DD2P}	Precharge Power-Down Standby Current All banks idle, power-down mode, CKE is LOW, t_{CK}=min(t_{CK}), Data bus inputs are STABLE (HIGH).
I_{DD2F}	Precharge Floating Standby Current All banks idle; $\overline{CS}$ is HIGH, CKE is HIGH, t_{CK}=min(t_{CK}); Address and control inputs are SWITCHING; Data bus input are STABLE (HIGH).
I_{DD2Q}	Precharge Quiet Standby Current $\overline{CS}$ is HIGH, all banks idle, CKE is HIGH, t_{CK}=min(t_{CK}), Address and other control inputs STABLE (HIGH), Data bus inputs are STABLE (HIGH).
I_{DD3P}	Active Power-Down Standby Current One bank active, CKE is LOW, Address and control inputs are STABLE (HIGH); Data bus inputs are STABLE (HIGH); standard active power-down mode.
I_{DD3N}	Active Standby Current One bank active, $\overline{CS}$ is HIGH, CKE is HIGH, t_{RAS}= $t_{RAS,max}$, t_{CK}=min(t_{CK}); Address and control inputs are SWITCHING; Data bus inputs are SWITCHING.
I_{DD4R}	Operating Current - Burst Read One bank active; Continuous read bursts, CL = CL(min); t_{CK}=min(t_{CK}); t_{RAS}= $t_{RAS,max}$; Address and control inputs are SWITCHING; Iout = 0 mA.
I_{DD4W}	Operating Current - Burst Write One bank active; Continuous write bursts; t_{CK}=min(t_{CK}); Address and control inputs are SWITCHING; Data bus inputs are SWITCHING.
I_{DD5B}	Burst Auto Refresh Current Refresh command at t_{RFC}=min(t_{RFC}); t_{CK}=min(t_{CK}); CKE is HIGH, $\overline{CS}$ is HIGH between all valid commands; Other command and address inputs are SWITCHING; Data bus inputs are SWITCHING.
I_{DD5D}	Distributed Auto Refresh Current t_{CK}=t_{CKmin}; Refresh command every t_{REFI}; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other command and address inputs are SWITCHING; Data bus inputs are SWITCHING.
I_{DD6}	Self Refresh Current CKE ≤ max(V_{IL}), external clock off, CK and $\overline{CK}$ LOW; Address and control inputs are STABLE (HIGH); Data Bus inputs are STABLE (HIGH).
I_{DD7}	Operating Bank Interleave Read Current 1. All banks interleaving with CL = CL(min); t_{RCD} = t_{RCDRD}(min); t_{RRD} = t_{RRD}(min); I_{out}=0 mA; Address and control inputs are STABLE (HIGH) during DESELECT; Data bus inputs are SWITCHING. 2: Timing pattern: tbd.

1. *0 °C ≤ Tc ≤ 85 °C*
2. *Data Bus consists of DQ, DM, WDQS.*

3. *Definitions for IDD :*
   LOW is defined as VIN = 0.4 × VDDQ; HIGH is defined as V_{IN} = V_{DDQ};
   TABLE is defined as inputs are stable at a HIGH level.
   SWITCHING is defined as inputs are changing between HIGH and LOW every clock cycle for address and control signals, and inputs changing 50% of each data transfer for DQ signals.
4. *Legend: A=Active; RA=Read with Autoprecharge; D=DESELECT.*

5.12 AC Timings (HYB18H512321AF–12/14/16/20)

Table 38 Timing Parameters (HYB18H512321AF–12/14/16/20)

Parameter	CAS latency	Symbol	Limit Values								Unit	
			–12		–14		–16		–20			
			min	max	min	max	min	max	min	max		
Clock and Clock Enable												
System frequency	CL= 11	f_{CK11}	350[1)]	800	350[1)]	700					MHz	
	CL =10	f_{CK10}	350[1)]	700	350[1)]	650	350[1)]	600			MHz	
	CL = 9	f_{CK9}	350[1)]	650	350[1)]	600	350[1)]	550			MHz	
	CL = 8	f_{CK8}	350[1)]	550	350[1)]	500	350[1)]	500	350[1)]	500	MHz	
	CL = 7	f_{CK7}	350[1)]	500	350[1)]	450	350[1)]	450	350[1)]	450	MHz	
Clock high level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Clock low level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Minimum clock half period		t_{HP}	0.45	—	0.45	—	0.45	—	0.45	—	t_{CK}	2)
Command and Address Setup and Hold Timing												
Address/Command input setup time		t_{IS}	0.3	—	0.35	—	0.4	—	0.5	—	ns	
Address/Command input hold time		t_{IH}	0.3	—	0.35	—	0.4	—	0.5	—	ns	
Address/Command input pulse width		t_{IPW}	0.7	—	0.7	—	0.7	—	0.7	—	t_{CK}	
Mode Register Set Timing												
Mode Register Set cycle time		t_{MRD}	6	—	6	—	6	—	6	—	t_{CK}	3)4)
Mode Register Set to READ timing		t_{MRDR}	12	—	12	—	12	—	12	—	t_{CK}	3)
Row Timing												
Row Cycle Time		t_{RC}	32	—	30	—	27	—	23	—	tck	
Row Active Time		t_{RAS}	21	—	18	—	17	—	14	—	tck	5)
ACT(a) to ACT(b) Command period		t_{RRD}	8	—	7	—	6	—	5	—	tck	
Row Precharge Time		t_{RP}	13	—	12	—	11	—	9	—	tck	
Row to Column Delay Time for Reads		t_{RCDRD}	12	—	11	—	10	—	8	—	tck	
Row to Column Delay Time for Writes		t_{RCDWR}	$t_{RCDWR(min)} = t_{RCDRD(min)} - (WL + 1) \times t_{CK}$								tck	
Column Timing												
CAS(a) to CAS(b) Command period		t_{CCD}	2	—	2	—	2	—	2	—	t_{CK}	6)
Write to Read Command Delay		t_{WTR}	6	—	5	—	5	—	4	—	tck	7)
Read to Write command delay		t_{RTW}	t_{RTW}(min)= (CL + BL/2 +2 -WL)								t_{CK}	8)
Write Cycle Timing Parameters for Data and Data Strobe												
Write command to first WDQS latching transition		t_{DQSS}	WL–0.25	WL+0.25	WL–0.25	WL+0.25	WL–0.25	WL+0.25	WL -0.25	WL+0.25	t_{CK}	

Table 38 Timing Parameters (HYB18H512321AF–12/14/16/20)

Parameter	CAS latency	Symbol	Limit Values								Unit	
			–12		–14		–16		–20			
			min	max	min	max	min	max	min	max		
Data-in and Data Mask to WDQS Setup Time		t_{DS}	0.16	—	0.18	—	0.20	—	0.24	—	ns	
Data-in and Data Mask to WDQS Hold Time		t_{DH}	0.16	—	0.18	—	0.20	—	0.24	—	ns	
Data-in and DM input pulse width (each input)		t_{DIPW}	0.40	—	0.40	—	0.40	—	0.40	—	t_{CK}	
DQS input low pulse width		t_{DQSL}	0.40	—	0.40	—	0.40	—	0.40	—	t_{CK}	
DQS input high pulse width		t_{DQSH}	0.40	—	0.40	—	0.40	—	0.40	—	t_{CK}	
DQS Write Preamble Time		t_{WPRE}	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
DQS Write Postamble Time		t_{WPST}	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
Write Recovery Time		t_{WR}	9	—	8	—	7	—	6	—	t_{CK}	7)
Read Cycle Timing Parameters for Data and Data Strobe												
Data Access Time from Clock		t_{AC}	-0.22	0.22	–0.25	0.25	–0.28	0.28	–0.35	0.35	ns	
Read Preamble		t_{RPRE}	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
Read Postamble		t_{RPST}	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
Data-out high impedance time from CLK		t_{HZ}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	ns	
Data-out low impedance time from CLK		t_{LZ}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	ns	
DQS edge to Clock edge skew		t_{DQSCK}	-0.22	0.22	–0.25	0.25	–0.28	0.28	–0.35	0.35	ns	
DQS edge to output data edge skew		t_{DQSQ}	—	0.140	—	0.160	—	0.180	—	0.225	ns	9)
Data hold skew factor		t_{QHS}	—	0.140	—	0.160	—	0.180	—	0.225	ns	
Data output hold time from DQS		t_{QH}	$t_{HP}-t_{QHS}$		$t_{HP}-t_{QHS}$		$t_{HP}-t_{QHS}$		$t_{HP}-t_{QHS}$		ns	
Refresh/Power Down Timing												
Refresh Period (8192 cycles)		t_{REF}	—	32	—	32	—	32	—	32	ms	
Average periodic Auto Refresh interval		t_{REFI}	3.9		3.9		3.9		3.9		µs	
Delay from AREF to next ACT/ AREF		t_{RFC}	52.0	—	52.0	—	52.8	—	54	—	ns	
Self Refresh Exit time		t_{XSC}	1000	—	1000	—	1000	—	1000	—	t_{CK}	
Power Down Exit time		t_{XPN}	7	—	6	—	5	—	4	—	t_{CK}	
Other Timing Parameters												
RES to CKE setup timing		t_{ATS}	10	—	10	—	10	—	10	—	ns	
RES to CKE hold timing		t_{ATH}	10	—	10	—	10	—	10	—	ns	
Termination update Keep Out timing		t_{KO}	10	—	10	—	10	—	10	—	ns	

Table 38 Timing Parameters (HYB18H512321AF–12/14/16/20)

Parameter	CAS latency	Symbol	Limit Values								Unit	
			–12		–14		–16		–20			
			min	max	min	max	min	max	min	max		
Rev. ID EMRS to DQ on timing		t_{RIDon}	—	20	—	20	—	20	—	20	ns	
REV. ID EMRS to DQ off timing		t_{RIDoff}	—	20	—	20	—	20	—	20	ns	

1) DLLon mode
2) t_{HP} is the lesser of t_{CL} minimum and t_{CH} minimum actually applied to the device CLK, $\overline{CLK}$ inputs
3) This value of tMRD applies only to the case where the 'DLL reset ' bit is not activated.
4) tMRD is defined from MRS to any other command then READ.
5) $t_{RAS,max}$ is 8*t_{REFi}
6) t_{CCD} is either for gapless consecutive reads or gapless consecutive writes. BL =4
7) WTR and t_{WR} start at the first rising edge of CLK after the last valid (falling) WDQS edge of the slowest WDQS signal.
8) Please round up t_{RTW} to the next integer of t_{CK}.
9) This parameter is defined per byte.

5.13 AC Timings (HYB18H512321AFL14/16/20)

Table 39 Timing Parameters (HYB18H512321AFL14/16/20)

Parameter	CAS latency	Symbol	Limit values						Unit	Notes
			–14		–16		–20			
			min	max	min	max	min	max		
Clock and Clock Enable										
System frequency	CL = 11	f_{CK11}	350[1)]	700	350[1)]	600			MHz	
	CL = 10	f_{CK10}	350[1)]	650	350[1)]	550	350[1)]	500	MHz	
	CL = 9	f_{CK9}	350[1)]	600	350[1)]	500	350[1)]	450	MHz	
	CL = 8	f_{CK8}	350[1)]	500	350[1)]	450	350[1)]	400	MHz	
	CL = 7	f_{CK7}	350[1)]	450	350[1)]	400	350[1)]	350	MHz	
Clock high level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Clock low level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Minimum clock half period		t_{HP}	0.45	—	0.45	—	0.45	—	t_{CK}	2)
Command and Address Setup and Hold Timing										
Address/Command input setup time		t_{IS}	0.35	—	0.4	—	0.5	—	ns	
Address/Command input hold time		t_{IH}	0.35	—	0.4	—	0.5	—	ns	
Address/Command input pulse width		t_{IPW}	0.7	—	0.7	—	0.7	—	t_{CK}	
Mode Register Set Timing										
Mode Register Set cycle time		t_{MRD}	6	—	6	—	6	—	t_{CK}	
Mode Register Set to READ timing		t_{MRDR}	12	—	12	—	12	—	t_{CK}	
Row Timing										
Row Cycle Time		t_{RC}	30	—	27	—	23	—	t_{CK}	
Row Active Time		t_{RAS}	18	—	17	—	14	—	t_{CK}	3)
ACT(a) to ACT(b) Command period		t_{RRD}	7	—	6	—	5	—	t_{CK}	
Row Precharge Time		t_{RP}	12	—	11	—	9	—	t_{CK}	5)
Row to Column Delay Time for Reads		t_{RCDRD}	11	—	10	—	8	—	t_{CK}	
Row to Column Delay Time for Writes		t_{RCDWR}	$t_{RCDWR(min)} = t_{RCDRD(min)} - (WL + 1) \times t_{CK}$						t_{CK}	
Column Timing										
CAS(a) to CAS(b) Command period		t_{CCD}	2	—	2	—	2	—	t_{CK}	4)
Write to Read Command Delay		t_{WTR}	5	—	5	—	4	—	t_{CK}	5)
Read to Write command delay		t_{RTW}	t_{RTW}(min)= (CL + BL/2 +2 -WL)						t_{CK}	6)
Write Cycle Timing Parameters for Data and Data Strobe										
Write command to first WDQS latching transition		t_{DQSS}	WL–0.25	WL+0.25	WL–0.25	WL+0.25	WL -0.25	WL +0.25	t_{CK}	
Data-in and Data Mask to WDQS Setup Time		t_{DS}	0.18	—	0.20	—	0.24	—	ns	

Table 39 Timing Parameters (HYB18H512321AFL14/16/20)

Parameter	CAS latency	Symbol	Limit values						Unit	Notes
			–14		–16		–20			
			min	max	min	max	min	max		
Data-in and Data Mask to WDQS Hold Time		t_{DH}	0.18	—	0.20	—	0.24	—	ns	
Data-in and DM input pulse width (each input)		t_{DIPW}	0.40	—	0.40	—	0.40	—	t_{CK}	
DQS input low pulse width		t_{DQSL}	0.40	—	0.40	—	0.40	—	t_{CK}	
DQS input high pulse width		t_{DQSH}	0.40	—	0.40	—	0.40	—	t_{CK}	
DQS Write Preamble Time		t_{WPRE}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
DQS Write Postamble Time		t_{WPST}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
Write Recovery Time		t_{WR}	8	—	7	—	6	—	t_{CK}	7)
Read Cycle Timing Parameters for Data and Data Strobe										
Data Access Time from Clock		t_{AC}	–0.25	0.25	–0.28	0.28	–0.35	0.35	ns	
Read Preamble		t_{RPRE}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
Read Postamble		t_{RPST}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
Data-out high impedance time from CLK		t_{HZ}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	ns	
Data-out low impedance time from CLK		t_{LZ}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	ns	
DQS edge to Clock edge skew		t_{DQSCK}	–0.25	0.25	–0.28	0.28	–0.35	0.35	ns	
DQS edge to output data edge skew		t_{DQSQ}	—	0.160	—	0.18	—	0.225	ns	7)
Data hold skew factor		t_{QHS}	—	0.160	—	0.18	—	0.225	ns	
Data output hold time from DQS		t_{QH}	t_{HP}–t_{QHS}		t_{HP}–t_{QHS}		t_{HP}–t_{QHS}		ns	
Refresh/Power Down Timing										
Refresh Period (8192 cycles)		t_{REF}	—	32	—	32	—	32	ms	
Average periodic Auto Refresh interval		t_{REFI}	3.9		3.9		3.9		µs	
Delay from AREF to next ACT/ AREF		t_{RFC}	52.0	—	52.8	—	54	—	ns	
Self Refresh Exit time		t_{XSC}	1000	—	1000	—	1000	—	t_{CK}	
Power Down Exit time		t_{XPN}	6	—	5	—	4	—	t_{CK}	
Other Timing Parameters										
RES to CKE setup timing		t_{ATS}	10	—	10	—	10	—	ns	
RES to CKE hold timing		t_{ATH}	10	—	10	—	10	—	ns	
Termination update Keep Out timing		t_{KO}	10	—	10	—	10	—	ns	
Rev. ID EMRS to DQ on timing		t_{RIDon}	—	20	—	20	—	20	ns	
REV. ID EMRS to DQ off timing		t_{RIDoff}	—	20	—	20	—	20	ns	

1) DLLon mode
2) t_{HP} is the lesser of t_{CL} minimum and t_{CH} minimum actually applied to the device CLK, $\overline{CLK}$ inputs
3) $t_{RAS,max}$ is 8*t_{REFi}

4) t_{CCD} is either for gapless consecutive reads or gapless consecutive writes. BL =4
5) WTR and t_{WR} start at the first rising edge of CLK after the last valid (falling) WDQS edge of the slowest WDQS signal.
6) Please round up t_{RTW} to the next integer of t_{CK}.
7) This parameter is defined per byte.

6 Package

6.1 Package Outline

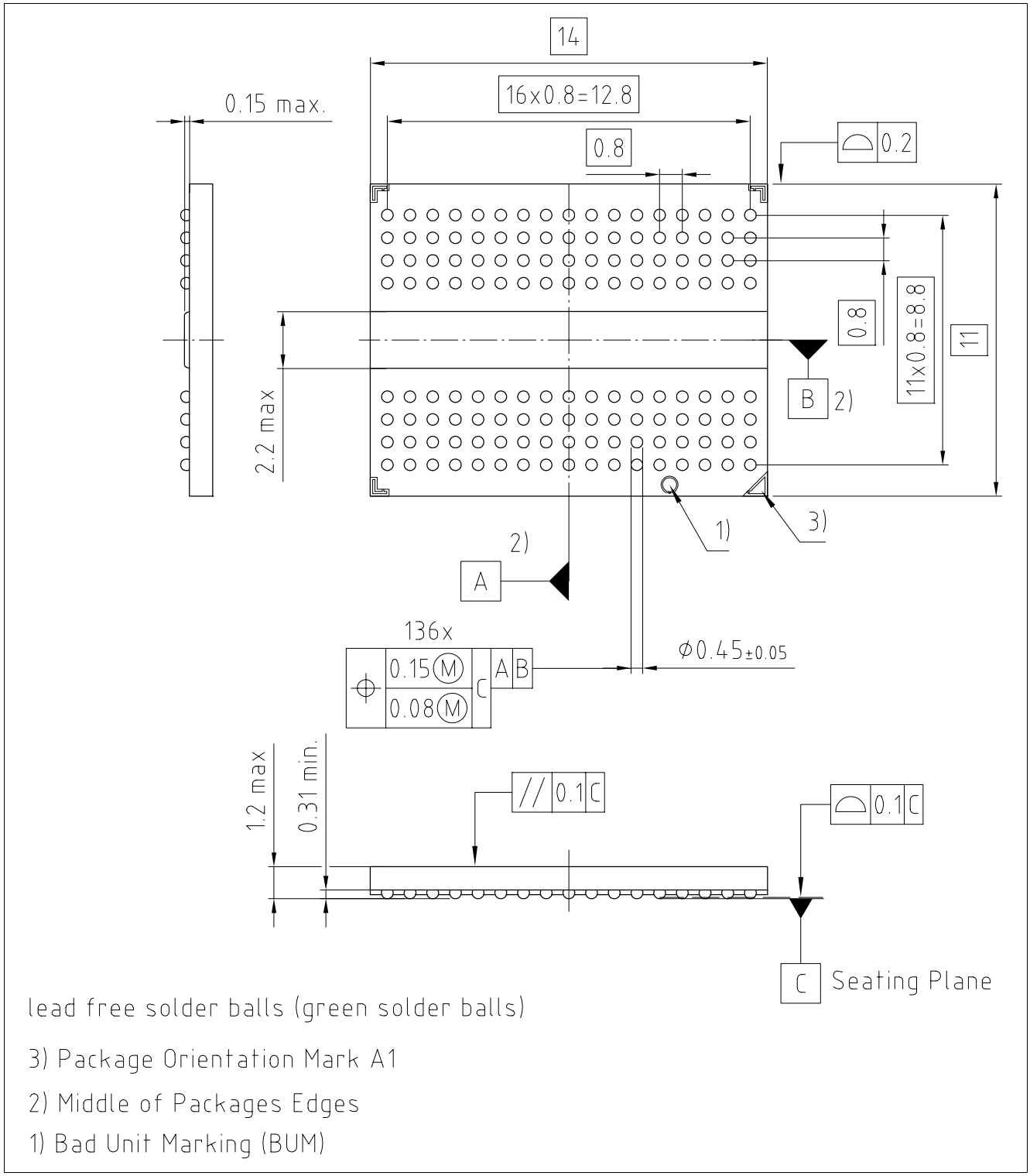

Figure 70 PG-TFBGA 136 package (11mm x 14mm)

Note:. The package is conforming with JEDEC MO-207i, VAR DR-z.

6.2 Package Thermal Characteristics

Table 40 PG-TFBGA 136 Package Thermal Resistances

	Theta_jA						Theta_jB	Theta_jC
JEDEC Board	1s0p			2s0p				
Air Flow	0 m/s	1 m/s	3 m/s	0 m/s	1 m/s	3 m/s	-	-
K/W	40	32	27	22	19	17	5	2

1. *Theta_jA : Junction to Ambient thermal resistance. The values have been obtained by simulation using the conditions stated in the JEDEC JESD-51 standard.*
2. *Theta_jB : Junction to Board thermal resistance. The value has been obtained by simulation.*
3. *Theta_jC : Junction to Case thermal resistance. The value has been obtained by simulation.*

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