APPLICATION NOTE

TRANSISTORS FOR HORIZONTAL DEFLECTION IN TELEVISIONS AND MONITORS

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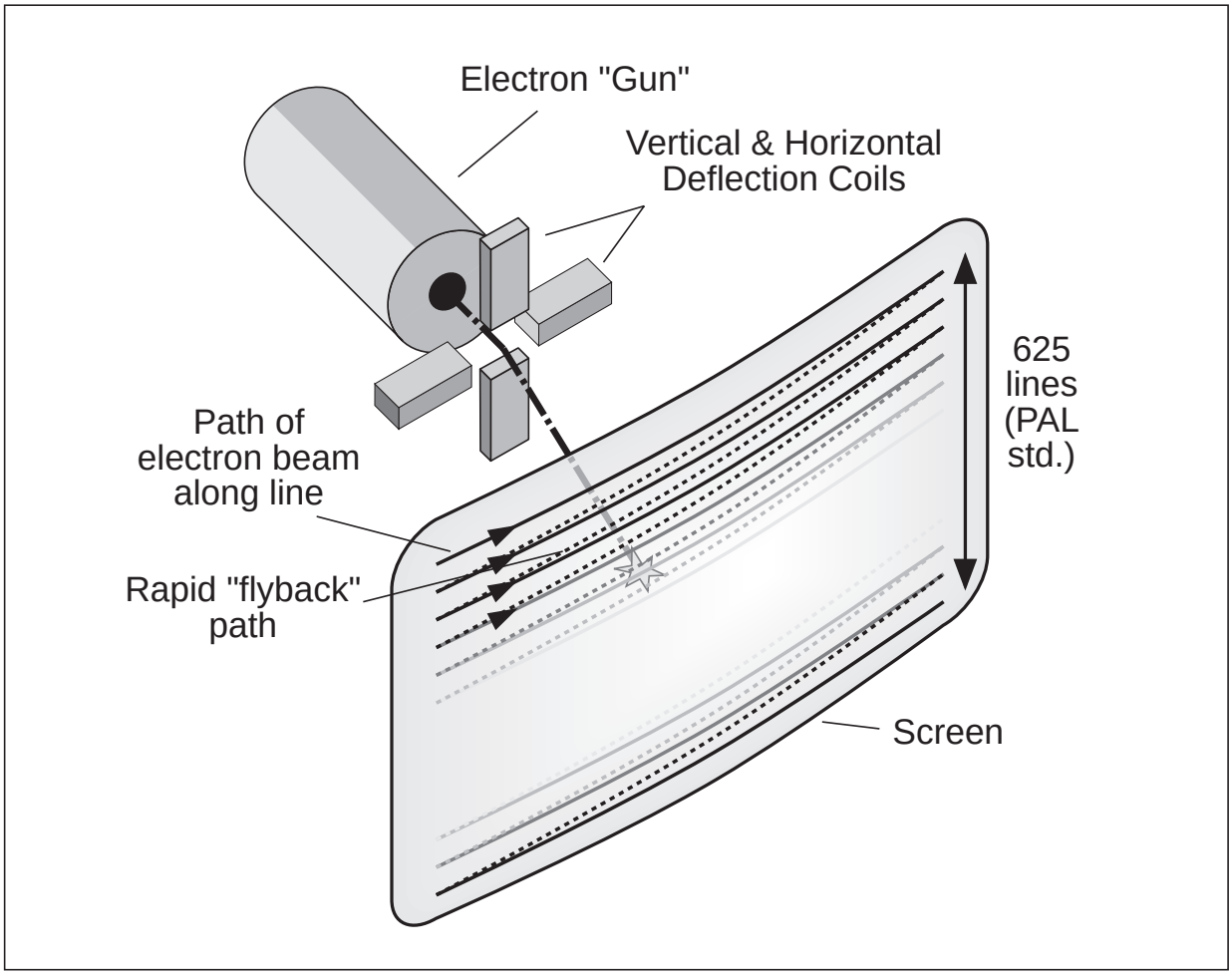
ABSTRACT

The low cost and good performance of high voltage bipolar transistors have meant that these devices remain as the designers first choice in horizontal deflection circuits. As higher definition monitors and television circuits appear, the frequency of operation of the transistors has moved from 16kHz to 32kHz, 64kHz, and up to 100kHz. This paper shows how improved design of die and packages result in transistors optimised for operation at these higher frequencies.

The first section of the paper is an introduction to the operation of the deflection transistor. The switching times and power losses are analysed. The following section describes the characteristics of different transistor technologies. The various options that a power transistor designer has are outlined. The transistor characteristics are divided into three areas: (i) edge termination, (ii) the emitter layout and (iii) the vertical structure. Each of these topics are dealt with in detail. The performance of transistors of similar voltage ratings and die size but with different

Figure 1. Simplified representation of horizontal deflection



design are compared. The possibility of higher frequency operation and the different techniques used to increase the speed of the transistors are also discussed. Isolated packages designed specially for TV and monitor applications are shown in the next section. The performance trade-offs implied in the integration of the damper diode are discussed briefly. The designed trends of the future are mentioned in brief.

1. INTRODUCTION

The designers of TV and monitor horizontal deflection circuits have traditionally required a switch working at around 1500V and at frequencies around 16kHz. The current requirements of the transistor switch varied between 2A and 7A, depending on the screen size, resolution of the picture tube etc. For many years the switch chosen for horizontal deflection has been a high voltage power bipolar transistor like the well known BU508A.

The trend towards monitors with better resolution and, to some extent, higher definition televisions has led to the development of high frequency transistors designed specifically for this application. While many modern TVs have their horizontal deflection frequency increased from 16kHz to 32kHz, the advances in computer graphics, especially monitors for workstations and desktop personal computers have pushed the horizontal deflection frequency of computer desktop monitors to 64, 80 and up to 100kHz.

Today, the low price and good performance of 1500V bipolar transistors have precluded other circuit options like MOSFETs and IGBTs.

We shall limit our discussion to the horizontal deflection transistor, since vertical deflection transistors are often incorporated into a vertical deflection power IC.

2. TELEVISION DEFLECTION

A greatly simplified view of the operation of the CRT in a domestic television using the PAL (625 line) standard is shown in figure 1.

The picture on a television or monitor tube is produced by an electron gun, which produces a beam which is scanned across the inner surface of the tube, causing a coating of phosphors to fluoresce. In order to cover the entire screen, the movement of the striking point of this beam is controlled by magnetic coils in two axes - horizontally and vertically - in such a way as to cover the screen in a pattern of horizontal lines. The refresh rate of the screen is thus defined by the rate at which the beam travels from the top of the screen to the bottom. The point of impact of the beam is moved in the vertical direction relatively slowly - often refreshing the screen at half the mains frequency, 25 or 30Hz. In these applications, the horizontal switching frequency is generally 16kHz, although for a very high resolution computer monitor with a high refresh rate (eg 72Hz) this can be around 80kHz.

3. THE HORIZONTAL DEFLECTION CIRCUIT

A basic deflection circuit using a base drive transformer is shown in figure 2, and figure 3 shows circuit waveforms.

The purpose of the horizontal deflection circuit is to provide a signal to the horizontal deflection coil to

Figure 2. Basic Deflection Circuit

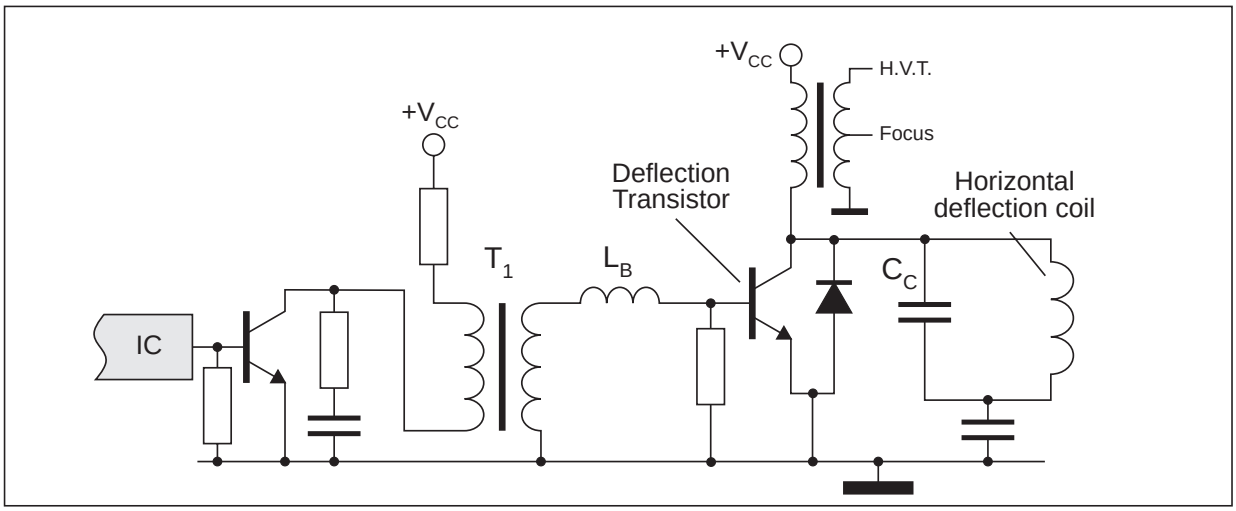
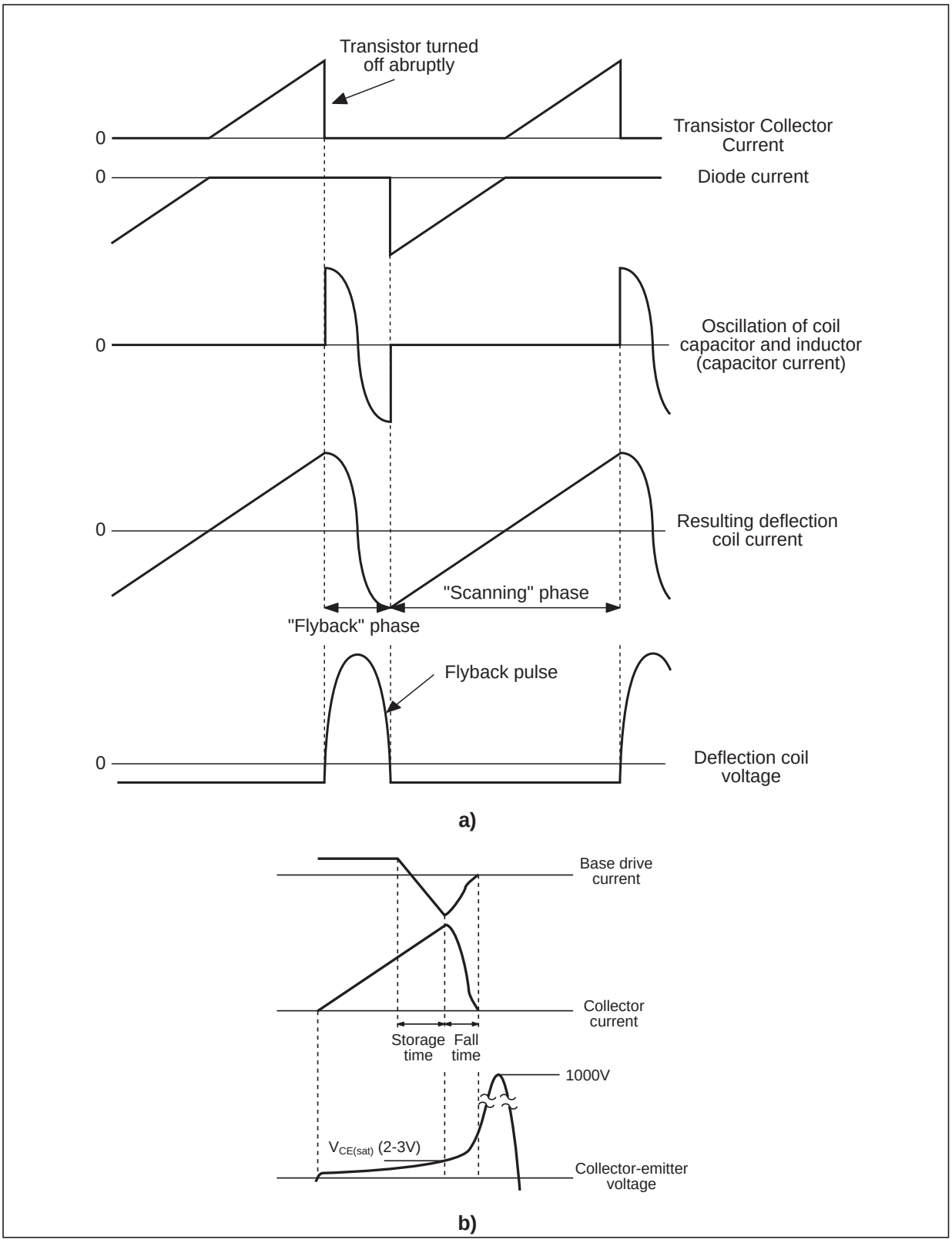


Figure 3. Transistor Switching Waveforms: a) Circuit operation
b) Transistor switching



cause the beam to scan across the screen at a constant speed, and then to make the beam to “fly back” at the end of the write cycle, ready to write another line on the screen. This is achieved by generating a current ramp for the duration of the write cycle, and then turning off the transistor abruptly at the end of the cycle, causing a high voltage pulse in the deflection coil. Transistor turn on causes a current ramp through the inductor. Abrupt turn off of the transistor results in a large flyback pulse seen at the collector of the transistor. This flyback pulse is stepped up to several kilovolts by the flyback transformer, which pulls the electron beam back from one side of the screen to the other. Normally a supply voltage of around 150V results in a peak collector voltage of over 1200V. Traditionally, this has made the use of 1500V (V_{CBO}) transistors common in this application.

Where possible, base drive of the high voltage transistor should follow the collector current ramp. A proportional base drive scheme is best to provide a constant forced gain of adequate level during the time the transistor is on and prevents the transistor from going into hard saturation. Hard saturation of the transistor can lead to current tailing, which in extreme cases can result in thermal runaway and destruction of the transistor. Often a base inductor, shown as L_B in figure 2, is used to decrease the fall time of the transistor and hence the losses. At turn-off, the high reverse base-emitter voltage caused by this inductor will result in the (harmless) avalanche breakdown of the base-emitter junction of the transistor every switching cycle.

4. DEFLECTION TRANSISTOR LOSSES

The most important power losses in the high voltage transistor are:

i) Saturation Losses or On State Losses. The on-state losses and transistor dynamic saturation are usually significantly less important than the turn off losses in the transistor.

ii) Turn Off Losses. This can be further divided into:

a) Losses in the storage time. During this time, the current through the transistor remains close to I_{Cmax} while the voltage across the transistor is increasing. Adequate forward base drive prior to turn off along with careful design of the transistor are needed to avoid dynamic desaturation of the transistor. Dynamic desaturation of the transistor leads to increased on-state voltage, $V_{CE(on)}$, during the storage time, which in turn increases the losses.

b) Losses associated with the fall time. This value is usually small but a current tail here could significantly increase the losses. Minimizing the current tail is an important goal in transistor design.

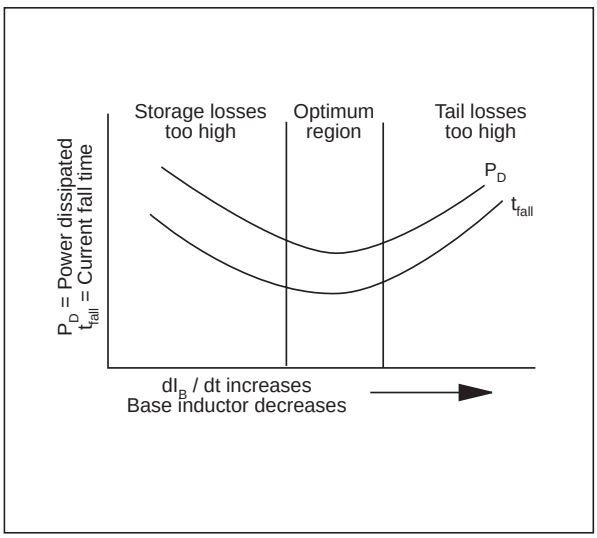
We will assume that the turn on and leakage losses are negligible. In general it is seen that the bulk of the losses are not during the ‘on’ condition but during turnoff (storage and fall time losses).

4.1 Rate of Change of Turn Off Base Current.

In traditional transistor designs, the rate of change of base current (dI_B/dt) at turn-off is very important in determining the losses. dI_B/dt, of course, depends on the inductor L_B in series with the base drive transformer. The power losses and the current fall time curves vary with the rate of fall of reverse base current, as shown in figure 4.

This curve shows that there is an optimum range of the rate of change of base current. If the transistor is turned off too slowly, the excess minority carriers are not extracted quickly enough from the lightly doped N- collector area. The voltage across the transistor increases, leading to higher switching losses. If the extraction of the charges is too fast, the collector-base diode junction recovers more slowly than the base-emitter junction. The minority carriers trapped in the lightly doped N- region give rise to a ‘current tail’ that can dramatically increase the switching losses. The current tail has a positive temperature coefficient and hence can lead to thermal

Figure 4. Variation of Losses with Base Current



runaway which can destroy the transistor. The optimal drive conditions therefore fall in between the high storage losses region and the high current tail losses region.

It is possible to some extent to design a transistor to make the extraction of minority carriers easier. From the point of view of a designer of the transistor die, the flatter the curves shown in figure 4 can be made, the more versatile the transistor will be, since it will be more immune to variations in the drive circuit. It is preferable to design a transistor with slightly higher power losses if the losses are reasonably independent of the base inductance (dI_B/dt).

4.2 Base drive design

The base drive design for the horizontal deflection transistor is important, to minimise the losses. There are a number of solutions available, and the choice of solution depends on the characteristics of the individual application. They fall into two basic classes: those used for TVs; and those used for monitors.

In a TV, the horizontal frequency and screen size are known and fixed, and hence many electrical parameters (e.g. I_C, $V_{CE(flyback)}$) are already defined. The main tasks of the drive are therefore to generate the base current to achieve these values (compensating for variations in the h_{FE} of the devices used), and to produce an optimised reverse base current to reduce turn-off losses.

In monitor circuits, the horizontal frequency and screen size are usually not fixed (monitors are often multi frequency, and the screen size may be varied by the user), and so I_C and $V_{CE(flyback)}$ are not fixed. In this case it is important to have a base drive which can adapt to the various conditions. One way in which this can be achieved is to use a proportional base drive, where the base current follows the collector current.

5. BIPOLAR TRANSISTOR TYPES

Having to switch voltages in the range of 1200V or more, and allowing a safety margin, means that 1500V transistors are the de facto standard. One goal in transistor design is to ensure that the transistor is, less dependent on variations in the base drive circuit (especially rate of change of base current). Switching speeds should be as fast as possible. The spread in device characteristics from device to device, especially the dc gain (h_{FE}), storage time etc. should be minimised. The same device used in horizontal deflection is, for cost reasons, often used in the SMPS in the TV or monitor as well. This means that although the transistor used in the deflection circuit does not require a large RBSOA, as the transistor used in the SMPS does, the transistor designer should design for the largest possible RBSOA to maximise the ruggedness for a given transistor area.

5.1 Edge termination

The design of the edge termination of the transistor is important (indirectly) in determining the switching performance of the transistor. The techniques used in edge termination could be used regardless of the type of transistor: MOSFET, bipolar, IGBT etc.

The two edge termination techniques most commonly used in horizontal deflection transistors are:

i) Mesa edge termination, and

ii) Planar edge termination techniques.

Both termination techniques are widely used in the industry today. Their advantages and disadvantages can only be evaluated in the context of the design of the entire transistor, especially the design of the vertical structure.

Once a decision is made to use mesa or planar edge termination design, the efficiency and reproducibility of the design process will greatly affect the transistor performance. For example, the quality of the edge termination determines whether, in order to meet a guaranteed 1500V V_{CES} specification, the average transistor will have a breakdown voltage of 1550V or 1800V. Process parameters will, in this way, affect switching losses and performance as much as design. The efficiency of edge termination of the transistor determines how the edge termination can be achieved in the minimal area and how much higher the bulk resistance of the silicon should be increased for good yield at the specification limit.

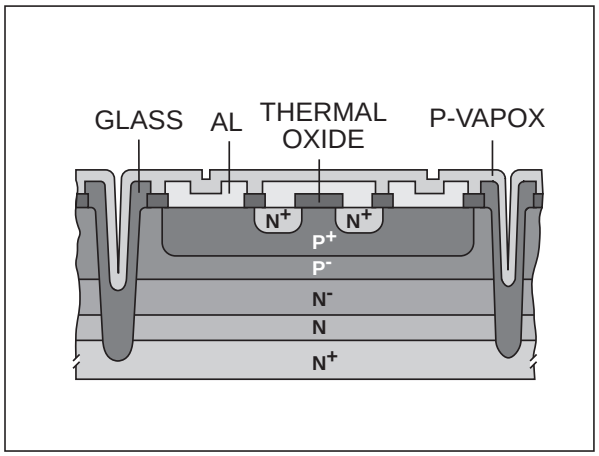
5.2 Layout Design of the transistor- Emitter Layout.

This part generally refers to the design of the emitter and base fingers or cells.

5.2.1 Design of the emitter structure

Figure 5 shows the structure of a hollow emitter transistor. The traditional structure has been a hollow emitter. The ‘hollow’ is created by an oxide layer in the centre of the emitter forcing the current only to the edges. The increased peripheral area reduces current crowding, leading to faster switching. Hollow

Figure 5. Hollow Emitter Transistor



emitter transistors have been in use for over ten years with good results. The major disadvantage of the hollow emitter transistor is that conduction is limited to the periphery of the emitter region. In other words, some of the silicon area of the hollow emitter transistor is "wasted" as the current that can be switched per unit area of silicon is reduced. Efficient emitter design can mean better cell layout, which significantly increase the power handling capability (especially turn off current at high temperature).

The latest trends in emitter design have included:

i) Emitter strips. This implies a finer geometry. This can be understood as the shrinking of the thickness of the emitter finger till, at the limit the oxide layer creating the hollow emitter disappears entirely.

ii) Cellular Emitter. This is the extension of the Emitter Strips technique to a second dimension to form small cells in the emitter structure. These cells, which are connected by a metal layer result in faster removal of charge at turn-off, improving switching speed. Figure 6 shows the structure of a cellular emitter design.

iii) Base Islands. This technology is similar to the cellular emitter. Here the base, not the emitter is placed inside an island and the emitter connections are interspersed between the base islands.

Figures 7 compares the various technologies. Planar transistors designed with these new layout designs have a better RBSOA than those of conventional design. Our results show that the cellular emitter has high current gain characteristics superior to alternative emitter structures. The difference between these three different emitter design technologies, however, is not very large.

Figure 6. Cellular Emitter Transistor:
a. Cross Section (single cell)
b. Plan View

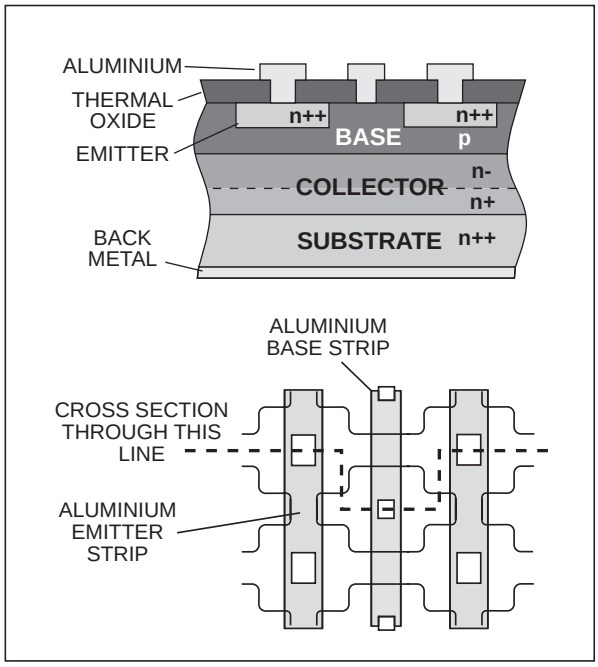
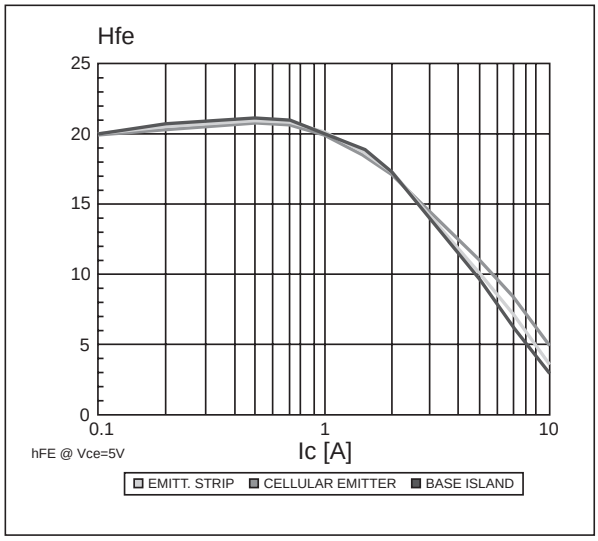


Figure 7. Effect of Emitter Geometry on hfe



5.3 Design of the Vertical Structure

As the transistor breakdown voltage increases, the variations in the emitter layout are not as important as those in the vertical structure. The 1500V deflection transistors that are used for horizontal deflection voltage have large lightly doped collector epitaxial structures (over 110 micrometers). There is not a great amount of variation possible in the

design of the collector structure.

The optimisation of the base structure is one of the most important parameters affecting device switching performance. In a transistor of conventional design, the safe operating area at turn off could be improved by the addition of an 'energy layer' a thin additional epitaxial N+ layer. This increases the RBSOA, but at the expense of switching speed. That is, the thicker the energy layer, the better the RBSOA but the slower the transistor. It has been found that by careful optimisation of base diffusion design of the planar transistor, the RBSOA can be increased while keeping the switching speed of the device high.

Significant other performance improvements can be achieved by optimising the base structure of the transistor. By optimising the design of the junction, better stability after HTRB is possible. The gain of the transistor can be made flatter and less dependent on the value of the current. An incidental benefit of this is that the variation of the current gain (h_{FE}) with temperature is lowered. This is important in horizontal deflection circuit design since it protects against transistor runaway.

The optimisation of the vertical structure and the emitter layout lead to a decrease in the (equivalent) base parasitic resistance $r_{bb'}$. This makes the turn off base current more effective in removing stored charge in the transistor. Switching times and hence switching losses are reduced.

Figures 8 and 9 compare the SOA and fall times of similar conventional hollow emitter and the newer generation planar transistor. In the conventional hollow emitter transistor, the rounded waveform of the reverse bias base current is caused by a high

Figure 8. Effect of Base Design on RBSOA: a. Hollow Emitter Transistor
b. Cellular Emitter Transistor

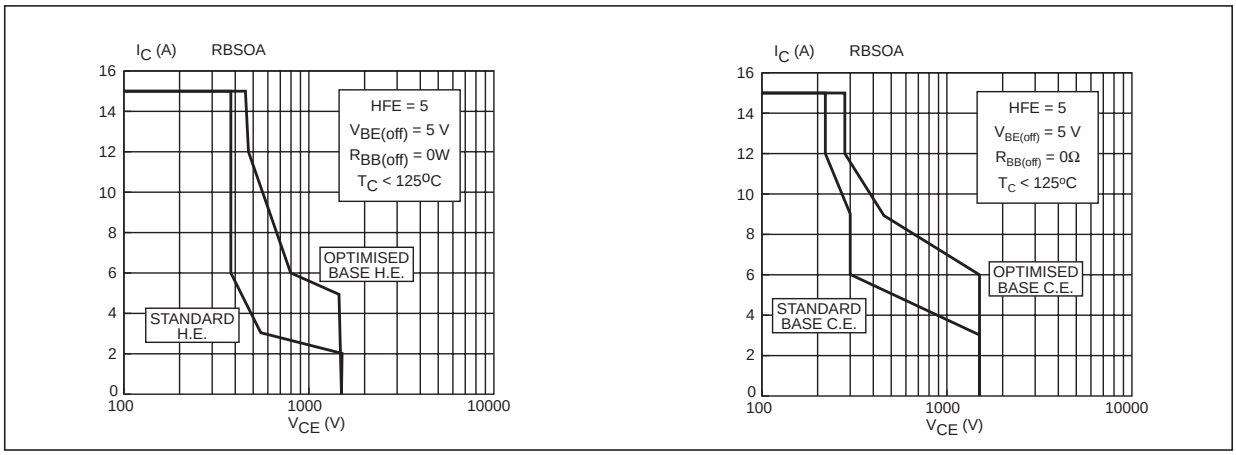
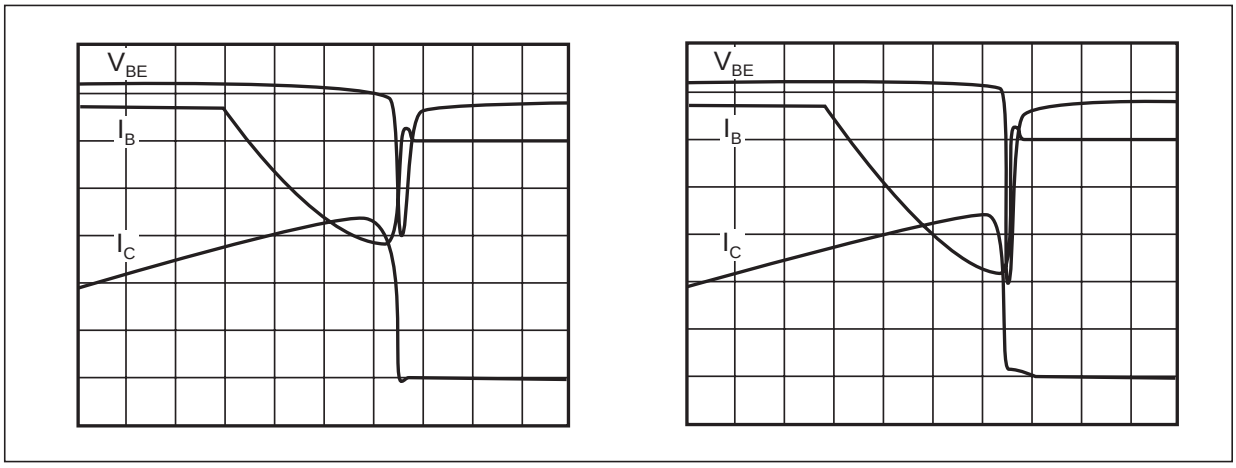


Figure 9. Turn Off Times: a. Hollow Emitter Transistor b. Cellular Emitter Transistor



value of the base spreading resistance. The new planar transistor with reduced rbb' has current fall times about two thirds of that of the conventional transistor. The techniques explained below can lead to a further reduction of storage and fall times in the transistor.

5.4 Techniques for Improved Switching Speed

Techniques of a similar nature are used in rectifier diodes, IGBTs and bipolar transistors to increase switching speeds. The excess charge present at turn off is removed by the creation of recombination centres. These recombination centres are made by precious metal (Pt, Au) doping or by fundamental particle irradiation. Electron irradiation is one example of how recombination centres are created The flaws in the crystalline structure caused by irradiation is where the recombination occurs. The minority carrier lifetime, a physical parameter of the transistor which controls the gain, and switching times for a transistor of a given breakdown voltage can be reduced significantly. As a result of the creation of these recombination centres, these devices exhibit higher on-state voltage than before but their switching times are reduced dramatically.

The storage times and the fall times are significantly reduced by irradiation. The tail in the collector current in turnoff is lowered. This results in significant reductions in the turn off losses and hence device junction temperature. The on voltage during the storage time period is also increased but the total losses during this period are marginally reduced because of the reduction in the storage time itself. The unit-to-unit spread in the switching parameters of the transistors are greatly reduced. This is also very important from the circuit design point of view.

Another method to increase the switching speed of the transistors is to monolithically integrate portions of the drive circuit on to the high voltage transistor. Here the challenge is to manufacture this complex circuit at the very competitive prices common in this market.

6. ISOLATED PACKAGES FOR DEFLECTION

Isolation of the high voltage transistors is very important. In high volume applications such as TVs and monitors, isolated packages save manufacturing costs and time and increase safety and reliability. Some of these packages, such as the ISOWATT218 are similar to their non-isolated counterparts but with a thin layer (a few tenths of a mm) of a thermally conductive but electrically insulating plastic layer to provide the isolation. To meet VDE and EN isolation requirements, a second generation of smaller, low cost packages was developed for increased isolation as well as creepage distances. These methods of moulding thermally conductive plastic over the heat spreader is easy to automate. This results in lower costs and better reliability.

7.THE DAMPER DIODE

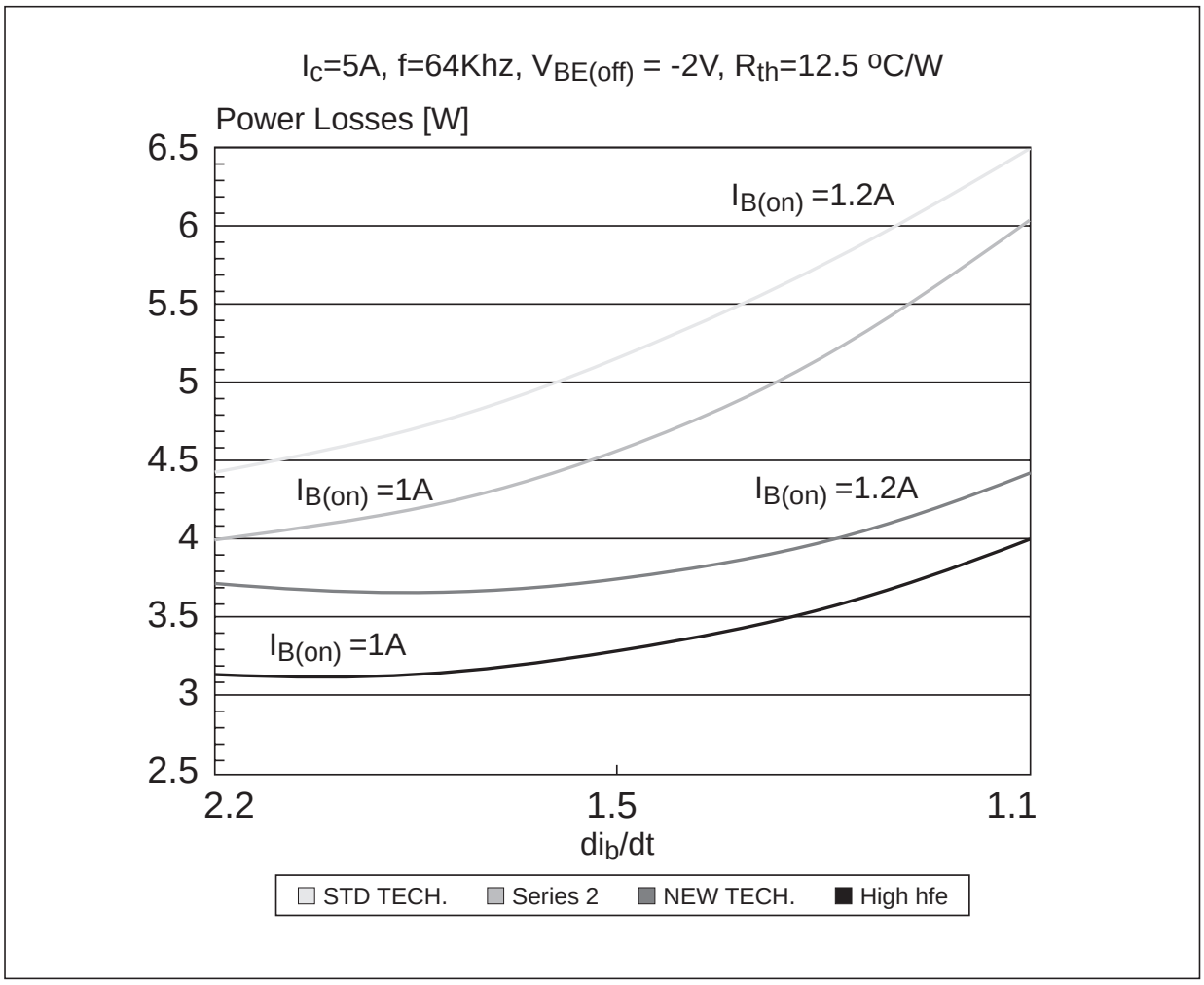
It is possible to manufacture a planar or mesa deflection transistor with an integral collector-emitter anti-parallel rectifier diode, simply by changing one or two masks in the process. Some design compromises are sure to result if the antiparallel diode is integrated. The integrated antiparallel diode, for example, will have recovery times at least twice that of an external rectifier diode designed solely for this application. Techniques designed to speed up the fall time of the transistor usually speed up the recovery times of the diode as well. Therefore, for low frequency operation, deflection transistors with integrated collector-emitter diodes can be used, while at high frequencies, specially designed “damper diodes” are used. These diodes designed specifically to minimise the forward recovery time and the turn on forward voltage overshoot. An example of this kind of damper diode is the DTV32F1500A.

8. FUTURE TRENDS

Figure 10 compares the total losses in two similar 1500V switching transistors while switching a peak collector current of 5A at 64kHz. These current and frequency specifications are a real challenge for the transistors of such a small die size. A typical modern planar transistor is compared with a conventional transistor, sorted for high gain. The low gain conventional transistors went into thermal runaway under these conditions. By using transistors with larger die size, even higher current and higher frequency operation is possible.

In the short to medium term, bipolar horizontal deflection transistors are not likely to be replaced by MOSFETs or IGBTs. A more likely replacement would perhaps be a Power IC, an intelligent power switch specifically designed for horizontal deflection. An example of this type of circuit is a 1500V monolithic emitter switch with built in drive and protection features.. In the near future, the careful layout and design will keep the bipolar transistor as the device of choice in horizontal deflection circuits.

Figure 10. Comparison of Transistor Losses



REFERENCES

(i) K. Rischmuller, “Bipolar Transistors and Darlingtons - Design , Function, Drive and Protection”, AN363/0789, SGS-THOMSON Power Transistor Application Manual, 1st Edition

(ii) A. Galluzzo and A. Morgan, “Improved Power Transistor Performance with Fast switch Hollow Emitter Technology”, AN360/0689, SGS-THOMSON Power Transistor Application Manual, 1st Edition.

(iii) L. Wuidart, “A Transistor for 100kHz Converters: ETD” , AN361/0689, SGS-THOMSON Designers Guide To Power Products, 2nd Edition.

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