

**DRAM MODULE**

**M53230804CY0/CT0-C**

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# 4Byte 8Mx32 SIMM

(4Mx16 base)

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Revision 0.0

June 1999



## DRAM MODULE

M53230804CY0/CT0-C

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### Revision History

#### Version 0.0 (June 1999)

- The 4th. generation of 64Mb DRAM components are applied for this module.

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**DRAM MODULE****M53230804CY0/CT0-C****M53230804CY0/CT0-C EDO Mode**

8M x 32 DRAM SIMM Using 4Mx16, 4K Refresh, 5V

**GENERAL DESCRIPTION**

The Samsung M53230804CY0/CT0-C is a 8Mx32bits Dynamic RAM high density memory module. The Samsung M53230804CY0/CT0-C consists of four CMOS 4Mx16bits DRAMs in TSOP packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The M53230804CY0/CT0-C is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

**PERFORMANCE RANGE**

Speed	t <sub>TRAC</sub>	t <sub>CAC</sub>	t <sub>RC</sub>	t <sub>HPC</sub>
-C50	50ns	13ns	84ns	20ns
-C60	60ns	15ns	104ns	25ns

**FEATURES**

- Part Identification
  - M53230804CY0-C(4K cycles/64ms Ref, TSOP, Solder)
  - M53230804CT0-C(4K cycles/64ms Ref, TSOP, Gold)
- Extended Data Out Mode Operation
- CAS-before-RAS & Hidden Refresh capability
- RAS-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1000mil), double sided component

**PIN CONFIGURATIONS**

Pin	Symbol	Pin	Symbol
1	V <sub>ss</sub>	37	NC
2	DQ0	38	NC
3	DQ18	39	<u>V<sub>ss</sub></u>
4	DQ1	40	<u>CAS0</u>
5	DQ19	41	<u>CAS2</u>
6	DQ2	42	<u>CAS3</u>
7	DQ20	43	<u>CAS1</u>
8	DQ3	44	<u>RAS0</u>
9	DQ21	45	RAS1
10	V <sub>cc</sub>	46	NC
11	NC	47	W
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	V <sub>cc</sub>
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	V <sub>cc</sub>	66	NC
31	A8	67	PD1
32	<u>A9</u>	68	PD2
33	<u>RAS3</u>	69	PD3
34	<u>RAS2</u>	70	PD4
35	NC	71	NC
36	NC	72	V <sub>ss</sub>

**PIN NAMES**

Pin Name	Function
A0 - A11	Address Inputs
DQ0-7, DQ9-16 DQ18-25, DQ27-34	Data In/Out
<u>W</u>	Read/Write Enable
<u>RAS0</u> - <u>RAS3</u>	Row Address Strobe
<u>CAS0</u> - <u>CAS3</u>	Column Address Strobe
PD1 -PD4	Presence Detect
V <sub>cc</sub>	Power(+5V)
V <sub>ss</sub>	Ground
NC	No Connection

**PRESENCE DETECT PINS (Optional)**

Pin	50NS	60NS
PD1	NC	NC
PD2	V <sub>ss</sub>	V <sub>ss</sub>
PD3	V <sub>ss</sub>	NC
PD4	V <sub>ss</sub>	NC

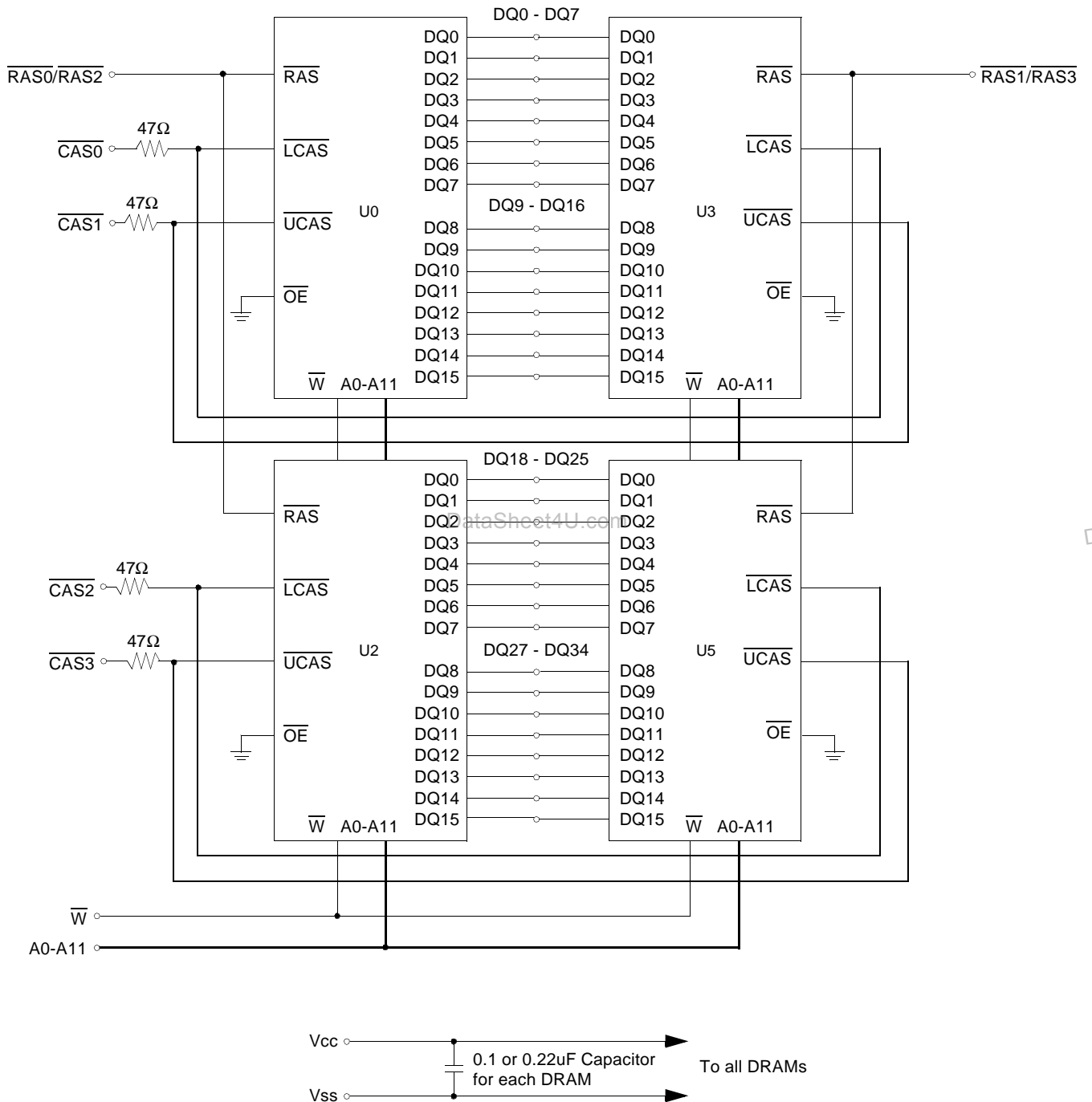
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# DRAM MODULE

# M53230804CY0/CT0-C

## FUNCTIONAL BLOCK DIAGRAM



## DRAM MODULE

## M53230804CY0/CT0-C

## ABSOLUTE MAXIMUM RATINGS \*

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-1 to +7.0	V
Storage Temperature	T <sub>stg</sub>	-55 to +125	°C
Power Dissipation	P <sub>d</sub>	4	W
Short Circuit Output Current	I <sub>OS</sub>	50	mA

\* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T<sub>A</sub> = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.4	-	V <sub>CC</sub> <sup>*1</sup>	V
Input Low Voltage	V <sub>IL</sub>	-1.0 <sup>*2</sup>	-	0.8	V

\*1 : V<sub>CC</sub>+2.0V at pulse width ≤ 20ns, which is measured at V<sub>CC</sub>.

\*2 : -2.0V at pulse width ≤ 20ns, which is measured at V<sub>SS</sub>.

## DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	M53230804CY0/CT0		Unit
		Min	Max	
I <sub>CC1</sub>	-50	-	244	mA
	-60	-	224	mA
I <sub>CC2</sub>	Don't care	-	8	mA
I <sub>CC3</sub>	-50	-	244	mA
	-60	-	224	mA
I <sub>CC4</sub>	-50	-	224	mA
	-60	-	204	mA
I <sub>CC5</sub>	Don't care	-	4	mA
I <sub>CC6</sub>	-50	-	244	mA
	-60	-	224	mA
I <sub>I(L)</sub> I <sub>O(L)</sub>	Don't care	-10	10	uA
		-10	10	uA
V <sub>OH</sub> V <sub>OL</sub>	Don't care	2.4	-	V
		-	0.4	V

I<sub>CC1</sub> : Operating Current \* ( $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ , Address cycling @trc=min)

I<sub>CC2</sub> : Standby Current ( $\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=\text{V}_{\text{IH}}$ )

I<sub>CC3</sub> :  $\overline{\text{RAS}}$  Only Refresh Current \* ( $\overline{\text{CAS}}=\text{V}_{\text{IH}}$ ,  $\overline{\text{RAS}}$  cycling @trc=min)

I<sub>CC4</sub> : Hyper Page Mode Current \* ( $\overline{\text{RAS}}=\text{V}_{\text{IL}}$ ,  $\overline{\text{CAS}}$  cycling : t<sub>HPC</sub>=min)

I<sub>CC5</sub> : Standby Current ( $\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=\text{V}_{\text{CC}}-0.2\text{V}$ )

I<sub>CC6</sub> :  $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$  Refresh Current \* ( $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  cycling @trc=min)

I<sub>I(L)</sub> : Input Leakage Current (Any input  $0 \leq \text{V}_{\text{IN}} \leq \text{V}_{\text{CC}}+0.5\text{V}$ , all other pins not under test=0 V)

I<sub>O(L)</sub> : Output Leakage Current(Data Out is disabled,  $0\text{V} \leq \text{V}_{\text{OUT}} \leq \text{V}_{\text{CC}}$ )

V<sub>OH</sub> : Output High Voltage Level (I<sub>OH</sub> = -5mA)

V<sub>OL</sub> : Output Low Voltage Level (I<sub>OL</sub> = 4.2mA)

\* **NOTE** : I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub> and I<sub>CC6</sub> are dependent on output loading and cycle rates. Specified values are obtained with the output open. I<sub>CC</sub> is specified as an average current. In I<sub>CC1</sub> and I<sub>CC3</sub>, address can be changed maximum once while  $\overline{\text{RAS}}=\text{V}_{\text{IL}}$ . In I<sub>CC4</sub>, address can be changed maximum once within one EDO mode cycle time, t<sub>HPC</sub>.



## DRAM MODULE

## M53230804CY0/CT0-C

## CAPACITANCE (TA = 25°C, VCC=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	CIN1	-	30	pF
Input capacitance[ $\overline{W}$ ]	CIN2	-	38	pF
Input capacitance[RAS0/RAS2, RAS1/RAS3]	CIN3	-	24	pF
Input capacitance[CAS0 - CAS3]	CIN4	-	24	pF
Input/Output capacitance[ $\overline{DQ0-7}$ , 9-16,18-25, 27-34]	CDQ	-	24	pF

## AC CHARACTERISTICS (0°C≤TA≤70°C, Vcc=5.0V±10%. See notes 1,2.)

Test condition :  $V_{ih}/V_{il}=2.6/0.8V$ ,  $V_{oh}/V_{ol}=2.0/0.8V$ , output loading  $CL=100pF$ 

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t <sub>RC</sub>	84		104		ns	
Access time from RAS	t <sub>RAC</sub>		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t <sub>CAC</sub>		13		15	ns	3,4,5
Access time from column address	t <sub>AA</sub>		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t <sub>CLZ</sub>	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t <sub>CEZ</sub>	3	13	3	13	ns	6,12
Transition time(rise and fall)	t <sub>T</sub>	1	50	1	50	ns	2
RAS precharge time	t <sub>RP</sub>	30		40		ns	
RAS pulse width	t <sub>RAS</sub>	50	10K	60	10K	ns	
RAS hold time	t <sub>RSH</sub>	13		15		ns	
$\overline{CAS}$ hold time	t <sub>CSH</sub>	38		45		ns	
$\overline{CAS}$ pulse width	t <sub>CAS</sub>	8	10K	10	10K	ns	4
RAS to $\overline{CAS}$ delay time	t <sub>RC<math>\overline{D}</math></sub>	20	37	20	45	ns	9
RAS to column address delay time	t <sub>RAD</sub>	15	25	15	30	ns	
$\overline{CAS}$ to RAS precharge time	t <sub>CRP</sub>	5		5		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		ns	
Row address hold time	t <sub>RAH</sub>	10		10		ns	
Column address set-up time	t <sub>ASC</sub>	0		0		ns	
Column address hold time	t <sub>CAH</sub>	8		10		ns	
Column address to RAS lead time	t <sub>RAL</sub>	25		30		ns	
Read command set-up time	t <sub>RCS</sub>	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t <sub>RCH</sub>	0		0		ns	8
Read command hold referenced to RAS	t <sub>RRH</sub>	0		0		ns	8
Write command set-up time	t <sub>WCS</sub>	0		0		ns	7
Write command hold time	t <sub>WCH</sub>	10		10		ns	
Write command pulse width	t <sub>WP</sub>	10		10		ns	
Write command to RAS lead time	t <sub>RWL</sub>	13		15		ns	
Write command to $\overline{CAS}$ lead time	t <sub>CWL</sub>	8		10		ns	
Data set-up time	t <sub>DS</sub>	0		0		ns	9
Data hold time	t <sub>DH</sub>	8		10		ns	9
Refresh period	t <sub>REF</sub>		64		64	ms	
$\overline{CAS}$ setup time ( $\overline{CAS}$ -before-RAS refresh)	t <sub>CSR</sub>	5		5		ns	
$\overline{CAS}$ hold time ( $\overline{CAS}$ -before-RAS refresh)	t <sub>CHR</sub>	10		10		ns	
RAS to $\overline{CAS}$ precharge time	t <sub>RPC</sub>	5		5		ns	
Access time from $\overline{CAS}$ precharge	t <sub>CPA</sub>		28		35	ns	3



## DRAM MODULE

## M53230804CY0/CT0-C

**AC CHARACTERISTICS** ( $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$ . See notes 1,2.)Test condition :  $V_{ih}/V_{il} = 2.6/0.8\text{V}$ ,  $V_{oh}/V_{ol} = 2.0/0.8\text{V}$ , output loading  $C_L = 100\text{pF}$ 

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Hyper page mode cycle time	tHPC	20		25		ns	11
$\overline{\text{CAS}}$ precharge time (Hyper page cycle)	tCP	8		10		ns	
$\overline{\text{RAS}}$ pulse width (Hyper page cycle)	tRASP	50	200K	60	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	30		35		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time (C-B-R refresh)	tWRP	10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time (C-B-R refresh)	tWRH	10		10		ns	
Output data hold time	tDOH	5		5		ns	
Output buffer turn off delay from $\overline{\text{RAS}}$	tREZ	3	13	3	15	ns	6,12
Output buffer turn off delay from $\overline{\text{W}}$	tWEZ	3	13	3	15	ns	6
$\overline{\text{W}}$ to data delay	tWED	15		15		ns	
$\overline{\text{W}}$ pulse width	tWPE	5		5		ns	

## NOTES

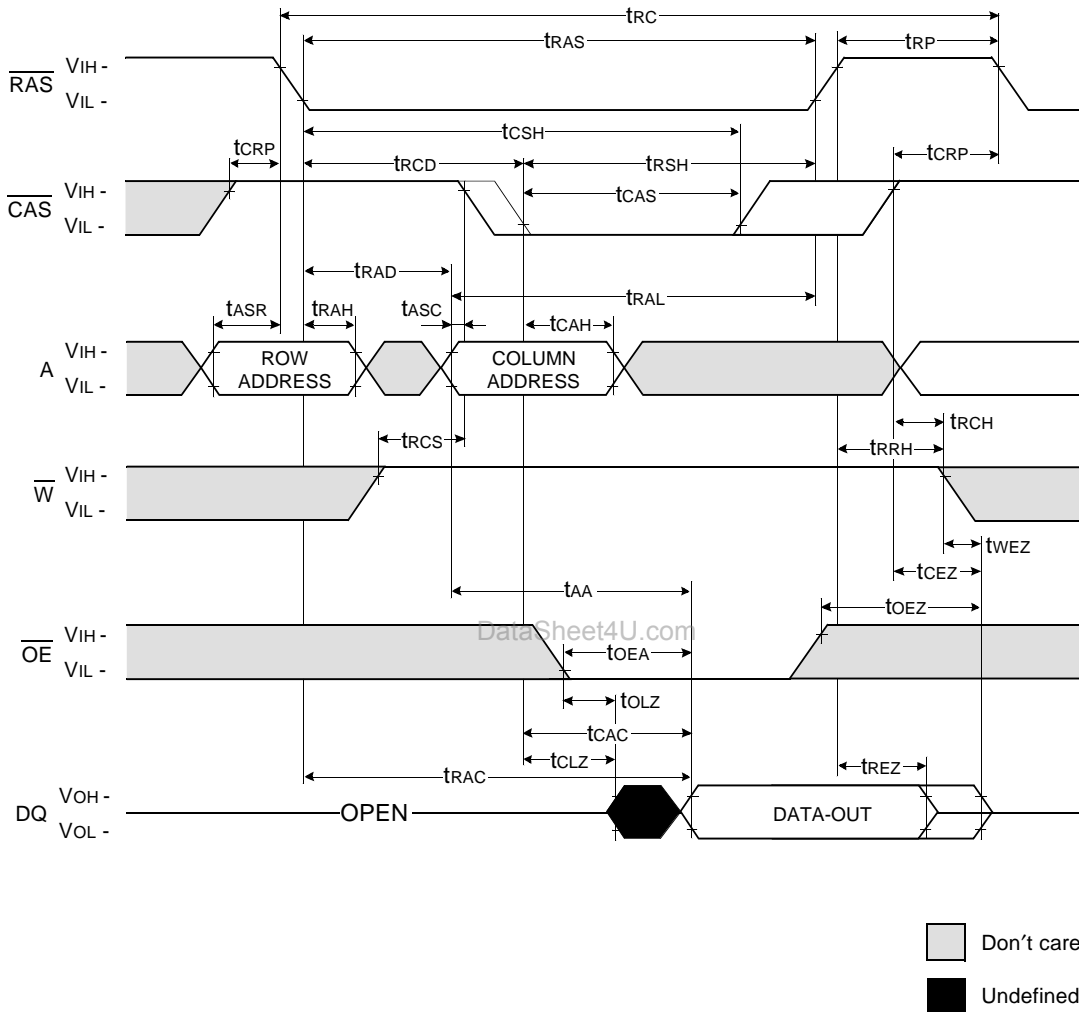
- An initial pause of 200us is required after power-up followed by any 8 RAS-only or  $\overline{\text{CAS}}$ -before-RAS refresh cycles before proper device operation is achieved.
- Input voltage levels are  $V_{ih}/V_{il}$ .  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  and are assumed to be 5ns for all inputs.
- Measured with a load equivalent to 2 TTL loads and 100pF.
- Operation within the  $t_{\text{RCD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met.  $t_{\text{RCD}}(\text{max})$  is specified as a reference point only. If  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{CAC}}$ .
- Assumes that  $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ .
- This parameter defines the time at which the output achieves the open circuit and is not referenced for  $V_{OH}$  or  $V_{OL}$ .
- $t_{\text{WCS}}$  is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If  $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ , the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
- Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycle.
- These parameters are referenced to the  $\overline{\text{CAS}}$  leading edge in early write cycles.
- Operation within the  $t_{\text{RAD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met.  $t_{\text{RAD}}(\text{max})$  is specified as reference point only. If  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}(\text{max})$  limit access time is controlled by  $t_{\text{AA}}$ .
- $t_{\text{ASC}} \geq 6\text{ns}$ , Assume  $t_{\text{T}} = 2.0\text{ns}$ .
- If  $\overline{\text{RAS}}$  goes high before  $\overline{\text{CAS}}$  high going, the open circuit condition of the output is achieved by  $\overline{\text{CAS}}$  high going. If  $\overline{\text{CAS}}$  goes high before  $\overline{\text{RAS}}$  high going, the open circuit condition of the output is achieved by  $\overline{\text{RAS}}$  going.



# DRAM MODULE

# M53230804CY0/CT0-C

## READ CYCLE



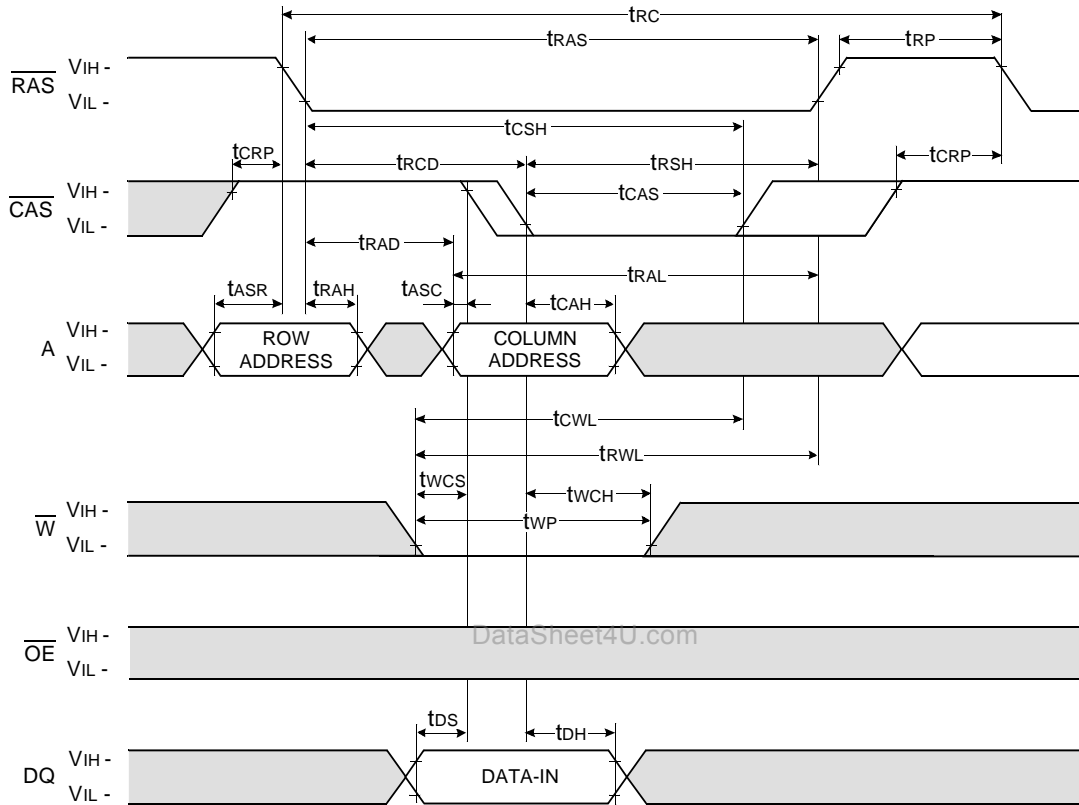


# DRAM MODULE

# M53230804CY0/CT0-C

## WRITE CYCLE ( EARLY WRITE )

NOTE : DoUT = OPEN



Don't care  
 Undefined

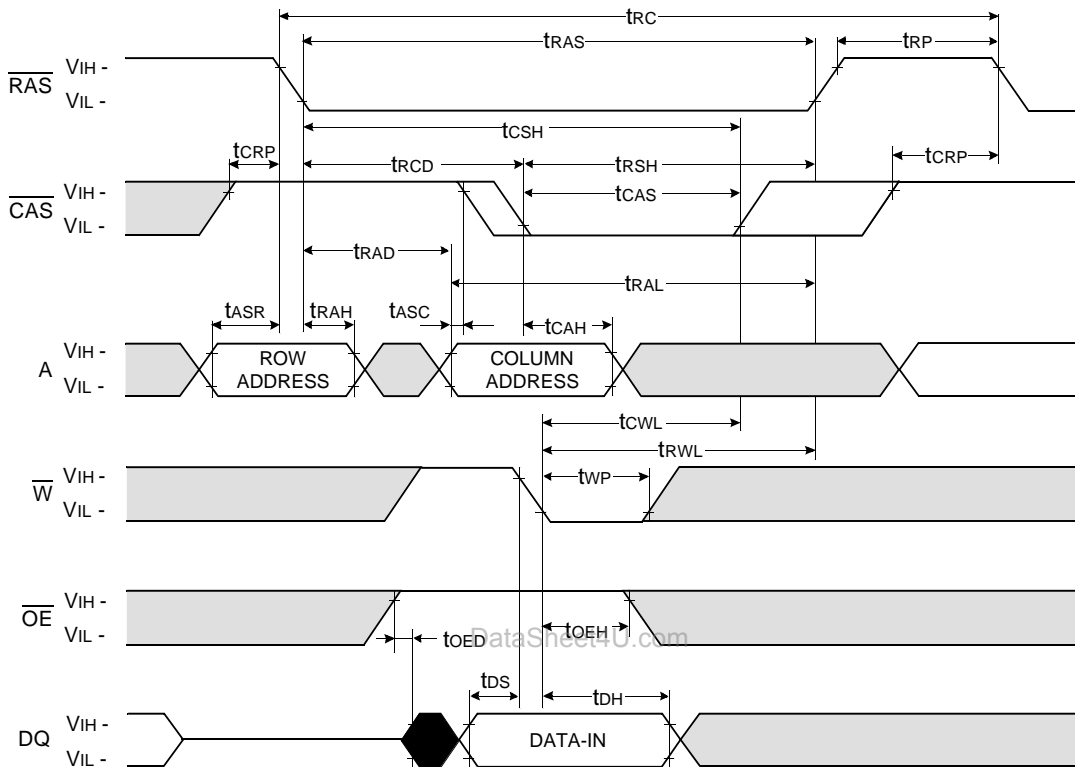


# DRAM MODULE

# M53230804CY0/CT0-C

## WRITE CYCLE ( $\overline{OE}$ CONTROLLED WRITE )

NOTE : DOUT = OPEN



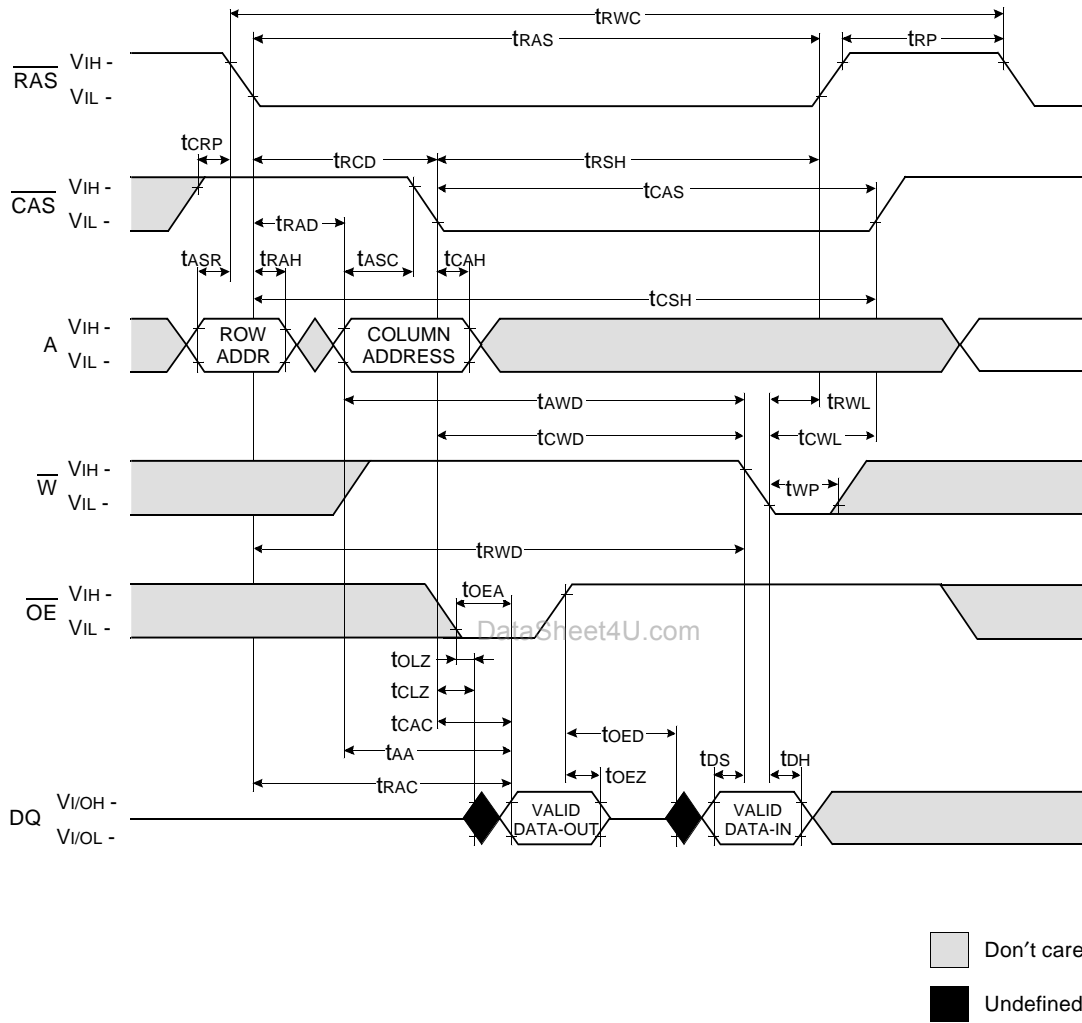
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# DRAM MODULE

# M53230804CY0/CT0-C

## READ - MODIFY - WRITE CYCLE



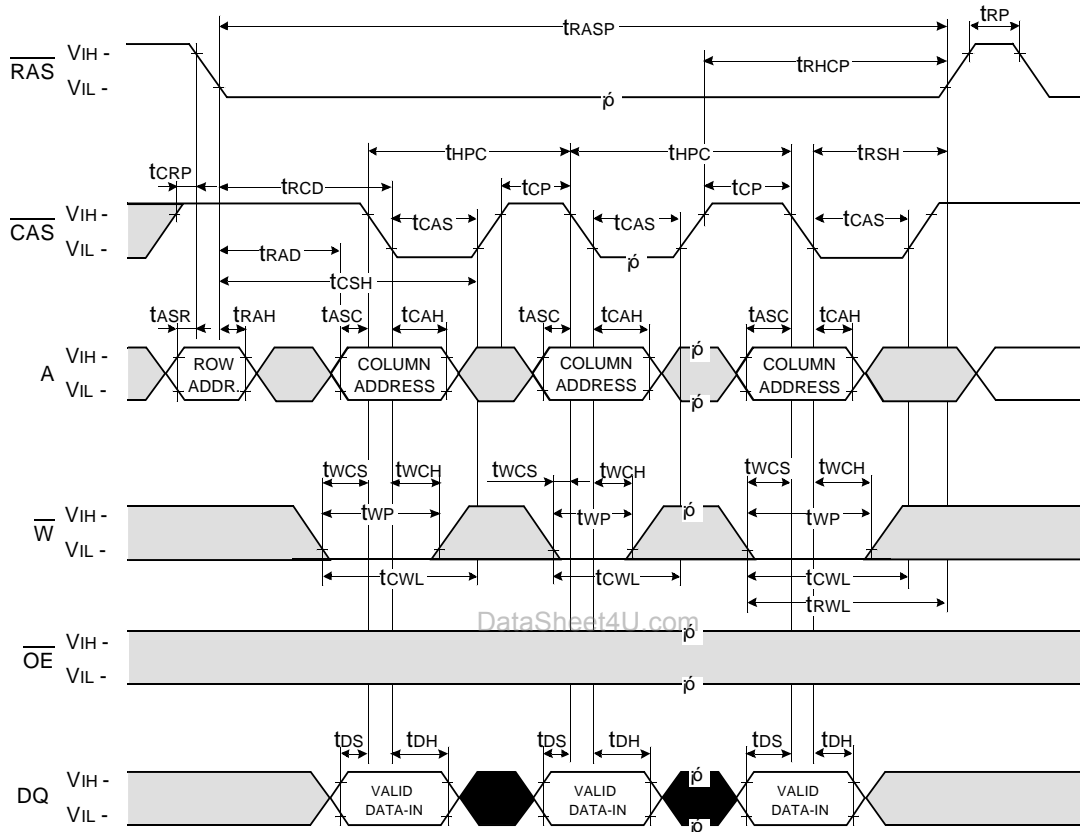


# DRAM MODULE

# M53230804CY0/CT0-C

## HYPER PAGE WRITE CYCLE ( EARLY WRITE )

NOTE : DOUT = OPEN



Don't care  
 Undefined

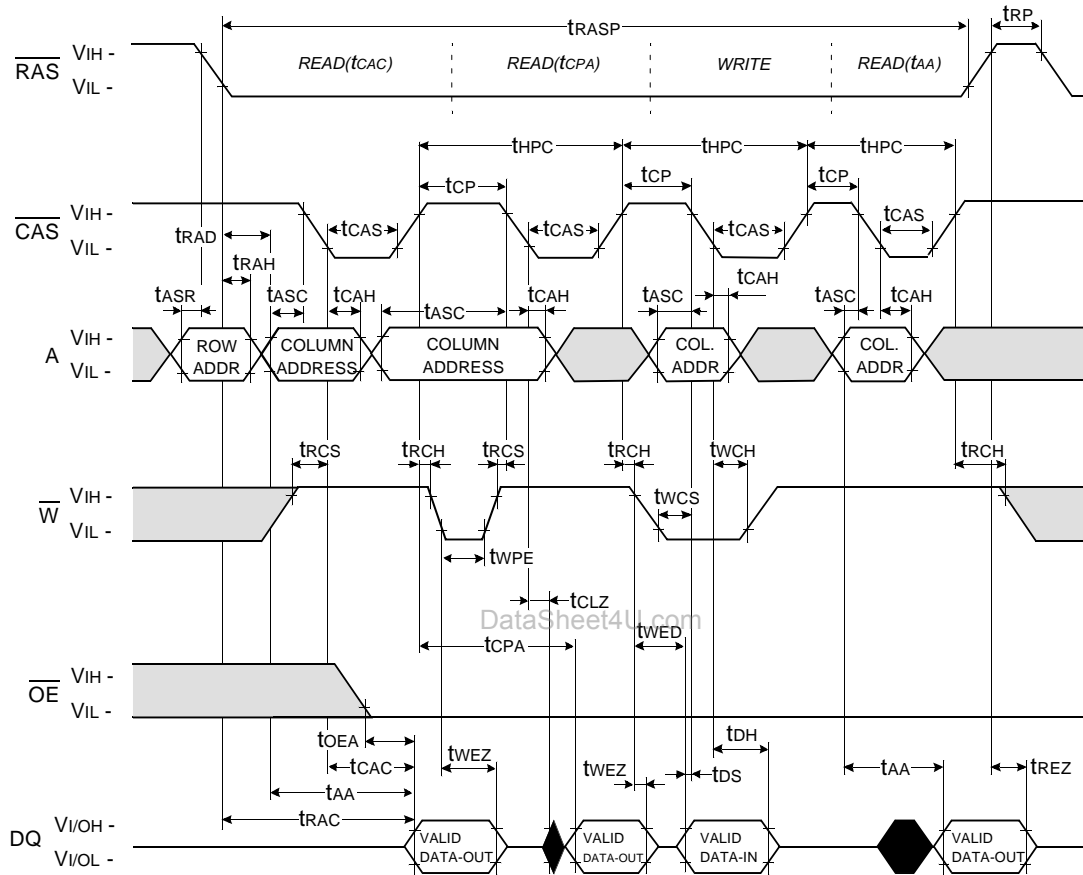




# DRAM MODULE

# M53230804CY0/CT0-C

## HYPER PAGE READ AND WRITE MIXED CYCLE



Don't care  
 Undefined



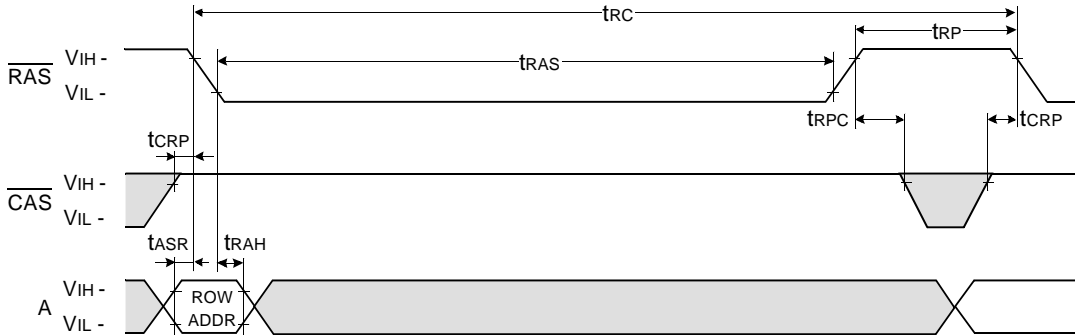
# DRAM MODULE

# M53230804CY0/CT0-C

## RAS - ONLY REFRESH CYCLE\*

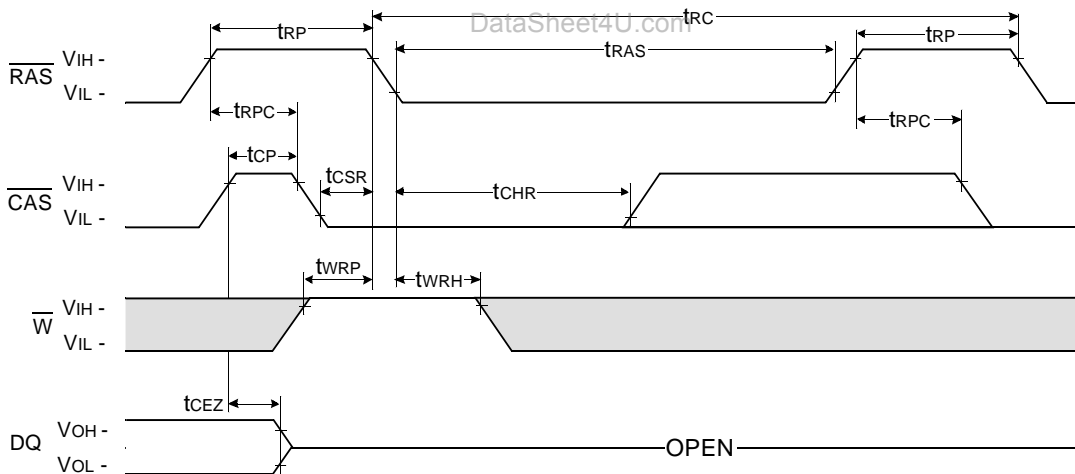
NOTE :  $\overline{W}$ ,  $\overline{OE}$ , DIN = Don't care

DOUT = OPEN



## CAS - BEFORE - RAS REFRESH CYCLE

NOTE :  $\overline{OE}$ , A = Don't care



Don't care  
 Undefined

\* In RAS-only refresh cycle of 64Mb A-die & B-die, when  $\overline{CAS}$  signal transits from Low to High, the valid data may be cut off.

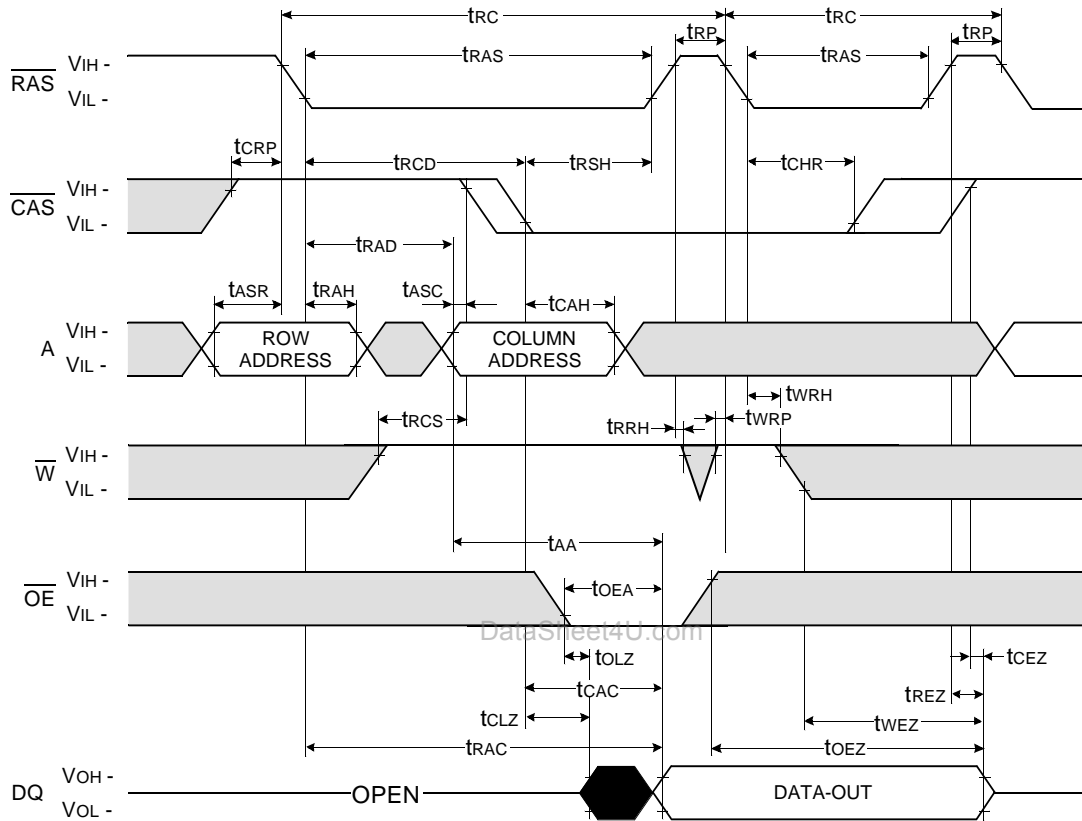




# DRAM MODULE

# M53230804CY0/CT0-C

## HIDDEN REFRESH CYCLE ( READ )



Don't care  
 Undefined

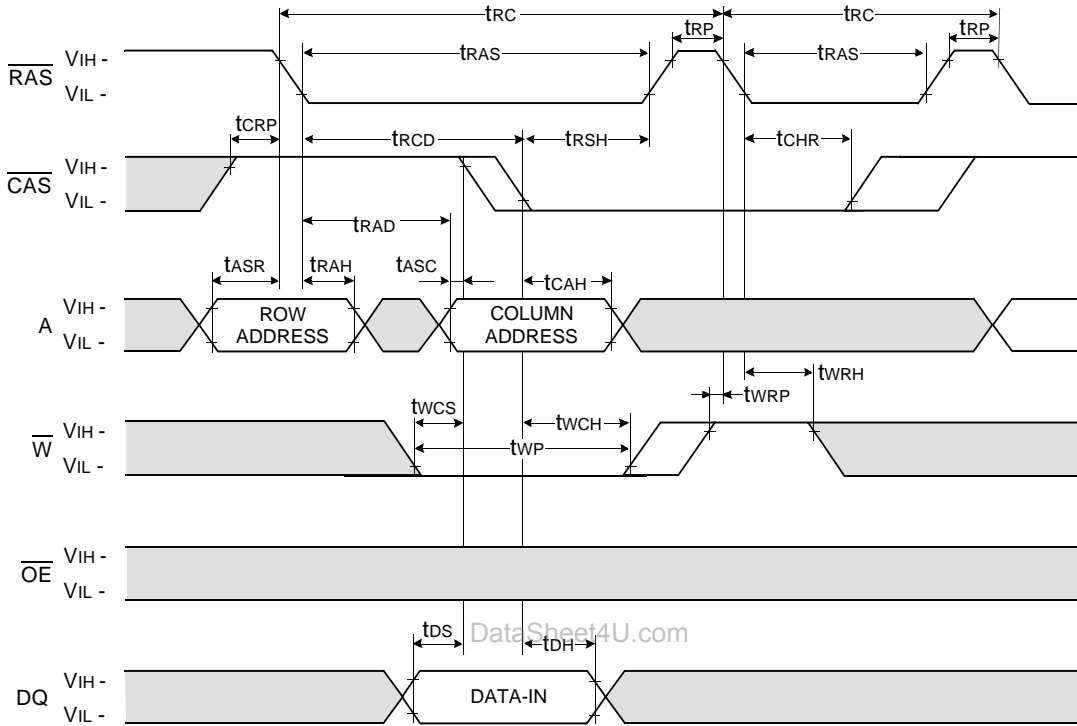


# DRAM MODULE

# M53230804CY0/CT0-C

## HIDDEN REFRESH CYCLE ( WRITE )

NOTE : DOUT = OPEN



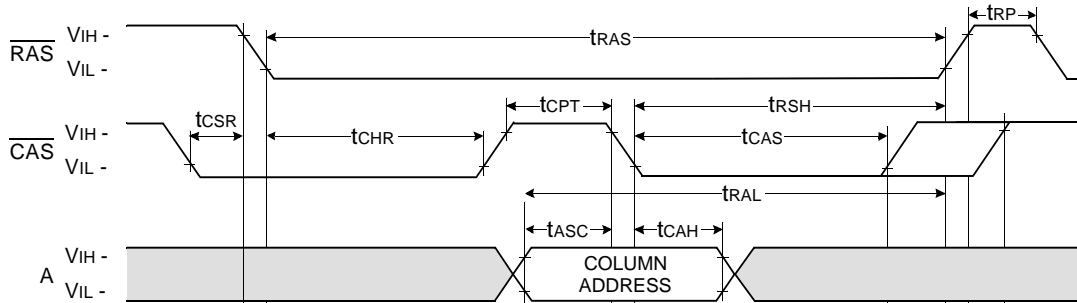
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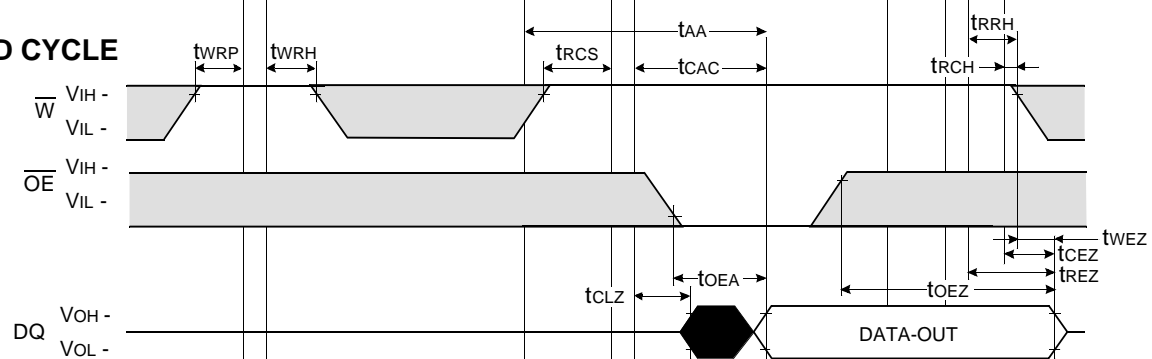
# DRAM MODULE

# M53230804CY0/CT0-C

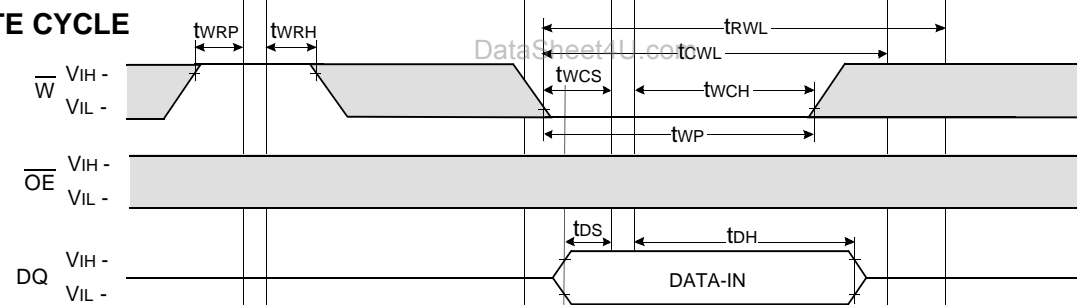
## CAS-BEFORE-RAS REFRESH CYCLE TEST CYCLE



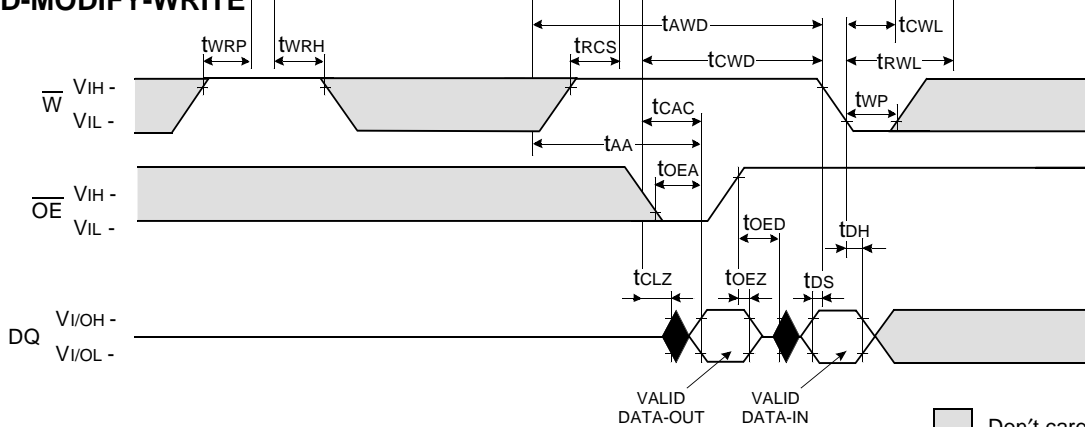
## READ CYCLE



## WRITE CYCLE



## READ-MODIFY-WRITE



NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

Don't care  
 Undefined



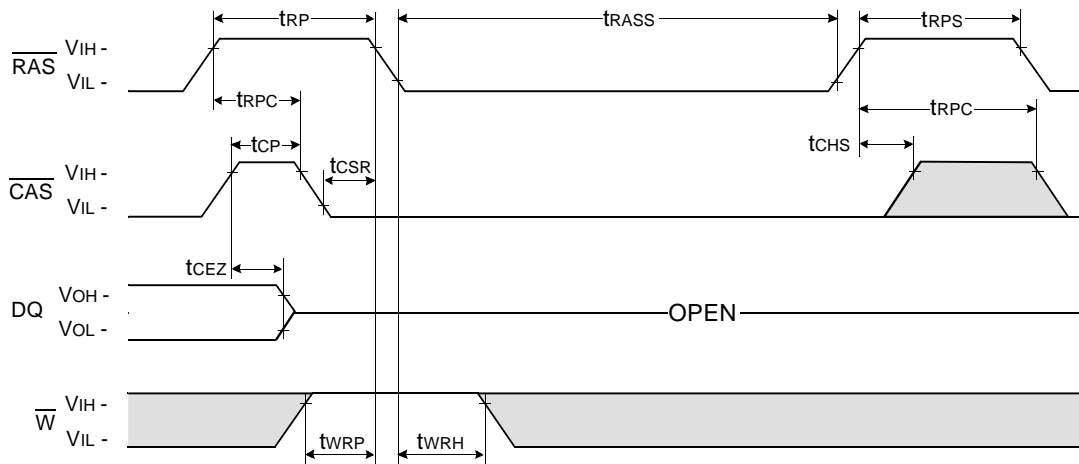
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# DRAM MODULE

# M53230804CY0/CT0-C

## CAS - BEFORE - RAS SELF REFRESH CYCLE

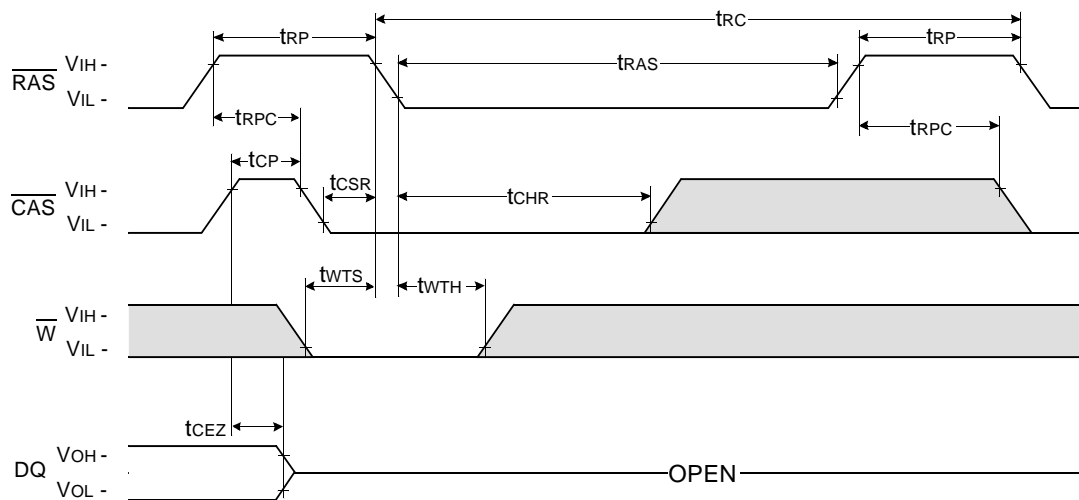
NOTE : OE, A = Don't care



## TEST MODE IN CYCLE

NOTE : OE, A = Don't care

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Don't care  
 Undefined



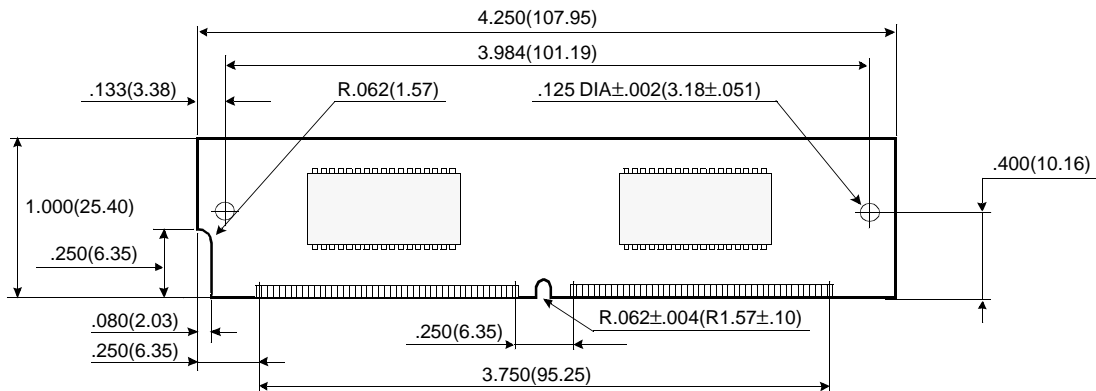
ELECTRONICS

# DRAM MODULE

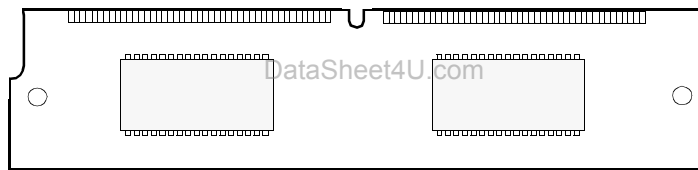
# M53230804CY0/CT0-C

## PACKAGE DIMENSIONS

Units : Inches (millimeters)

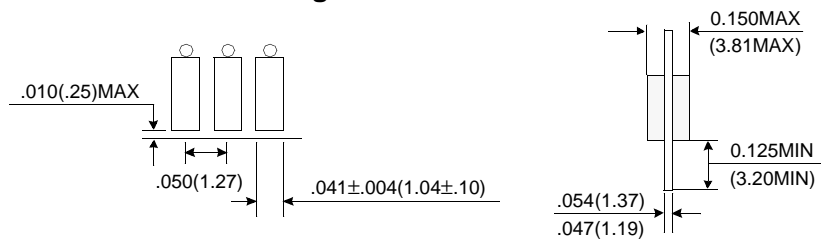


( Front view )



( Back view )

### Gold/Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 4Mx16 DRAM, TSOPII

DRAM Part No. : M53230804CY0/CT0 -- K4E641611C (400 mil)

