PLEASE NOTE:

An EOL notice was issued on this product in 2001. However, ASI has a large amount of die inventory available. For assistance, please contact your local sales representative.

128K x 32 EEPROM

Radiation Tolerant
EEPROM Memory Array

AVAILABLE AS MILITARY SPECIFICATIONS

- MIL-STD-883
- SMD 5962-94585

FEATURES

- Access time of 150ns
- Operation with single 5V + 10% supply
- Power Dissipation:
  Active: 1.43 W (MAX), Max Speed Operation
  Standby: 7.7 mW (MAX), Battery Back-up Mode
- On-Chip Latches: Address, Data, CE\, OE\, WE\
- Automatic Byte Write: 10 ms (MAX)
- Automatic Page Write (128 bytes): 10 ms (MAX)
- Data protection circuit on power on/off
- Low power CMOS
- 10^4 Erase/Write cycles (in Page Mode)
- Software data protection
- TTL Compatible Inputs and Outputs
- Data Retention: 10 years
- Ready/Busy\ and Data Polling Signals
- Write protection by RES\ pin
- Radiation Tolerant: Proven total dose 40K to 100K RADS*
- Operating Temperature Ranges:
  Military: -55°C to +125°C
  Industrial: -40°C to +85°C

OPTIONS MARKINGS

- Timing
  150 ns -150
  200 ns -200
  250 ns -250
- Package
  Ceramic Quad Flat pack Q No. 703
  Ceramic Quad Flat pack QB

GENERAL DESCRIPTION

The Austin Semiconductor, Inc. AS8ER128K32 is a 4 Megabit Radiation Tolerant EEPROM Module organized as 128K x 32 bit. User configurable to 256K x16 or 512Kx 8. The module achieves high speed access, low power consumption and high reliability by employing advanced CMOS memory technology.

The military grade product is manufactured in compliance to MIL-STD 883, making the AS8ER128K32 ideally suited for military or space applications.

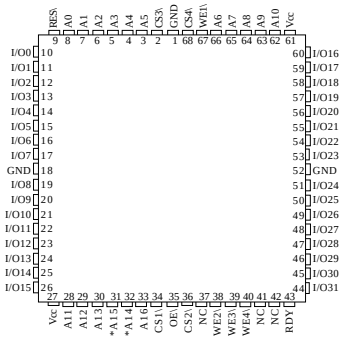
The module is offered as a 68 lead 0.990 inch square ceramic quad flat pack. It has a max. height of 0.200 inch. This package design is targeted for those applications which require low profile SMT Packaging.

** contact factory for test reports. ASI does not guarantee or warrant these performance levels, but references these third party reports.*

PIN ASSIGNMENT

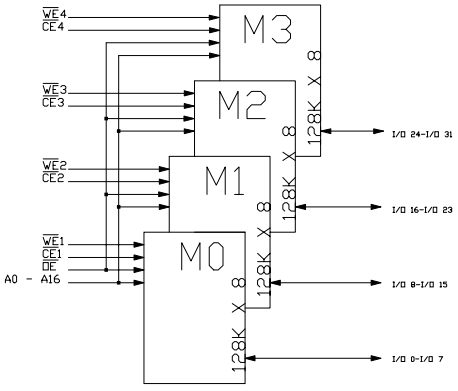
(Top View)

68 Lead CQFP



***Pin #'s 31 and 32, A15 and A14 respectively, are reversed from the AS8E128K32. Correct use of these address lines is required for operation of the SDP mode to work properly.**

PIN NAME	FUNCTION
A0 to A16	Address Input
I/O0 to I/O31	Data Input/Output
OE\	Output Enable
CE\	Chip Enable
WE\	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground
RDY/BUSY\	Ready Busy
RES\	Reset



FUNCTIONAL BLOCK DIAGRAM

For more products and information
please visit our web site at
www.austinsemiconductor.com

TRUTH TABLE

MODE	CE\	OE\	WE\	RES\	RDY/BUSY\[1]	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H[2]	High-Z	Dout
Standby	V_{IH}	X[3]	X	X	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z to V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Wirte Inhibit	X	X	V_{IH}	X	---	---
	X	V_{IL}	X	X	---	---
Data\ Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Dout (I/O7)
Program Reset	X	X	X	V_{IL}	High-Z	High-Z

NOTES: 1. RDY/Busy\ output has only active LOW V_{OL} and high impedance state. It can not go to HIGH (V_{OH}) state.
2. V_{CC} -0.5 < V_H < V_{CC} +1.0
3. X : DON'T CARE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss
Vcc .....-0.6V to +7.0V
Operating Temperature Range(1) .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Voltage on any Pin Relative to Vss.....-0.5V to +7.0V (2)
Max Junction Temperature**.....+150°C
Thermal Resistance junction to case (θ_{JC}):
Package Type Q.....11.3° C/W
Package Type P & PN.....2.8° C/W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow, and humidity (plastics).

NOTES:

1) Including electrical characteristics and data retention.
2) V_{IN} MIN = -3.0V for pulse width < 20ns.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55°C≤T_A≤125°C or -40°C to +85°C; Vcc = 5V ± 10%)

PARAMETER	CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input High Voltage		V_{IH}	2.2	V_{CC} +0.3	V
Input High Voltage (RES\)		V_H	V_{CC} -0.5	V_{CC} +1.0	V
Input Low Voltage		V_{IL}	-0.3[1]	0.8	V
INPUT LEAKAGE CURRENT	OV ≤ V_{IN} ≤ V_{CC}	I_{LI}	-10	10 [2]	µA
OUTPUT LEAKAGE CURRENT	Outputs(s) Disabled, OV ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-10	10	µA
Output High Voltage	I_{OH} = -0.4mA	V_{OH}	2.4	--	V
Output Low Voltage	I_{OL} = 2.1mA	V_{OL}	--	0.4	V
Supply Voltage		V_{CC}	4.5	5.5	V

NOTE: 1) V_{IL} (MIN): -1.0V for pulse width < 20ns.
2) I_{LI} on RES\ : 500µA (MAX)

PARAMETER	CONDITIONS	SYM	MAX -15	UNITS
Power Supply Current: Operating	Iout = 0mA, V_{CC} = 5.5V Cycle = 1µS, Duty = 100%	I_{cc3}	80	mA
	Iout = 0mA, V_{CC} = 5.5V Cycle = MIN, Duty = 100%		260	
Power Supply Current: Standby	CE\ = $V_{CC,}$ V_{CC} = 5.5V	I_{CC1}	1.4	mA
	CE\ = $V_{IH,}$ V_{CC} = 5.5V	I_{CC2}	12	mA

CAPACITANCE TABLE[1] (V_{IN} = 0V, f = 1 MHz, T_A = 25°C)

SYMBOL	PARAMETER	MAX	UNITS
C_{ADD}	A0 - A16 Capacitance	40	pF
C_{OE}	OE\, RES\, RDY Capacitance	40	pF
$C_{WE,}$ C_{CE}	WE\ and CE\ Capacitance	12	pF
C_{IO}	I/O 0- I/O 31 Capacitance	20	pF

NOTE: 1. This parameter is guaranteed but not tested.

AC TEST CHARACTERISTICS

TEST SPECIFICATIONS

Input pulse levels.....V_{SS} to 3V
Input rise and fall times.....5ns
Input timing reference levels.....1.5V
Output reference levels.....1.5V
Output load.....See Figure 1

NOTES:
Vz is programmable from -2V to + 7V.
I_{OL} and I_{OH} programmable from 0 to 16 mA.
Vz is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.

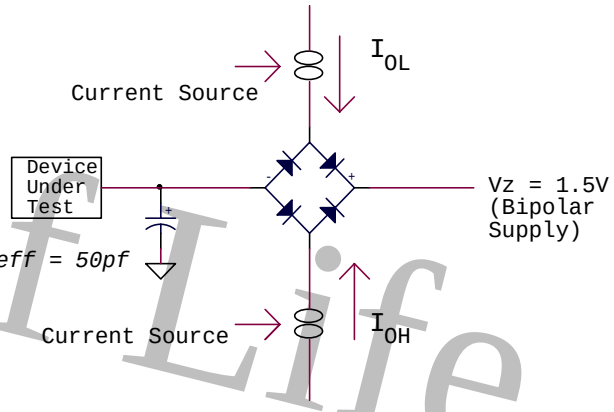


Figure 1

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(-55°C ≤ T_A ≤ +125°C or -40°C to +85°C; Vcc = 5V ±10%)

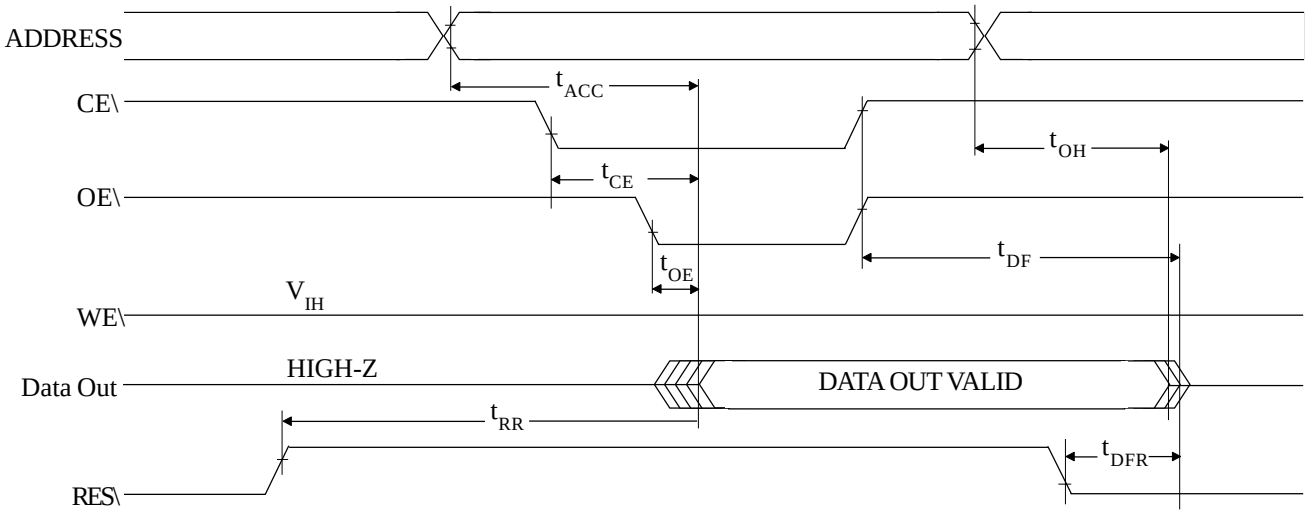
DESCRIPTION	TEST CONDITIONS	SYMBOL	150		UNITS
			MIN	MAX	
Address to Output Delay	CE\ = OE\ = V_{IL}, WE\ = V_{IH}	t_{ACC}		150	ns
CE\ to Output Delay	OE\ = V_{IL}, WE\ = V_{IH}	t_{CE}		150	ns
OE\ to Output Delay	OE\ = V_{IL}, WE\ = V_{IH}	t_{OE}	10	75	ns
Address to Output Hold	CE\ = OE\ = V_{IL}, WE\ = V_{IH}	t_{OH}	0		ns
CE\ or OE\ high to Output Float (1)	OE\ = V_{IL}, WE\ = V_{IH}	t_{DF}	0	50	ns
RES\ low to Output Float (1)	CE\ = OE\ = V_{IL}, WE\ = V_{IH}	t_{DFR}	0	350	ns
RES\ to Output Delay	CE\ = OE\ = V_{IL}, WE\ = V_{IH}	t_{RR}	0	450	ns

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC WRITE CHARACTERISTICS

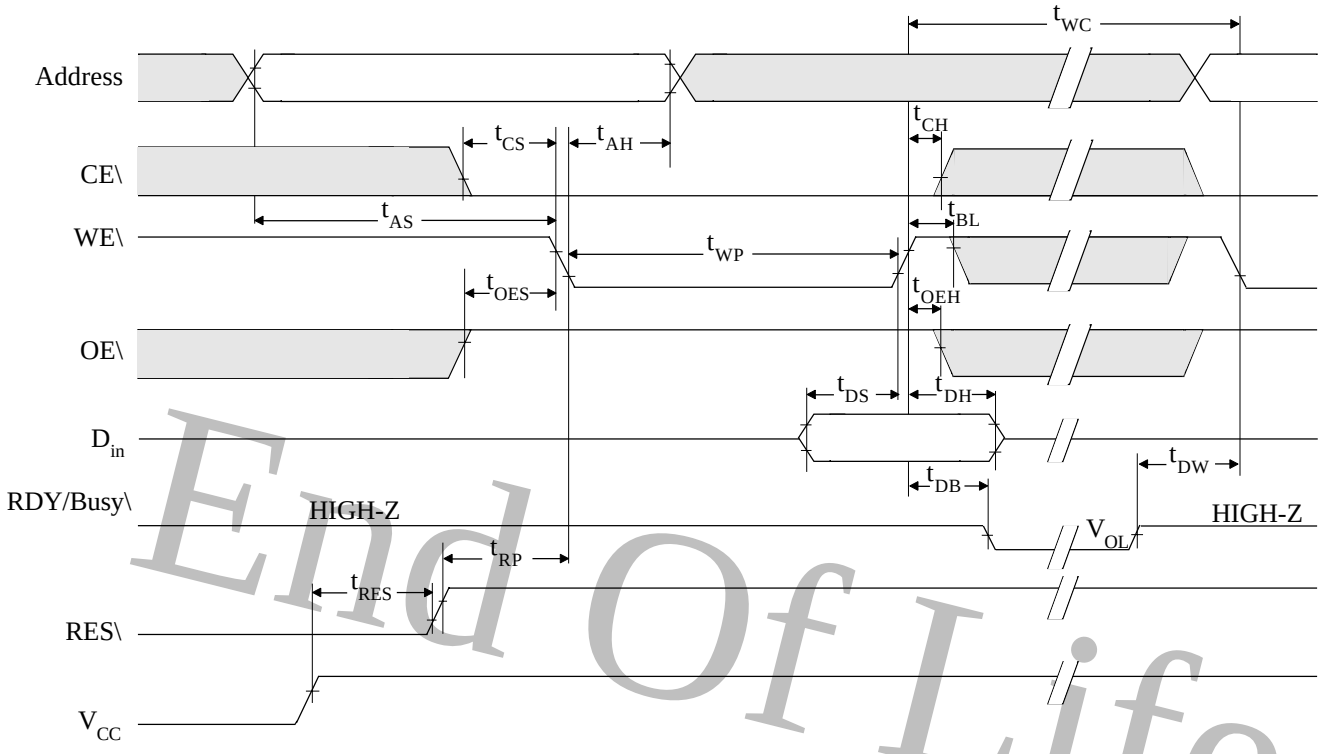
($-55^{o}C \leq T_A \leq +125^{o}C$; Vcc = 5V ±10%)

SYMBOL	PARAMETER	MIN[2]	MAX	UNITS
t_{AS}	Address Setup Time	0		ms
t_{AH}	Address Hold Time	150		ns
t_{CS}	CE\ to Write Setup Time (WE\ controlled)	0		ns
t_{CH}	CE\ Hold Time (WE\ controlled)	0		ns
t_{WS}	WE\ to Write Setup Time (CE\ controlled)	0		ns
t_{WH}	WE\ to Hold Time (CE\ controlled)	0		ns
t_{OES}	OE\ to Write Setup Time	0		ns
t_{OEH}	OE\ to Hold Time	0		ns
t_{DS}	Data Setup Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	WE\ Pulse Width (WE\ controlled)	250		ns
t_{CW}	CE\ Pulse Width (CE\ controlled)	250		ns
t_{DL}	Data Latch Time	300		ns
t_{BLC}	Byte Load Cycle	0.55	30	µs
t_{BL}	Byte Load Window	100		µs
t_{WC}	Write Cycle Time		10 [3]	ms
t_{DB}	Time to Device Busy	120		ns
t_{DW}	Write Start Time	150 [4]		ns
t_{RP}	Reset Protect Time	100		µs
t_{RES}	Reset High Time [5]	1		µs

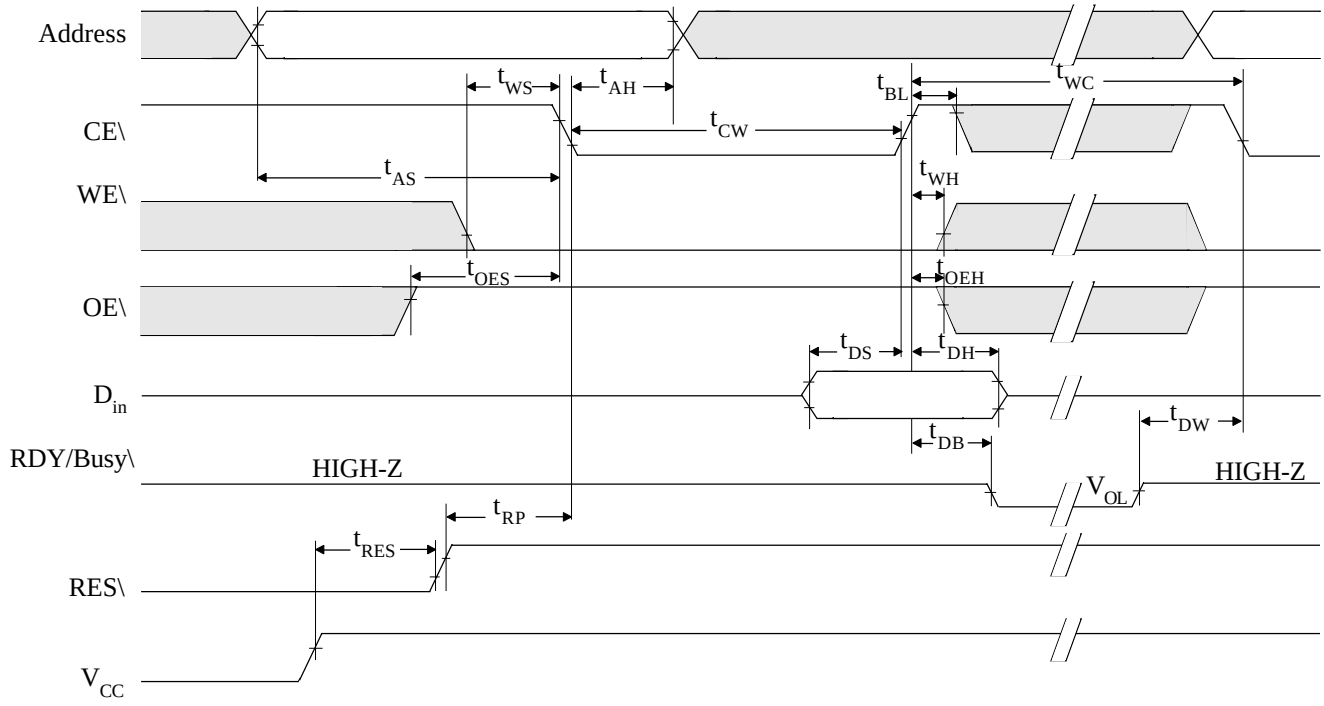
READ TIMING WAVEFORM



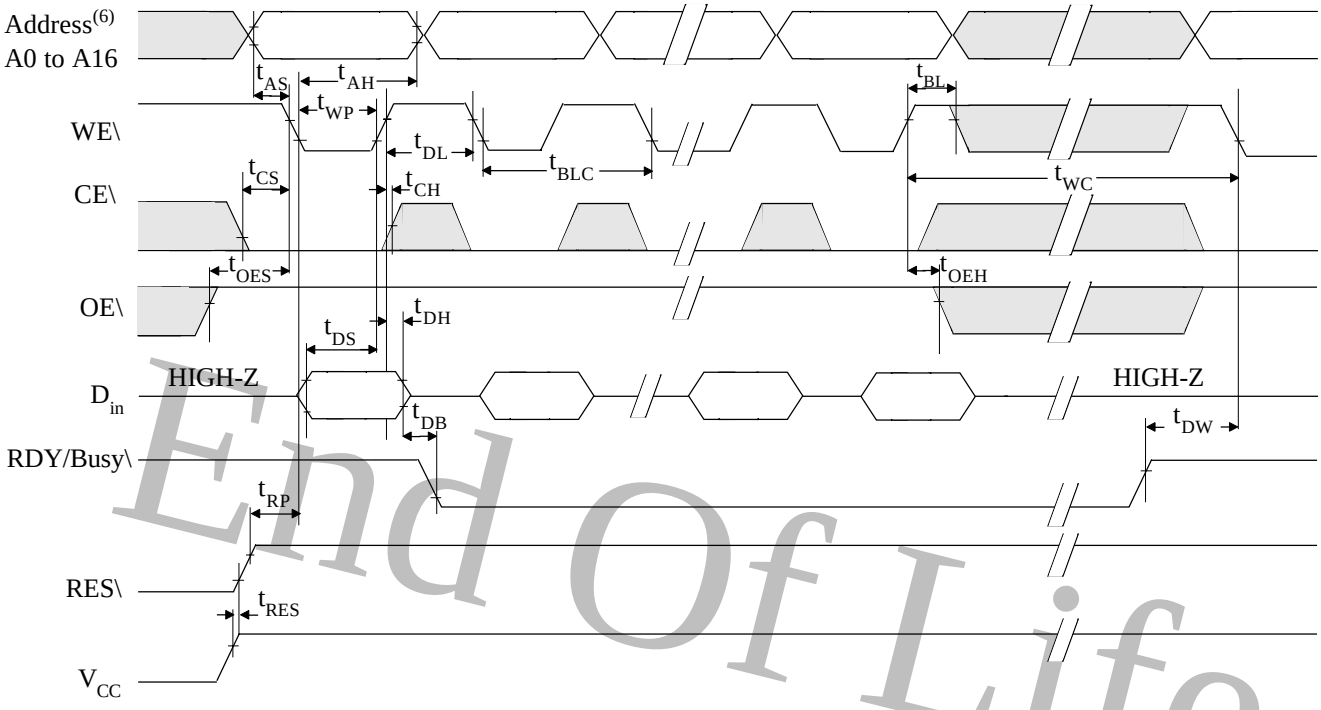
BYTE WRITE TIMING WAVEFORM (WE\ CONTROLLED)



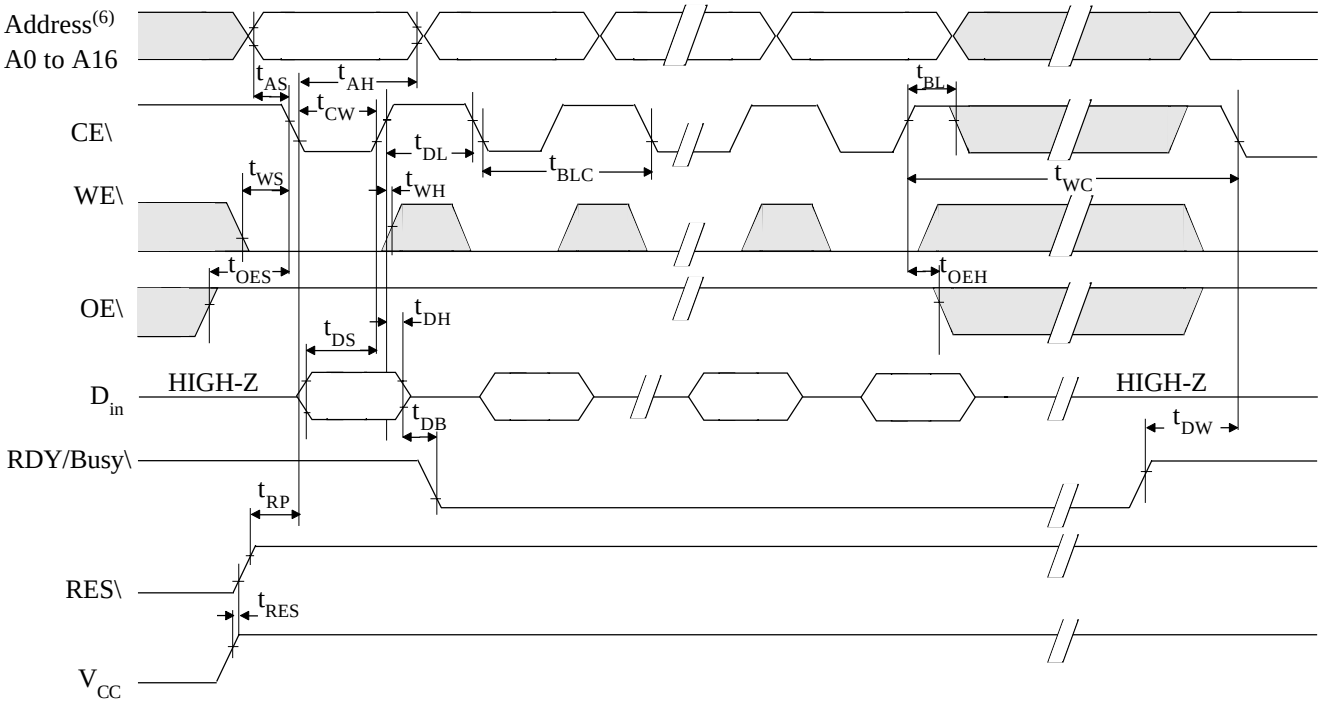
BYTE WRITE TIMING WAVEFORM (CE\ CONTROLLED)



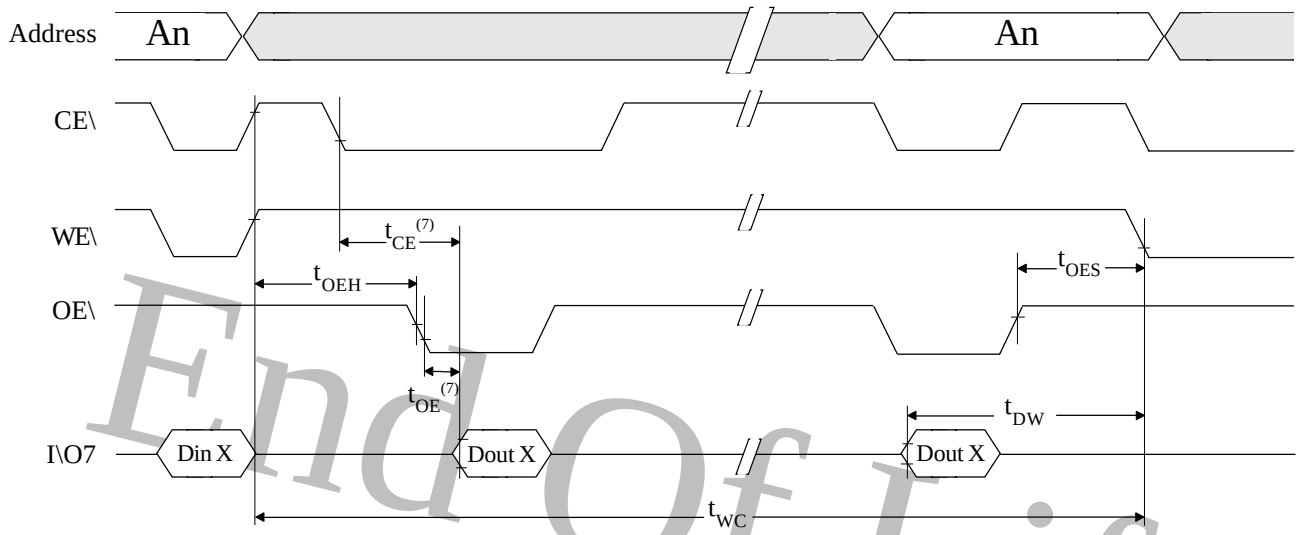
PAGE WRITE TIMING WAVEFORM (WE\ CONTROLLED)



PAGE WRITE TIMING WAVEFORM (CE\ CONTROLLED)



DATA POLLING TIMING WAVEFORM



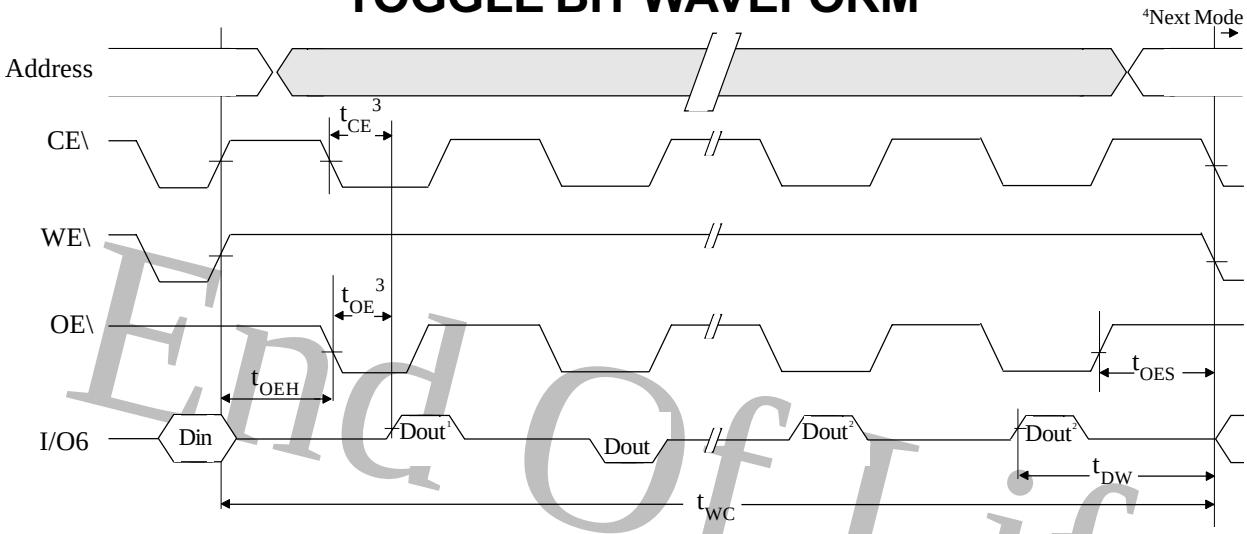
NOTES:

1. t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.
2. Use this device in longer cycle than this value.
3. t_{WC} must be longer than this value unless polling techniques or RDY/Busy\ are used. This device automatically completes the internal write operation within this value.
4. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/Busy\ are used.
5. This parameter is sampled and not 100% tested.
6. A7 to A16 are page addresses and must be same within the page write operation.
7. See AC read characteristics.

TOGGLE BIT

This device provides another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O6 will charge from "1" to "0" (toggling) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

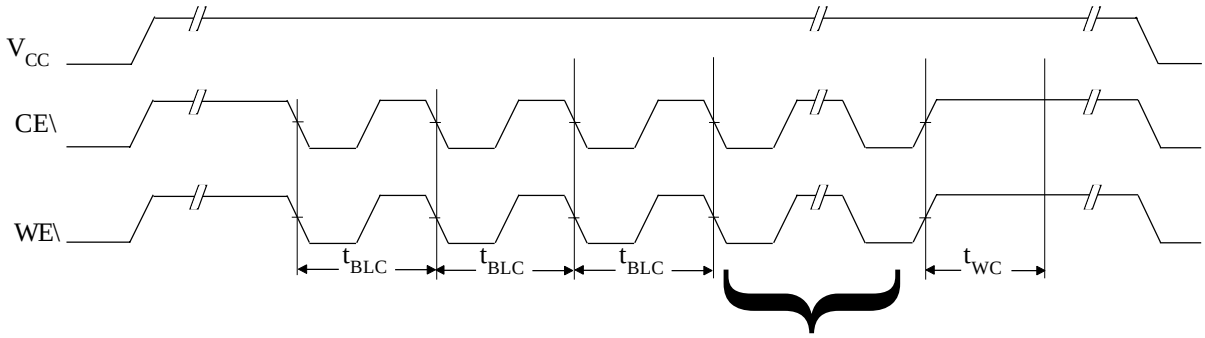
TOGGLE BIT WAVEFORM



NOTES:

1) I/O6 beginning state is "1".
2) I/O6 ending state will vary.
3) See AC read characteristics.
4) Any locations can be used, but the address must be fixed.

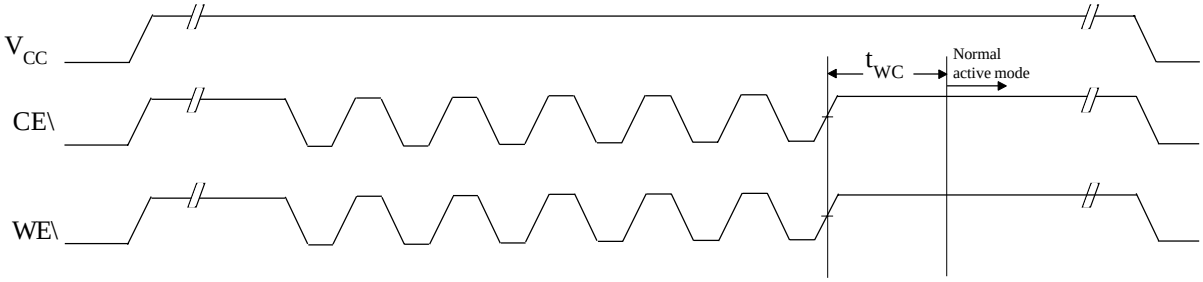
SOFTWARE DATA PROTECTION TIMING WAVEFORM (In protection mode)



Address	5555	AAAA or 2AAA	5555	Write Address*
Data (each byte)	AA	55	A0	Write Data

** During this write cycle, data is physically written to the address provided.*

SOFTWARE DATA PROTECTION TIMING WAVEFORM (In non-protection mode)



Address	5555	AAAA or 2AAA	5555	5555	AAAA or 2AAA	5555
Data (each byte)	AA	55	80	AA	55	20

FUNCTIONAL DESCRIPTION

Automatic Page Write

Page-mode write feature allows 1 to 128 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 128 bytes can be written in the same manner. Each additional byte load cycle must be started within 30µs from the preceding falling edge of WE\ or CE\. When CE\ or WE\ is kept high for 100µs after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

DATA\ Polling

DATA\ polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during the write cycle, an inversion of the last byte of data to be loaded outputs from I/O's 7, 15, 23, and 31 to indicate that the EEPROM is performing a write operation.

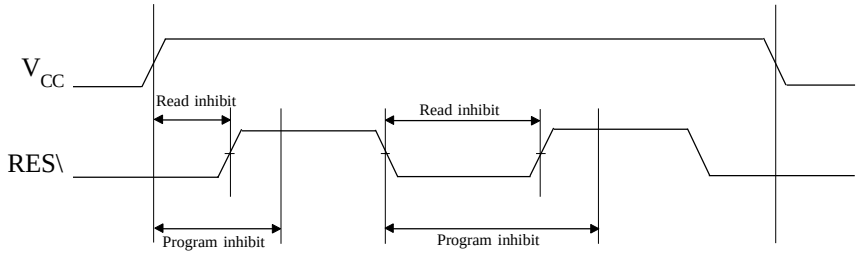
RDY/Busy\ Signal

RDY/Busy\ signal also allows status of the EEPROM to be determined. The RDY/Busy\ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of write cycle, the RDY/Busy\ signal changes state to high impedance.

RES\ Signal

When RES\ is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping RES\ low when V_{CC} is switched. RES\ should be high during read and programming because it doesn't provide a latch function. See timing diagram below.

RES\ Signal Diagram



WE\, CE\ Pin Operation

During a write cycle, address are latched by the falling edge of WE\ or CE\, and data is latched by the rising edge of WE\ or CE\.

Write/Erase Endurance and Data Retention Time

The endurance is 10^4 cycles in case of the page programming and 10^3 cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

RDY/Busy\ SIGNAL

RDY/Busy\ signal also allows status of the EEPROM to be determined. The RDY/Busy\ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of the write cycle, the RDY/Busy\ signal changes state to high impedance. This allows many 58C1001 devices RDY/Busy\ signal lines to be wired-OR together.

PROGRAMMING/ERASE

The 58C1001 does **NOT** employ a BULK-erase function. The memory cells can be programmed '0' or '1'. A write cycle performs the function of erase & write on every cycle with the erase being transparent to the user. The internal erase data state is considered to be '1'. To program the memory array with background of ALL 0's or All 1's, the user would program this data using the page mode write operation to program all 1024 128-byte pages.

Data Protection

1. ***Data Protection against Noise on Control Pins (CE\, OE\, WE\) During Operation***

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, this device has a noise cancellation function that cuts noise if its width is 20ns or less in program mode.

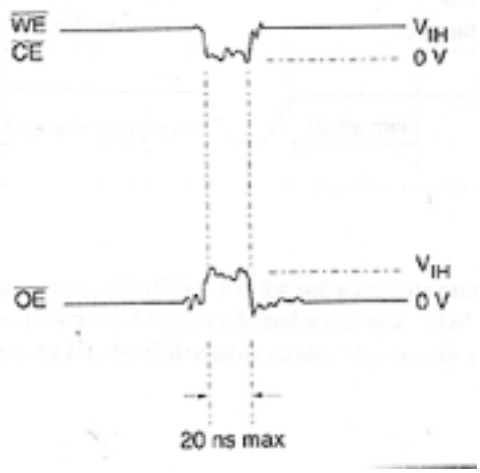
Be careful not to allow noise of a width more than 20ns on the control pins. See Diagram 1 below.

2. ***Data Protection at V_{CC} On/Off***

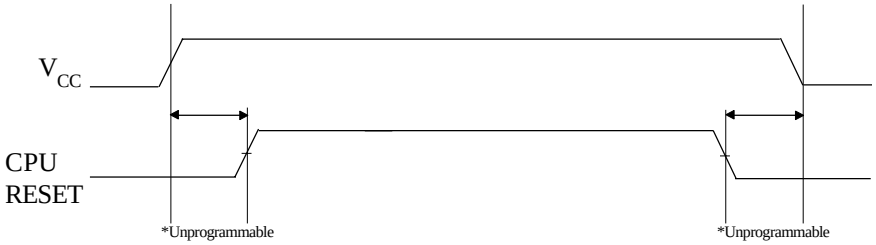
When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc.) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPR is in an unstable state.

NOTE: The EEPROM should be kept in unprogrammable state during V_{CC} on/off by using CPU RESET signal. See the timing diagram below.

DIAGRAM 1



DATA PROTECTION AT V_{CC} ON/OFF



Data Protection Cont.

a. *Protection by RES*

The unprogrammable state can be realized by the CPU's reset signal inputs directly to the EEPROM's RES pin. RES should be kept V_{SS} level during V_{CC} on/off.

The EEPROM brakes off programming operation when RES becomes low, programming operation doesn't finish correctly in case that RES falls low during programming operation. RES should be kept high for 10ms after the last data inputs. See the timing diagram below.

3. ***Software data protection***

To prevent unintentional programming, this device has the software data protection (SDP) mode. The SDP is enabled by inputting the 3 bytes code and write data in Chart 1. SDP is not enabled if only the 3 bytes code is input. To program data in the SDP enable mode, 3 bytes code must be input before write data. This 4th cycle during write is required to initiate the SDP and physically writes the address and data. While in SDP the entire array is protected in which writes can only occur if the exact SDP sequence is re-executed or the unprotect sequence is executed.

The SDP is disabled by inputting the 6 bytes code in Chart 2. Note that, if data is input in the SDP disable cycle, data can not be written.

The software data protection is not enabled at the shipment.

NOTE: These are some differences between ASI's and other company's for enable/disable sequence of software data protection. If these are any questions, please contact ASI.

PROTECTION BY RES*

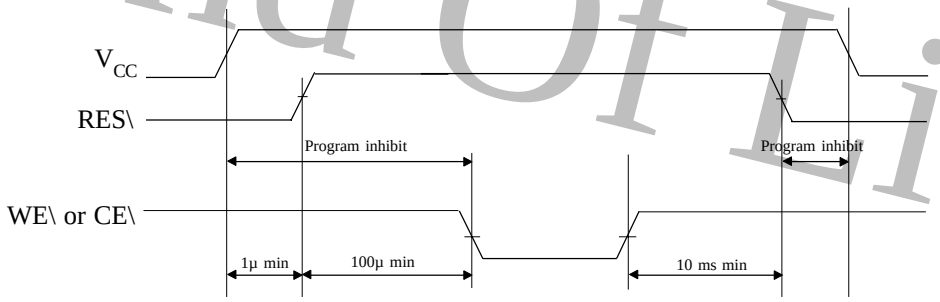


CHART 1

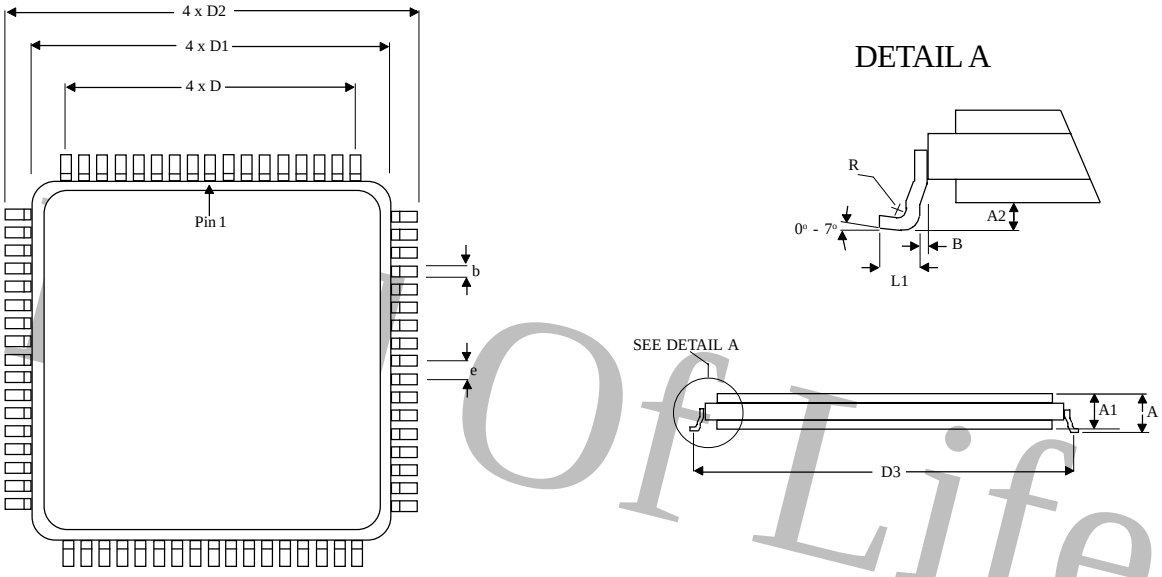
Address	Data (each Byte)	
5555	AA	
↓	↓	
AAAA or 2AAA	55	
↓	↓	
5555	A0	
↓	↓	
Write Address	Write Data}	Normal data input

CHART 2

Address	Data (each Byte)
5555	AA
↓	↓
AAAA or 2AAA	55
↓	↓
5555	80
↓	↓
5555	AA
↓	↓
AAAA or 2AAA	55
↓	↓
5555	20

MECHANICAL DEFINITIONS*

ASI Case #703 (Package Designator Q)

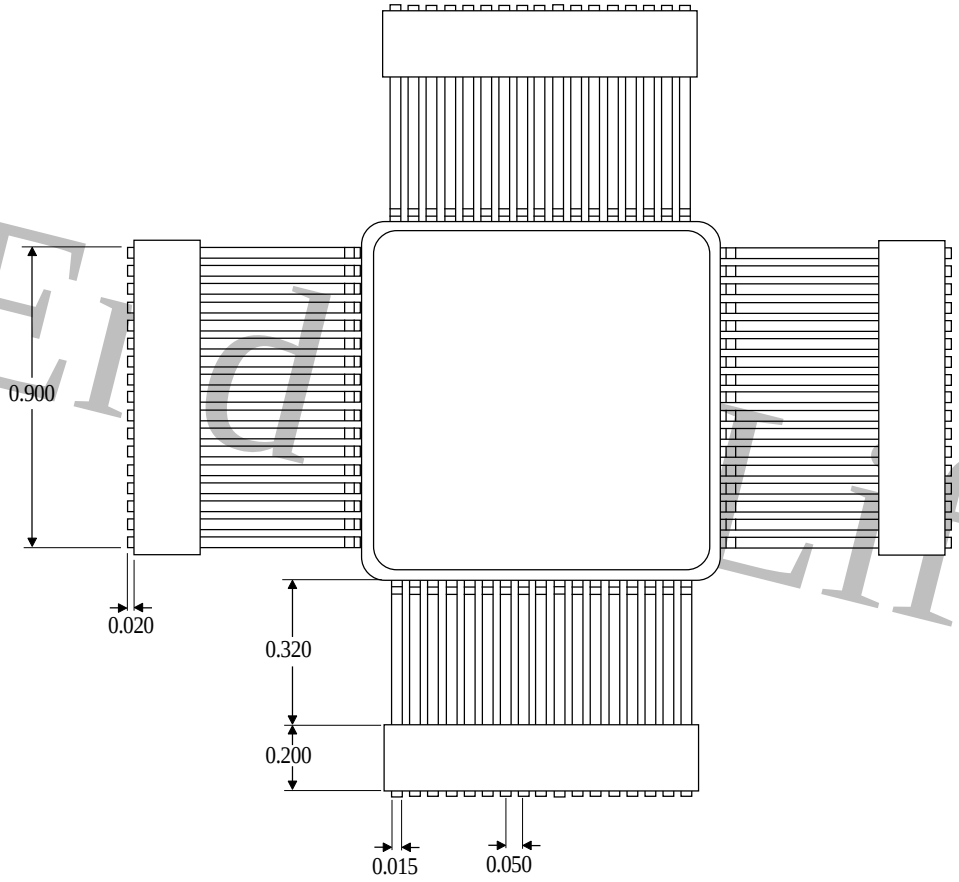


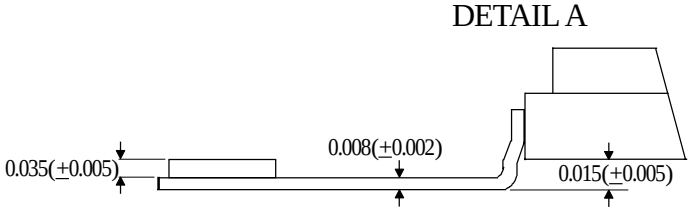
SYMBOL	ASI PACKAGE SPECIFICATIONS	
	MIN	MAX
A	0.123	0.200
A1	0.118	0.186
A2	0.000	0.020
b	0.013	0.017
B	0.010 REF	
D	0.800 BSC	
D1	0.870	0.890
D2	0.980	1.000
D3	0.936	0.956
e	0.050 BSC	
R	0.005	
L1	0.035	0.045

All measurements are in inches.

MECHANICAL DEFINITIONS*

ASI Case (Package Designator QB)





All measurements are in inches.

ORDERING INFORMATION

EXAMPLE: AS8ER128K32Q-15/IT

Device Number	Package Type	Speed ns	Process
AS8ER128K32	Q	-150	/*
AS8ER128K32	Q	-200	/*
AS8ER128K32	Q	-250	/*

EXAMPLE: AS8ER128K32QB-250/XT

Device Number	Package Type	Speed ns	Process
AS8ER128K32	QB	-150	/*
AS8ER128K32	QB	-200	/*
AS8ER128K32	QB	-250	/*

*AVAILABLE PROCESSES

IT = Industrial Temperature Range	-40°C to +85°C
XT = Extended Temperature Range	-55°C to +125°C
883C = Full Military Processing	-55°C to +125°C

ASI TO DSCC PART NUMBER CROSS REFERENCE*

Package Designator Q

ASI Part #	SMD Part
AS8ER128K32Q-250/883C	5962-9458507HMX
AS8ER128K32Q-200/883C	5962-9458508HMX
AS8ER128K32Q-150/883C	5962-9458509HMX

Package Designator QB

ASI Part #	SMD Part
AS8ER128K32QB-250/883C	5962-9458507HZC
AS8ER128K32QB-200/883C	5962-9458508HZC
AS8ER128K32QB-150/883C	5962-9458509HZC

** ASI part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.*