VIDEO AND SYSTEM CONTROLLER

FEATURES

- Full bit-map organization
- Direct interface for 680XX bus compatible devices
- Screen resolution: up to 768 x 560 pixels
- 4 or 8 bits per pixel
- Capability to display run-length code files
- Mosaic effect
- Shift register for up to 15 MHz pixel rate
- On-chip oscillator circuitry
- Synchro generator for 50 and 60 Hz scan
- Double frequency scan
- Synchronization with external video
- 1.5 MByte DRAM direct drive
- 1 MBit device support
- 0.5 MByte ROM control
- 1 KByte I/O control
- Reset sequencer, including ROM shadowing
- Watch-dog timer
- Fast 16-bit PIXEL test-and-modify logic (PIXBLT)
- CMOS technology
- 120-pin quad flat-pack plastic package

APPLICATIONS

- CD-I video controller
- Home computers
- Personal computers
- Home entertainment
- Intelligent colour terminals
- Graphics, text, I/O systems
- Frame grabbing
- Industrial man machine interface

GENERAL DESCRIPTION

The SCC66470 is a CMOS Video and System Controller (VSC), integrating a high resolution bit mapped colour display and a 680XX family system controller. The SCC66470 drastically reduces system costs.

The SCC66470 can directly drive up to 2 Mbytes of memory and provides chip-select signals for both system ROM and peripherals. The on-chip DRAM controller can support up to 1.5 MByte DRAM and controls access to the combined system/video DRAM. The CPU can access any memory location even during active video display lines, thus improving system performance.

The display timing is compatible with European, Japanese and USA standards for TV and VIDEOTEX applications. The resolution is programmable up to 768 x 560 and the number of bits per pixel may be 4 or 8 corresponding to an 8 or 256 colour display. The number of colours can be increased further by an additional slave SCC66470 to achieve studio quality pictures. A real time file decoder permits the display of run-length and mosaic compressed files. High-speed pixel manipulation logic (PIXAC) is provided on-chip to accelerate image manipulation and the memory organization is such that a full pixel blitter is implemented.

A coprocessor interface is provided to allow very high speed memory access and manipulation. This allows a huge mailbox for a host computer and the use of specialized processors. PIXAC is usable from this interface.

PACKAGE OUTLINE

120-lead quad flat-pack (QFP); plastic (SOT220B)

ORDERING INFORMATION

EXTENDED TYPE NUMBER	TEMPERATURE RANGE (°C)	CLOCK FREQUENCY (MHz)	PACKAGE CODE
SCC66470 CAB/03	0 to 70	30.3	SOT220B
SCC66470 AAB/03	−40 to +85	30.3	SOT220B

INTEGRATED CIRCUITS IC21

9397 319 30011

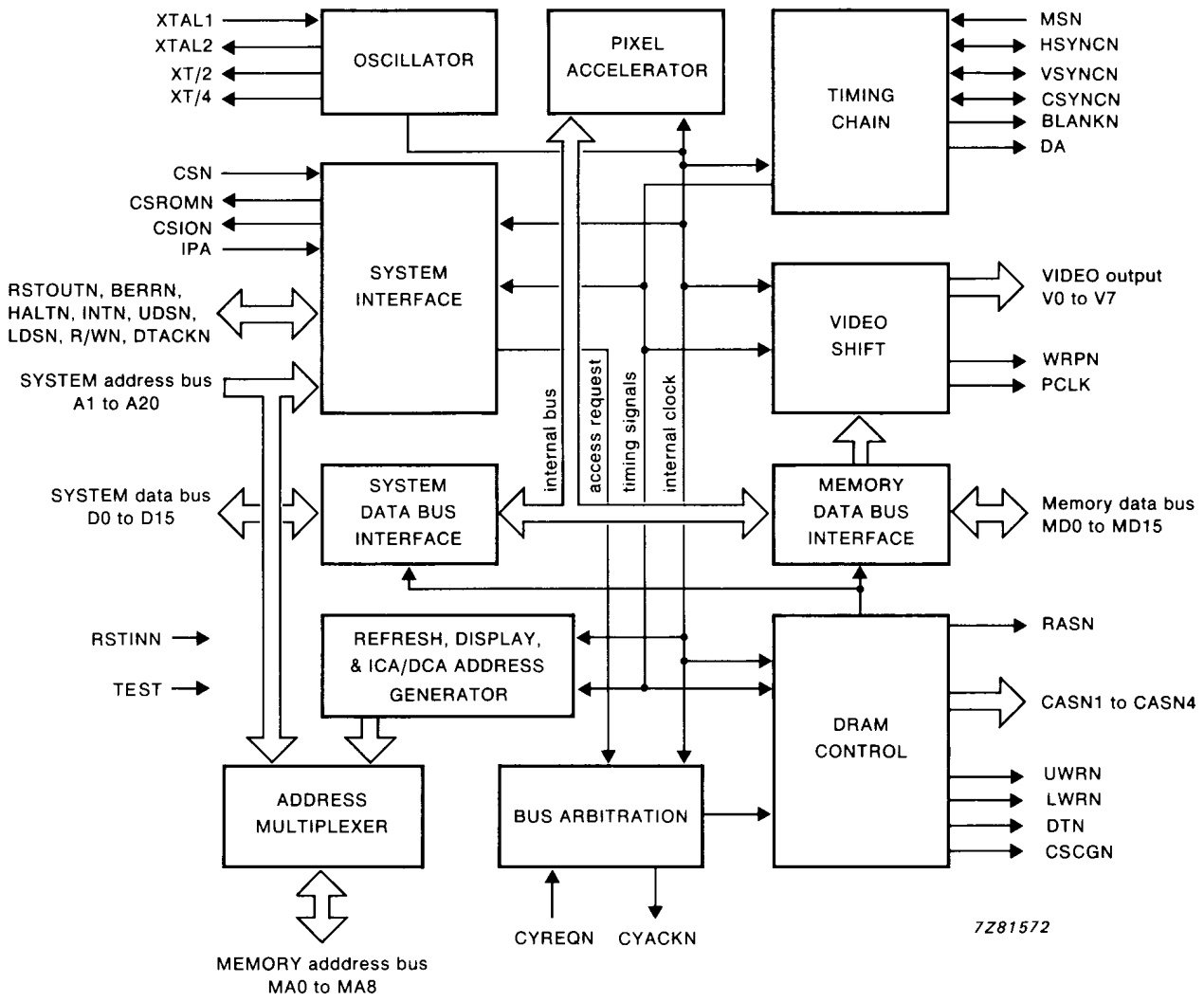


Fig.1 Block diagram.

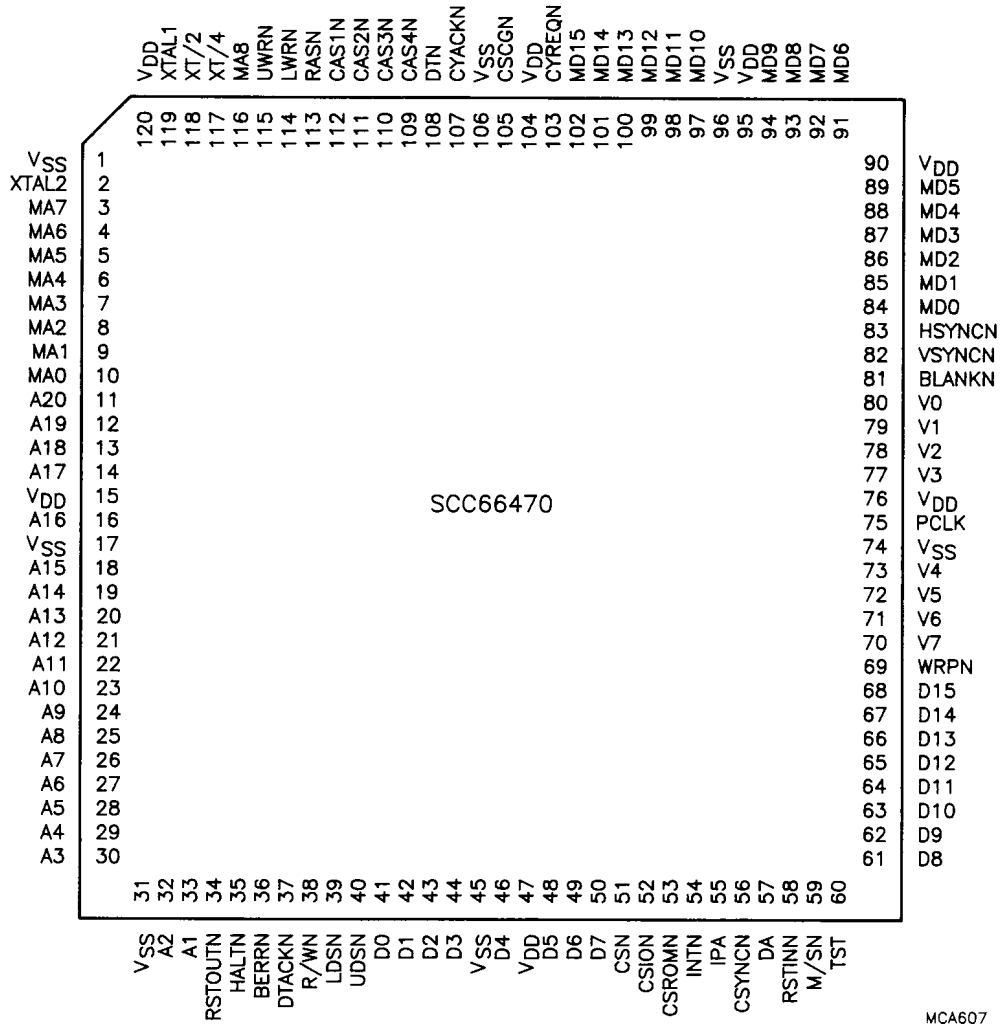


Fig.2 Pinning diagram.

SIGNAL DESCRIPTION

Signals ending in 'N' are active low, all other signals are active high. The terms active, inactive, asserted and negated are used in the signal description independent of whether the signal is active in the HIGH state (logic 1) or in the LOW state (logic 0). The definition of the active level of each signal may be found in the individual signal descriptions.

MNEMONIC	TYPE	PIN NO	FUNCTION
			System bus
A1-A20	I	33, 32, 30-18, 16, 14-11	System address bus. A1 to A20 provide the system address during system bus accesses. The address bus must be stable when UDSN and/or LDSN are asserted.
D0-D15	I/O	61-68, 50-48, 46, 44-41	Data bus (bidirectional, 3-state). Used to transfer data between the system bus and the SCC66470. The SCC66470 drives the data bus during read cycles. The data bus must be stable when UDSN and/or LDSN are asserted for a write cycle.
UDSN	I	40	Upper Data Strobe (active LOW). When asserted, UDSN indicates that data is being addressed on D8 to D15.
LDSN	I	39	Lower Data Strobe (active LOW). When asserted, LDSN indicates that data is being addressed on D0 to D7.
R/WN	I	38	Read/Write. This input indicates the transfer direction on the system bus. When LOW, data is being written into SCC66470 controlled resources or internal registers.
CSN	I	51	Chip Select (active LOW). When asserted, data transfer between System bus and SCC66470 controlled resources, is enabled. Validates address decode for system access.
DTACKN	I/O	37	Data Transfer Acknowledge (active LOW, open drain). Asserted by the SCC66470 when the system bus cycle can be continued. This pin must be pulled up.
RSTOUTN	O	34	RESET Output (active LOW, 3-state). Asserted by the SCC66470 Reset Sequencer during the reset procedure. Internally pulled up.
HALTN	O	35	HALT (active LOW, 3-state). Asserted by the SCC66470 Reset Sequencer during the reset procedure. Internally pulled up.
BERRN	O	36	BUS ERROR (active LOW, 3-state). Asserted by the SCC66470 if UDSN or LDSN are still asserted at the end of the time-out period. Internally pulled up.
CSROMN	O	53	Chip Select ROM (active LOW). The SCC66470 asserts CSROM during a system bus access in the ROM address area when UDSN and/or LDSN are asserted.
CSION	O	52	Chip Select I/O (active LOW). Asserted by the SCC66470 during a system bus access in the external I/O area when UDSN and/or LDSN are asserted.
INTN	O	54	Interrupt request (active LOW, open drain). This output is used to generate interrupt requests to the CPU. Internally pulled up.

MNEMONIC	TYPE	PIN NO	FUNCTION
IPA	I	55	Implicit Pixel accelerator addressing (active HIGH). Used by the CPU to implicitly address the SCC66470 pixel accelerator to increase manipulation speed.
			Dynamic RAM interface
MA0-MA8	I/O	10-3, 116	Memory Address lines (3-state). Multiplexed ROW/COLUMN address line outputs for DRAM control. Only MA0 to MA7 are significant when 64K DRAMs are used. MA0 - MA8 are the least significant bits for address input bits (A1 to A9) from a coprocessor when CYACKN output is asserted.
MD0-MD15	I/O	84-89, 91-94 97-102	Memory Data bus (bidirectional, 3-state). Used to transfer data between DRAM bus and the SCC66470. MD0 - MD15 are stable when UWRN and LWRN are asserted. MD0 - MD15 also function as address and control inputs during coprocessor cycle.
RASN	O	113	Row Address Strobe (active LOW). RASN is also used for coprocessor handshaking.
CAS1N-CAS4N	I/O	112-109	Column Address Strobes (active LOW). Column address strobes for memory banks 1 to 4. On the falling edge of CASnN the column address of memory bank n becomes valid. In the 256K mode, CAS4N HIGH indicates a display, ICA/DCA or refresh window. CAS4N in the high impedance state indicates a CPU or coprocessor window. CAS1N to CAS4N are inputs during reset sequence to select/deselect corresponding memory bank.
CSCGN	O	105	Chip Select Character ROM (active LOW). Used only with the coprocessor interface.
UWRN	O	115	Upper Write signal (active LOW). UWRN is asserted when the most significant DRAM byte is being written.
LWRN	O	114	Lower Write signal (active LOW). LWRN is asserted when the least significant DRAM byte is being written.
DTN	O	108	Data Transfer (active LOW). Used to initialize the serial port of dual port VRAMs.
			CRT controller interface
V0-V7	O	80-77, 73-70,	Video output (3-state). V0 - V7 are used to output pixels or control words.
PCLK	O	75	Pixel Clock (3-state). On the rising edge of PCLK the video output lines (V0 - V7) are valid.
WRPN	O	69	Write Palette (active LOW, 3-state). When WRPN is active the data available on V0-V7 is control information. Used with an external palette or a back-end chip.

MNEMONIC	TYPE	PIN NO	FUNCTION
VSYNCN	I/O	82	Vertical Synchronization (active LOW, 3-state). In Master mode, this output is used as a Vertical synchronization signal for the monitor. In Slave TV mode or in Slave Dual mode it becomes a vertical synchronization Input.
HSYNCN	I/O	83	Horizontal Synchronization (active LOW, 3-state). In the Master mode or Slave TV mode, HSYNSN is used as a horizontal synchronization output signal. In Slave dual mode it becomes a horizontal synchronization input.
CSYNCN	I/O	56	Composite Synchronization (active LOW, 3-state). Internally pulled-up. In the Master mode, CSYNSN generates the composite synchronization output signal. In the Slave TV mode, CSYNCN generates a symmetrical signal which generates a horizontal frequency. In the Slave Dual mode it generates the phase error between the master SCC66470 and the slave SCC66470. When the display is disabled this input is used to initialize the synchronization mode.
BLANKN	O	81	Blanking output (active LOW, 3-state). BLANKN is asserted during vertical and horizontal blanking periods. At all other times, it is HIGH.
DA	O	57	Display Active (active HIGH, 3-state). DA is low during the vertical retrace period. DA is in the high impedance state during the horizontal retrace period and HIGH at all other times.
M/SN	I	59	Master/Slave input. The Master mode is selected when M/SN is HIGH.
			Coprocessor handshake
CYREQN	I	103	Cycle Request (active LOW). When CYREQN is asserted, an information transfer cycle for the coprocessor is provoked.
CYACKN	O	107	Cycle Acknowledge (active LOW). CYACKN is used for coprocessor handshaking.
			Miscellaneous signals
XTAL1	I	119	Crystal Oscillator Input. XTAL1 may also be used to input an external clock signal.
XTAL2	O	2	Crystal Oscillator Output.
RSTINN	I	58	Reset Input (active LOW). Schmitt trigger input. RSTINN is used to initiate a reset sequence and is pulled HIGH by an internal pull-up resistor.
XT/2	O	118	Xtal/2 clock output. Output frequency = $f_{OSC}/2$.
XT/4	O	117	Xtal/4 clock output. Output frequency = $f_{OSC}/4$.
TST	I	60	Test (active HIGH). Tied to V_{SS} for normal operation.
V_{DD}	I	15, 47, 76, 90, 95, 104, 120	Power supply pins.
V_{SS}	I	1, 17, 31, 45, 74, 96, 106	Ground pins.

Note

All pins are TTL compatible, except for XTAL1 and XTAL2, which are CMOS compatible.

FUNCTIONAL DESCRIPTION

The SCC66470 performs the following functions:

System control: Integrates the necessary functions for a minimal system.

Dynamic RAM Control: Direct drive for several types of DRAM.

Display Control: On-chip timing chain, video address generator and shift register. A special reload mechanism permits the use of dynamic control words during the display.

Display file decoder: Permits the display of either bit-map files, run-length files or mosaic files.

Pixel Accelerator: On-chip logic optimized for image manipulation.

Coprocessor Interface: For use with a graphic coprocessor or CPU.

SYSTEM CONTROL

The SCC66470 performs several 680XX system control functions:

Reset and Halt Generation

The SCC66470 is reset when the RSTINN pin is released. The timing chain counts 8 video frames before RSTOUTN is released. The HALTN pin is released one video line after.

Memory Swapping

After RSTINN is released, the SCC66470 routes the first four 680XX accesses to the ROM (CSN must be asserted). After swapping, the ROM, is decoded normally (180000H).

Address Decoding

The SCC66470 is connected to the system bus via 20 Address lines, therefore 2 Mbytes may be accessed via the SCC66470. The memory mapping depends on the type of DRAM used (256K or 64K) and on the synchronization mode (see Table 1).

Table 1 Address Map

ADDRESS	256K		64K	
	MASTER OR SLAVE TV	**SLAVE DUAL**	**MASTER OR SLAVE TV**	**SLAVE DUAL**
000000 01FFFF	BANK 1	BANK 1	BANK 1	unaccessable
020000 03FFFF			BANK 2	
040000 05FFFF			BANK 3	
060000 07FFFF			BANK 4	
080000 09FFFF	BANK 2	BANK 2	unaccessable	BANK 1
0A0000 0BFFFF				BANK 2
0C0000 ODFFFF				BANK 3
0E0000 0FFFFF				BANK 4
100000 17FFFF	BANK 3	BANK 3	unaccessable	unaccessable
180000 1FFBFF	SYSTEM ROM	SYSTEM ROM	SYSTEM ROM	SYSTEM ROM
1FFC00 1FFF7F	SYSTEM I/O	SYSTEM I/O	SYSTEM I/O	SYSTEM I/O
1FFF80 1FFFBF	DRAM I/O	DRAM I/O	DRAM I/O	DRAM I/O
1FFFCO 1FFFDF	unaccessable	INT REGISTERS	unaccessable	INT REGISTERS
1FFFE0 1FFFFF	INT REGISTERS	unaccessable	INT REGISTERS	unaccessable

Notes to Table 1.

1. Each bank corresponds to a DRAM area and is associated to a CASN pin (CAS1N to CAS4N).
2. The system ROM decoding asserts the CSROMN pin which is not sensitive to the RWN signal.
3. The system I/O or DRAM I/O decoding asserts the CSION pin.
4. The internal registers have different mapping in SLAVE and MASTER modes thus allowing for independent accesses when the SLAVE SCC66470 has the same chip select as the MASTER.

DTACK Generation

The SCC66470 generates the Data Acknowledge (DTACKN) depending on the addressed device:

- Access to DRAM is acknowledged as soon as it is certain that data is available for the CPU. DTACKN can be advanced by two clock periods using the ED bit in the CSR register. For a Write cycle DTACKN can be advanced by 2 clock periods (4 if ED is set), using the EW bit of the CSR register. See Figures 3 and 4.
- Access to the System ROM is acknowledged after approximately 16 clock periods. When the DD bit in the CSR register is set, DTACKN may be advanced by 4 to 14 clock periods depending on the levels of the DD1 and DD2 bits in the CSR register. This gives a maximum DTACKN delay of 140 ns to 600 ns using a 30 MHz crystal.
- Access to the SYSTEM I/O device (CSION pin) is acknowledged by the addressed device and not by the SCC66470.
- Access to the DRAM I/O (CSION) is acknowledged in the same way as access to DRAM. The device is considered synchronous with the accesses on the memory data bus.
- Access to the internal registers is acknowledged immediately after arbitration against a potential access from the coprocessor.

Bus Error Generation

The BERRN signal is asserted when the BE bit of the Control register CSR is set and when the selection is not acknowledged for at least one complete video line (approximately 64 µs). The BE FLAG bit is then set in the CSR. The BERRN pin is released as soon as the CPU releases UDSN and LDSN. The BE flag is reset after the CPU has read the Status register.

Interrupt Generation

The SCC66470 generates interrupt requests to the CPU by asserting its INTN pin. The following conditions can generate an interrupt:

- The Dynamic Control Mechanism (DCA) fetches an interrupt instruction. Then the IT1 bit of the CSR register is set.
- The pixel accelerator (PIXAC) code is reset by the coprocessor. Then, the IT2 bit of the CSR register is set.

The INTN pin and IT1 are reset after the CPU reads the CSR register. When the DI1 and the DI2 bits of the CSR register are set, it is possible to avoid propagation to the INTN pin for the respective IT1 and IT2 bits.

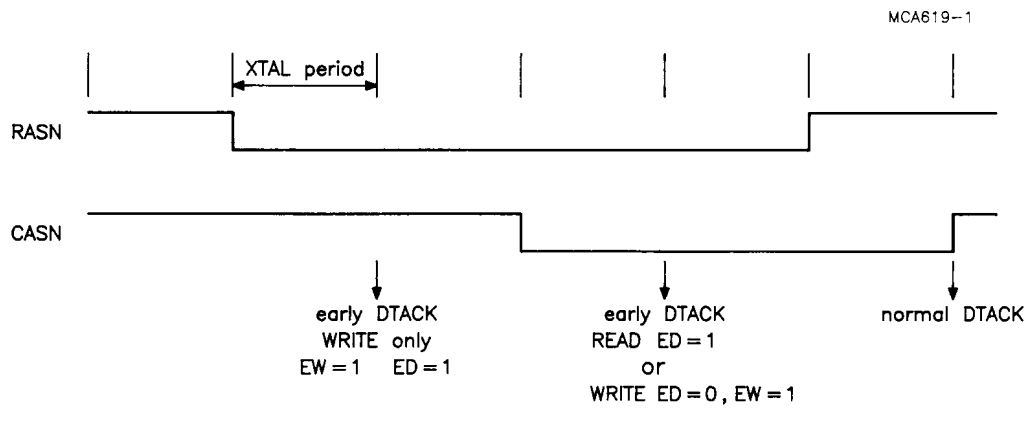


Fig.3 DTACK assertion in FAST mode timing.

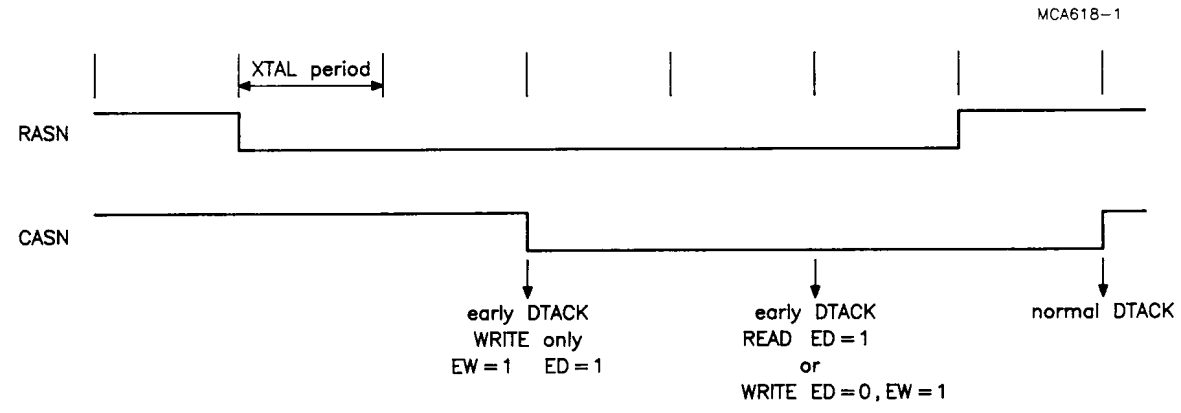


Fig.4 DTACK assertion in SLOW mode timing.

DRAM INTERFACE

The SCC66470 has an on-chip Dynamic RAM controller which may be programmed for normal, page, nibble, and video RAM devices.

Driving Modes

The SCC66470 can directly drive up to 16 memory devices. These may be arranged in one bank of 16 (using 64K x 1 or 256K x 1 devices) or several banks of four (using 64K x 4 or 256K x 4 devices). The TD bit in the CSR register selects either 256K or 64K DRAM's.

DRAM Access and Arbitration

The SCC66470 allows the DRAM to be used simultaneously as both video memory and system memory. Therefore the CPU or coprocessor can access any portion of the entire memory space during active video display time. The DRAM bus can be accessed by several masters and on-chip bus arbitration logic is implemented to provide each master with a guaranteed access time (or timing window). The various masters are:

- The system bus (CPU or DMA cycles)
- The display
- ICA/DCA controller
- The DRAM refresh controller
- The coprocessor bus

The DRAM access consists of consecutive timing windows of 16 XTAL periods, divided by 2 sub-windows. The 1st sub-window is used by a video related function (Display or ICA/DCA controller) or by the DRAM refresh controller. The 2nd sub-window is available for a DRAM access from the system bus (CPU or DMA cycles) or from the coprocessor bus. When no video or refresh functions are required, the access to DRAM is free-running with no windows, so that a system or coprocessor bus access can occur at anytime.

Fig.5 shows the number of timing windows related to the time domain of a video frame, the following should be noted:

Notes to Fig.5.

1. RF is the refresh area.
2. ICA and DCA only exist if enabled.
3. If the display is not enabled, the entire area is FREE-RUN except the refresh areas.
4. In Dual-port Video DRAM mode, all display windows are available to the system bus, except the first display cycle of each line.
5. The horizontal resolution is 8 bits/pixel, FAST DRAM.

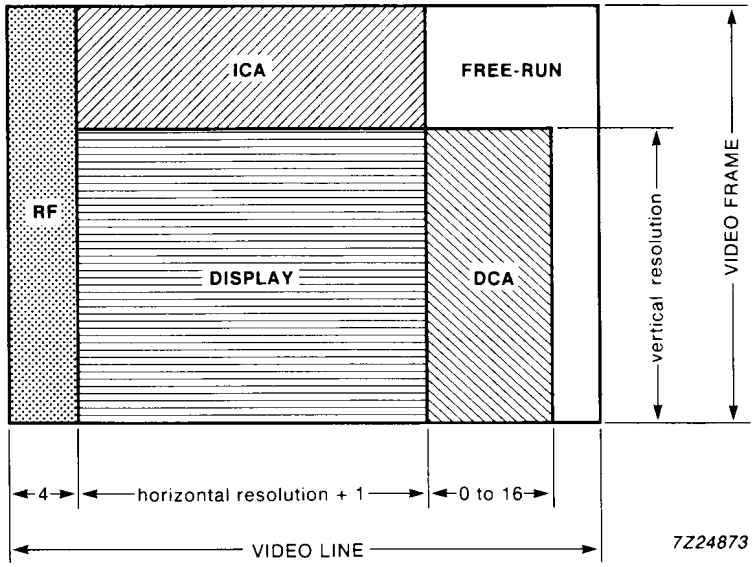


Fig.5 DRAM Timing Windows.

DRAM Timing

The SCC66470 can use normal, nibble, page or dual-port video DRAM types. Two bits of the CSR Register (DM1 and DM2) are used to select the DRAM type (see Table 2).

Table 2 Selection of Dram type.

DM1	DM2	DRAM MODE	TIMING SPEED MODE
0	0	NORMAL	SLOW
0	1	PAGE	FAST
1	0	NIBBLE	FAST
1	1	DUAL PORT	SLOW

In FAST mode, two display fetches are performed in the same cycle. In NIBBLE mode, the LSB and MSB memory address must be switched externally.

In Dual port video RAM mode, the CPU has twice as much access time available during the display window. The DTN pin is asserted at the beginning of each video line. It permits the use of dual port VRAM serial port in Logical Screen mode (see DISPLAY chapter).

Fig.6 shows cycle windows in the display area in SLOW and FAST modes.

The memory address bus MA is multiplexed in order to present the row address on the RASN falling edge and the column address on the CASN falling edge. The correspondence between memory address bus MA(8:0) and CPU or coprocessor address A(18:1) is indicated in Table 3.

DRAM Deselect

During the RESET period, a bank can be devalidated if its corresponding CASN pin is grounded, then DTACKN will not be generated for this bank. To select the memory bank, a pull-up resistor is required.

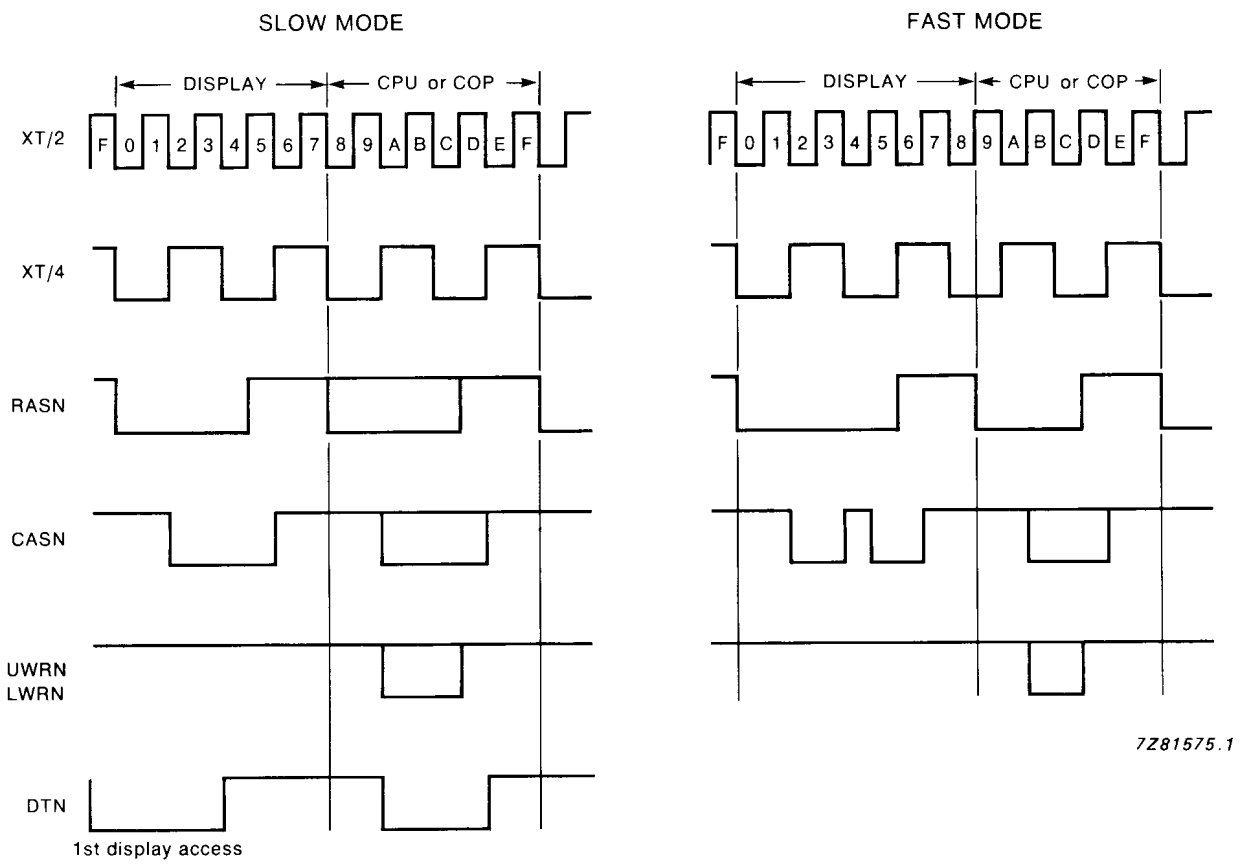


Fig.6 DRAM timing

Table 3 Memory address distribution.

	MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	MA8
RASN	α	A2	A3	A4	A5	A6	A7	A8	A9
CASN	ß	A11	A12	A13	A14	A15	A16	γ	A18

Notes to Table 3.

1. α = A1 NORMAL or NIBBLE mode; A10 PAGE MODE
2. ß = A10 NORMAL or NIBBLE mode; A1 PAGE MODE
3. γ = A9 - 64K; A17 - 256K

DISPLAY CONTROL

The SCC66470 is programmable for several pre-defined modes of display. It contains a Video Start address register (VSR) which locates the video display within the first 1 Mbyte of the DRAM address space. The display logic reads words from the video display area and sends them to the display file decoder.

Resolution

Horizontal resolution

Table 4 shows the horizontal resolution as set by bits CF1, CF2, SS and CM in the DCR register, and the mask bit ST in the CSR register. If the SLOW mode is selected or the Double Frequency mode is active, then the horizontal resolution shown in Table 4 is halved.

Table 4 Horizontal resolution.

CF1	CF2	SS	ST	FREQUENCY MHz	PIXELS/LINE CM = 1	CM = 0	ACTIVE LINE µs
0	0	0	X	20	448	224	44.8
0	0	1	X	20	512	256	51.2
0	1	0	X	24	512	256	42.6
0	1	1	X	24	640	320	53.3
1	0	0	X	28	640	320	45.7
1	0	1	X	28	720	360	51.4
1	1	0	X	30	640	320	42.6
1	1	1	0	30	768	384	51.2
1	1	1	1	30	720	360	48

X = don't care states.

Vertical Resolution

Table 5 shows the vertical resolution as set by bits FD and SS in the DCR register and also by the ST bit in the CSR register. Table 5 corresponds to the non-interlace scan mode.

Table 5 Vertical Resolution.

FD	SS	ST	DISPLAY LINES	FRAME DURATION (ms)	IMAGE FREQUENCY (Hz)
0	0	0	250	16	50
0	0	1	210	13.4	50
0	1	0	280	18	50
0	1	1	240	15.3	50
1	0	X	210	13.4	60
1	1	X	240	15.3	60

X = don't care states.

The vertical resolution is also dependent on the scan mode. The SCC66470 has four different scan modes which are selected by the SM and DF bits in the DCR register.

Table 6 Scan mode selection.

SM	DF	SCAN MODE DESCRIPTION
0	0	**Non-interlace mode**. An image is composed of one frame. The line duration is 64 µs.
0	1	**Double frequency mode**. Same as non-interlace mode except that the line duration is 32 µs. Therefore, in this mode, the vertical resolution is doubled and the horizontal resolution is halved.
1	0	**Interlace mode**. One image is composed of 2 frames. The odd frame has the odd memory lines and the even frame, the even memory lines. The SCC66470 displays alternatively the odd frame and then the even frame. During a frame display the SCC66470 displays memory line n and then memory line n + 2. The vertical resolution and the image duration are doubled.
1	1	**Interleaved field repeat mode**. Same as interlace mode but the 2 frames are identical. The horizontal and vertical resolutions are the same as non-interlace mode.

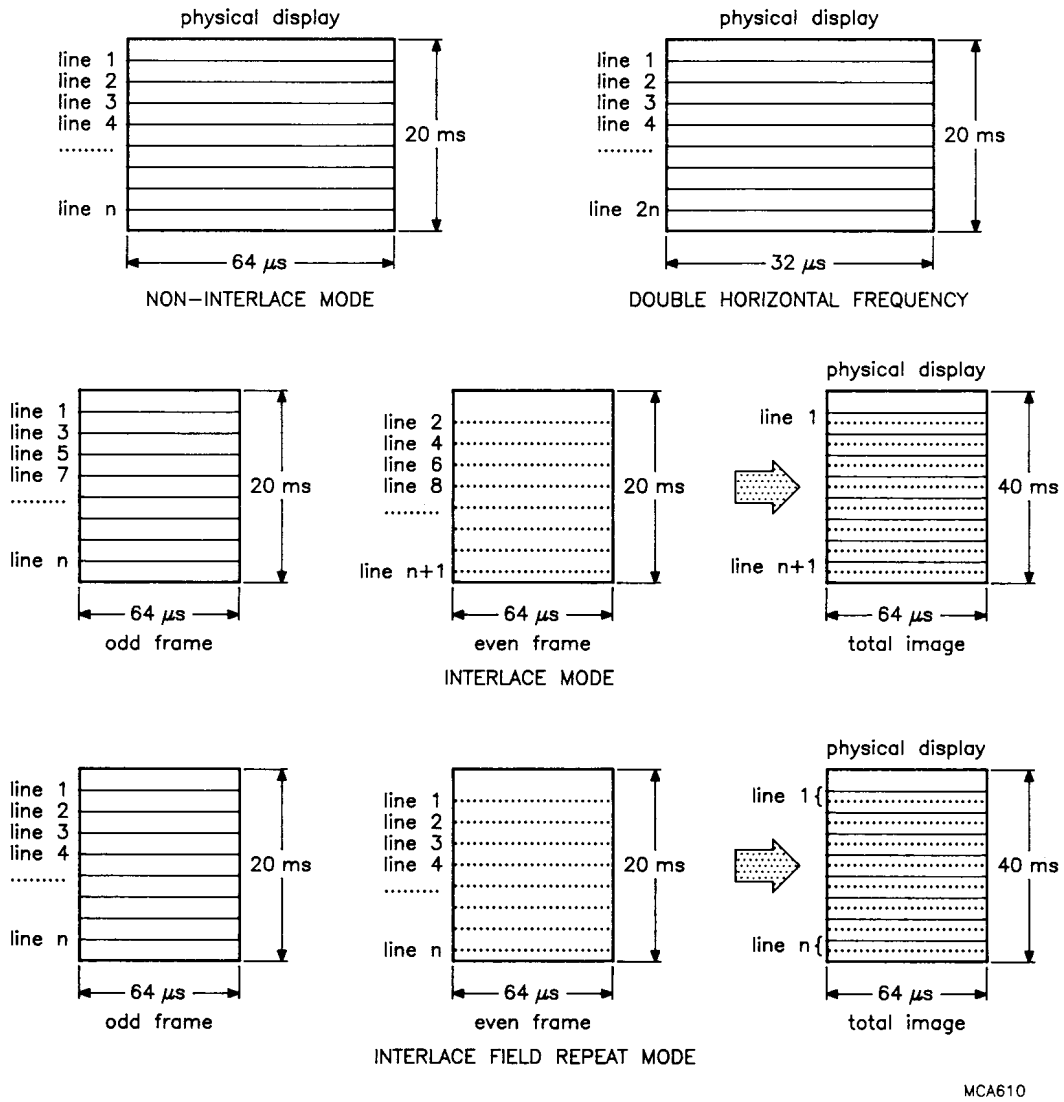


Fig.7 Scan modes.

Reduced and full screens

In Full Screen mode (SS = 1), the picture covers the entire TV screen. In Reduced Screen mode (SS = 0), a border of programmable colour is displayed on the top, bottom, left and right parts of the visible screen. The Border Colour register (BCR) is 8 bits wide. In the 8 bits per pixel mode, 256 colours are possible. In the 4 bits per pixel mode, 16 colours are possible.

Physical and logical screen

The SCC66470 can organize the display memory in either of two ways: logical screen mode or physical screen mode. The logical screen mode is selected when the LS bit of the DCR register is set and the physical screen is selected when the LS bit is reset. The Video Start Register (VSR) points to the start of the physical display.

BMW = Bit-Map Width. HRES = Horizontal Resolution.

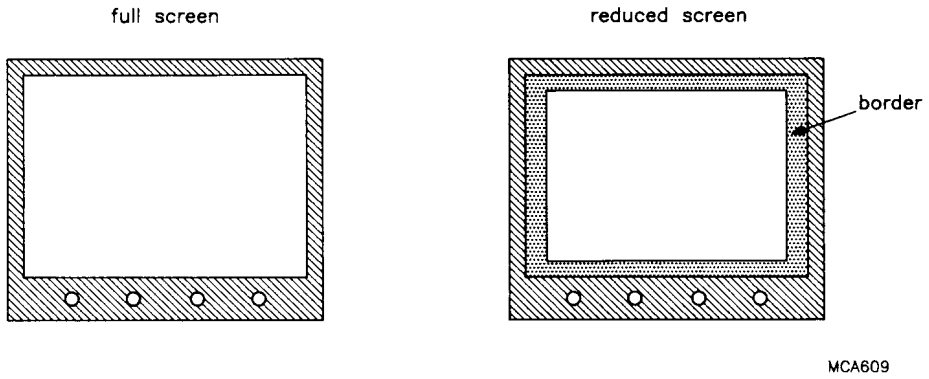


Fig.8 Full screen and Reduced screen modes.

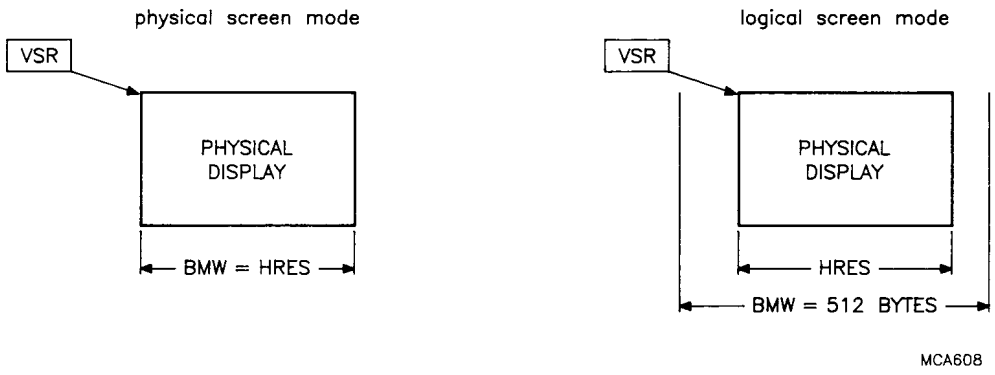


Fig.9 Physical and logical screen

In logical screen mode, the bit map width is 512 bytes. The 9 LSB's of the Video Start Register are reloaded at the beginning of each display line. If the VSR points too far to the right of a memory line, a horizontal wrap-around occurs.
In physical screen mode, the bit-map width is the same as the display line width, except in the following two cases:

1. In interleaved DCA, the bit-map width is equal to the display line width plus the DCA allocated width in memory.
2. In physical screen 28 MHz, full screen mode, the bit map width is not always equal to the horizontal resolution when the ST bit is set, or when the interlace mode selected.

The first pixel of a line immediately follows the last pixel of the of the previous line. The use of the Dual Port VRAM serial port is not allowed in this mode.

Table 7 Bit map width in Physical screen, full screen f = 28 MHz.

INTERLACE MODE	ST	HORIZONTAL RESOLUTION	BIT-MAP WIDTH
no	0	360	360
no	1	360	384
yes	X	360	384

X = don't care state.

Image Control Area (ICA) and Dynamic Control Area (DCA) Mechanisms

The SCC66470 permits control information to be fetched during vertical and horizontal retrace periods. This feature is enabled by using the IC and DC bits in the DCR register.

ICA Mechanism

This mechanism consists of fetching Long Word instructions during the vertical phase period. The ICA pointer is either 400H or 80400H at the beginning of the vertical retrace period (see Table 8). The possible number of ICA fetches is equal to:

Lines during vert. retrace x display line width (in longwords).

This permits at least 500 instructions to be fetched in the worst case. The Video Start Register is also used as an ICA pointer to perform indirect ICA addressing during ICA instructions fetches.

Table 8 ICA pointer.

	256K		64K	
	BANK 1 ENABLED	BANK 1 DISABLED	MASTER/ SLAVE TV	SLAVE DUAL
ICA POINTER	400H	80400H	400H	80400H

In interlace and interleaved field repeat mode, the ICA pointer is 404H or 80404H at the end of the even frame (parity bit of status register is low, the next displayed will be the odd one).

DCA Mechanism

In this case, the instruction fetch takes place during the horizontal retrace period. The DCA size is either 64 bytes/line or 16 bytes/line (reduced DCA). The memory allocation for the DCA depends on which mode is set by the ID bit in the DCR2 register.

Interleaved DCA (ID = 0)

The DCA is located in the memory display area, the bit map shape being modified accordingly. In Logical screen mode, the 9 LSB's of the address counter are forced to 1C0 or 1F0 for reduced DCA, in order to jump to the DCA at the end of the display line. If the VSR is close to the DCA, an automatic horizontal wrap around is performed. In Physical screen mode, the DCA is adjacent to the bit map. The bit map width is thus increased by the DCA allocated width in memory.
The VSR register can be used as a DCA pointer to perform indirect DCA addressing as for the ICA.

Independent DCA (ID = 1)

The DCA is completely independent of the bit-map or display file area therefore the bit map shape is not modified by the DCA. The DCA pointer DCP, points to the first line of the independent DCA. The second DCA line is pointed to automatically by DCP+64 bytes, or DCP+16 bytes for reduced DCA. The DCP can be changed on the fly in order to perform indirect DCA addressing.

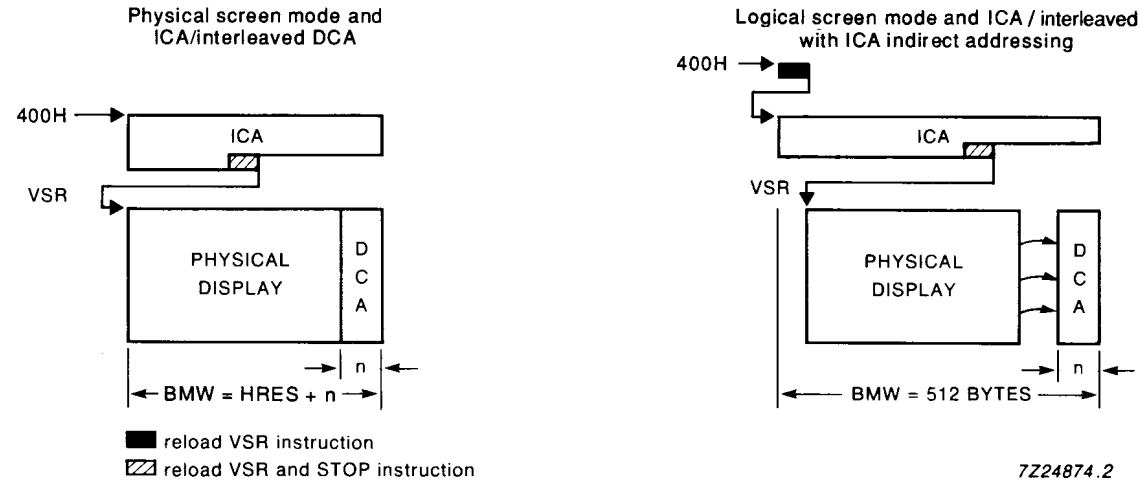


Fig.10 ICA/interleaved DCA and Physical display.

Notes to Fig.10.

1. BMW: Bit Map Width.
2. HRES: Horizontal Resolution.
3. n = 64 bytes or 16 bytes for reduced DCA.

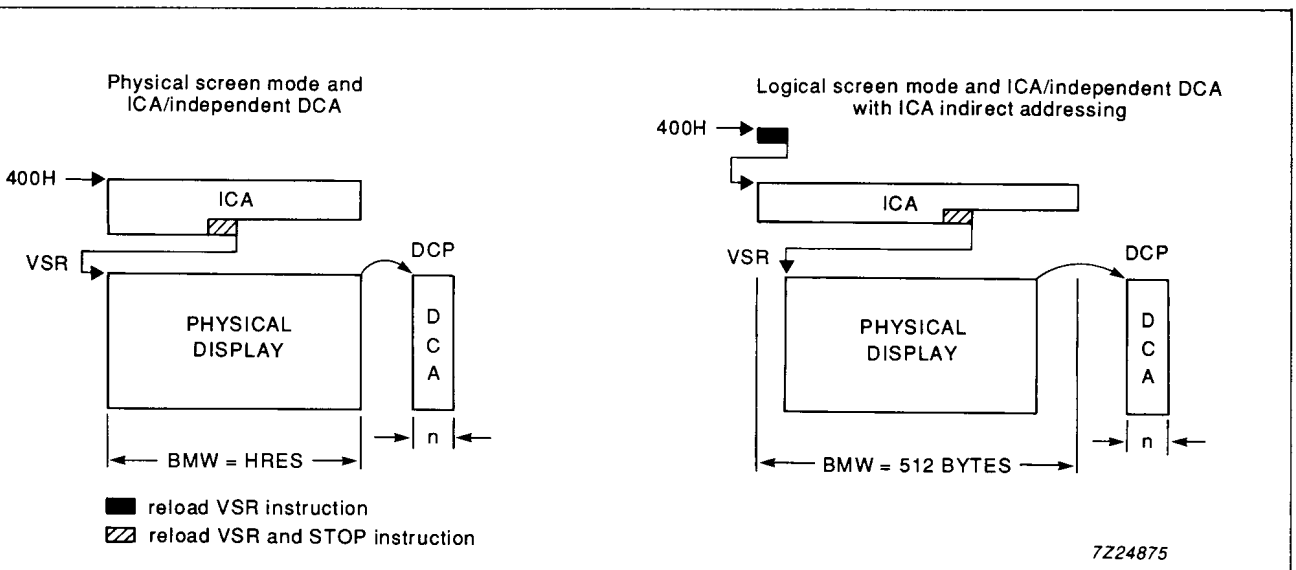


Fig.11 ICA/independent DCA and Physical display.

Notes to Fig.11.

1. BMW: Bit Map Width.
2. HRES: Horizontal Resolution.
3. n = 64 bytes or 16 bytes for reduced DCA.

ICA/DCA initialization

The IC and DC bits in the DCR register select the four possible ICA/DCA modes as shown in Table 9.

Table 9 ICA/DCA modes.

IC	DC	ICA	DCA
0	0	no	no
0	1	yes	yes Reduced DCA mode, DCA = 16 bytes
1	0	yes	no
1	1	yes	yes DCA = 64 bytes

When IC = DC = 1, the number of possible DCA fetches can be limited by the line retrace duration as is shown in Table 10.

Table 10 DCA possible fetches.

IC	DC	DOUBLE FREQUENCY SM = 0; DF = 1	SS	CF1	CF2	DCA (BYTES)
X	0	X	X	X	X	0
0	1	X	X	X	X	16 (Reduced DCA mode)
1	1	yes	X	X	X	16
1	1	no	0	X	X	64
1	1	no	1	0	X	32
1	1	no	1	1	0	32
1	1	no	1	1	1	64

Notes to Table 10.

1. X = don't care states.
2. An automatic stop instruction is performed at the end of the available area.
3. The allocated memory size is always 64 bytes or 16 bytes even if the possible number of fetches is lower.
4. In SLOW mode, the number of fetches is halved and the DCA allocated memory size is also halved in the physical screen mode.

ICA/DCA instructions

ICA/DCA instructions are Long Word Aligned and Long Word Wide.

Table 11 ICA/DCA instruction list.

INSTRUCTION	ACRONYM	ACTION
0000 -	STOP	Stop the control sequence. The instruction fetches are then stopped.
0001 -	NOP	No operation.
0010 - - - - - - - - PPPP PPPP PPPP PPPP PP- -	RELOAD DCP	Reload the DCP and its associated address counter with the specified pointer. The following fetches will use the new value. This permits indirect addressing for the independent DCA mechanism.
0011 - - - - - - - - PPPP PPPP PPPP PPPP PP- -	RELOAD DCP and STOP	Reload the DCP with the specified pointer then stop the control fetches as for a STOP instruction.
0100 - - - - - - - - PPPP PPPP PPPP PPPP PPPP	RELOAD VSR	Reload the VSR and the video address counter with the specified pointer. The following fetches will use the new value. The VSR is considered as an ICA or interleaved DCA pointer.
0101 - - - - - - - - PPPP PPPP PPPP PPP PPPP	RELOAD VSR and STOP	Reload the VSR with the specified pointer and then stop the control fetches. This instruction permits the display of vertical subscreens.
0110 -	INTERRUPT	Generate an interrupt to the CPU and set the IT1 bit in the CSR register.
0111 0- - - CCCC CCCC - - - - - - - - - - - - - - - -	RELOAD BORDER	Reload the Border Colour Register with specified colour immediately.
0111 1- - - CCCC CCCC - - - - - a- b - cd - e f g h	RELOAD BORDER and DISPLAY parameters	Reload the Border Colour Register and relevant bits in the DCR and DCR2 registers. a = SS; b = CM; c = OM1; d = OM2; e = MF1; f = MF2; g = FT1; h = FT2.
1XXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX	BEP CONTROL	Control of the Back-End processor. WRPN signal active. The 32 bits are passed via the video output port V(7:0) to the BEP without alteration. The information is always output by a group of 8 bits (8-bits/pixel mode).

Notes to Table 11.

1. ' - ' denotes not used.
2. ' X ' denotes output via the video output port.

PIXEL OUTPUT

There are six video output modes (A to F). The mode selected depends on the CM bit in the DCR register, and also on OM1 and OM2 bits in the DCR2 register. The Output modes are shown in Table 12 below.

Table 12 Output modes.

MODE	CM	OM1	OM2	MODE DESCRIPTION
A	0	0	X	8 bits/pixel mode. The video port V0 to V7 corresponds exactly to the pixel to output.
B	0	1	0	Same as mode A.
C	X	1	1	The video port is in the high impedance state.
D	1	0	0	4 bits/pixel. Only V4 to V7 are used.
E	1	0	1	4 bits/pixel. Only V0 to V3 are used.
F	1	1	0	4 bits/pixel. Only V7, V6, V4, V3, V1, and V0 are used.

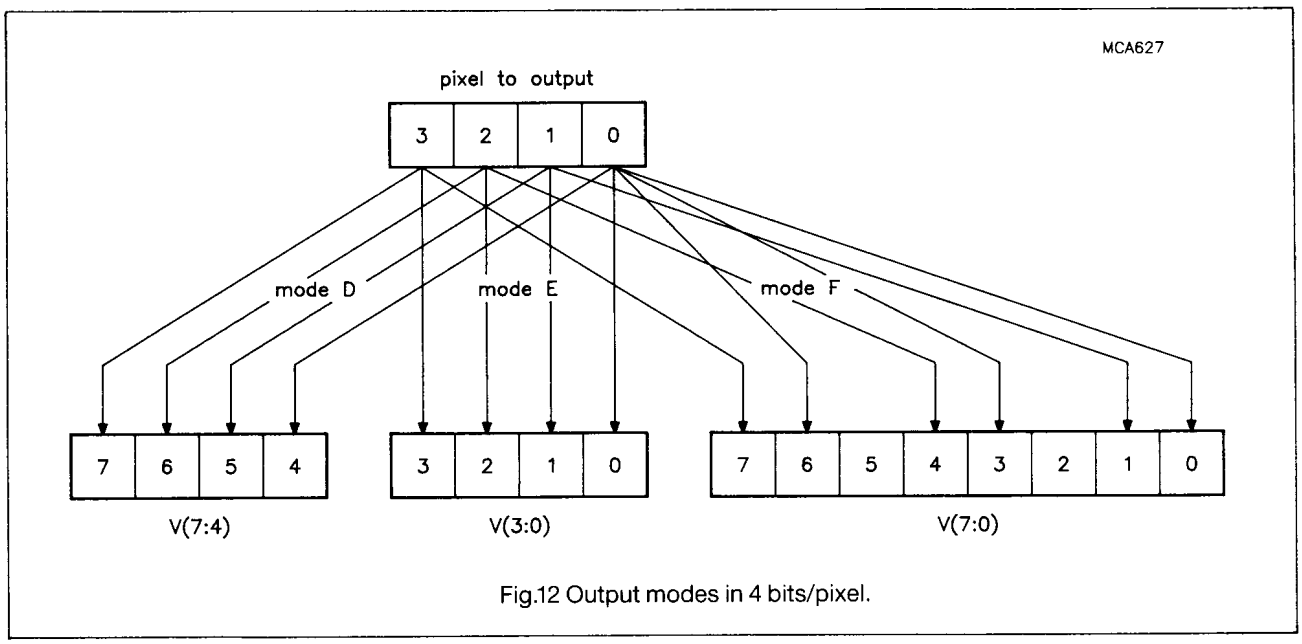


Fig.12 Output modes in 4 bits/pixel.

The Pixel Clock frequency (PCLK) depends on the value of the CM bit in the DCR register (number of bits/pixel) and also on the DRAM speed.

Table 13 Pixel clock frequency.

BITS/PIXEL	TIMING SPEED	PCLK FREQUENCY
4	FAST	XTAL/2
8	FAST	XTAL/4
4	SLOW	XTAL/4
8	SLOW	XTAL/8

If the ICA/DCA instruction BEP CONTROL is active, the WRPN signal is asserted and the video output port is in 8 bits/pixel, even if CM = 0 (4 bits/pixel). If BLANKN pin is reset (retrace period) and if WRPN is inactive, the pixel port is forced to 0.

VIDEO SYNCHRONIZATION

The SCC66470 can operate in the following modes:

Master mode: HSYNCN and VSYNCN are both outputs.

Slave TV mode: HSYNCN is an output and VSYNCN is an input.

Slave dual mode: HSYNCN and VSYNCN are both inputs.

The SCC66470 is initialized when the DE bit in the DCR register is set, taking into account the state of the signals CSYNCN and MSN (see Table 14).

Table 14 Synchronization.

MSN	CSYNCN (DE = 0)	SYNCHRO MODE
1	X	Master
0	1 (no pull-down)	Slave TV
0	0 (pull-down)	Slave DUAL

Figs.13, 14, 15, 16 show HSYNCN, VSYNCN, CSYNCN, BLANKN, DA timing in the MASTER and reduced screen mode.

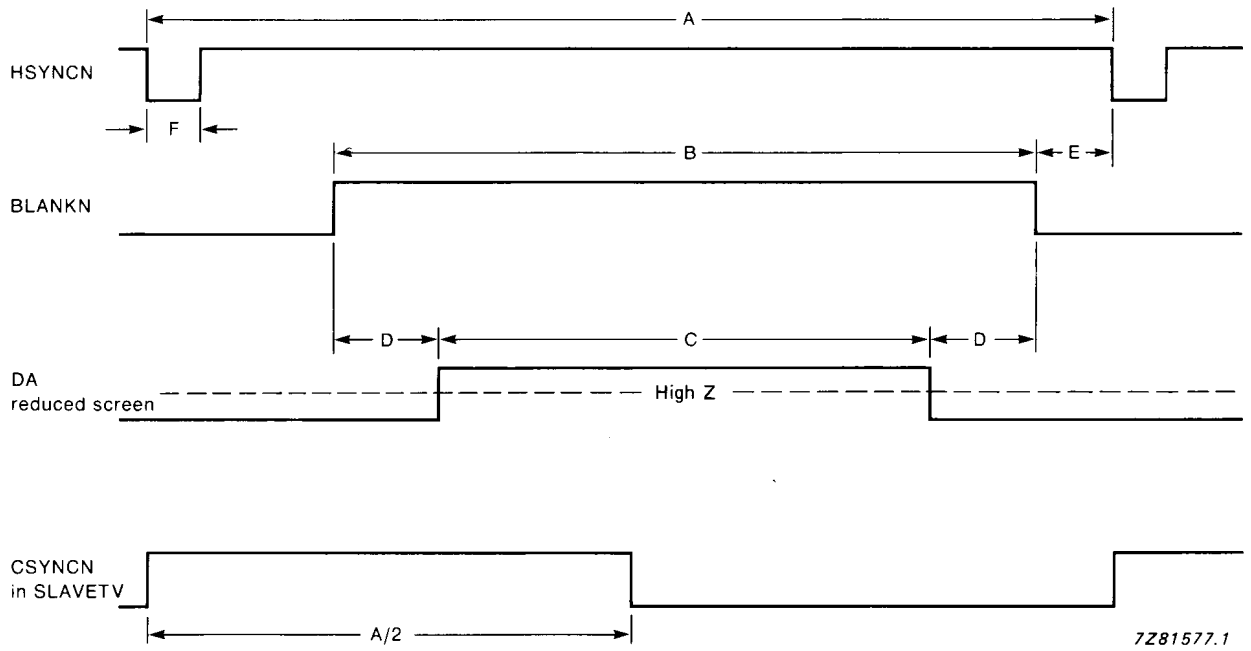


Fig.13 Horizontal synchronization timing.

Table 15 Horizontal synchronization timing.

	20 MHz		24 MHz		28 MHz		30 MHz	
	CYCLES	µs	CYCLES	µs	CYCLES	µs	Cycles	µs
A	80	64	96	64	112	64	120	64
B	64	51.2	80	53.33	90	51.43	96	51.2
C	56	44.8	64	42.67	80	45.71	80	42.67
D	4	3.2	8	5.33	5	2.86	8	4.27
E	2	1.44	1	0.52	3	1.59	3	1.49
F	6	4.8	7	4.67	8	4.57	9	4.8
G	3	2.4	3	2	4	2.29	4	2.13
H	6	4.8	7	4.67	8	4.57	9	4.8

Note.

One cycle is equivalent to a timing window (16 slots) or to a 32 bits display fetch in FAST mode.

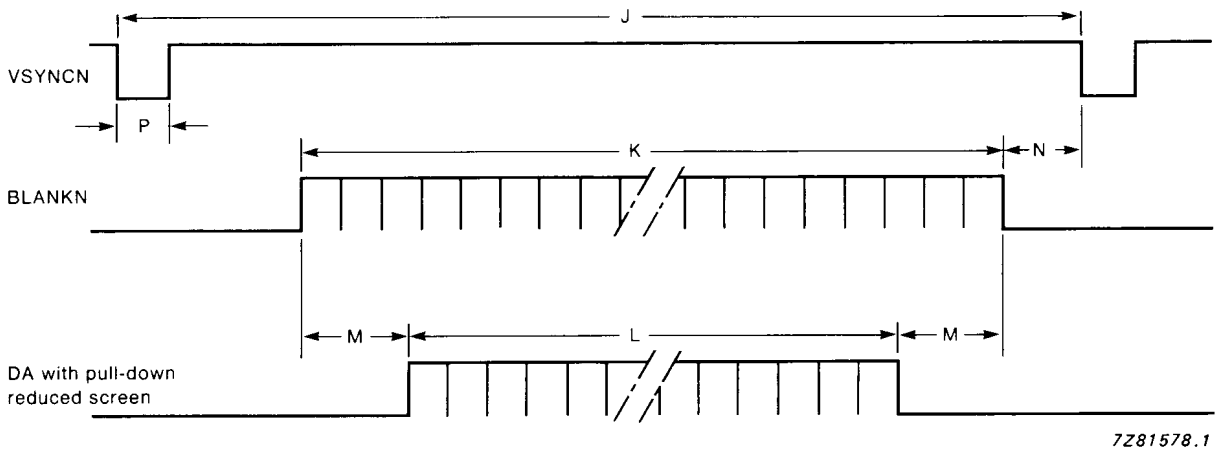


Fig.14 Vertical synchronization timing.

Table 16 Vertical synchronization timing.

	50 Hz NON-INTERLACE		50 Hz INTERLACE		60 Hz NON-INTERLACE		60 HZ INTERLACE	
	LINES	**ms**	**LINES**	**ms**	**LINES**	**ms**	**LINES**	**ms**
J	312	19.97	312.5	20	262	16.77	262.5	16.8
K	280	17.92	280	17.92	240	15.36	240	15.36
L	250	16	250	16	210	13.44	210	13.44
M	15	0.96	15	0.96	15	0.96	1	0.96
N	6	0.385	6 or 6.5	0.417	4	0.257	4 or 4.5	0.290
P	2.5	0.16	2.5	0.16	3	0.192	3	0.192

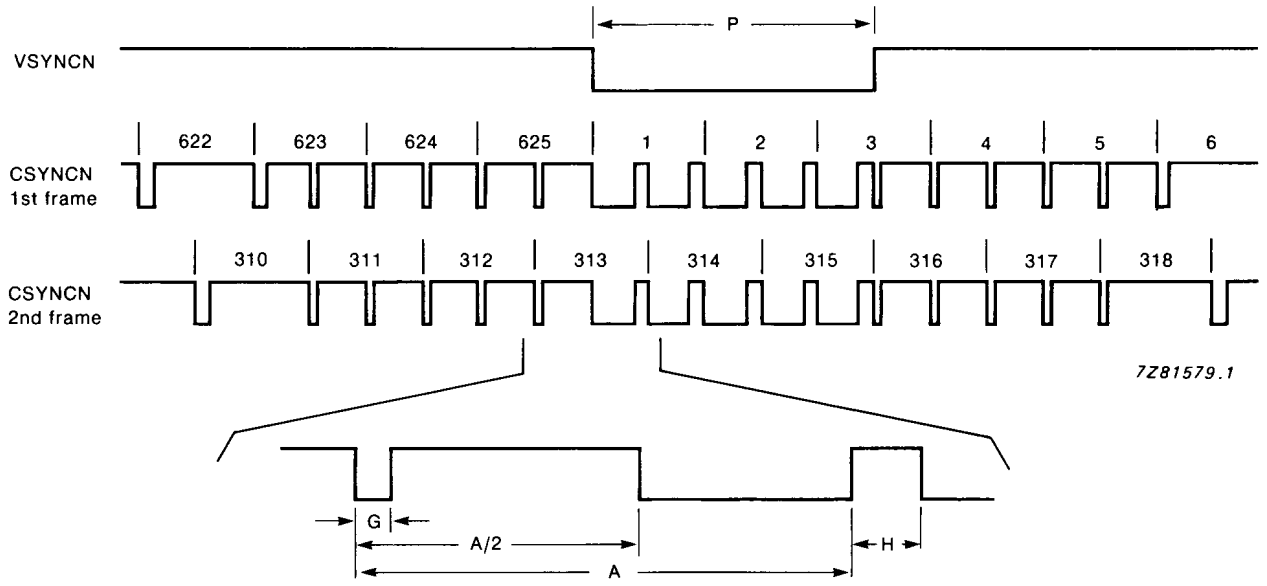


Fig.15 CSYNCN timing in the 50 Hz, interlace or interlace field repeat mode.

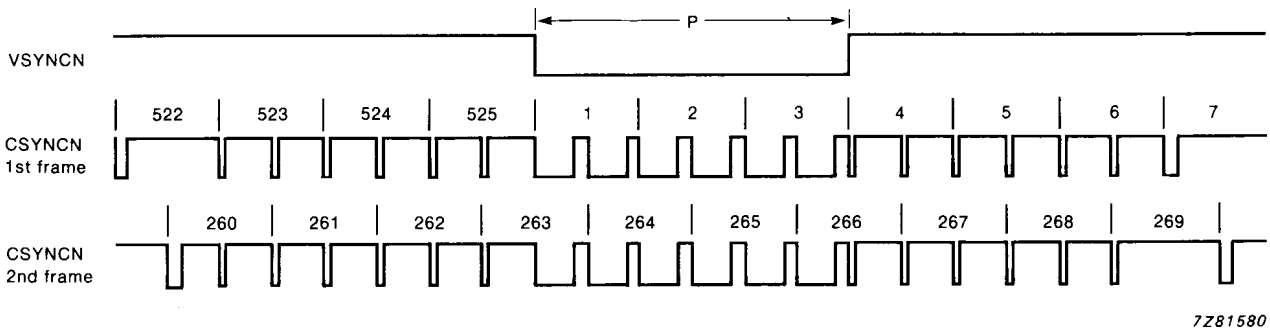


Fig.16 CSYNCN timing in the 60 Hz, interlace or interlace field repeat mode.

Frame grabbing

When the Frame-Grabbing bit (FG) in the DCR register is set, the SCC66470 completes the current frame before the grabbing period starts. The grabbing period consists of either one, or two frames in interlace mode. During the grabbing period, UWRN and LWRN are asserted during the display window. DRAM accesses are allowed during the CPU window. The CPU polls the FG bit in the CSR to detect the end of the grabbing period.

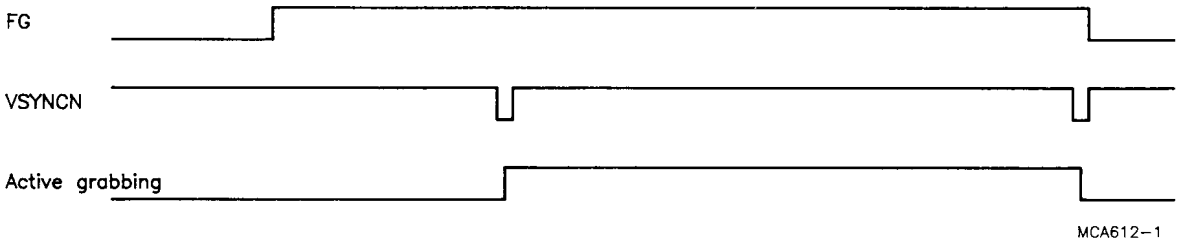


Fig.17 Frame Grabbing in the non-interlace, double frequency and interlace field repeat modes.

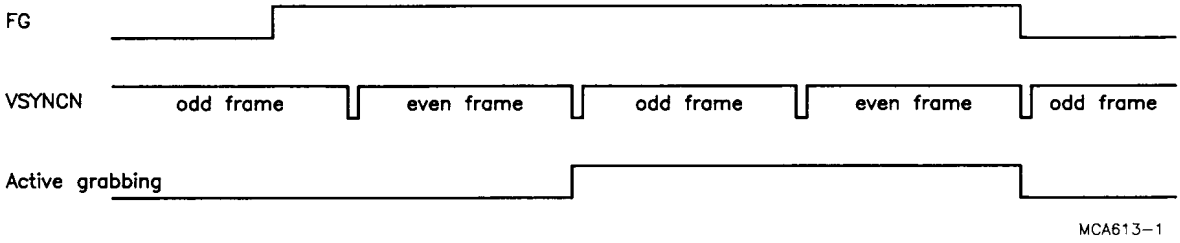


Fig.18 Frame Grabbing in the interlace mode.

DISPLAY FILE DECODER

The SCC66470 handles three types of files:-

1. NORMAL or BIT MAP file: each pixel has its own address.
2. RUN-LENGTH file: consecutive pixels with the same colour are grouped in the same block of information.
3. MOSAIC file: as for the NORMAL file but with the resolution divided by a MOSAIC factor. The SCC66470 duplicates each pixel following the MOSAIC factor (2, 4, 8 or 16).

The initialization of the file type is achieved using the FT1 and FT2 bits of the DCR2 register as shown in Table 17.

Table 17 Selection of display file type.

FT1	FT2	FILE TYPE
0	X	BIT MAP
1	0	RUN-LENGTH
1	1	MOSAIC

Bit map file

The pixels are packed in memory. Each word that the SCC66470 fetches for display is serialized in one of two ways, as shown in Figs. 19 and 20.

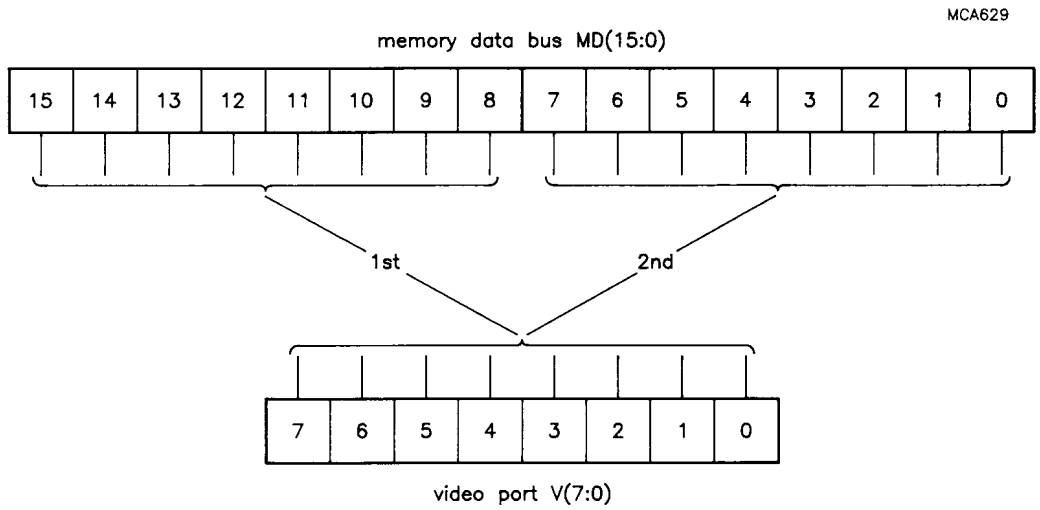


Fig.19 Bit map serialization in 8 bits/pixel.

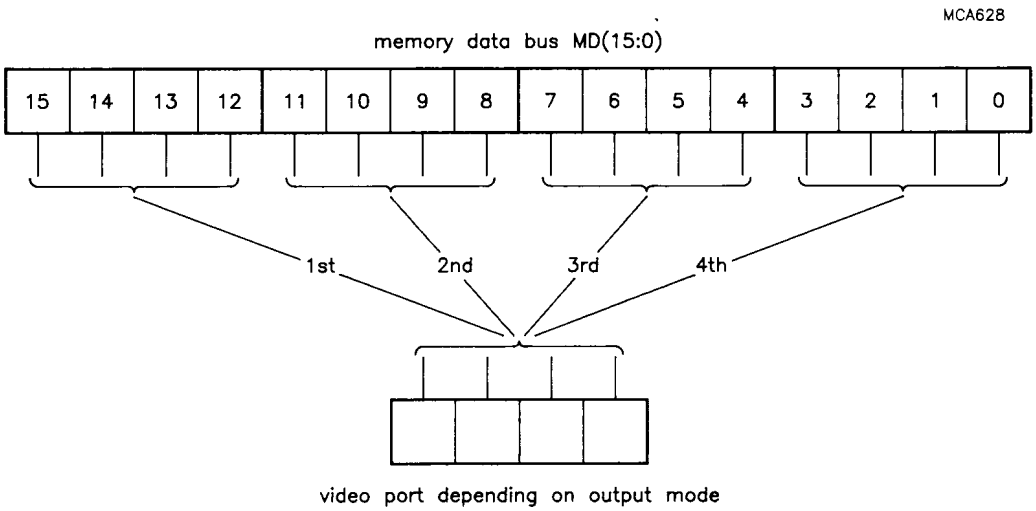


Fig.20 Bit map serialization in 4 bits/pixel.

Run length file

The Run-length coding technique permits file compression by grouping in one block, consecutive pixels which have the same colour. The run-length compression is applied to each video line independently of the others.
The Run-length file is organized as a list of information about pixels without notion of width and height as in bit map files. The information indicates either the pixel colour followed by the number of consecutive pixels having the same colour, or the simple pixel. Thus, two formats are possible; Type A and Type B (see Fig.21).

The flag indicates if the information is of Type A (pixel alone) or of Type B (consecutive pixels having the same colour). The number of colours in 8 bits/pixel mode is therefore limited to 128 and the pixel MSB is forced to 0 when the pixel is output to the video port. The number of consecutive pixels, N, is between 2 and 255. When N = 0, the display controller of the SCC66470 finishes the display line with the last indicated colour.

The Run-length decoder always works at the byte level. In 4 bits/pixel mode, the Run-length format is the same as 8 bits/pixel except that each colour byte contains two colour nibbles.
Each pixel is limited to 8 colours, the pixel MSB is forced to 0 when the pixel is output to the video port.

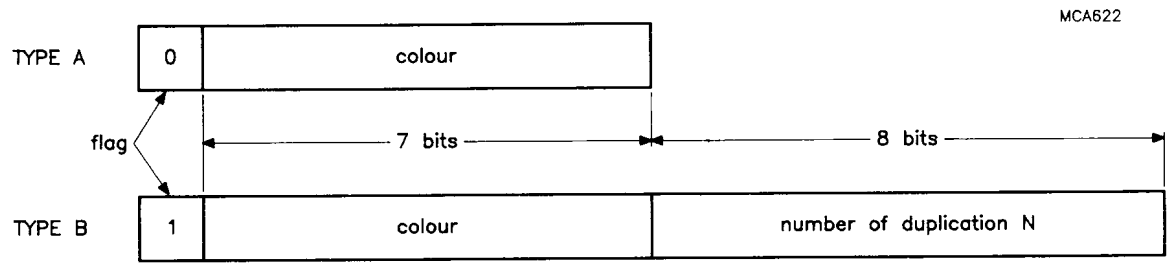


Fig.21 Run-length format in 8 bits/pixel

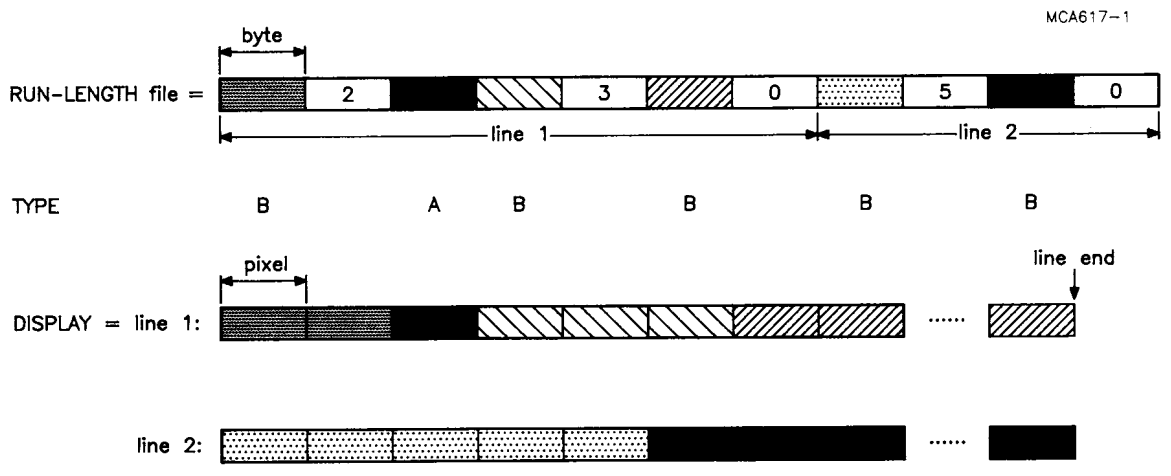


Fig.22 Run-length file display, 8 bits/pixel.

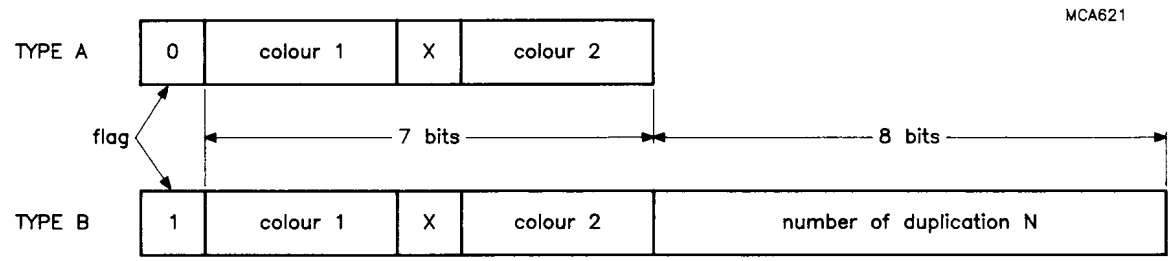


Fig.23 Run-length format in 4 bits/pixel.

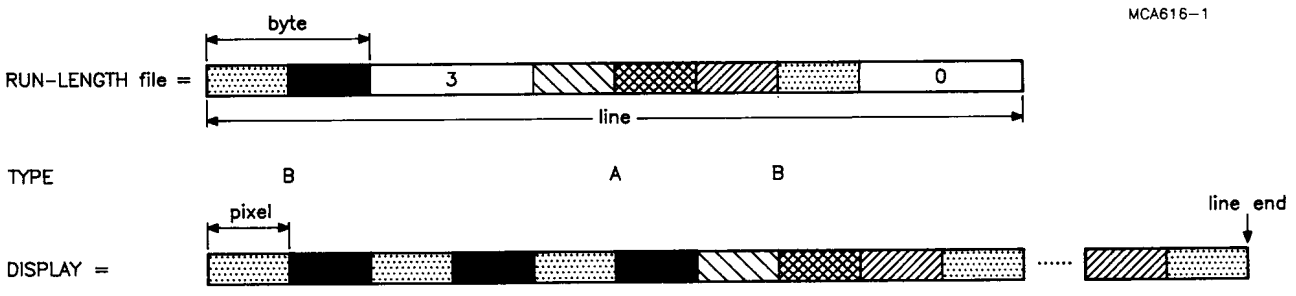


Fig.24 Run-length file display, 4 bits/pixel.

Mosaic file

The Mosaic technique consists of changing the resolution of the screen by duplicating pixels and lines using a Mosaic factor. The Mosaic file is then compressed by a factor n x m, where n is the horizontal Mosaic factor and m the vertical Mosaic factor. The effect on the screen is a granulation. Depending on the horizontal Mosaic factor, the SCC66470 automatically duplicates the pixel on the line (horizontal Mosaic). The Mosaic factor is held in the DCR2 register as shown in Table 18.

Table 18 Mosaic factor bits of the DCR2 register.

MF1	MF2	MOSAIC FACTOR
0	0	2
0	1	4
1	0	8
1	1	16

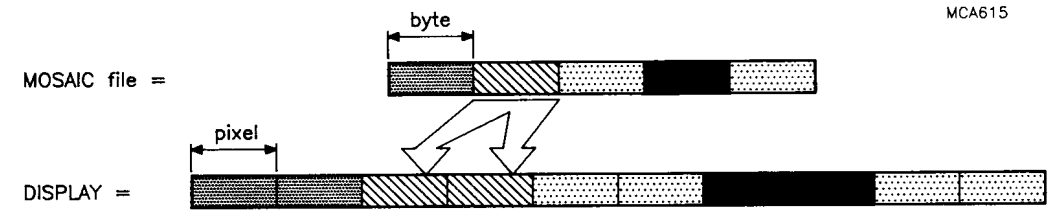


Fig.25 Mosaic file display, 8 bits/pixel (Mosiac factor = 2).

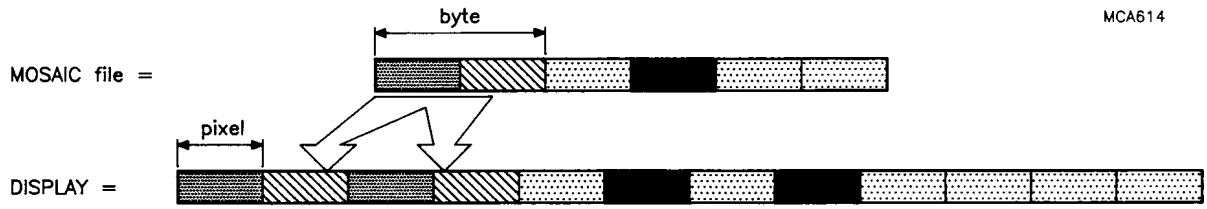


Fig.26 Mosaic file display, 4 bits/pixel (Mosaic factor = 2).

The vertical mosaic is not supported by the SCC66470. The independent DCA can be used to duplicate the lines. The vertical Mosaic can therefore be independent of the horizontal Mosaic factor.

The Mosaic file works at byte level. In 4 bits/pixel mode, the pixels are duplicated by group of 2.

The following points on the use of the three types of display file should be noted:

Physical/Logical screen:	This arrangement cannot be used for Run-length or Mosaic files. The LS bit of the DCR register must be zero to display them.
Dual port VRAM mode:	This cannot be used with Run-length or Mosaic files.
DCA:	Only the independent DCA can be used with a Run-length or Mosaic files.
Interlace mode:	Cannot be used with Run-length or Mosaic files. The interleaved field repeat mode can be used to get the interlace effect.
Horizontal rolling:	The VSR being a byte address, the byte incrementation between 2 images gives the following effects in 8 bits/pixel mode: For a Bit map file, horizontal rolling of one pixel is performed. For a Mosaic file, horizontal rolling of N pixels is performed, N being the Mosaic factor. For a Run-length file, the decoder starts with the new byte. Horizontal rolling occurs only if the previous byte was in the TYPE A format.

PIXEL ACCELERATOR (PIXAC)

The SCC66470 has on-chip pixel accelerator logic to speed up the manipulation of pixel contents in memory. The PIXAC may be used with either the CPU or Coprocessor. The PIXAC logic consists of three main blocks. These are described below:-

- The pixel path receives source and destination words and operates on them depending on the selected functions. It consists of a source register, colour register, two carry registers, a multiplexor, a logic unit and a destination register.
- The sequencer takes into account the PIXAC commands and controls the Pixel Path.
- The logic unit controls masking, shifting, colour selection and transparency colour testing.

Pixac operations

A software PIXAC driver is required to write pixels, trigger an operation and read the resulting pixels. PIXAC operations process words via the pixel path. Words are organized in four pixels of 4 bits or two pixels of 8 bits. The pixel path is determined by register A, which holds the source pixels, and register B which holds the destination pixels. The PIXAC sequencer generates signals to execute operations. According to the operation type, the sequencer is triggered either by writing into the source Register A (operation Type A) or by writing into the destination Register B (operation Type B). The multiplexor of the pixel path shifts the contents of the two carry registers (if there is no mask) into register B. The shift operation is always to the right (see Fig.28).

The result of the operation is always in the destination register B.

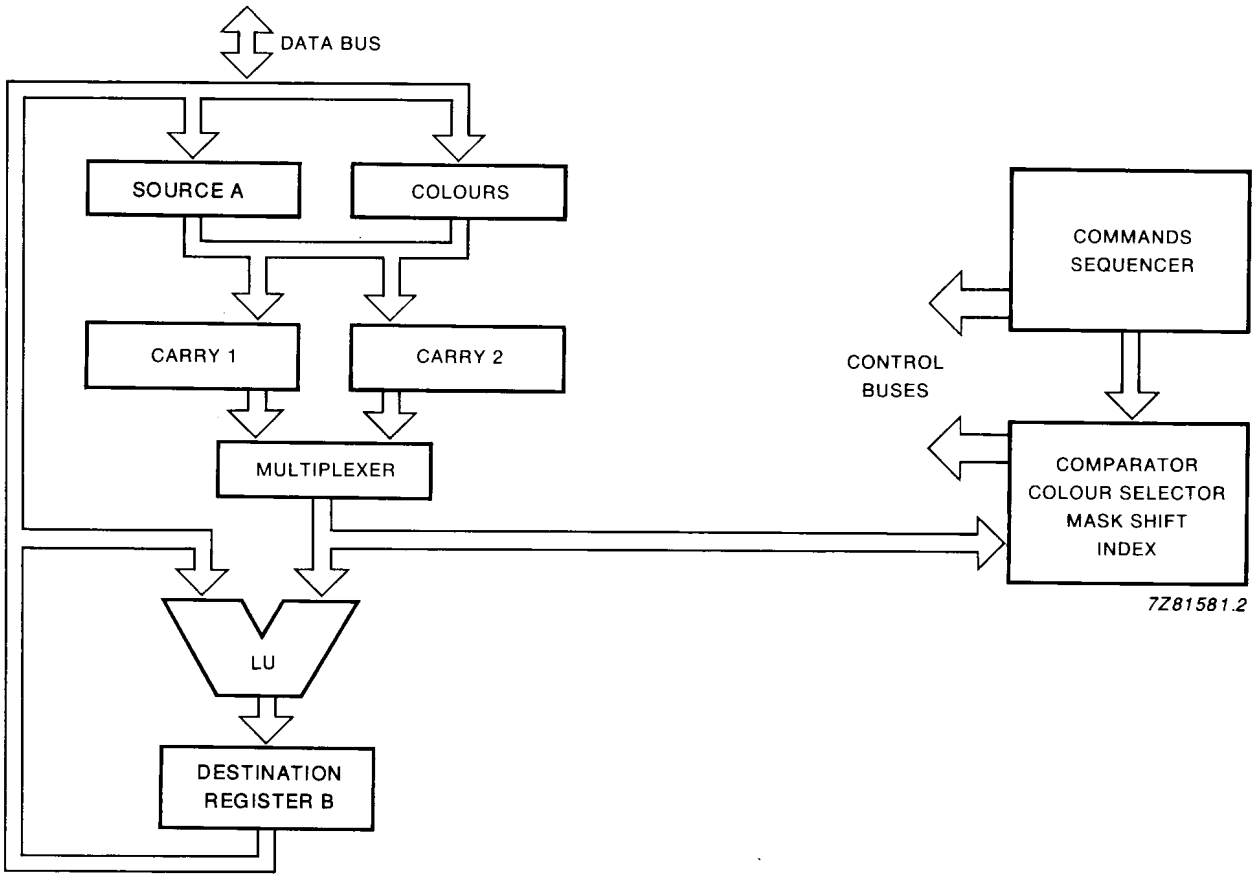


Fig.27 PIXAC block diagram.

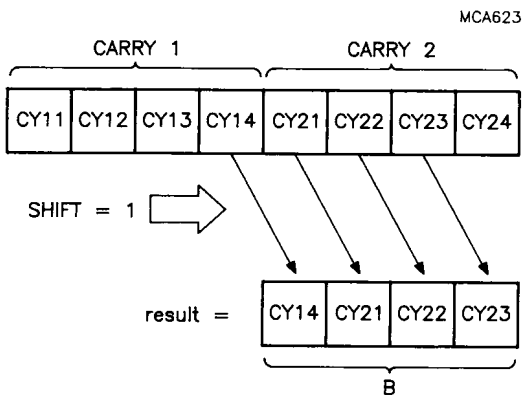


Fig.28 Shift operation.

Four main types of operations are performed:

1. Operations to copy patterns.
2. Operations to exchange patterns.
3. Operations to colour patterns.
4. Operations to compress patterns.

Operations to copy patterns.

COPY Source pixels are copied into destination pixels.

PATCH Same as COPY except that the transparent source pixels do not overwrite the respective destination pixels.

A pixel is transparent when its value is the same as the transparent colour in Register TC. For clearing patterns, software can create a WRITE operation which consists of repeatedly copying a sourceword into the destination pattern.

Operations to exchange patterns.

EXCHANGE Source pixels are exchanged with destination pixels.

SWAP Same as EXCHANGE except that the transparent source pixels are not exchanged.

As the shift operation is from left to right, if the nibbles in the destination word are misaligned to the left of the source word nibbles, then an apparent right-to-left shift operation must be performed. This 'inverted' sequence operation is enabled by setting bit 2 in the Pixac command register.

Operations to colour patterns

Patterns may be coloured using two different colours. The foreground colour is held in register FC and the background colour held in register BC.

COLOUR1 For non-transparent source pixels, the destination pixels are changed to the current foreground colour. For transparent source pixels, destination pixels are not overwritten.

COLOUR2 Same as COLOUR1 except that for transparent source pixels, the destination pixels are changed to the current background colour.

BCOLOUR1 The source word contains bits and they are extended into pixels via the pixel path.
For source bits = 1, the destination pixels are changed to the current foreground colour. For source bits = 0, the destination pixels are not overwritten. An index is used to point to the source nibble to be processed, it is automatically incremented .

BCOLOUR2 Same as BCOLOUR1 except that for source bits = 0, the destination pixels are changed to the current background colour.

Operations to compress patterns

COMPARE The source pixels are tested with the transparent colour. The result is in the most significant nibble of the Register B.

COMPACT Same as COMPARE except that for each test, the result is placed in the nibble indicated by an index. The index is automatically incremented.

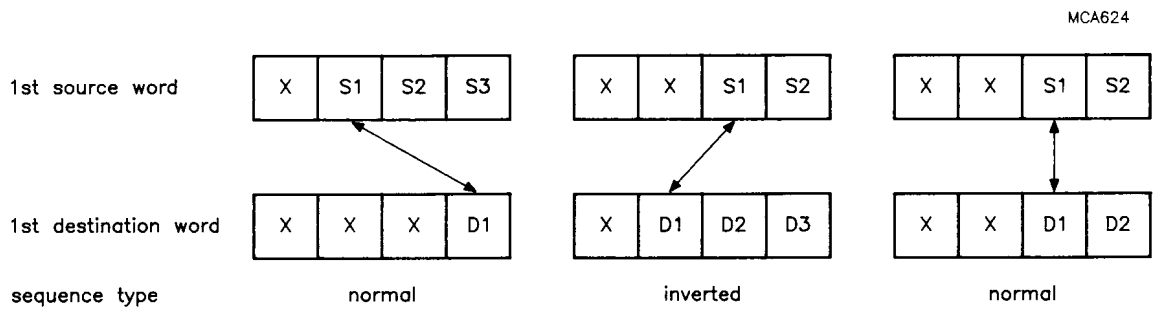


Fig.29 Inverted exchange sequence.

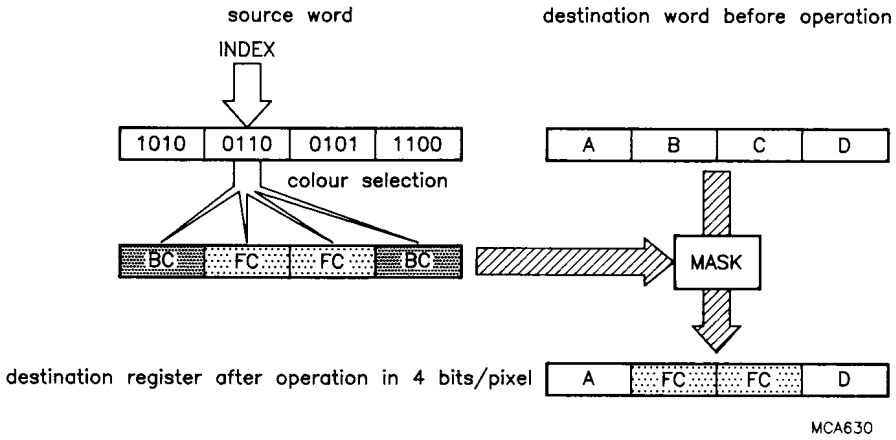


Fig.30 BCOLOUR1 example.

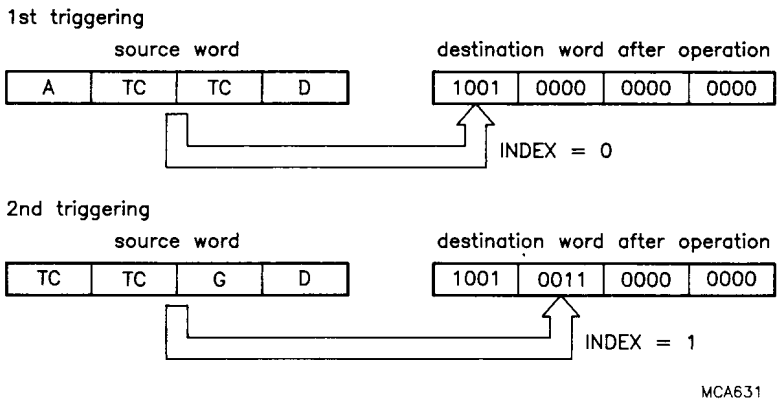


Fig.31 COMPACT example in 4 bits/pixel.

Note to Fig.31.

The previous nibble has been masked automatically and the index has been incremented.

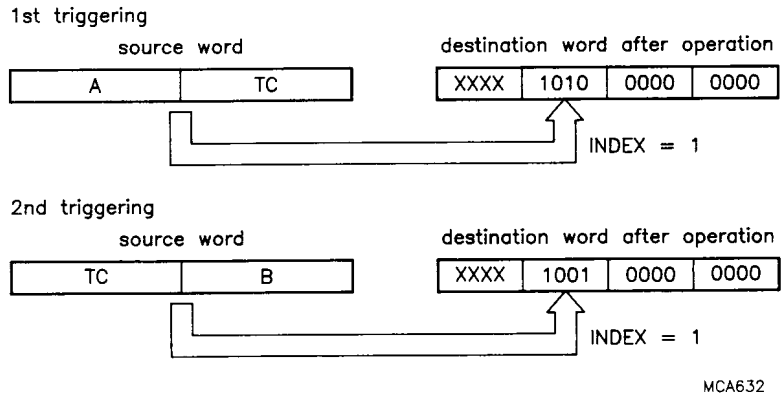


Fig.32 COMPACT example in 8 bits/pixel.

Note for Fig.32.

In 8 bits/pixel mode the 2 bits resulting from the first trigger are duplicated and a second trigger is required for a complete resulting nibble. This is also true for COMPARE.

Pixac driver loops

The PIXAC logic must be used with a software routine in order to perform manipulations on patterns of pixels. Using a rectangular pattern of 'm' lines and 'n' words, the general flowchart would be as shown in Fig.33.

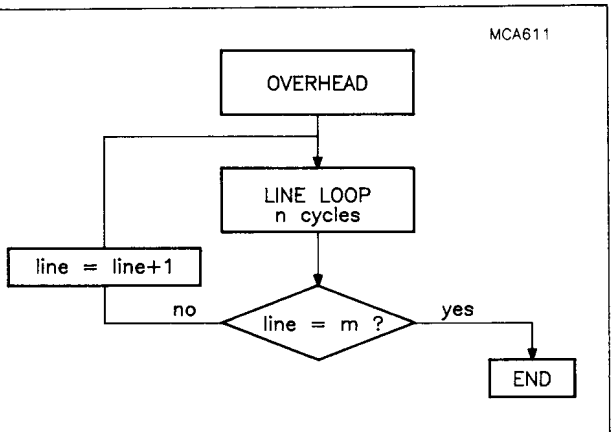


Fig.33 PIXAC software loop.

The overhead consists of:

1. The calculation of the shift necessary for the alignment of source and destination pixels.
2. The determination of the mask template which will be placed at the beginning and at the end of the lines, in order to protect destination pixels which are not involved in the manipulation.
3. Initialization of the operation, mask, shift and colour registers in PIXAC.

The loop itself consists of:

1. Loading the PIXAC source and destination registers with the source and destination data thus triggering the PIXAC sequencer.
2. Saving the results of the manipulation.
3. Counting the number of words to manipulate in the line.

Loop description

The loops described below are only concerned with pixel transfers via the source and destination registers. The following should be noted:

1. The pixel count and mask change are not considered.
2. The loop entry point is not necessarily, at the top.
3. The loop exit point is not necessarily, at the bottom.

The notation used to describe the operations is as follows:

S = source word
D = destination word
A = Register A
B = Register B

Writing to registers:

D -> A
or D -> B
or S -> A

Reading registers:

B -> D
or B -> S

The PIXAC sequencer is triggered by writing to Register A for Type A operations, or by writing to Register B for Type B operations (see below).

Type A operation: S -> A Trigger
Type B operation: D -> B Trigger

COPY and PATCH type B

1. Basic operation

```
S  -> A
D  -> B          Trigger
      B -> D
```

2. Operation with zoom factor 2

```
S  -> A
D  -> B          Trigger
      B -> D
D  -> B          Trigger
      B -> D
```

COPY and PATCH type A

1. Basic operation

```
D  -> B          (optional if COPY)
S  -> A          Trigger
      B -> D
```

2. Operation with shrink factor 2

```
D  -> B          (optional if COPY)
S  -> A          Trigger
S  -> A          Trigger
      B -> D
```

EXCHANGE and SWAP

1. Operation with normal sequence

```
S  -> A          Trigger
      B -> D
D  -> A          Trigger
      B -> S
```

2. Operation with inverted sequence

```
D  -> A          Trigger
      B -> S
S  -> A          Trigger
      B -> D
```

Note.

Prior to the first loop a (D -> A) operation is required, if an inverted sequence then a (S -> A) operation is required.

COLOUR1 and COLOUR2

```
S  -> A
D  -> B          Trigger
      B -> D
```

BCOLOUR1 and BCOLOUR2

The source nibbles are processed from left to right. At each triggering, the processed nibbles are specified.
Source word = | nibble 1 | nibble 2 | nibble 3 | nibble 4 |.

1. Operation with shrink factor 2 in 4 bits/pixel

```
S  -> A
D  -> B          Trigger     nibble 1 and 2
      B -> D
D  -> B          Trigger     nibble 3 and 4
      B -> D
```

Note. The INDEX must be 1 or 3.

2. Basic operation in 4 bits/pixel or operation with shrink factor 2 in 8 bits/pixel

```
S  -> A
D  -> B          Trigger     nibble 1
      B -> D
D  -> B          Trigger     nibble 2
      B -> D
D  -> B          Trigger     nibble 3
      B -> D
D  -> B          Trigger     nibble 4
      B -> D
```

3. Operation with zoom factor 2 in 4 bits/pixel or basic operation in 8 bits/pixel.

```
S  -> A
D  -> B          Trigger     2 MSB's of nibble 1
      B -> D
D  -> B          Trigger     2 LSB's of nibble 1
      B -> D
      :
      :
D  -> B          Trigger     2 LSB's of nibble 4
      B -> D
```

4. Operation with zoom factor 2 in 8 bits/pixel

```
S  -> A
D  -> B          Trigger     MSB of nibble 1
      B -> D
D  -> B          Trigger     2nd MSB of nibble 1
      B -> D
D  -> B          Trigger     3rd MSB of nibble 1
      B -> D
D  -> B          Trigger     LSB of nibble 1
      B -> D
      :
      :
D  -> B          Trigger     LSB of nibble 4
      B -> D
```

COMPARE

The feature of COMPARE is to read the results of the transparency test. In this case the concept of destination is not necessary.

```
S  -> A          Trigger
      B = result
```

COMPACT

1. Operation in 4 bits/pixel

D -> B (optional)
S -> A Trigger
S -> A Trigger
S -> A Trigger
S -> A Trigger
B -> D

2. Operation in 8 bits/pixel

D -> B Optional
S -> A Trigger
S -> A Trigger
S -> A Trigger
S -> A Trigger
S -> A Trigger
S -> A Trigger
S -> A Trigger
S -> A Trigger
B -> D

PIXAC implicit addressing

This mode reduces the CPU load and allows faster pixel manipulation by allowing in fewer instructions to:

1. Read memory
2. Trigger PIXAC sequence
3. Read PIXAC register B
4. Store the result into memory

When the CPU accesses the PIXAC, the implicit PIXAC addressing mode is validated by using the IPA pin.

In normal mode (without implicit addressing mode), a minimum number of instructions are required in the software loops typically:-

- Read memory and write to register A or B in order to trigger the PIXAC sequence (one instruction).
- Write the contents of register B into memory (one instruction).

In implicit addressing mode, this can be achieved using one CPU instruction.

Example using COPY type A loop and 68000 assembly code:

Normal mode

move.w (a0),PIXAC-A
move.w PIXAC-B,(a1)

Where:- a0 is the Source memory address
a1 is the Destination address

IPA mode

move.w (a0),(a1)

Where:- a0 is the Source memory address with IPA high
a1 is the Destination address with IPA high

Setting the IPA is achieved if any of the address bits A21 to A23 are HIGH. Before addressing data in memory, the actual address should be OR-ed with the correct address MSB's. Therefore a ghost memory space must be made available and reserved for implicit addressing of the PIXAC.
When the IPA pin is set to 1, the PIXAC register implicitly addressed is either:

- Register A: Memory is read for a PIXAC operation type A.
- Register B: Memory is read for a PIXAC operation type B or when memory is written to.

Loop description using IPA

The syntax is the same as in normal mode but also when IPA is set, the bold font is used. "d" means any CPU data register (preferable) or any other register.

COPY and PATCH type B

1. Basic operation

S ->A
D - - - -> **D** Trigger

2. Operation with zoom factor 2

S ->A
D - - - -> **D** Trigger
D - - - -> **D** Trigger

COPY and PATCH type A

1. Basic operation

D -> B (optional if COPY)
S - - - -> **D** Trigger

2. Operation with shrink factor 2

D -> B (optional if COPY)
S -> **d** Trigger
S - - - -> **D** Trigger

EXCHANGE and SWAP

1. Operation with normal sequence

S - - - -> **D** Trigger
D - - - -> **S** Trigger

2. Operation with inverted sequence

D ----> **S** Trigger
S ----> **D** Trigger

Note.

Prior to the first loop a (D -> A) operation is required, if an inverted sequence then a (S -> A) operation is required.

COLOUR1 and COLOUR2

S ->A
D - - - -> **D** Trigger

BCOLOUR1 and BCOLOUR2

1. Operation with shrink factor 2 in 4 bits/pixel mode

S ->A
D ----> **D** Trigger Nibble 1 and 2
D ----> **D** Trigger Nibble 3 and 4

Note: The first INDEX value must be 1 or 3.

2. Basic operation in 4bits/pixel mode or operation with shrink factor 2 in 8bits/pixel mode

S ->A
D ----> **D** Trigger nibble 1
D ----> **D** Trigger nibble 2
D ----> **D** Trigger nibble 3
D ----> **D** Trigger nibble 4

3. Operation with zoom factor 2 in 4 bits/pixel mode or basic operation in 8 bits/pixel mode

S ->A
D ----> **D** Trigger 2 MSB's of nibble 1
D ----> **D** Trigger 2 LSB's of nibble 1
D ----> **D** Trigger 2 LSB's of nibble 4

4. Operation with zoom factor 2 in 8 bits/pixel mode

S ->A
D ----> **D** Trigger 1st MSB of nibble 1
D ----> **D** Trigger 2nd MSB of nibble 1
D ----> **D** Trigger 3rd MSB of nibble 1
D ----> **D** Trigger 4th MSB of nibble 4

COMPACT

1. Operation in 4 bits/pixel mode

D ->B (optional)
S ->**d** Trigger
S ->**d** Trigger
S ->**d** Trigger
S ----> **D** Trigger

2. Operation in 8bits/pixel mode

D ->B (optional)
S ->**d** Trigger
S ->**d** Trigger
S ->**d** Trigger
S ->**d** Trigger
S ->**d** Trigger
S ->**d** Trigger
S ->**d** Trigger
S ----> **D** Trigger

COPROCESSOR INTERFACE

The SCC66470 interface permits an additional CPU or coprocessor to access the DRAM, PIXAC and registers. The coprocessor is connected to the SCC66470 via the Memory Data bus (MD), the Memory Address bus (MA), and the Control lines. Handshake pins CYREQN, CYACKN and RASN are provided to request and acknowledge the information exchange between the SCC66470 and the coprocessor. The coprocessor (or CPU) can use the pixel accelerator of the SCC66470 to speed up the manipulation.

Interface

Three types of exchange are possible:

Type A: Exchange between the coprocessor and the memory.
Type B: Exchange between the coprocessor and the internal registers.
Type C: Exchange between the memory and PIXAC registers (driven by the coprocessor).

An exchange takes place as follows:

1. The coprocessor asserts CYREQN.
2. On the rising edge of CYACKN, the coprocessor supplies address and control information to the MA and MD buses.
3. On the falling edge of RASN; CYREQN and the Memory Address bus must be released. The Memory Data bus must be released for a Type C exchange and for a read cycle. For a write cycle and for Type A or B exchanges, the data bus must contain the written data.
4. For a Type A or B exchange, the rising edge of a second CYACKN indicates that the exchange is completed and that the MD bus must be released for a write cycle.

The information the coprocessor sends to the SCC66470 after the rising edge of CYACKN must contain the following:

- The address information, 20 bits for 256K DRAMs or 18 bits for 64K DRAMs.
- The Read/Write information, 2 bits to work at byte level.
- The direct PIXAC register selection SELA or SELB. If one of these signals is active then an exchange Type C is performed (pixac registers are implicitly addressed), otherwise it is a Type A or B exchange (pixac registers are addressed as memory locations).

The correspondence between the coprocessor control information and the Memory Address and Memory Data buses is shown in Table 19.

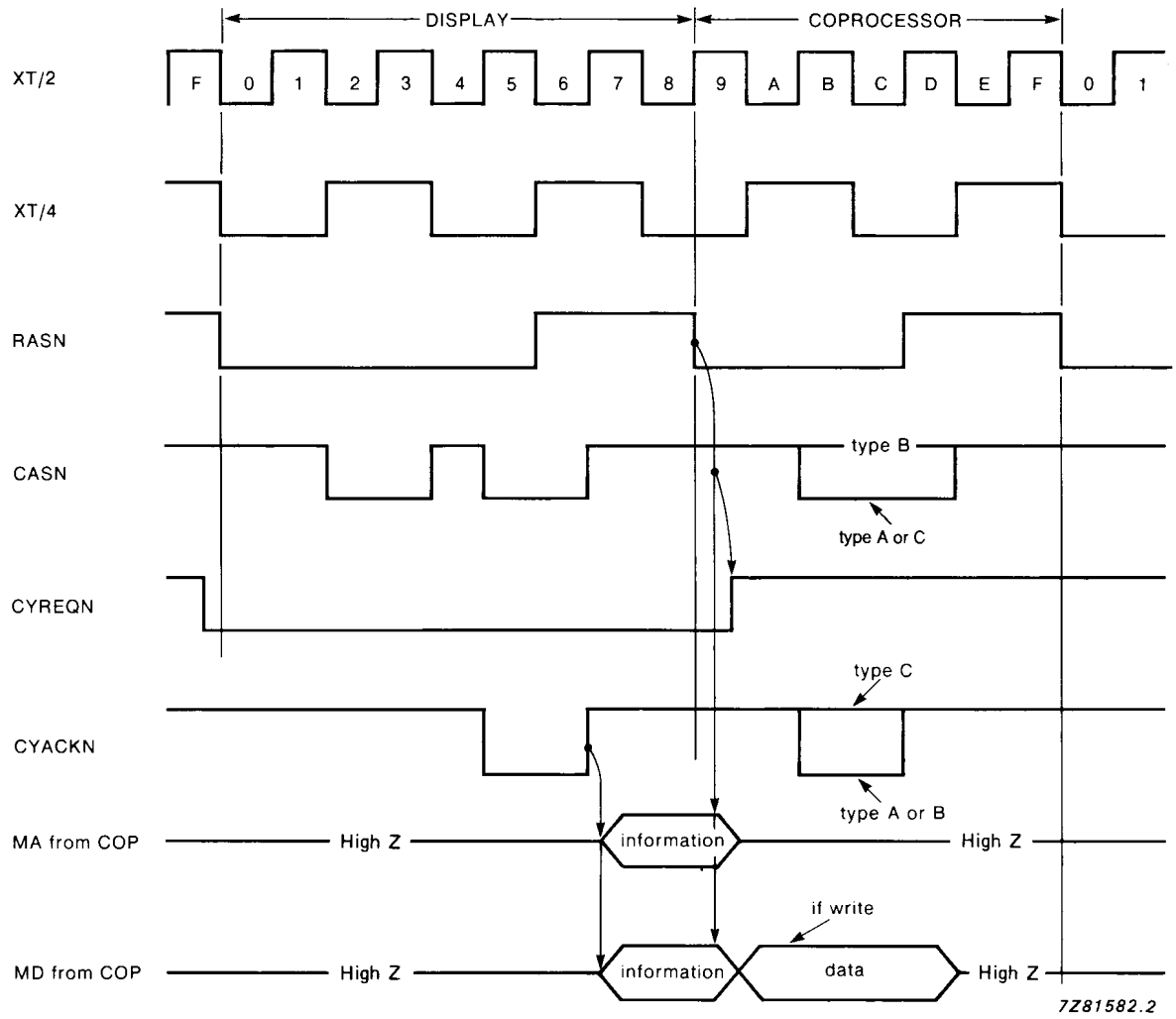


Fig.34 Coprocessor interface in FAST mode.

Table 19 Coprocessor information.

COPROCESSOR INFORMATION	256K			64K		
	NORMAL AND NIBBLE	PAGE	VRAM	NORMAL AND NIBBLE	PAGE	VRAM
A1	MA0 R	MD0 C	MD0 C	MA0 R	MD0 C	MD0 C
A2	MA1 R	MA1 R	MD1 C	MA1 R	MA1 R	MD1 C
A3	MA2 R	MA2 R	MD2 C	MA2 R	MA2 R	MD2 C
A4	MA3 R	MA3 R	MD3 C	MA3 R	MA3 R	MD3 C
A5	MA4 R	MA4 R	MD4 C	MA4 R	MA4 R	MD4 C
A6	MA5 R	MA5 R	MD5 C	MA5 R	MA5 R	MD5 C
A7	MA6 R	MA6 R	MD6 C	MA6 R	MA6 R	MD6 C
A8	MA7 R	MA7 R	MD7 C	MA7 R	MA7 R	MD7 C
A9	MA8 R	MA8 R	MD8 C	MA8 R	MA8 R	MA7 R
A10	MD0 C	MA0 R	MA0 R	MD0 C	MA0 R	MAO R
A11	MD1 C	MD1 C	MA1 R	MD1 C	MD1 C	MA1 R
A12	MD2 C	MD2 C	MA2 R	MD2 C	MD2 C	MA2 R
A13	MD3 C	MD3 C	MA3 R	MD3 C	MD3 C	MA3 R
A14	MD4 C	MD4 C	MA4 R	MD4 C	MD4 C	MA4 R
A15	MD5 C	MD5 C	MA5 R	MD5 C	MD5 C	MA5 R
A16	MD6 C	MD6 C	MA6 R	MD6 C	MD6 C	MA6 R
A17	MD7 C	MD7 C	MA7 R	MD7 CAS	MD7 CAS	MA8 CAS
A18	MD8 C	MD8 C	MA8 R	MD8 CAS	MD8 CAS	MD8 CAS
A19	MD9 CAS	MD9 CAS	MD9 CAS	- - -	- - -	- - -
A20	MD10 CAS	MD10 CAS	MD10 CAS	- - -	- - -	- - -
SELA	MD12	MD12	MD12	MD12	MD12	MD12
SELB	MD13	MD13	MD13	MD13	MD13	MD13
R/WNL	MD14	MD14	MD14	MD14	MD14	MD14
R/WNH	MD15	MD15	MD15	MD15	MD15	MD15

Notes to Table 19.

1. A1 to A20 are the coprocessor address bits (word address).
2. R/WHN and R/WLN are the write signals, i.e. the HIGH and LOW bytes of the DRAM bus.
3. SELA or (exclusive) SELB are asserted for the EXCHANGE Type C and correspond to implicit addressing of the PIXAC.
   If SELA is asserted, only register A of pixac is implicitly addressed, whatever pixac operation type used.
   If SELB is asserted, only register B of pixac is implicitly addressed, whatever pixac operation is type A or type B.
4. R or C means that the coprocessor information will be valid either on RASN or CASN assertion.
5. CAS means that the coprocessor information bit is used to select a DRAM bank.
6. "- - -" means that the coprocessor address bit is not useful.

Example of SELA or SELB use:

PIXAC registers can be addressed without implicit addressing mode using exchange Type A or Type B. Registers A and B can be implicitly addressed, using SELA or SELB.

The COPY Type B basic operation is represented as:

S -> A		Read memory and write pixac
D -> B	Trigger	Read memory and write pixac
B -> D		Read pixac and write memory

This operation can be driven using SELA, SELB. In such a case the sequence then becomes:

S -> d		using SELA	Read memory. Pixac is implicitly addressed. 'd' represents any internal data register of the coprocessor.
D -> D	Trigger	using SELB	Read and write to memory. Pixac is implicitly written then read.

Character generator ROM access

Setting the CG bit in the CSR register enables a Type A or Type C exchange with ROM. The ROM must be placed on the DRAM bus instead of the system bus. The ROM can then directly be used by the coprocessor. An interesting application is a character ROM which can be used with PIXAC in order to perform character insertion.

The ROM must reside in the BANK 3 area. As ROM access times are relatively slow the SCC66470 postpones the data transfer to the next available window. ROM addresses must be latched after the first CAS3N assertion. ROM data output is enabled by the CSCGN signal; the exchange is completed when CSCGN becomes inactive. Character ROM may not be accessed through the CPU port.

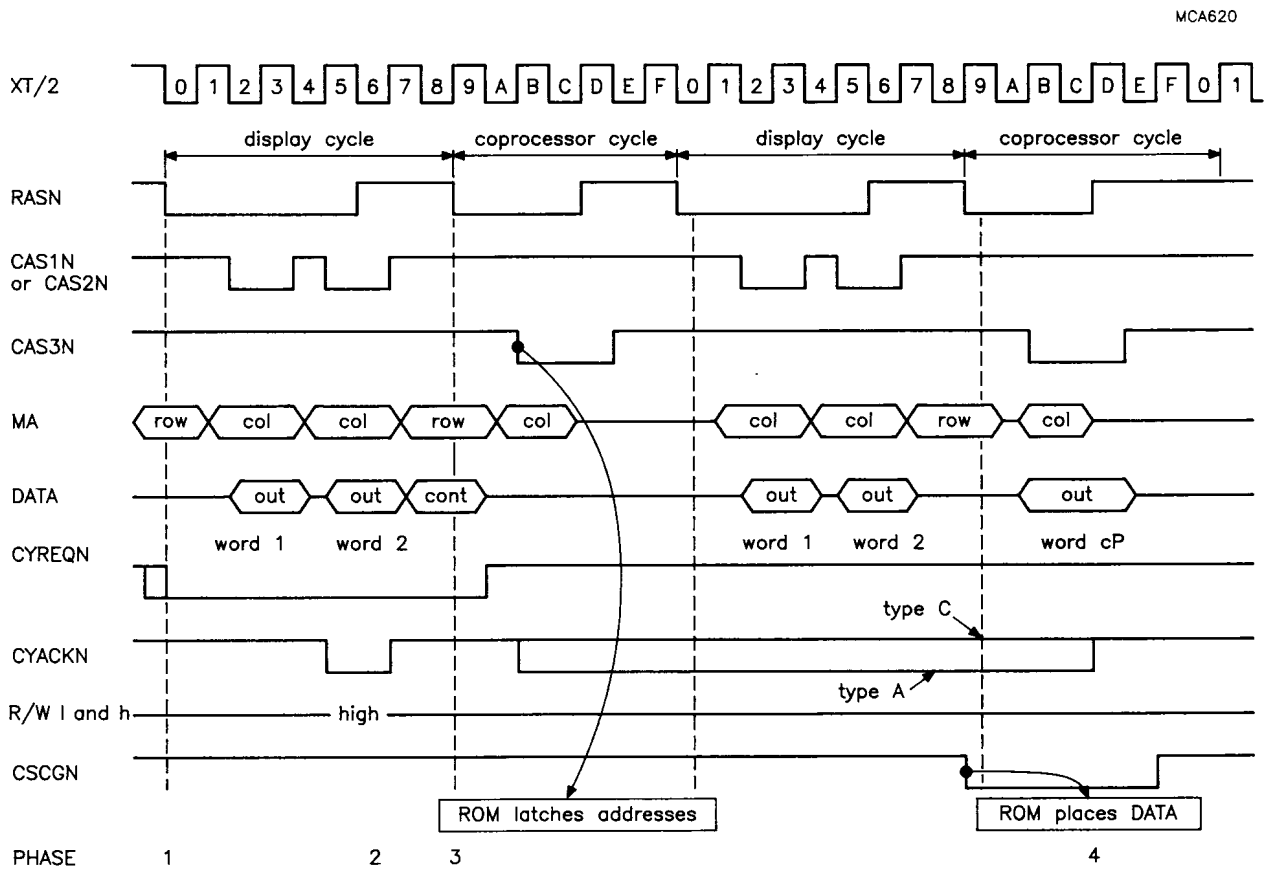


Fig.35 Timing COP <-> CHAR. ROM (type A)
CHAR. ROM <-> PIXAC (type C).

REGISTER DESCRIPTION

The SCC66470 registers are described in Table 20.

Table 20 SCC66470 registers.

ACRONYM	ADDRESS (HEX)	R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSR	1FFFEO	W	D11	D12	x	x	x	EW	DD1	DD2	DM1	DM2	TD	CG	DD	ED	ST	BE
CSR	1FFFE1	R	x	x	x	x	x	x	x	x	DA	FG	PA	x	x	IT2	IT2	BE
DCR	1FFFE2	W	DE	CF1	CF2	FD	SM	SS	LS	CM	FG	DF	IC	DC	*	*	*	*
VSR	1FFFE4	W	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
BCR	1FFFE7	W	x	x	x	x	x	x	x	x	*	*	*	*	*	*	*	*
DCR2	1FFFE8	W	x	OM1	OM2	ID	MF1	MF2	FT1	FT2	x	x	x	x	*	*	*	*
DCP	1FFFEA	W	*	*	*	*	*	*	*	*	*	*	*	*	*	*	x	x
SWM	1FFFEC	W	*	*	*	*	*	*	*	*	x	x	x	x	x	x	x	x
STM	1FFFEF	W	x	x	x	x	x	x	x	x	*	*	*	*	*	*	*	*
A	1FFFF0	W	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
B	1FFFF2	R/W	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
PCR	1FFFF4	W	4N	COL	EXC	CPY	CMP	RTL	SHK	ZOM	*	*	*	*	INV	BIT	TT	NI
MASK	1FFFF7	W	x	x	x	x	x	x	x	x	x	x	x	x	*	*	*	*
SHIFT	1FFFF8	W	x	x	x	x	x	x	*	*	x	x	x	x	x	x	x	x
INDEX	1FFFFB	W	x	x	x	x	x	x	x	x	x	x	x	x	x	x	*	*
FC	1FFFFC	W	*	*	*	*	*	*	*	*	x	x	x	x	x	x	x	x
BC	1FFFFD	W	x	x	x	x	x	x	x	x	*	*	*	*	*	*	*	*
TC	1FFFFE	W	*	*	*	*	*	*	*	*	x	x	x	x	x	x	x	x

Notes to Table 20.

1. '*' denotes data, the LSB is on the right.
2. 'x' denotes don't care states.
3. Specified addresses in this table are valid for master and slave TV mode only.

SYSTEM AND DISPLAY ORIENTED REGISTERS

Control and Status register (CSR)

The CSR register controls the system related functions of the device. When written to, it functions as a CONTROL register and when read acts as a STATUS register. The Control register is reset to zero during the initialization sequence.

Control register (write operations).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DI1	DI2	-	-	-	EW	DD1	DD2	DM1	DM2	TD	CG	DD	ED	ST	BE

DI1-DI2 When set to 1, disables the propagation to the INTN pin for the respective IT1 and IT2 bits (see STATUS register). These bits do not disable the IT1 and IT2 bits.

EW When set to 1, the DTACKN for a write cycle is generated 2 slots (66 ns at 30 MHZ) before the DTACKN for the read cycle.

DD1-DD2 Enabled when DD = 1. These 2 bits permit 4 different delays for the DTACKN generation when the CPU accesses the system ROM. The theoretical delay between the CPU request and the DTACKN generation is as following:

DD	DD1	DD2	SLOTS	nS AT 30MHz
0	X	X	16 - 18	533 - 600
1	0	0	8 - 10	266 - 333
1	0	1	4 - 6	133 - 200
1	1	0	6 - 8	200 - 266
1	1	1	12 - 14	400 - 466

DM1-DM2 DRAM access mode control bits. The following configurations may be selected:

DM1	DM2	DRAM MODE	TIMING SPEED
0	0	NORMAL	SLOW mode
0	1	PAGE	FAST mode
1	0	NIBBLE	FAST mode
1	1	DUAL PORT	SLOW mode

TD — DRAM type. '0' for 64K devices and '1' for 256K devices.

CG — When set to 1, enables the character generator mode. In this case the timing of the CAS3N and the CSCGN pins change to be ROM compatible.

DD — DTACK DELAY enable for the ROM. See DD1-DD2.

ED — EARLY DTACK. If ED bit = 0, DTACKN will be asserted when data is available on system bus. If ED = 1, an EARLY DTACK will be generated two slots (66 ns at 30 MHz) before data is valid.

ST — STANDARD bit. When set to 1, this bit permits a resolution modification in order to display images which have not the resolution indicated by the DCR register. The effect as follows:
Vertical resolution: In 50 Hz mode (FD = 0), the resolution is shortened by 20 lines at the top and 20 lines at the bottom. Images created in a 60 Hz system are then directly usable in a 50 Hz system.
Horizontal resolution: The effect is active in full screen and physical screen mode.

- In 28 MHz, the bit-map file is 384 pixels wide instead of 360 pixels. The horizontal resolution is unchanged but it is possible to display bit-map, run-length or mosaic coded images created with a 30 MHz system.
- In 30 MHz, the horizontal resolution is decreased from 384 pixels to 360 pixels. 24 pixels are masked at the right hand side of the screen.

BE — Bus error enable. When BE is set, the watchdog timer and BERR generation are both enabled.

Status register (read operations).

7	6	5	4	3	2	1	0
DA	FG	PA	-	-	IT2	IT1	BE

DA — Vertical display active. The DA bit is set when the display controller is fetching information from the video memory. It is not affected by a horizontal retrace.

FG — This bit is set when frame grabbing is enabled. (Frame grabbing is selected by setting the FG bit in the DCR register). It is reset at the end of the grabbing period which lasts for one frame, or 2 frames when in interlace mode.

PA — This bit indicates the frame parity when the scan mode is in the interlace or interlace field repeat mode. It is a logic 1 for the odd frame, and logic 0 for the even frame.

IT1 — IT1 can be set by the DCA mechanism to generate an interrupt to the CPU. At the same time, the INTN pin goes LOW. When the CPU reads the status register, the IT1 bit is reset and the INTN output is deactivated.

IT2 — IT2 can be set by clearing bits 11 to 14 in the Pixac Command Register (PCR). This action informs the CPU that the PIXAC is free and generates an interrupt request by asserting the INTN pin. The pin is reset when the CPU reads the status register or when a logic 1 is present in any of the bits 11 to 14 of the PCR register.

BE — This bit is set when a BUS ERROR condition is generated by the Watch-Dog timer. BE is reset when the CPU reads the Status register.

Display Command Register (DCR)

The Display Command Register (DCR) contains the display control bits and the four MSB's of the Video start address. Bits 4 to 15 are reset to zero during the RESET sequence.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DE	CF1	CF2	FD	SM	SS	LS	CM	FG	DF	IC	DC	A19	A18	A17	A16

DE Display enable. When set, the display controller is enabled.

CF1-CF2 The state of these bits are to be set as determined by the frequency of the crystal oscillator. See below:

CF1	CF2	FREQUENCY (MHz)
0	0	20
0	1	24
1	0	28
1	1	30

FD Frame duration control. When FD = 0, a 50 Hz scan is generated. When FD = 1, a 60 Hz scan frequency is generated.

SM-DF These two bits are used to select the scan mode, as shown below:

SM	DF	SCAN MODE
0	0	non interlace
0	1	double frequency (not allowed when 20 MHz mode is progammed)
1	0	interlace
1	1	interlace field repeat

SS Screen size control. When SS is set to 1, a full screen display is generated. When SS is reset, a display with borders is generated.

LS Logical screen select. LS selects either a Logical screen (LS = 1) or a physical screen (LS = 0). A Logical screen takes 512 Bytes per video line regardless of the status of CF1 and CF2.

CM Colour mode select. When CM is set, the 4 bits per pixel mode is selected. When CM is reset, the 8 bits per pixel mode is selected.

FG Frame grabbing enable. When the FG bit is set to 1, frame grabbing is active during the next frame (or the next two frames for the interlace mode). It is automatically reset after the grabbing operation. FG may be read from the CSR register.

IC, DC These two bits enable the ICA and DCA mechanisms.

IC	DC	MECHANISM
0	0	ICA and DCA inactive
0	1	ICA active, Reduced DCA mode, (DCA = 16 bytes)
1	0	ICA active, DCA inactive
1	1	ICA active, DCA active (DCA size = 64 bytes)

A19-A16 Most Significant Bits of the Video Start Address. These four bits are used in conjunction with the VSR register.

Display Command Register 2 (DCR2)

This second DCR register contains the display control bits and the four MSB bits of the DCA pointer. Only the display control bits are reset to zero during the reset sequence.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	OM1	OM2	ID	MF1	MF2	FT1	FT2	-	-	-	-	A19	A18	A17	A16

OM1-OM2 The OM1 and OM2 bits, in conjunction with the CM bit in the DCR register select one of the six video output modes.

ID Independent DCA bit. If the IC or DC bits in the DCR register are set, this bit is also set and the independent DCA is enabled. When ID is reset to zero, the interleaved DCA mode is enabled.

MF1-MF2 The MF1 and MF2 bits select the horizontal Mosaic Factor as shown in the table below:

MF1	MF2	MOSAIC FACTOR
0	0	2
0	1	4
1	0	8
1	1	16

FT1-FT2 These bits select the type of file to be displayed.

FT1	FT2	FILE TYPE
0	X	BIT MAP
1	0	RUN-LENGTH
1	1	MOSAIC

A19-A16 Bits A16 to A19 are the MSB's of the DCA pointer.

Video Start Register (VSR)

This 16 bit register, plus bits 0 to 3 in the DCR register form the 20 bit Video Start Register. The contents of the VSR register point to the first byte of the display area which can be located anywhere in the first DRAM Megabyte. Horizontal or vertical rolling and subscreens can be implemented on the fly by the "reload VSR and STOP" ICA/DCA instruction. The VSR register may also be used as an ICA/interleaved DCA pointer with the "reload VSR" instruction. This allows indirect addressing inside ICA or DCA.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

DCA Pointer (DCP)

This 14 bit register plus bits 0 to 3 in the DCR2 register, form the 18 bit DCA pointer. The DCA pointer, which must be long word aligned, points to the first long word of the independent DCA. The independent DCA can thus be located anywhere in the first DRAM Mbyte.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	-	-

Border Colour Register (BCR)

This 8 bit register contains the BORDER colour. In the 4 bits per pixel mode, only bits 4 to 7 are significant.

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

PIXAC REGISTERS

The PIXAC logic contains registers necessary for data manipulation between source and destination registers. Only the destination register may be read.

Pixac command register (PCR)

This 16 bit register specifies the required operation and must be loaded prior to any data manipulation. Table 21 describes the PCR register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4N	COL	EXC	CPY	CMP	RTL	SHK	ZOM	LGF 3	LGF 2	LGF 1	LGF 0	INV	BIT	TT	NI

Table 21 The Pixac Command Register.

<table>
<tr><th>Bit</th><th>Name</th><th>Function</th></tr>
<tr><td>15</td><td>4N</td><td>When set to '0' the 4 bits/pixel mode is selected. When set to '1' the 8 bits/pixel mode is selected.</td></tr>
<tr><td>14</td><td>COL</td><td>When set to '1' the COLOUR and BCOLOUR functions are enabled.</td></tr>
<tr><td>13</td><td>EXC</td><td>When set, the EXCHANGE and SWAP functions are enabled.</td></tr>
<tr><td>12</td><td>CPY</td><td>The COPY and PATCH functions are enabled when this bit is a logic '1'.</td></tr>
<tr><td>11</td><td>CMP</td><td>A logic '1' enables the COMPARE and COMPACT functions.</td></tr>
<tr><td>10</td><td>RTL</td><td>RTL defines the data manipulation direction in order to avoid problems when the source and destination overlap. Depending on the state of RTL, the effective carry register is either carry1 (CY1) or carry 2 (CY2). When RTL is set, manipulation is from right to left and when RTL is reset manipulation from left to right.</td></tr>
<tr><td>9</td><td>SHK</td><td>When set, the source size is shrunk by a factor of 2. For COPY and PATCH, one source pixel (selected by NI) out of 2 is used for the manipulation. For BCOLOUR, one source bit out of 2 is used. SHK may not be. used for the other functions.</td></tr>
<tr><td>8</td><td>ZOM</td><td>When set the source size is zoomed by a factor of 2. For COPY and PATCH operations, each source pixel is duplicated. For BCOLOUR, each source bit is duplicated. ZOM may not be used for other functions.</td></tr>
<tr><td>7-4</td><td>LGF</td><td>These fours bits select one of the possible 16 logical functions which can be performed between the destination register and the expected result from the pixel path (see Logical Functions).</td></tr>
<tr><td>3</td><td>INV</td><td>When set, the transparency state of source pixels or source bits is inverted. Used for functions needing the transparency test. For BCOLOUR1 and COLOUR1, the destination pixels which are overwritten, change to the current background colour instead of foreground colour.</td></tr>
<tr><td>2</td><td>BIT</td><td>BIT affects the COPY, COLOUR, EXCHANGE and COMPARE operations as follows:
<table>
<tr><th>OPERATION</th><th>BIT = 0</th><th>BIT = 1</th></tr>
<tr><td>COPY</td><td>enables COPY Type B</td><td>enables COPY type A</td></tr>
<tr><td>COLOUR</td><td>enables COLOUR</td><td>enables BCOLOUR</td></tr>
<tr><td>EXCHANGE</td><td>normal exchange sequence; A is loaded first with the source word and then the destination word</td><td>inverted exchange; A is first loaded with the destination word and then the source word.</td></tr>
<tr><td>COMPARE</td><td>enables COMPARE</td><td>enables COMPACT</td></tr>
</table></td></tr>
<tr><td>1</td><td>TT</td><td>When TT is set, the PIXAC logic performs a transparency test between the source pixels and the transparent colour TC. When the test is positive, the respective destination pixels are not overwritten. TT is used for enabling PATCH, SWAP, Colour1 and BColour1 functions.</td></tr>
<tr><td>0</td><td>NI</td><td>Used for COPY with SHRINK. The bits selects 2 out for 4 source nibbles to be used in the manipulation as indicated in this table:
<table>
<tr><th>NI</th><th>4N</th><th>SOURCE NIBBLES</th></tr>
<tr><td>0</td><td>0</td><td>0 and 2</td></tr>
<tr><td>0</td><td>1</td><td>0 and 1</td></tr>
<tr><td>1</td><td>0</td><td>1 and 3</td></tr>
<tr><td>1</td><td>1</td><td>2 and 3</td></tr>
</table></td></tr>
</table>

The PCR register offers many possible combinations. Table 22 gives an overview of all the possibilities:

Table 22 Possible PIXAC functions.

		15	14	13	12	11	10	9	8	7-4	3	2	1	0
OPERATION	**TRIG**	**4N**	**COL**	**EXC**	**CPY**	**CMP**	**RTL**	**SHK**	**ZOM**	**LGF**	**INV**	**BIT**	**TT**	**NI**
COPY type A	A	n	0	0	1	0	n	n	0	n	X	1	0	n
COPY type B	B	n	0	0	1	0	n	0	n	n	X	0	0	0
PATCH type A	A	n	0	0	1	0	n	n	0	n	n	1	1	n
PATCH type B	B	n	0	0	1	0	n	0	n	n	n	0	1	0
EXCHANGE	A	n	0	1	0	0	0	0	0	n	X	n	0	0
SWAP	A	n	0	1	0	0	0	0	0	n	n	n	1	0
COLOUR1	B	n	1	0	0	0	n	0	0	n	n	0	1	0
COLOUR2	B	n	1	0	0	0	n	0	0	n	X	0	0	0
BCOLOUR1	B	n	1	0	0	0	0	n	n	n	n	1	1	0
BCOLOUR2	B	n	1	0	0	0	0	n	n	n	X	1	0	0
COMPARE	A	n	0	0	0	1	0	0	0	n	n	0	0	0
COMPACT	A	n	0	0	0	1	0	0	0	n	n	1	0	0

Notes to Table 22.

1. TRIG operations can be triggered by writing to either register A or register B. The name of the relevant register (A or B) is indicated.
2. n = 0 or 1.
3. X = Don't care states.

Logical functions

The PIXAC logic can perform operations between the result (R) of the pixel data path and the contents (D) of register B. The result (D') is stored in register B. The Logical Function bits (7 to 4 in the PCR register) are used to define the logical function as indicated in Table 23.

Table 23 Logical functions.

LGF BIT NUMBER 7	6	5	4	FUNCTION
0	0	0	0	D' = R
0	0	0	1	D' = NOT R
0	0	1	0	D' = 0
0	0	1	1	D' = 1
0	1	0	0	D' = NOT (D XOR R)
0	1	0	1	D' = D XOR R
0	1	1	0	D' = D AND R
0	1	1	1	D' = NOT D AND R
1	0	0	0	D' = NOT D AND NOT R
1	0	0	1	D' = D AND NOT R
1	0	1	0	D' = NOT D OR R
1	0	1	1	D' = D OR R
1	1	0	0	D' = D OR NOT R
1	1	0	1	D' = NOT D OR NOT R
1	1	1	0	D' = D
1	1	1	1	D'= NOT D

Source Register A

Register A is a 16-bit data register which must be loaded with the source word to be processed. During an EXCHANGE operation register A contains the source and destination word alternatively. Certain PIXAC operations (TYPE A) are triggered by writing into A.

Destination Register B

Register B is a 16-bit data register which must be loaded with the destination word before the pixels are processed. At the end of the process, register B holds the result. Certain PIXAC operations (TYPE B) are triggered by writing to B.

Mask Register (MASK)

This 4 bit register is used during the manipulation to mask the nibbles within the destination word. When reset to zero, the corresponding nibble is not changed by the PIXAC logic. A Mask example is shown in Fig.36.

Shift Register (SHIFT)

This 2-bit register specifies the shift to be performed during source alignment. The shift operation is always performed from left to right. The inverted shift operation can be performed by starting the PIXAC sequence with a dummy destination word associated with the 1st source word, and then the 1st destination word associated with the 2nd source word.

Index Register (INDEX)

This is a 2-bit pointer is used for BCOLOUR operations and determines which nibble in the source is to be used. For COMPACT operations the Index register indicates which nibble holds the result. In all cases (4 or 8 bits/pixel, ZOOM, SHRINK etc), it is automatically incremented after the PIXAC operation.

Foreground colour register (FC)

This 8-bit register contains the foreground colour which is used for COLOUR or BCOLOUR operations. In the 4 bits/pixel mode both nibbles are displayed alternately.

Background colour register (BC)

This 8-bit register contains the background colour which is used for COLOUR or BCOLOUR operations. In the 4 bits/pixel mode both nibbles are displayed alternately.

Transparent colour register (TC)

This 8-bit register contains the transparent colour. In 4 bits/pixel mode both nibbles are tested alternately.

Selective write mask register (SWM)

This 8-bit register contains the "Selective Write Mask". This feature enables each byte of the B register to be masked by the contents of SWM register, simultaneously. This allows manipulation on groups of bits of any length up to 8 bits.

Example: In 8 bits/pixel mode, 1 screen can use 5 bits/pixel and another screen can use 3 bits/pixel. The screen manipulation id made completely independently using the SWM register.

SWM = 11111000 for the first screen using the 5 MSBs.
SWM = 00000111 for the second screen using the 3 LBSs.

Selective test mask register (STM)

This 8-bit register contains the selective test mask. The "selective test mask" feature permits the disabling of the transparency test on bits indicated by the STM register. This allows many transparent colours for the same operation and manipulation on groups of bits of any length up to 8 bits.

example: TC = 0100 1001
STM = 1111 1100

Implies effective transparent colour = 0100 10nn
->0100 1000
->0100 1001
->0100 1010
->0100 1011

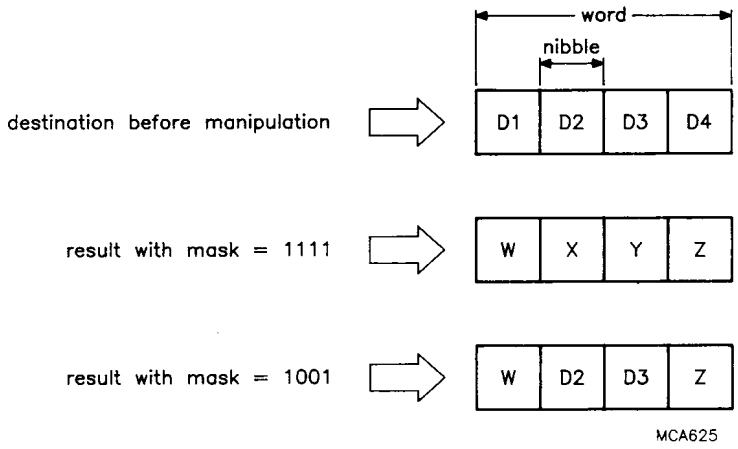


Fig.36 Mask example.

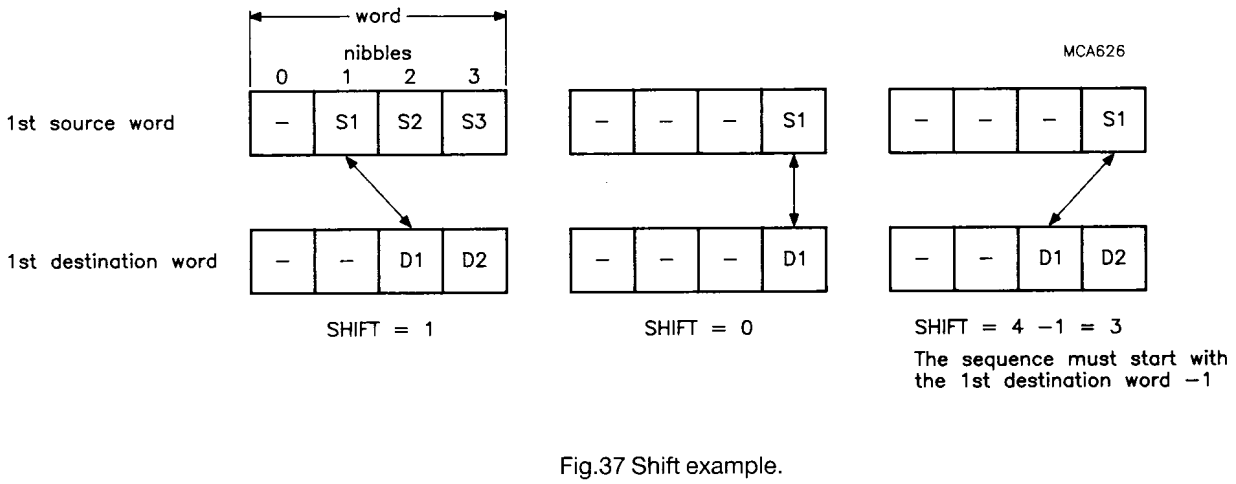


Fig.37 Shift example.

Note:

In the PIXAC 8 bits/pixel mode (4N = 1), the shift values to be used are 0 and 2.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply voltage	V_{DD}	−0.3	+6.5	V
Input voltage	V_I	−0.3	V_{DD} + 0.3	V
Output voltage	V_O	−0.3	V_{DD} + 0.3	V
Output current	I_O	-	± 20	mA
Power dissipation	P_{tot}	-	500	mW
Operating temperature range*	T_{amb}	−40	+85	°C
Storage temperature range	T_{stg}	−55	+150	°C

* Operating temperature is dependent on type number.

DC CHARACTERISTICS

V_{DD} = 5 V (±10%); V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; all voltages with respect to V_{SS} unless otherwise stated.

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{DD}	-	4.5	5	5.5	V
Operating supply current	I_{DDO}	XTAL = 30 MHz	-	-	100	mA
Input voltage						
All pins except RSTINN, XTAL1	V_{IH}	V_{DD} = 5 V	2.0	-	-	V
and HSYNCN	V_{IL}	V_{DD} = 5 V	-	-	0.8	V
Input voltage						
RSTINN and HSYCN	V_{IH}	V_{DD} = 5 V	2.4	-	-	V
	V_{IL}	V_{DD} = 5 V	-	-	0.8	V
XTAL1	V_{IH}	V_{DD} = 5 V	$0.8V_{DD}$	-	-	V
	V_{IL}	V_{DD} = 5 V	-	-	$0.2V_{DD}$	V
Input leakage	I_{LI}	-	−10	-	10	µA
Output voltage						
All pins except RASN, CASxN,						
UWRN, LWRN and PCLK	V_{OH}	I_O = −4 mA	V_{DD} − 0.8	-	-	V
	V_{OL}	I_O = +4 mA	-	-	0.4	V
Output voltage						
RASN, CASxN, UWRN, LWRN and						
PLCK	V_{OH}	I_O = −8 mA	V_{DD} − 0.8	-	-	V
	V_{OL}	I_O = +8 mA	-	-	0.4	V
Output leakage current	I_{LO}		−10	-	10	µA
Input capacity	C_I	$V_{DD} = V_I = 0$	-	-	10	pF
Output capacity	C_O	$V_{DD} = V_I = 0$	-	-	15	pF
Input/output capacity	$C_{I/O}$	$V_{DD} = V_I = 0$	-	-	15	pF
Pull-up resistance	R_{pup}	-	20	-	-	KΩ

Note.

1. I_{DDO} measurement conditions are to be defined.

AC CHARACTERISTICS

V_{DD} = 5 V (±10%); V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; V_{IL} = 0.8 V, V_{IH} = 2.2 V; V_{OL} = V_{OH} = 1.3 V. C_L (MA0-MA8, UWRN, LWRN) = 80 pF; C_L (CAS1N-CAS4N, RASN) = 160 pF; C_L (MD01-MD15, HSYNCN, CSYCN) = 75pF; C_L (system signals) = 130 pF; C_L (XT/2, PCLK, V0-V7, WRPN, BLANK, DA) = 75 pF; C_L (DTN, CSCGN) = 40 pF.
Frequency range (XTAL1, XTAL2) = 15 to 30.3 MHz.

NO.	CHARACTERISTIC	20 MHz		24 MHz		28 MHZ		30 MHz		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT
1	XTAL2 high to XT/2 high	5	33	5	33	5	33	5	33	ns
2	U/LDSN Low to slot set-up time	50	-	50	-	50	-	50	-	ns
3	Address to slot set-up time (read)	40	-	40	-	40	-	40	-	ns
4	CASN to Data valid (read)	-	50+Δ	-	50+Δ	-	50+Δ	-	50+Δ	ns
5	XT/2 to DTACK Low	-	15	-	15	-	15	-	15	ns
6	U/LDSN high to Data 3-state	-	50	-	50	-	50	-	50	ns
7	U/LDSN High to DTACKN high	-	45	-	45	-	45	-	45	ns
8	XT/2 to DTACK 3-state	-	15	-	15	-	15	-	15	ns
9	U/LDSN to RASN low in free-run	160	290	135	250	115	220	110	210	ns
10	U/LDSN to RASN low in free-run	110	240	95	205	80	185	75	180	ns
11	XT/2 to RASN low	−20	5	−20	5	−20	5	−20	5	ns
12	XT/2 to CASN low	−20	5	−20	5	−20	5	−20	5	ns
13	XT/2 to U/LWRN low	−20	5	−20	5	−20	5	−20	5	ns
14	XT/2 to MA0-MA8 valid	−10	30	−10	30	−10	30	−10	30	ns
15	Data to CASN high set-up time	0	-	0	-	0		0	-	ns
16	Data to CASN high hold time	15	-	15	-	15		15	-	ns
17	XT/2 high to PLCK low	0	40	0	40	0	40	0	35	ns
18	XT/2 high to PLCK high	0	40	0	40	0	40	0	35	ns
19	RASN high precharge time	155	-	130	-	110	-	95	-	ns
20	CASN high precharge time	190	-	160	-	135		125	-	ns
21	CASN high toggle precharge time	40	-	30	-	25		25	-	ns
22	XT/2 to RASN high	−20	10	−20	10	−20	10	−20	10	ns
23	XT/2 to CASN high	−20	15	−20	15	−20	15	−20	15	ns
24	PCLK low to pixels/BLANKN/DA valid	−5	10	−5	10	−5	10	−5	10	ns
25	Pixels/BLANKN/DA to PLCK valid	35	-	25	-	20	-	15	-	ns
26	CYREQN low to slot 3 set-up time	50	-	50	-	50	-	50	-	ns
27	CASN high to CYACKN high*	5	25	5	25	5	25	5	25	ns
28	CYACKN high to MA/MD valid*	0	20	0	20	0	20	0	20	ns
29	MA/MD to RASN low set-up time*	10	-	10	-	10	-	10	-	ns
30	MA/MD to RASN low hold time*	10	-	10	-	10	-	10	-	ns
31	CYREQN high to MA valid*	-	40	-	40	-	40	-	40	ns
32	MD to CYACKN high hold time*	0	-	0	-	0	-	0	-	ns
33	XT/2 to CSION	-	40	-	40	-	40	-	40	ns
34	U/LDSN to CSROMN or CSION	-	45	-	45	-	45	-	45	ns
35	U/LDSN to DTACKN low	-	70+sl	-	70+sl	-	70+sl	-	70+sl	ns

Notes.

1. Δ = DRAM access time from CASN.
2. sl = number of slots.
3. * = C_L (CASN, RASN) = 40 pF; C_L (CYACKN) = 30 pF; C_L (MA0-MA8) = 40 pF.

AC CHARACTERISTICS (continued)

NO.	CHARACTERISTIC	20 MHz		24 MHz		28 MHZ		30 MHz		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT
36	CASN pulse width during display	80	110	65	95	55	80	50	75	ns
37	CASN pulse width during CPU access	140	160	115	135	100	120	80	100	ns
38	RASN pulse width during display	290	310	240	260	205	255	190	210	ns
39	RASN pulse width during CPU access	190	210	155	175	130	150	125	145	ns
40	RASN hold time during display	35	55	30	50	25	45	20	40	ns
41	RASN hold time during CPU access	85	105	60	90	55	80	50	75	ns
42	CASN to RASN precharge time during display	90	110	70	90	60	80	55	75	ns
43	CASN to RASN precharge time during CPU access	90	110	70	90	60	80	55	75	ns
44	Write command pulse width	80	105	60	85	50	75	45	75	ns
45	CASN hold time during display	190	215	155	185	130	165	120	150	ns
46	CASN hold time during CPU access	240	270	195	225	165	195	155	185	ns
47	Write command set-up time	0	10	0	10	0	10	0	10	ns
48	Column address set-up time	30	-	20	-	15	-	10	-	ns
49	Row address hold time	50	-	40	-	35	-	35	-	ns
50	CPU address set-up time	0	-	0	-	0	-	0	-	ns
51	Request to DTACKN delay	120	265	105	230	90	210	80	200	ns
52	DTACKN to data valid (read)	-	30	-	30	-	30	-	30	ns
53	XT/2 to XT/4 delay	−5	30	−5	30	−5	30	−5	30	ns
54	RWN/IPA valid to U/LDSN low set-up time	0	-	0	-	0	-	0	-	ns
55	XT/2 low to HSYNCN	−5	20	−5	20	−5	20	−5	20	ns
56	XT/2 low to CSYNCN	0	45	0	45	0	45	0	45	ns
57	XT/2 to DTN	−20	0	−20	0	−20	0	−20	0	ns
58	XT/2 low to CSCGN	−20	0	−20	0	−20	0	−20	0	ns
59	IPA to UDSN/LDSN hold time	5	-	5	-	5	-	5	-	ns
60	RWN to UDSN/LDSN hold time for IPA accesses	5	-	5	-	5	-	5	-	ns
61a	XTAL2 high to PCLK high	12	34	12	34	12	34	12	34	ns
61b	XTAL2 high to PCLK high	8	37	8	37	8	37	8	37	ns
62a	XTAL2 high to V0-V7, WPRN, BLANKN valid	6	36	6	36	6	36	6	36	ns
62b	XTAL2 high to V0-V7, WPRN, BLANKN valid	2	39	2	39	2	39	2	39	ns

Notes.

1. The above timings are valid in FAST MODE only.
2. For timings 61a and 62a, temperature range 0 to +70 °C, C_L = 50 pF.
3. For timings 61b and 62b, temperature range −40 to +85 °C, C_L = 50 pF.

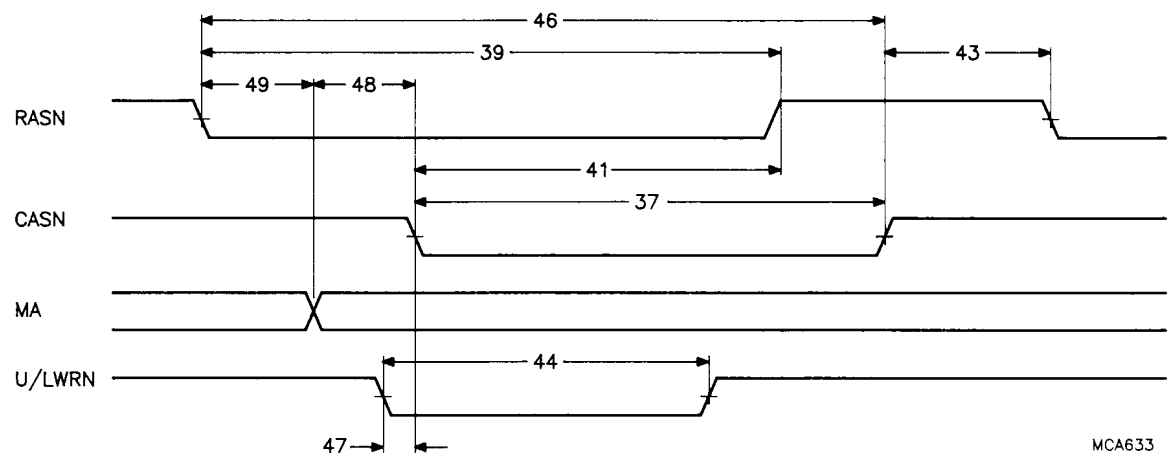


Fig.38 Signals in CPU window.

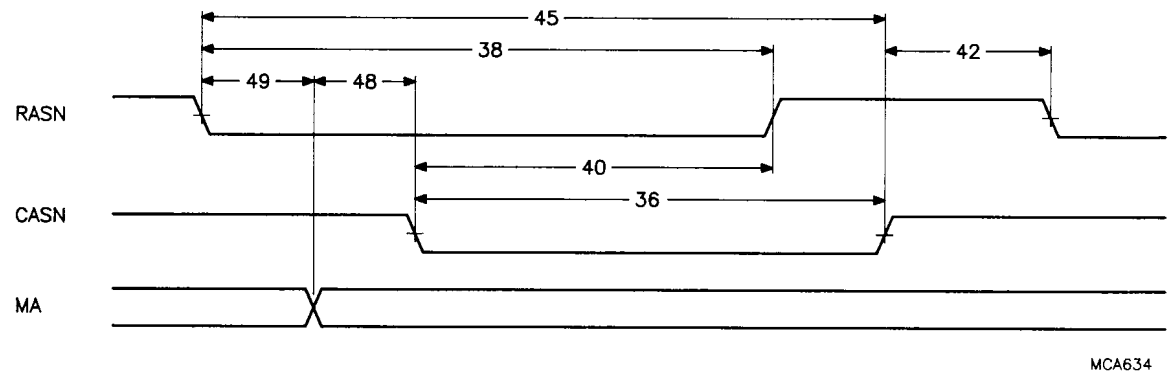


Fig.39 Signals in display window.

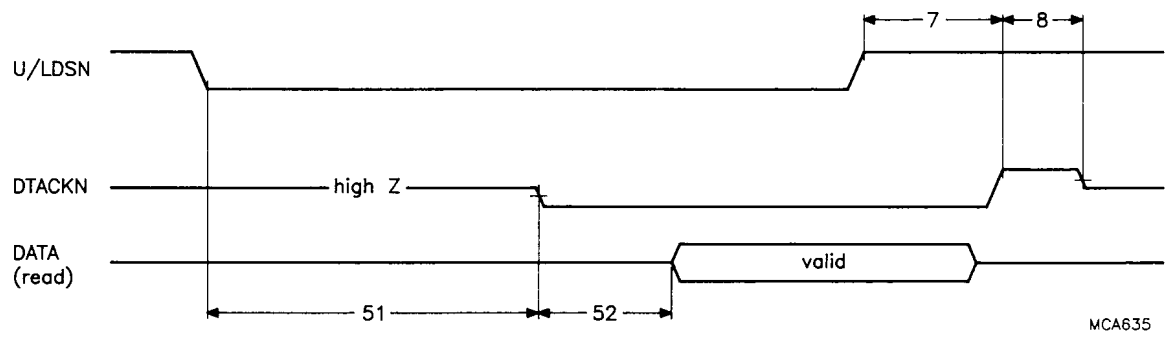


Fig.40 Internal register access.

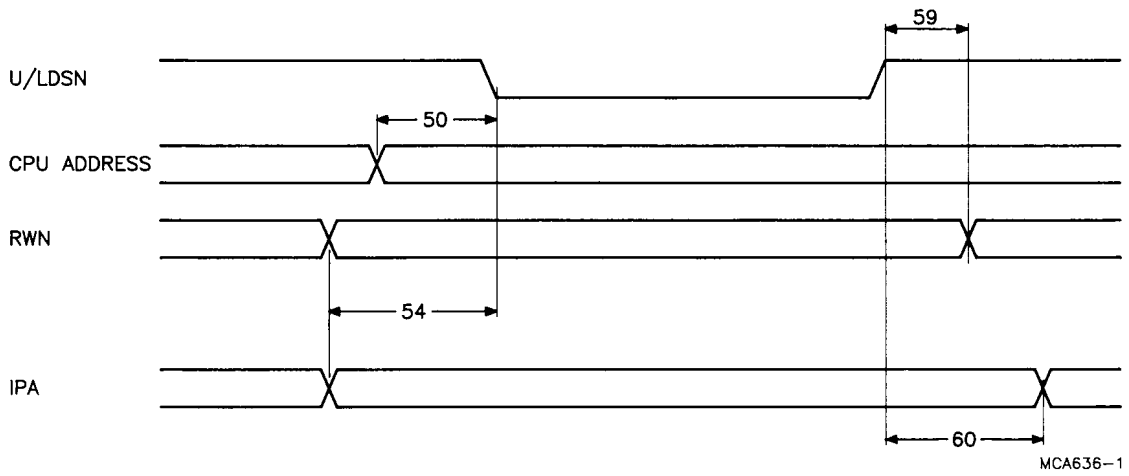


Fig.41 CPU access.

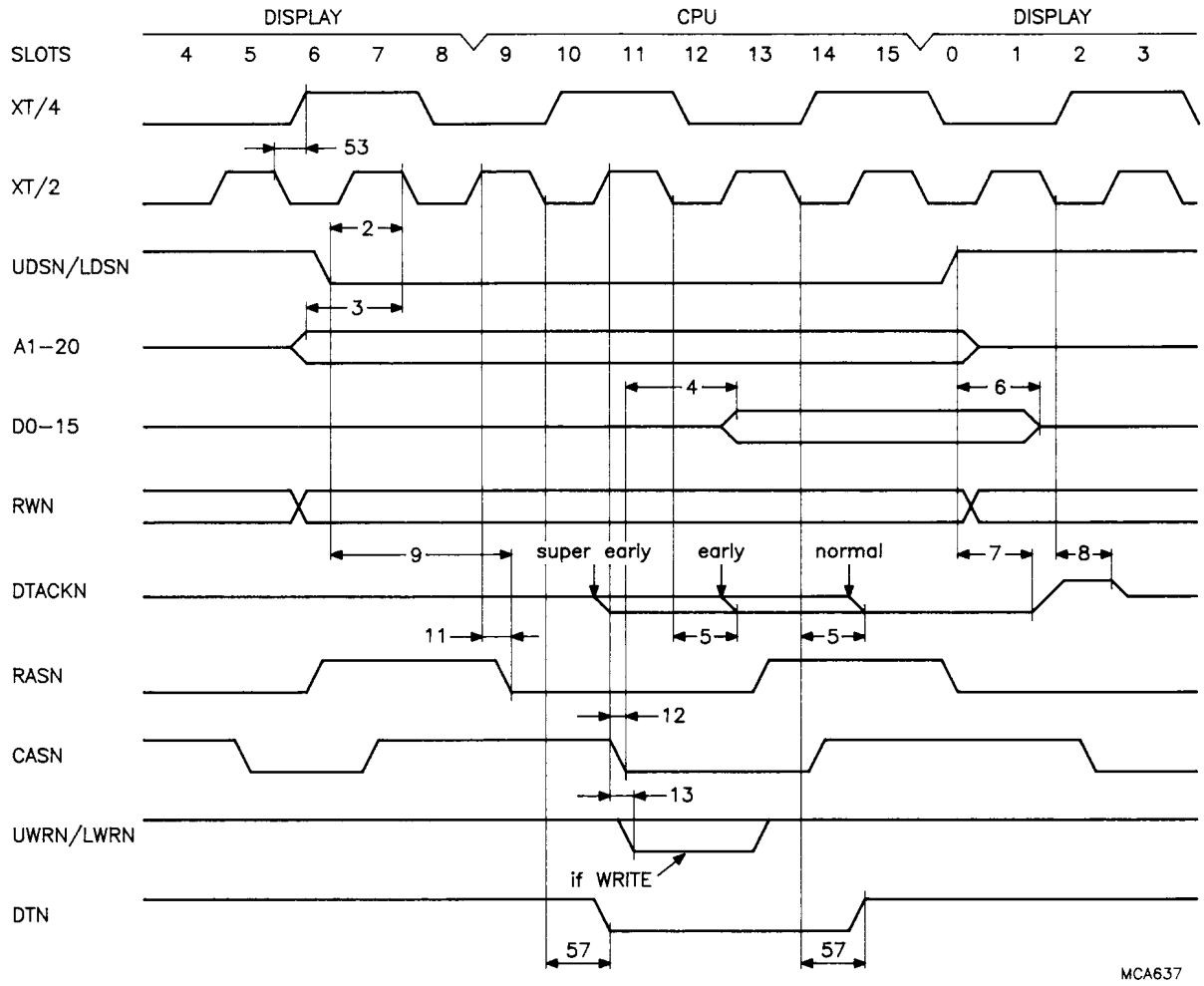
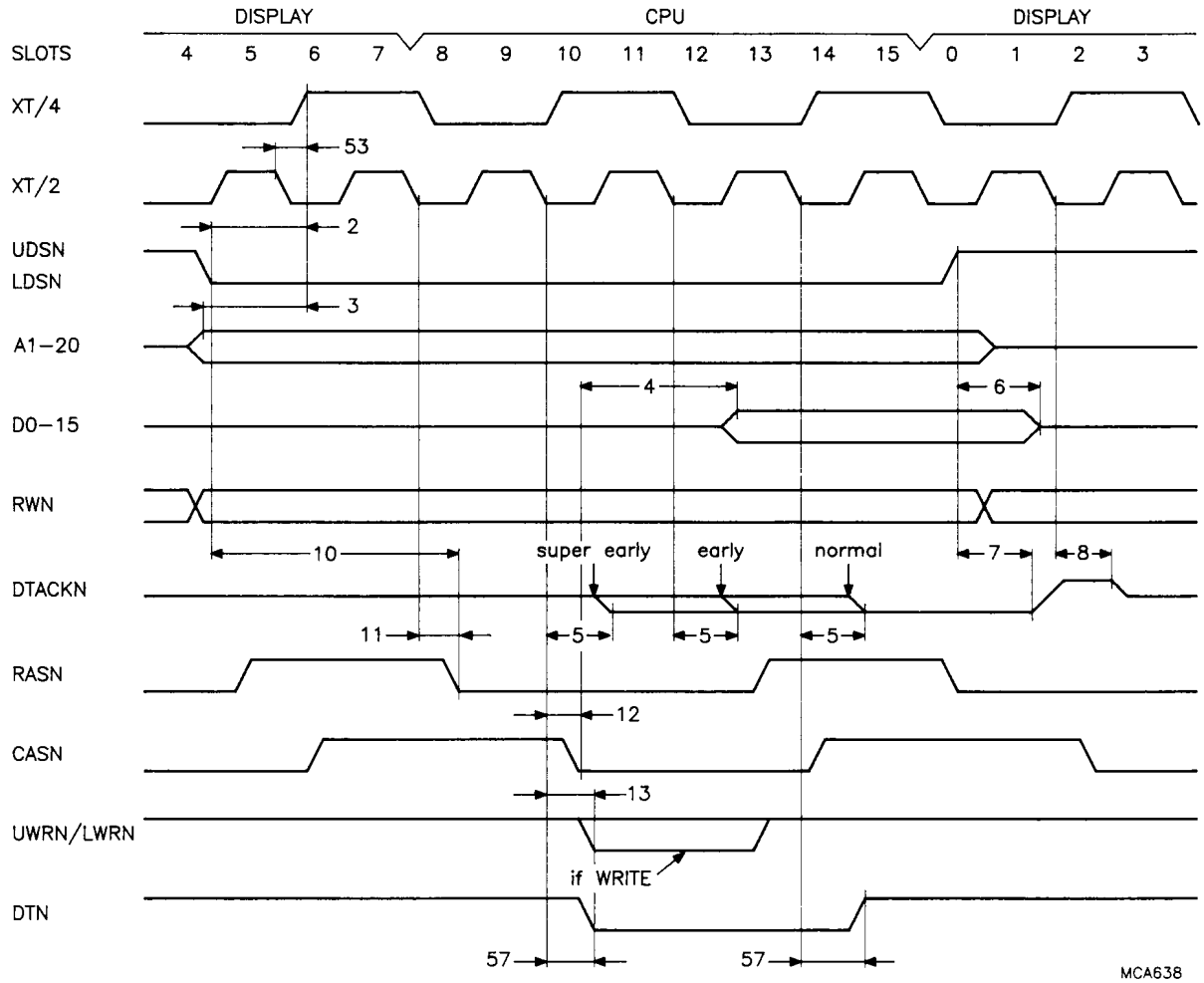


Fig.42 CPU <–> memory access in FAST mode.



Note. In DUAL PORT VRAM mode, the CPU access can be done during the display window.

Fig.43 CPU <–> memory access in SLOW mode.

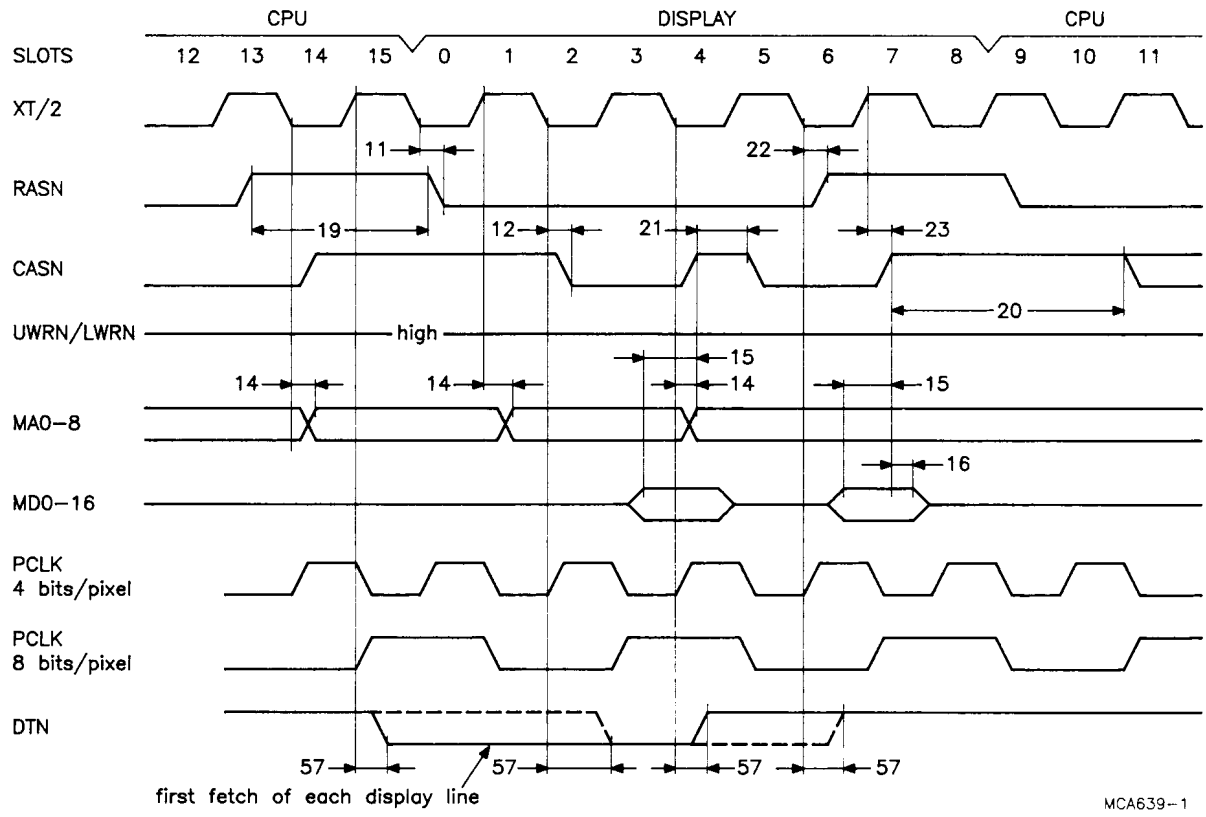


Fig.44 Display cycle in FAST mode.

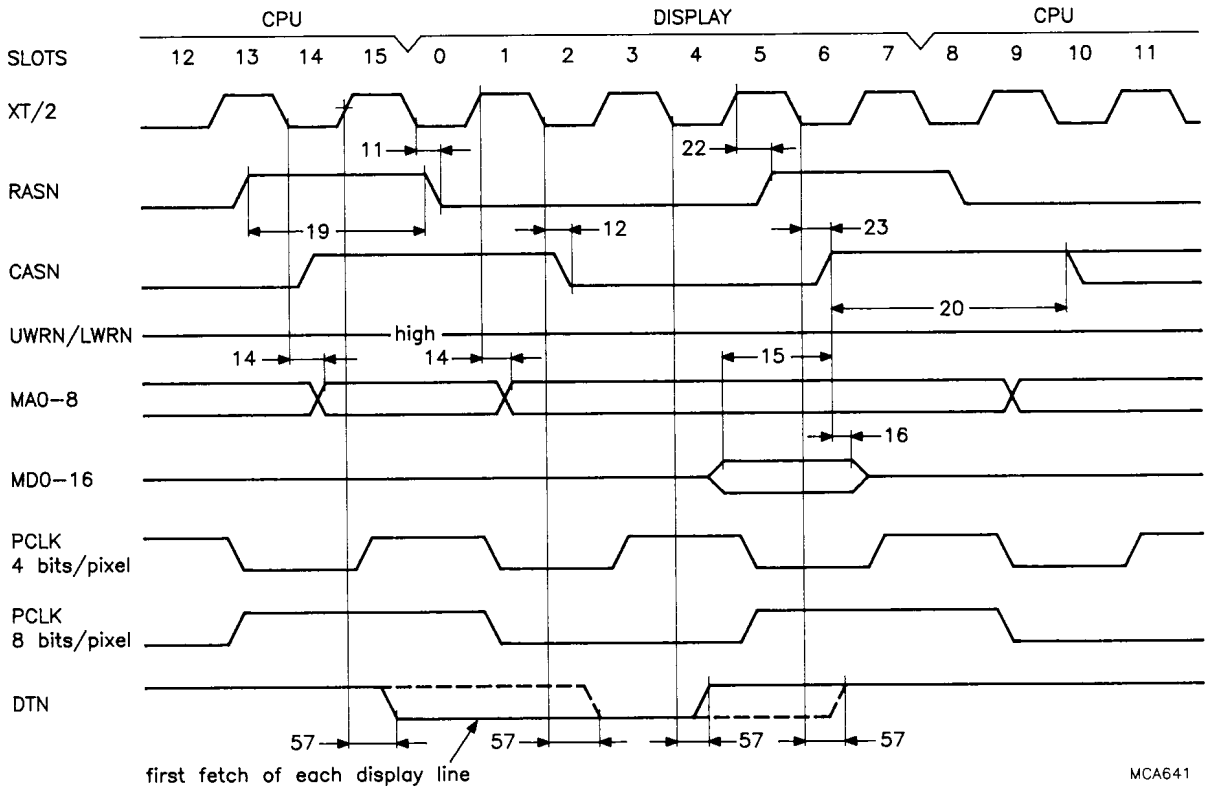


Fig.45 Display cycle in NORMAL mode.

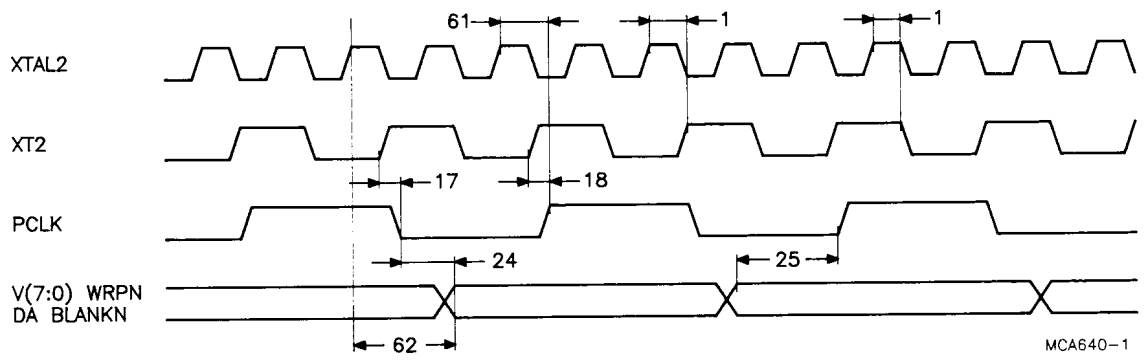


Fig.46 Pixel output timing.

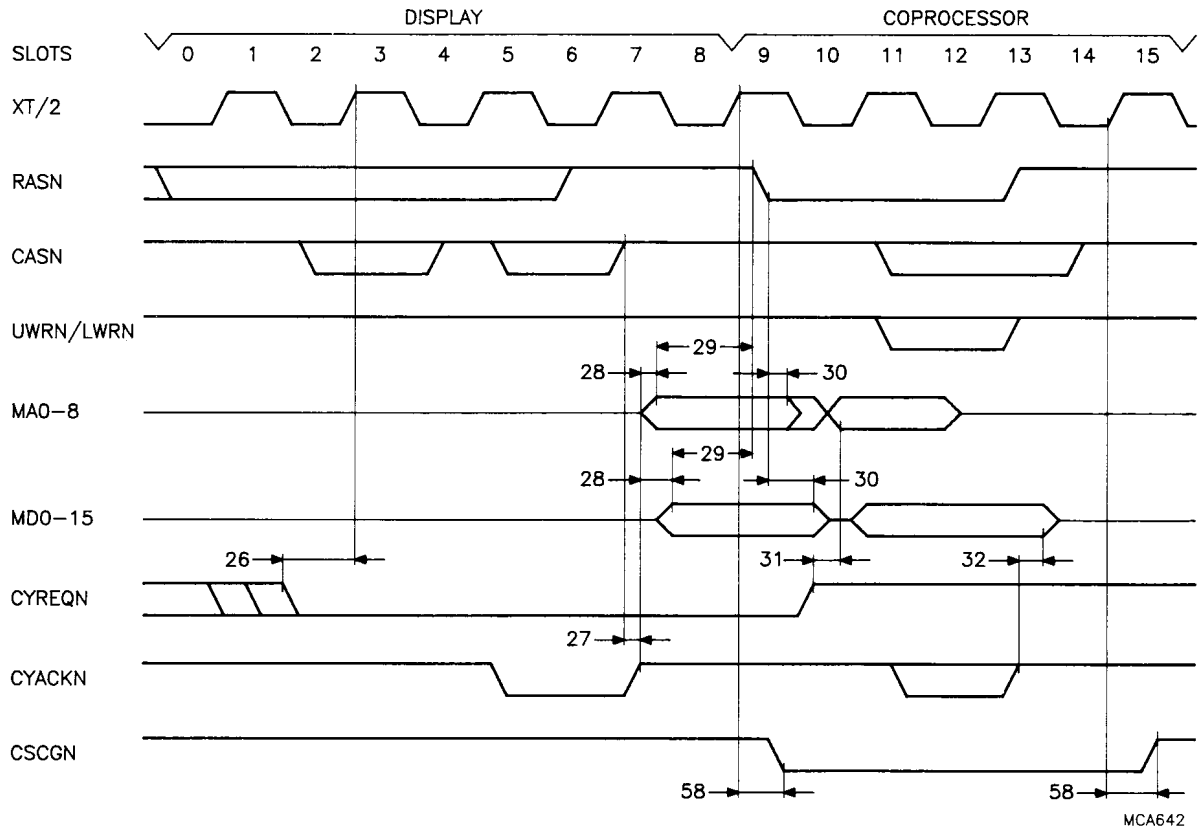


Fig.47 Coprocessor <–> memory or register access in FAST mode.

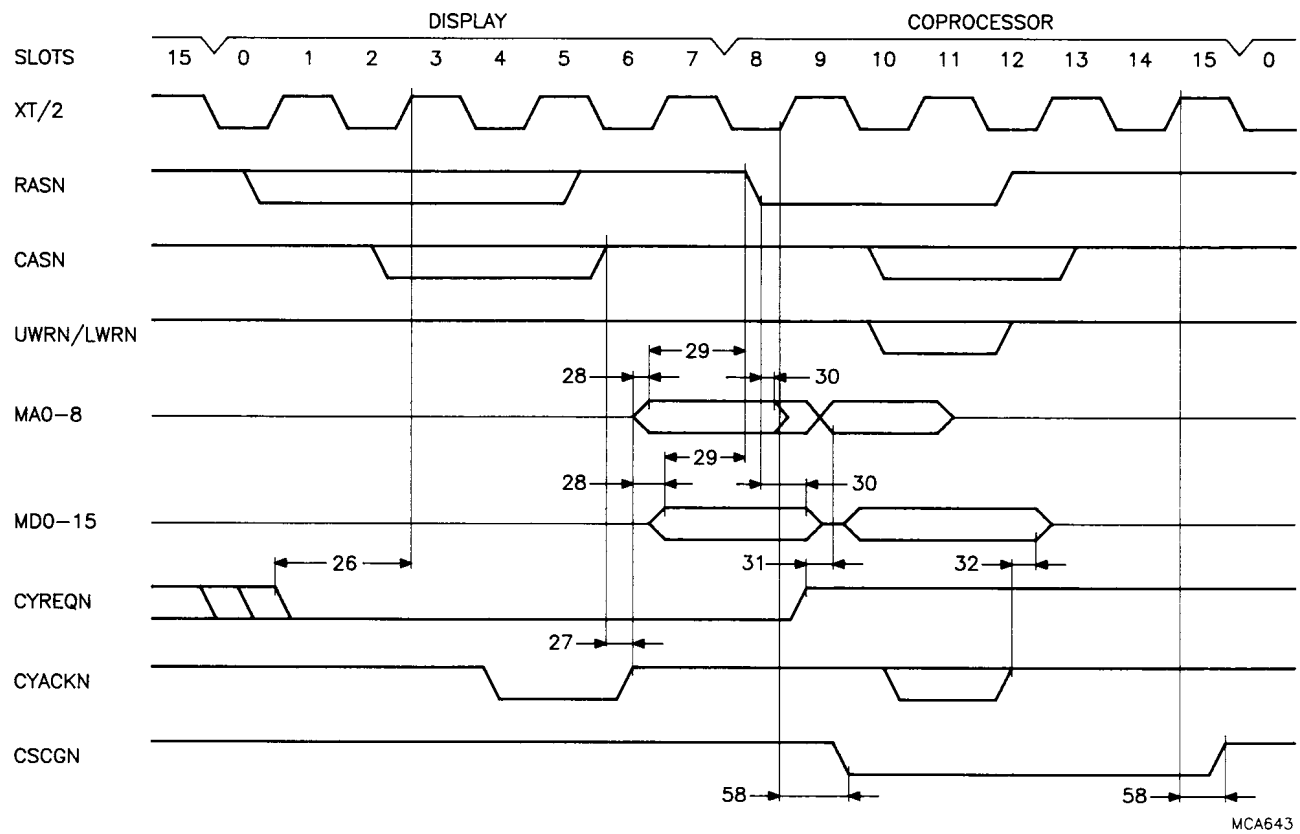


Fig.48 Coprocessor <–> memory or register access in SLOW mode.

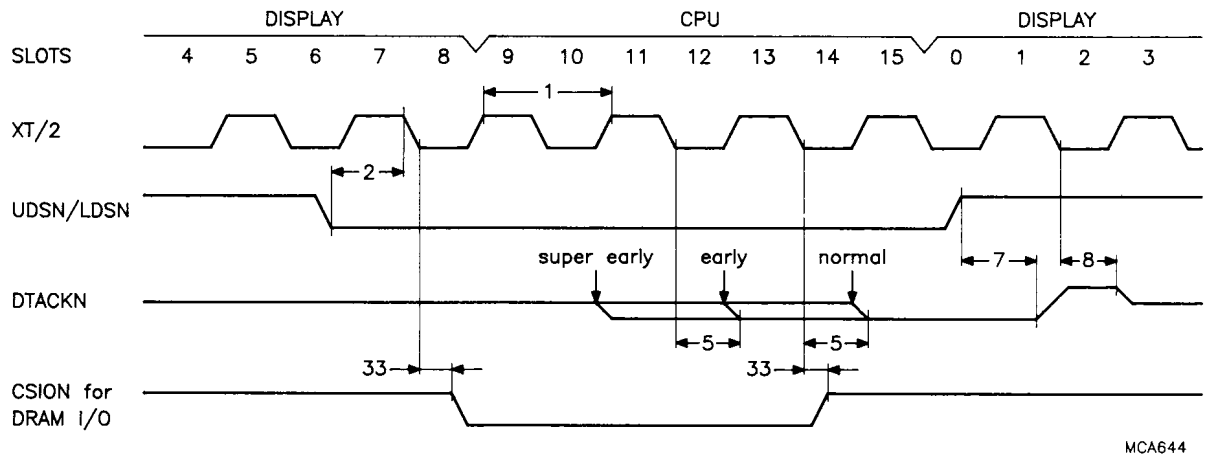


Fig.49 CSION timing in fast mode for a DRAM I/O access.

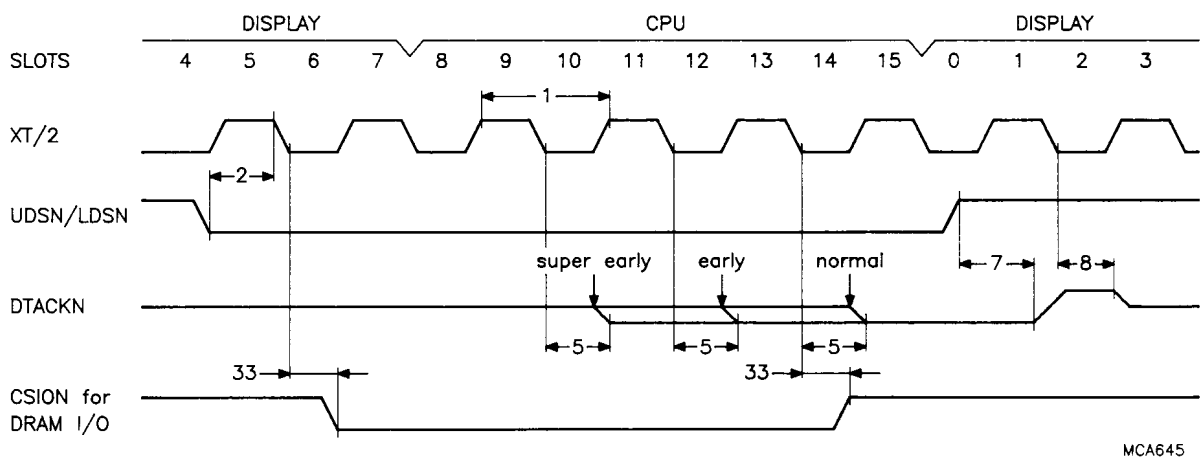


Fig.50 CSION timing in SLOW mode for a DRAM I/O access.

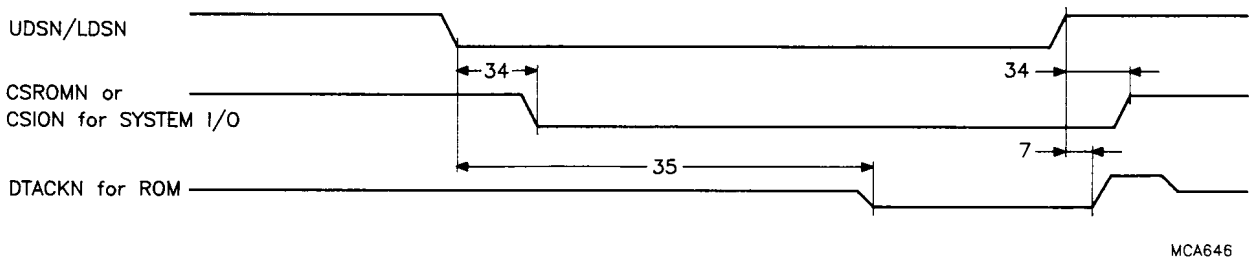


Fig.51 CSROMN and SYSTEM I/O timing.

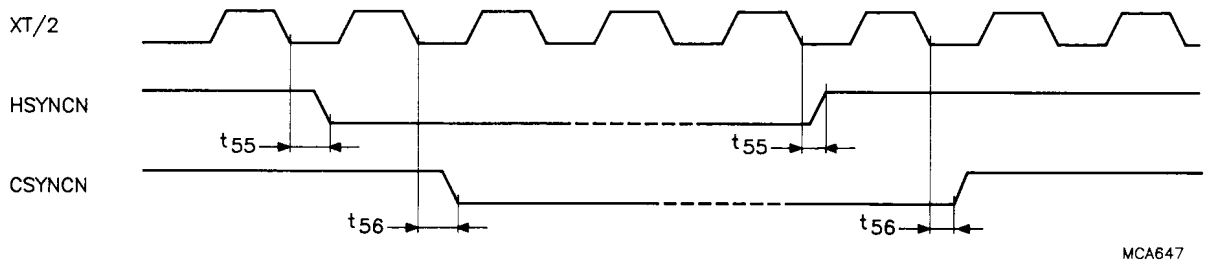
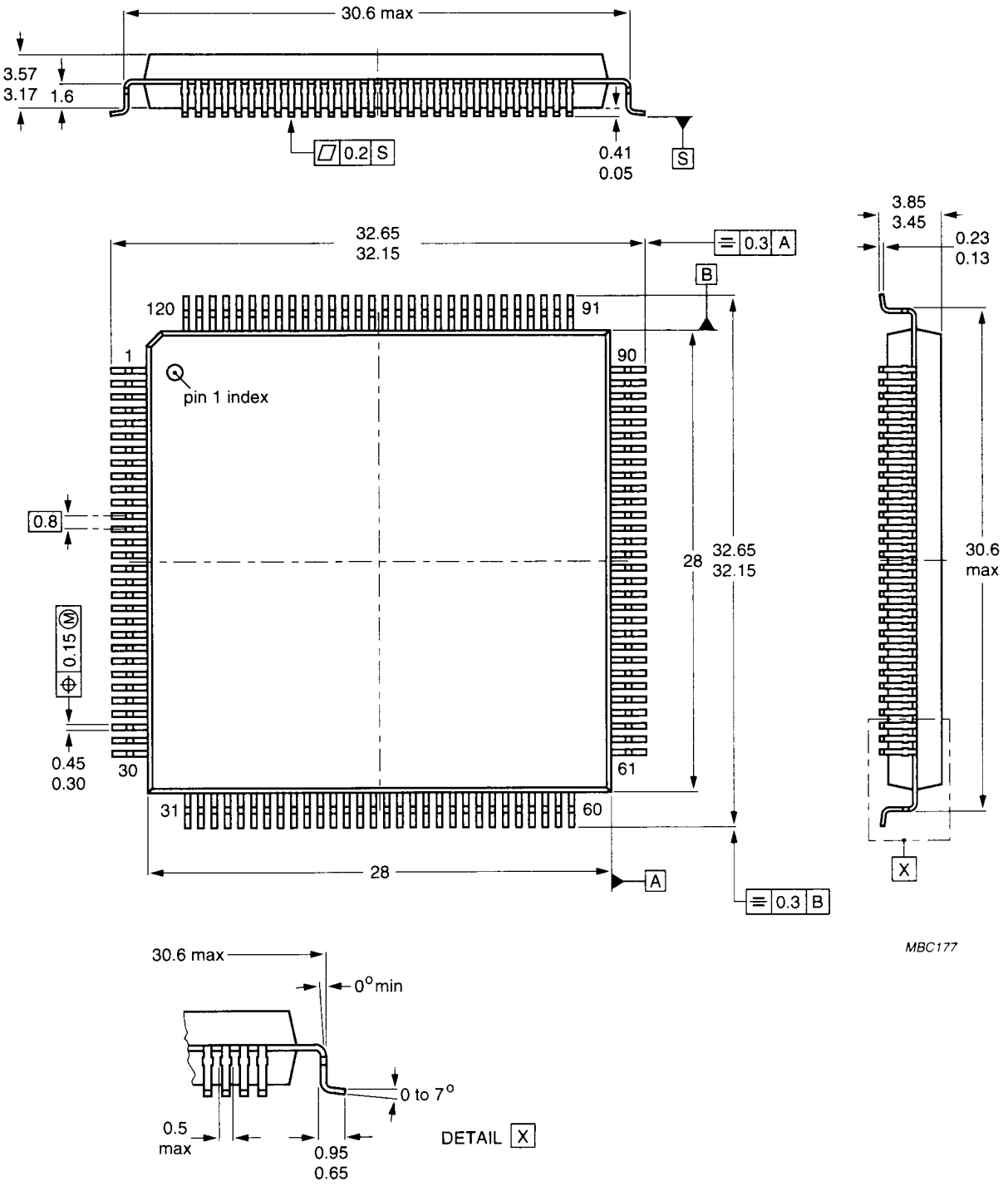


Fig.52 Synchronisation Timing.

120-LEAD QUAD FLAT-PACK; PLASTIC (SOT220B)



120-LEAD QUAD FLAT-PACK; PLASTIC (SOT220B)

SOLDERING

1. By hand-held soldering iron or pulse-heated solder tool

Fix the component by first soldering two, diagonally opposite end leads. Apply the heating tool to the flat end of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

2. By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.
Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure syringe dispensing before device placement.
Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.
Pre-heating is necessary to dry paste and to evaporate binding agent.
Pre-heating duration: 45 minutes at 45 °C.

4. Repairing soldered joints

The same precautions and limits apply as in (1) above.