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Motorola Part
Numbers Affected:
PPC7457RX1000NB
PPC7457RX867NB
PPC7457RX733NB
PPC7457RX600NB
PPC7447RX1000NB
PPC7447RX867NB
MC7447RX1000NB
MC7447RX867NB
MC7447RX733NB
MC7447RX600NB

This document describes part-number-specific changes to recommended operating conditions and revised electrical specifications, as applicable, from those described in the general *MPC7457 RISC Microprocessor Hardware Specifications* (Order No. MPC7457EC). The MPC7457 and MPC7447 are implementations of the PowerPC™ microprocessor family of reduced instruction set computer (RISC) microprocessors.

Specifications provided in this document supersede those in the *MPC7457 RISC Microprocessor Hardware Specifications*, Rev. 2 or later, for the part numbers listed in Table A only. This document is primarily concerned with the MPC7457; however, unless otherwise noted, all information herein also applies to the MPC7447 part numbers listed in Table A. Specifications not addressed herein are unchanged. Because this document is frequently updated, refer to http://www.motorola.com/semiconductors or to your Motorola sales office for the latest version.

Note that headings and table numbers in this document are not consecutively numbered. They are intended to correspond to the heading or table affected in the general hardware specification.

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Part numbers addressed in this document are listed in Table A.

Table A. Part Numbers Addressed by this Data Sheet

Motorola Part Number	Operating Conditions			Significant Differences from Hardware Specification
	CPU Frequency (MHz)	V_{DD}	T_j (°C)	
PPC7457RX1000NB	1000	1.1 V ± 50 mV	0 to 105	Modified core frequency and voltage to reduce power consumption, modified processor bus AC timing.
PPC7447RX1000NB				
MC7447RX1000NB				
PPC7457RX867NB	867			
PPC7447RX867NB				
MC7447RX867NB				
PPC7457RX733NB	733			
MC7447RX733NB				
PPC7457RX600NB	600			
MC7447RX600NB				

Note: The P prefix in a Motorola part number designates a "Pilot Production Prototype" as defined by Motorola SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

1.2 Features

This section summarizes changes to the features of the MPC7457 described in the *MPC7457 RISC Microprocessor Hardware Specifications*.

- Power management
  — 1.1-V processor core

1.3 General Parameters

- Core power supply: 1.1 V ± 50 mV DC nominal

1.5.1 DC Electrical Characteristics

Table 4 provides the recommended operating conditions for the MPC7457 part numbers described herein.

Table 4. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit
Core supply voltage	V_{DD}	1.1 V ± 50 mV	V
PLL supply voltage	AV_{DD}	1.1 V ± 50 mV	V

Note: These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

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Table 7 provides the power consumption for the MPC7457 part numbers described herein.

Table 7. Power Consumption for MPC7457

	Processor (CPU) Frequency				Unit	Notes
	600 MHz	**733 MHz**	**867 MHz**	**1000 MHz**		
Full-Power Mode						
Typical	5.3	6.3	7.3	8.3	W	1, 3
Maximum	7.9	9.1	10.3	11.5	W	1, 2
Doze Mode						
Typical	—	—	—	—	W	4
Nap Mode						
Typical	1.3	1.3	1.3	1.3	W	1, 2
Sleep Mode						
Typical	1.2	1.2	1.2	1.2	W	1, 2
Deep Sleep Mode (PLL Disabled)						
Typical	1.1	1.1	1.1	1.1	W	1, 3

Notes:
1. These values apply for all valid processor bus and L3 bus ratios. The values do not include I/O supply power (OV_{DD} and GV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} and GV_{DD} power is system dependent, but is typically <5% of V_{DD} power. Worst case power consumption for AV_{DD} < 3 mW.
2. Maximum power is the maximum measured at nominal V_{DD} and maximum operating junction temperature (see Table 4) while running an entirely cache-resident, contrived sequence of instructions which keep all the execution units maximally busy.
3. Typical power is an average value measured at the nominal recommended V_{DD} (see Table 4) and 65°C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz.
4. Doze mode is not a user-definable state; it is an intermediate state between full-power and either nap or sleep mode. As a result, power consumption for this mode is not tested.

Table 8 provides the clock AC timing specifications for the MPC7457 part numbers described herein.

Table 8. Clock AC Timing Specifications

At recommended operating conditions. See Table 4.

Characteristic	Symbol	Maximum Processor Core Frequency								Unit	Notes
		600 MHz		733 MHz		867 MHz		1000 MHz			
		Min	Max	Min	Max	Min	Max	Min	Max		
Processor frequency	f_{core}	500	600	500	733	500	867	500	1000	MHz	1
VCO frequency	f_{VCO}	1000	1200	1000	1466	1000	1733	1000	2000	MHz	1
SYSCLK frequency	f_{SYSCLK}	33	167	33	167	33	167	33	167	MHz	
SYSCLK cycle time	t_{SYSCLK}	6.0	30	6.0	30	6.0	30	6.0	30	ns	

Note:

1. **Caution**: The SYSCLK frequency, PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in Section 1.9.1, "PLL Configuration," for valid PLL_CFG[0:4] settings.

1.5.2.2 Processor Bus AC Specifications

Table 9 provides the processor bus AC timing specifications for the MPC7457 part numbers described herein.

Table 9. Processor Bus AC Timing Specifications [1]

At recommended operating conditions. See Table 4.

Parameter	Symbol [2]	All Speed Grades		Unit	Notes
		Min	Max		
Input setup times: A[0:35], AP[0:4] D[0:63], DP[0:7] $\overline{\text{AACK}}$, $\overline{\text{ARTRY}}$, $\overline{\text{BG}}$, $\overline{\text{CKSTP\_IN}}$, $\overline{\text{DBG}}$, DTI[0:3], $\overline{\text{GBL}}$, $\overline{\text{HIT}}$, TT[0:3], $\overline{\text{QACK}}$, $\overline{\text{TA}}$, TBEN, $\overline{\text{TEA}}$, $\overline{\text{TS}}$, EXT_QUAL, $\overline{\text{PMON\_IN}}$, $\overline{\text{SHD}}$[0:1], BMODE[0:1], $\overline{\text{BMODE}}$[0:1], BVSEL, L3VSEL	t_{AVKH} t_{DVKH} t_{IVKH} t_{MVKH}	2.0 2.0 2.0 2.0	— — — —	ns	 8
Input hold times: A[0:35], AP[0:4] D[0:63], DP[0:7] $\overline{\text{AACK}}$, $\overline{\text{ARTRY}}$, $\overline{\text{BG}}$, $\overline{\text{CKSTP\_IN}}$, $\overline{\text{DBG}}$, DTI[0:3], $\overline{\text{GBL}}$, $\overline{\text{HIT}}$, TT[0:3], $\overline{\text{QACK}}$, $\overline{\text{TA}}$, TBEN, $\overline{\text{TEA}}$, $\overline{\text{TS}}$, EXT_QUAL, $\overline{\text{PMON\_IN}}$, $\overline{\text{SHD}}$[0:1] $\overline{\text{BMODE}}$[0:1], BVSEL, L3VSEL	t_{AXKH} t_{DXKH} t_{IXKH} t_{MXKH}	0 0 0 0	— — — —	ns	 8
Output valid times: A[0:35], AP[0:4] D[0:63], DP[0:7] $\overline{\text{AACK}}$, $\overline{\text{ARTRY}}$, $\overline{\text{BR}}$, $\overline{\text{CI}}$, $\overline{\text{CKSTP\_IN}}$, $\overline{\text{DRDY}}$, DTI[0:3], $\overline{\text{GBL}}$, $\overline{\text{PMON\_OUT}}$, $\overline{\text{QREQ}}$, $\overline{\text{TBST}}$, TSIZ[0:2], TT[0:3], $\overline{\text{TS}}$, $\overline{\text{SHD}}$[0:1], $\overline{\text{WT}}$	t_{KHAV} t_{KHDV} t_{KHOV}	— — —	2.0 2.0 2.0	ns	
Output hold times: A[0:35], AP[0:4] D[0:63], DP[0:7] $\overline{\text{AACK}}$, $\overline{\text{ARTRY}}$, $\overline{\text{BR}}$, $\overline{\text{CI}}$, $\overline{\text{CKSTP\_IN}}$, $\overline{\text{DRDY}}$, DTI[0:3], $\overline{\text{GBL}}$, $\overline{\text{PMON\_OUT}}$, $\overline{\text{QREQ}}$, $\overline{\text{TBST}}$, TSIZ[0:2], TT[0:3], $\overline{\text{TS}}$, $\overline{\text{SHD}}$[0:1], $\overline{\text{WT}}$	t_{KHAX} t_{KHDX} t_{KHOX}	0.5 0.5 0.5	— — —	ns	
SYSCLK to output enable	t_{KHOE}	0.5	—	ns	
SYSCLK to output high impedance (all except $\overline{\text{TS}}$, $\overline{\text{ARTRY}}$, $\overline{\text{SHD0}}$, $\overline{\text{SHD1}}$)	t_{KHOZ}	—	3.5	ns	
SYSCLK to $\overline{\text{TS}}$ high impedance after precharge	t_{KHTSPZ}	—	1	t_{SYSCLK}	3, 4, 5
Maximum delay to $\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$ precharge	t_{KHARP}	—	1	t_{SYSCLK}	3, 5, 6, 7

Table 9. Processor Bus AC Timing Specifications [1] (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol [2]	All Speed Grades		Unit	Notes
		Min	Max		
SYSCLK to $\overline{ARTRY}/\overline{SHD0}/\overline{SHD1}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{SYSCLK}	3, 5 6, 7

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4 in the *MPC7457 RISC Microprocessor Hardware Specifications)*. Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2. The symbology used for timing specifications herein follows the pattern of $t_{(signal)(state)(reference)(state)}$ for inputs and $t_{(reference)(state)(signal)(state)}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).

3. t_{SYSCLK} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.

4. According to the bus protocol, $\overline{TS}$ is driven only by the currently active bus master. It is asserted low then precharged high before returning to high impedance, as shown in Figure 6 in the *MPC7457 RISC Microprocessor Hardware Specifications*. The nominal precharge width for $\overline{TS}$ is $0.5 \times t_{SYSCLK}$, that is, less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{TS}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-impedance behavior is guaranteed by design.

5. Guaranteed by design and not tested.

6. According to the bus protocol, $\overline{ARTRY}$ can be driven by multiple bus masters through the clock period immediately following $\overline{AACK}$. Bus contention is not an issue because any master asserting $\overline{ARTRY}$ will be driving it low. Any master asserting it low in the first clock following $\overline{AACK}$ will then go to high impedance for one clock before precharging it high during the second cycle after the assertion of $\overline{AACK}$. The nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{SYSCLK}; that is, it should be high impedance, as shown in Figure 6 in the *MPC7457 RISC Microprocessor Hardware Specifications,* before the first opportunity for another master to assert $\overline{ARTRY}$. Output valid and output hold timing is tested for the signal asserted. The high-impedance behavior is guaranteed by design.

7. According to the MPX bus protocol, $\overline{SHD0}$ and $\overline{SHD1}$ can be driven by multiple bus masters beginning the cycle of $\overline{TS}$. Timing is the same as $\overline{ARTRY}$, that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{SHD0}$ and $\overline{SHD1}$ is 1.0 t_{SYSCLK}. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).

8. $\overline{BMODE}$[0:1] and BVSEL are mode select inputs and are sampled before and after $\overline{HRESET}$ negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. These inputs must remain stable after the second sample. See Figure 5 in the *MPC7457 RISC Microprocessor Hardware Specifications* for sample timing.

1.5.2.3 L3 Clock AC Specifications

Devices described by this part number specification conform to the L3 clock AC timing specifications provided in the *MPC7457 RISC Microprocessor Hardware Specifications*. Refer to the hardware specifications for additional information.

1.5.2.4 L3 Bus AC Specifications

Devices described by this part number specification conform to the L3 clock AC timing specifications provided in the *MPC7457 RISC Microprocessor Hardware Specifications*. Refer to the hardware specifications for additional information.

1.11 Ordering Information

1.11.1 Part Numbers Addressed by This Specification

Table 22 provides the ordering information for the MPC7457 parts described in this document.

Table 22. Part Marking Nomenclature

xxx	*74x7*	RX	*nnnn*	*x*	*x*
Product Code	**Part Identifier**	**Package**	**Processor Frequency** [1]	**Application Modifier**	**Revision Level**
PPC [2]	7457	RX = CBGA	1000	N: 1.1 V ± 50 mV 0° to 105°C	B: 1.1: PVR = 8002 0101
			867		
			733		
			600		
	7447		1000		
			867		
MC	7447		1000		
			867		
			733		
			600		

Notes:

1. Processor core frequencies supported by parts addressed by this specification only. Parts addressed by other specifications may support other maximum core frequencies.

2. The P prefix in a Motorola part number designates a "Pilot Production Prototype" as defined by Motorola SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

1.11.3 Part Marking

Parts are marked as the example shown in Figure 29.
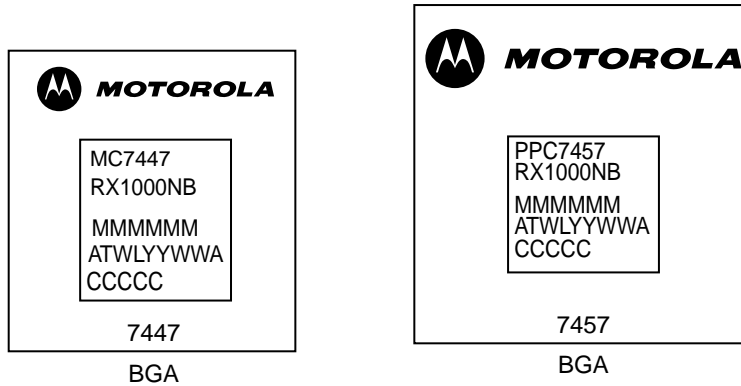
Notes:
    MMMMMM is the 6-digit mask number.
    ATWLYYWWA is the traceability code.
    CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 29. Motorola Part Marking for BGA Devices

Document Revision History

Table B provides a revision history for this part number specification.

Table B. Document Revision History

Rev. No.	Substantive Change(s)
0	Initial release.
0.1	Edited introductory paragraphs to clarify which part numbers are affected by this specification.
1	Corrected product code in part numbers on page 1 and in Table A.
	Updated power consumption specifications in Table 7.
	Corrected product code in Section 1.11 and Table 21.
2	Added "MC7447..." part numbers to reflect qualification status.
	Table 8: Increased maximum system bus frequency (f_{SYSCLK}) to 167 MHz.
	Table 9: Corrected numerous errors in lists of pins associated with t_{KHOV}, t_{KHOX}, t_{IVKH}, and t_{IXKH}. Updated (improved) AC timing parameters based on latest characterization data.
	Added 867, 733, and 600 MHz speed grades.
	Removed Tables 10, 13, and 14: devices described by this specification conform to the AC timing found in the MPC7457 hardware specifications.
	Corrected typo in Figure 29: 7447 device was incorrectly marked...RX10000NB.

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