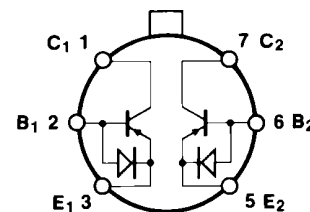


**FEATURES**

Dual Matched PNP Transistor  
Low Offset Voltage: 100  $\mu\text{V}$  max  
Low Noise: 1  $\text{nV}/\sqrt{\text{Hz}}$  @ 1 kHz max  
High Gain: 100 min  
High Gain Bandwidth: 190 MHz typ  
Tight Gain Matching: 3% max  
Excellent Logarithmic Conformance:  $r_{\text{BE}} \approx 0.3 \Omega$  typ  
Available in Die Form

**PIN CONNECTION**

**TO-78  
(H Suffix)**

**GENERAL DESCRIPTION**

The MAT03 dual monolithic PNP transistor offers excellent parametric matching and high frequency performance. Low noise characteristics (1  $\text{nV}/\sqrt{\text{Hz}}$  max @ 1 kHz), high bandwidth (190 MHz typical), and low offset voltage (100  $\mu\text{V}$  max), makes the MAT03 an excellent choice for demanding preamplifier applications. Tight current gain matching (3% max mismatch) and high current gain (100 min), over a wide range of collector current, makes the MAT03 an excellent choice for current mirrors. A low value of bulk resistance (typically 0.3  $\Omega$ ) also makes the MAT03 an ideal component for applications requiring accurate logarithmic conformance.

Each transistor is individually tested to data sheet specifications. Device performance is guaranteed at 25°C and over the extended industrial and military temperature ranges. To insure the long-term stability of the matching parameters, internal protection diodes across the base-emitter junction clamp any reverse base-emitter junction potential. This prevents a base-emitter breakdown condition which can result in degradation of gain and matching performance due to excessive breakdown current.

**REV. B**

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# MAT03-SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ T<sub>A</sub> = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	MAT03A			MAT03E			MAT03F			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Current Gain <sup>1</sup>	$h_{FE}$	$V_{CB} = 0\text{ V}, -36\text{ V}$ $I_C = 1\text{ mA}$ $I_C = 100\text{ }\mu\text{A}$ $I_C = 10\text{ }\mu\text{A}$	100	165		100	165		80	165		
Current Gain Matching <sup>2</sup>	$\Delta h_{FE}$	$I_C = 100\text{ }\mu\text{A}, V_{CB} = 0\text{ V}$		0.5	3		0.5	3		0.5	6	%
Offset Voltage <sup>3</sup>	$V_{OS}$	$V_{CB} = 0\text{ V}, I_C = 100\text{ }\mu\text{A}$		40	100		40	100		40	200	$\mu\text{V}$
Offset Voltage Change vs. Collector Voltage	$DV_{OS}/DV_{CB}$	$I_C = 100\text{ }\mu\text{A}$ $V_{CB1} = 0\text{ V}$ $V_{CB2} = -36\text{ V}$		11	150		11	150		11	200	$\mu\text{V}$
Offset Voltage Change vs. Collector Current	$DV_{OS}/DI_C$	$V_{CB} = 0\text{ V}$ $I_{C1} = 10\text{ }\mu\text{A}, I_{C2} = 1\text{ mA}$		12	50		12	50		12	75	$\mu\text{V}$
Bulk Resistance	$r_{BE}$	$V_{CB} = 0\text{ V}$ $10\text{ }\mu\text{A} \leq I_C \leq 1\text{ mA}$		0.3	0.75		0.3	0.75		0.3	0.75	$\Omega$
Offset Current Collector-Base Leakage Current	$I_{OS}$	$I_C = 100\text{ }\mu\text{A}, V_{CB} = 0\text{ V}$		6	35		6	35		6	45	nA
Noise Voltage Density <sup>4</sup>	$I_{CBO}$ $e_N$	$V_{CB} = -36\text{ V} = V_{MAX}$ $I_C = 1\text{ mA}, V_{CB} = 0$ $f_0 = 10\text{ Hz}$ $f_0 = 100\text{ Hz}$ $f_0 = 1\text{ kHz}$ $f_0 = 10\text{ kHz}$		50	200		50	200		50	400	pA
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_C = 1\text{ mA}, I_B = 100\text{ }\mu\text{A}$		0.025	0.1		0.025	0.1		0.025	0.1	V

## ELECTRICAL CHARACTERISTICS (at -55°C ≤ T<sub>A</sub> ≤ +125°C, unless otherwise noted.)

Parameter	Symbol	Conditions	MAT03A			Units	
			Min	Typ	Max		
Current Gain	$h_{FE}$	$V_{CB} = 0\text{ V}, -36\text{ V}$ $I_C = 1\text{ mA}$ $I_C = 100\text{ }\mu\text{A}$ $I_C = 10\text{ }\mu\text{A}$		70	110		
Offset Voltage	$V_{OS}$	$I_C = 100\text{ }\mu\text{A}, V_{CB} = 0\text{ V}$			40	150	$\mu\text{V}$
Offset Voltage Drift <sup>5</sup>	$TCV_{OS}$	$I_C = 100\text{ }\mu\text{A}, V_{CB} = 0\text{ V}$			0.3	0.5	$\mu\text{V}/^\circ\text{C}$
Offset Current	$I_{OS}$	$I_C = 100\text{ }\mu\text{A}, V_{CB} = 0\text{ V}$			15	85	nA
Breakdown Voltage	$BV_{CEO}$			36	54		V

## ELECTRICAL CHARACTERISTICS (at -40°C ≤ T<sub>A</sub> ≤ +85°C, unless otherwise noted.)

Parameter	Symbol	Conditions	MAT03E			MAT03F			Units	
			Min	Typ	Max	Min	Typ	Max		
Current Gain	$h_{FE}$	$V_{CB} = 0\text{ V}, -36\text{ V}$ $I_C = 1\text{ mA}$ $I_C = 100\text{ }\mu\text{A}$ $I_C = 10\text{ }\mu\text{A}$		70	120		60	120		
Offset Voltage	$V_{OS}$	$I_C = 100\text{ }\mu\text{A}, V_{CB} = 0\text{ V}$			30	135		30	265	$\mu\text{V}$
Offset Voltage Drift <sup>5</sup>	$TCV_{OS}$	$I_C = 100\text{ }\mu\text{A}, V_{CB} = 0\text{ V}$			0.3	0.5		0.3	1.0	$\mu\text{V}/^\circ\text{C}$
Offset Current	$I_{OS}$	$I_C = 100\text{ }\mu\text{A}, V_{CB} = 0\text{ V}$			10	85		10	200	nA
Breakdown Voltage	$BV_{CEO}$			36				36		V

### NOTES

<sup>1</sup>Current gain is measured at collector-base voltages ( $V_{CB}$ ) swept from 0 to  $V_{MAX}$  at indicated collector current. Typical values are measured at  $V_{CB} = 0\text{ V}$ .

<sup>2</sup>Current gain matching ( $\Delta h_{FE}$ ) is defined as:  $\Delta h_{FE} = \frac{100 (\Delta I_B) h_{FE}(\text{min})}{I_C}$

<sup>3</sup>Offset voltage is defined as:  $V_{OS} = V_{BE1} - V_{BE2}$ , where  $V_{OS}$  is the differential voltage for  $I_{C1} = I_{C2}$ :  $V_{OS} = V_{BE1} - V_{BE2} = \frac{KT}{q} \ln \left( \frac{I_{C1}}{I_{C2}} \right)$ .

<sup>4</sup>Sample tested. Noise tested and specified as equivalent input voltage for each transistor.

<sup>5</sup>Guaranteed by  $V_{OS}$  test ( $TCV_{OS} = V_{OS}/T$  for  $V_{OS} \ll V_{BE}$ ) where  $T = 298\text{ K}$  for  $T_A = 25^\circ\text{C}$ . Specifications subject to change without notice.

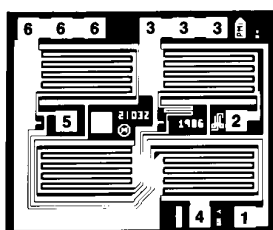
**WAFER TEST LIMITS** (at 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	MAT03N Limits	Units
Breakdown Voltage	$BV_{CEO}$		36	V min
Offset Voltage	$V_{OS}$	$I_C = 100 \mu A, V_{CB} = 0 V$	200	$\mu V$ max
		$10 \mu A \leq I_C \leq 1 mA$	200	$\mu V$ max
Current Gain	$h_{FE}$	$I_C = 1 mA, V_{CB} = 0 V, -36 V$	80	min
		$I_C = 10 \mu A, V_{CB} = 0 V, -36 V$	60	min
Current Gain Match	$\Delta h_{FE}$	$I_C = 100 \mu A, V_{CB} = 0 V$	6	% max
Offset Voltage Change vs. $V_{CB}$	$\Delta V_{OS}/\Delta V_{CB}$	$V_{CB1} = 0 V, I_C = 100 \mu A$	200	$\mu V$ max
		$V_{CB2} = -36 V$	200	$\mu V$ max
Offset Voltage Change vs. Collector Current	$\Delta V_{OS}/\Delta I_C$	$V_{CB} = 0$	75	$\mu V$ max
		$I_{C1} = 10 \mu A, I_{C2} = 1 mA$	75	$\mu V$ max
Bulk Resistance	$r_{BE}$	$10 \mu A \leq I_C \leq 1 mA$	0.75	$\Omega$ max
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_C = 1 mA, I_B = 100 \mu A$	0.1	V max

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

**DICE CHARACTERISTICS**



- 1. COLLECTOR (1)
- 2. BASE (1)
- 3. EMITTER (1)
- 4. COLLECTOR (2)
- 5. BASE (2)
- 6. EMITTER (2)

SUBSTRATE CAN BE CONNECTED TO V- OR FLOATED

DIE SIZE 0.070 × 0.060 inch, 4,200 sq. mils  
(1.78 × 1.52 mm, 2.70 sq. mm)

**ORDERING GUIDE<sup>1</sup>**

Model	$V_{OS}$ max ( $T_A = +25^\circ C$ )	Temperature Range	Package Option
MAT03AH <sup>2</sup>	100 $\mu V$	-55°C to +125°C	TO-78
MAT03EH	100 $\mu V$	-40°C to +85°C	TO-78
MAT03FH	200 $\mu V$	-40°C to +85°C	TO-78

NOTES

<sup>1</sup>Burn-in is available on industrial temperature range parts.

<sup>2</sup>For devices processed in total compliance to MIL-STD-883, add/883 after part number. Consult factory for 883 data sheet.

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

Collector-Base Voltage ( $BV_{CBO}$ )	36 V
Collector-Emitter Voltage ( $BV_{CEO}$ )	36 V
Collector-Collector Voltage ( $BV_{CC}$ )	36 V
Emitter-Emitter Voltage ( $BV_{EE}$ )	36 V
Collector Current ( $I_C$ )	20 mA
Emitter Current ( $I_E$ )	20 mA
Total Power Dissipation	
Ambient Temperature $\leq 70^\circ C$	500 mW
Operating Temperature Range	
MAT03A	-55°C to +125°C
MAT03E/F	-40°C to +85°C
Operating Junction Temperature	-55°C to +150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C
Junction Temperature	-65°C to +150°C

NOTES

<sup>1</sup>Absolute maximum ratings apply to both DICE and packaged devices.

<sup>2</sup>Rating applies to TO-78 not using a heat sink, and LCC; devices in free air only. For TO-78, derate linearly at 6.3 mW/°C above 70°C ambient temperature; for LCC, derate at 7.8 mW/°C.

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the MAT03 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# MAT03

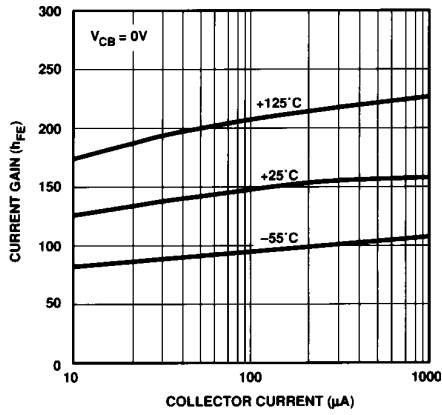


Figure 1. Current Gain vs. Collector Current

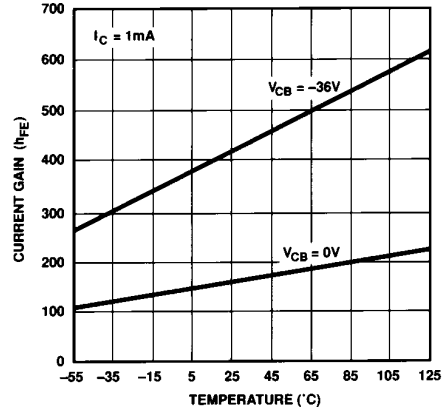


Figure 2. Current Gain vs. Temperature

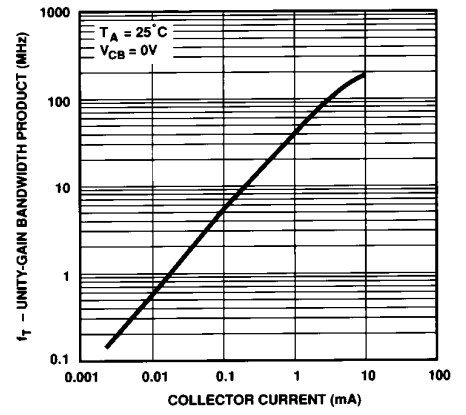


Figure 3. Gain Bandwidth vs. Collector Current

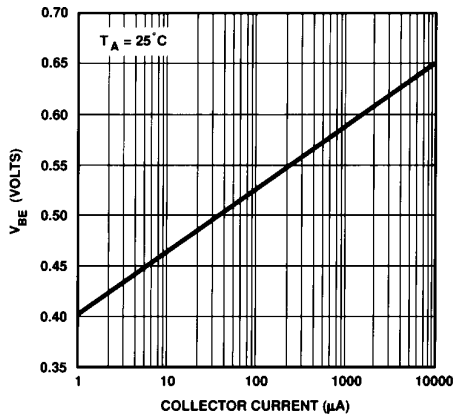


Figure 4. Base-Emitter Voltage vs. Collector Current

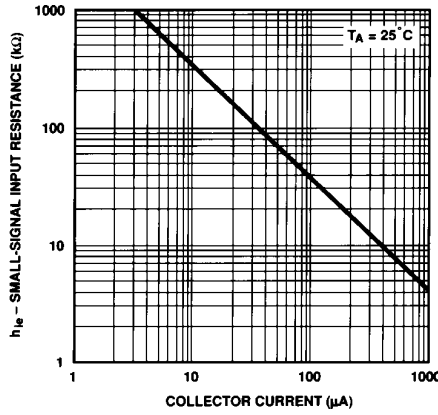


Figure 5. Small-Signal Input Resistance ( $h_{ie}$ ) vs. Collector Current

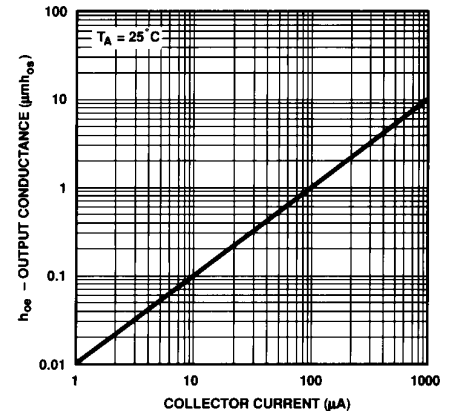


Figure 6. Small Signal Output Conductance ( $h_{oe}$ ) vs. Collector Current

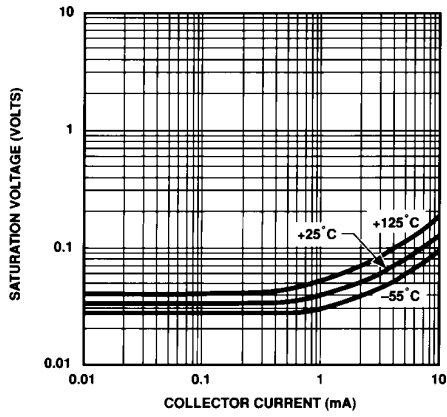


Figure 7. Saturation Voltage vs. Collector Current

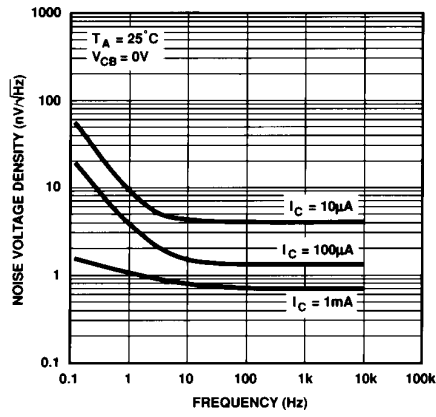


Figure 8. Noise Voltage Density vs. Frequency

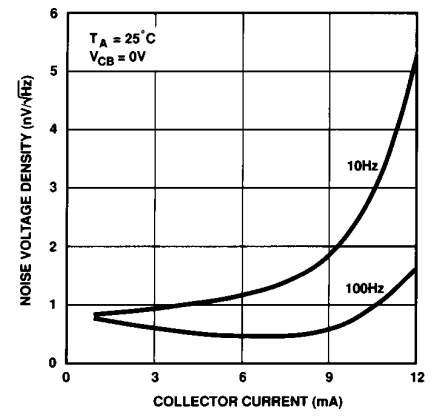


Figure 9. Noise Voltage Density vs. Collector Current

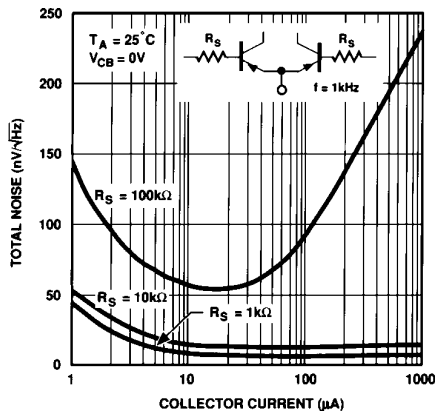


Figure 10. Total Noise vs. Collector Current

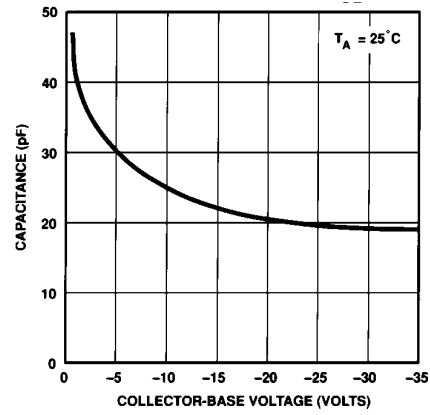
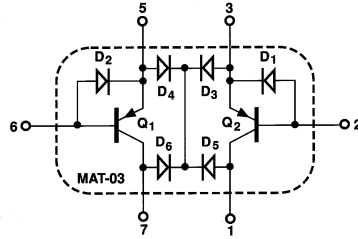


Figure 11. Collector-Base Capacitance vs.  $V_{CB}$

# MAT03



### SPICE MODEL PARAMETERS

```

•SUBCKT MAT03 1 2 3 5 6 7
Q1 1 2 3 PMAT
Q2 7 6 5 PMAT
D1 2 3 DMAT1
D2 6 5 DMAT1
D3 3 4 DMAT1
D4 5 4 DMAT1
D5 1 4 DMAT2
D6 7 4 DMAT2
•MODEL DMAT1 D IS = 7.2E-16 RS = 20
•MODEL DMAT2 D IS = 1E-14 VJ = 0.6 CJ = 68P
•MODEL PMAT PNP BF = 160 IS = 1.4E-13 VAF = 60 BR = 5 VAR = 7 RB = 16
+ PC = 12 RE = 0.35 CJE = 57P VJE = 0.7 MJE = 0.4 IF = 1.08E-9
+ TR = 3E-8 CJC = 40P VJC = 0.55 MJC = 0.5 CJS = 0 IKF = 1 60M
    
```

### SABER\* MODEL PARAMETERS

```

template mat03 n1 n2 n3 n5 n6 n7
electrical n1,n2,n3,n5,n6,n7
{
d..model dmat1 = (is = 7.2e-16,rs = 20)
d..model dmat2 = (is = 1e-14,vj = 0.6,cjo = 68p)
q..model pmat = (type = __ p,bf = 160, is = 1.4e-13,vaf = 60,br = 5,var = 7,
rb = 16,rc = 12,re = 0.45,cje = 57p,vje = 0.7,mje = 0.4,tf = 1.08e-9,tr = 3e-8,
cjc = 40p,vjc = 0.55, mjc = 0.5,cjs = 0,ikf = 160m)
q.q1 n1 n2 n3 n4 = model = pmat
q.q2 n7 n6 n5 n4 = model = pmat
d.d1 n2 n3 = model = dmat1
d.d2 n6 n5 = model = dmat1
d.d3 n3 n4 = model = dmat1
d.d4 n5 n4 = model = dmat1
d.d5 n1 n4 = model = dmat2
d.d6 n7 n4 = model = dmat2
}
    
```

\*SABER is a registered trademark of Analogly Inc.

Figure 12. SPICE or SABER Model

## APPLICATIONS INFORMATION

### MAT03 MODELS

The MAT03 model (Figure 12) includes parasitic diodes D<sub>3</sub> through D<sub>6</sub>. D<sub>1</sub> and D<sub>2</sub> are internal protection diodes which prevent zenering of the base-emitter junctions.

The analysis programs, SPICE and SABER, are primarily used in evaluating the functional performance of systems. The models are provided only as an aid in utilizing these simulation programs.

### MAT03 NOISE MEASUREMENT

All resistive components (Johnson noise,  $e_n^2 = 4kTBR$ , or  $e_n = 0.13\sqrt{R}$  nV/ $\sqrt{Hz}$ , where R is in k $\Omega$ ) and semiconductor junctions (Shot noise, caused by current flowing through a junction, produces voltage noise in series impedances such as transistor-collector load resistors,  $I_n = 0.566\sqrt{I}$  pA/ $\sqrt{Hz}$  where I is in  $\mu$ A) contribute to the system input noise.

Figure 13 illustrates a technique for measuring the equivalent input noise voltage of the MAT03. 1 mA of stage current is used

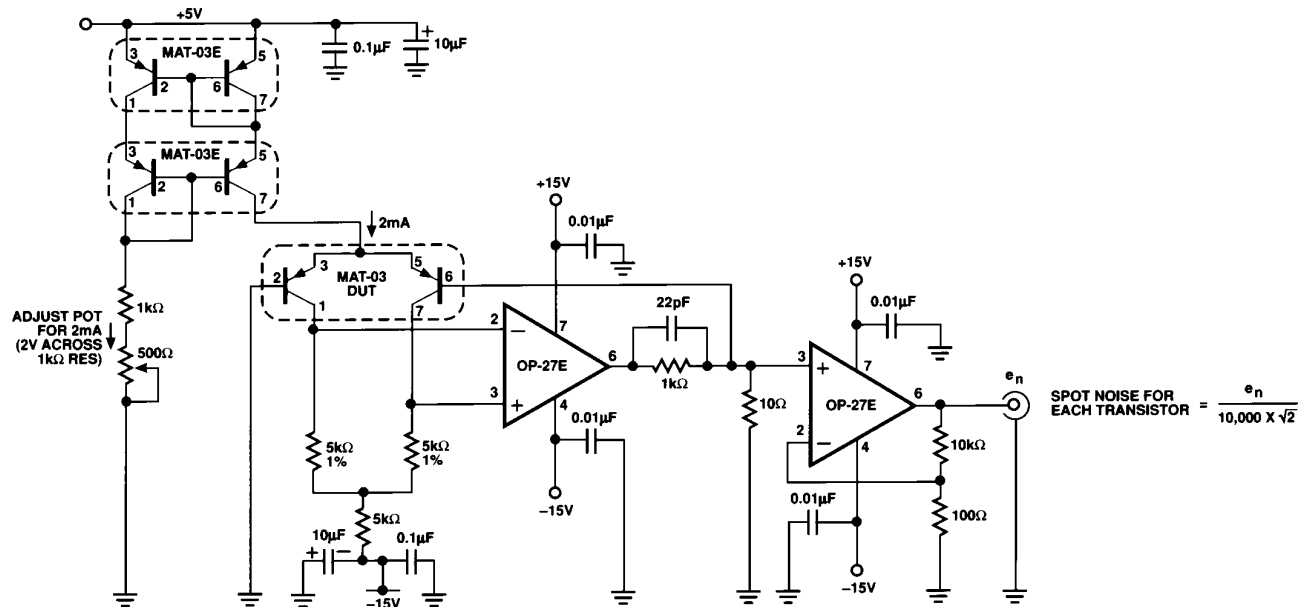


Figure 13. MAT03 Voltage Noise Measurement Circuit

to bias each side of the differential pair. The 5 kΩ collector resistors noise contribution is insignificant compared to the voltage noise of the MAT03. Since noise in the signal path is referred back to the input, this voltage noise is attenuated by the gain of the circuit. Consequently, the noise contribution of the collector load resistors is only 0.048 nV/√Hz. This is considerably less than the typical 0.8 nV/√Hz input noise voltage of the MAT03 transistor.

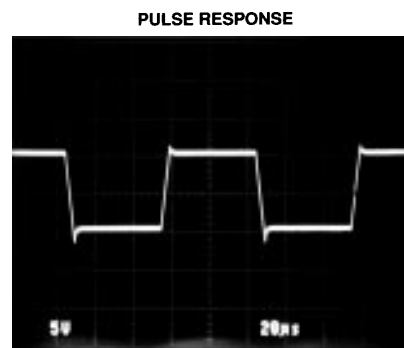
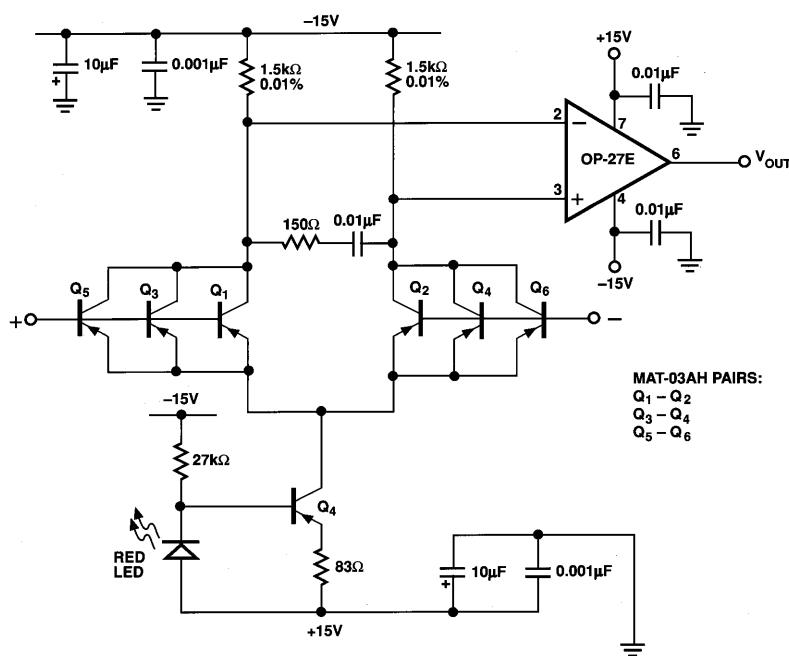
The noise contribution of the OP27 gain stages is also negligible due to the gain in the signal path. The op amp stages amplify the input referred noise of the transistors to increase the signal strength to allow the noise spectral density ( $e_{in} \times 10000$ ) to be measured with a spectrum analyzer. And, since we assume equal noise contributions from each transistor in the MAT03, the output is divided by  $\sqrt{2}$  to determine a single transistor's input noise.

Air currents cause small temperature changes that can appear as low frequency noise. To eliminate this noise source, the

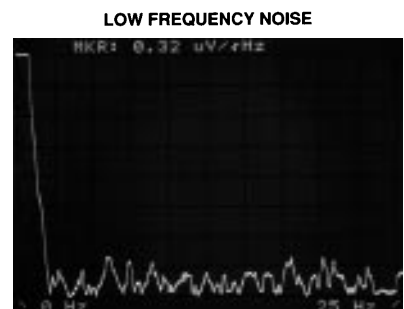
measurement circuit must be thermally isolated. Effects of extraneous noise sources must also be eliminated by totally shielding the circuit.

**SUPER LOW NOISE AMPLIFIER**

The circuit in Figure 14a is a super low noise amplifier with equivalent input voltage noise of 0.32 nV/√Hz. By paralleling three MAT03 matched pairs, a further reduction of amplifier noise is attained by a reduction of the base spreading resistance by a factor of 3, and consequently the noise by  $\sqrt{3}$ . Additionally, the shot noise contribution is reduced by maintaining a high collector current (2 mA/device) which reduces the dynamic emitter resistance and decreases voltage noise. The voltage noise is inversely proportional to the square root of the stage current, and current noise increases proportionally to the square root of the stage current. Accordingly, this amplifier capitalizes on voltage noise reduction techniques at the expense of increasing the current noise. However, high current noise is not usually important when dealing with low impedance sources.



$A_V = 10$   
 $C_f = 30pF$



$A_V = 1000$   
 $V_{ERT} = 1nV/DIV$

Figure 14a. Super Low Noise Amplifier

# MAT03

This amplifier exhibits excellent full power ac performance, 0.08% THD into a 600 Ω load, making it suitable for exacting audio applications (see Figure 14b).

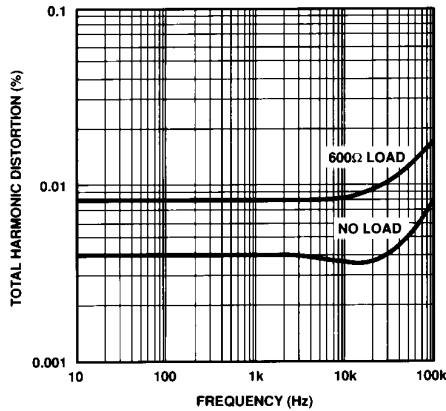


Figure 14b. Super Low Noise Amplifier—Total Harmonic Distortion

## LOW NOISE MICROPHONE PREAMPLIFIER

Figure 15 shows a microphone preamplifier that consists of a MAT03 and a low noise op amp. The input stage operates at a relatively high quiescent current of 2 mA per side, which reduces the MAT03 transistor's voltage noise. The 1/f corner is less than 1 Hz. Total harmonic distortion is under 0.005% for a 10 V p-p signal from 20 Hz to 20 kHz. The preamp gain is 100, but can be modified by varying R<sub>5</sub> or R<sub>6</sub> ( $V_{OUT}/V_{IN} = R_5/R_6 + 1$ ).

A total input stage emitter current of 4 mA is provided by Q<sub>2</sub>. The constant current in Q<sub>2</sub> is set by using the forward voltage of a GaAsP LED as a reference. The difference between this voltage

and the V<sub>BE</sub> of a silicon transistor is predictable and constant (to a few percent) over a wide temperature range. The voltage difference, approximately 1 V, is dropped across the 250 Ω resistor which produces a temperature stabilized emitter current.

## CURRENT SOURCES

A fundamental requirement for accurate current mirrors and active load stages is matched transistor components. Due to the excellent V<sub>BE</sub> matching (the voltage difference between V<sub>BE</sub>'s required to equalize collector current) and gain matching, the MAT03 can be used to implement a variety of standard current mirrors that can source current into a load such as an amplifier stage. The advantages of current loads in amplifiers versus resistors is an increase of voltage gain due to higher impedances, larger signal range, and in many applications a wider signal bandwidth.

Figure 16 illustrates a cascode current mirror consisting of two MAT03 transistor pairs.

The cascode current source has a common base transistor in series with the output which causes an increase in output impedance of the current source since V<sub>CE</sub> stays relatively constant. High frequency characteristics are improved due to a reduction of Miller capacitance. The small-signal output impedance can be determined by consulting "h<sub>OF</sub> vs. Collector Current" typical graph. Typical output impedance levels approach the performance of a perfect current source.

Considering a typical collector current of 100 μA, we have:

$$r_{OQ3} = \frac{1}{1.0 \mu\text{MHOS}} = 1 \text{ M}\Omega$$

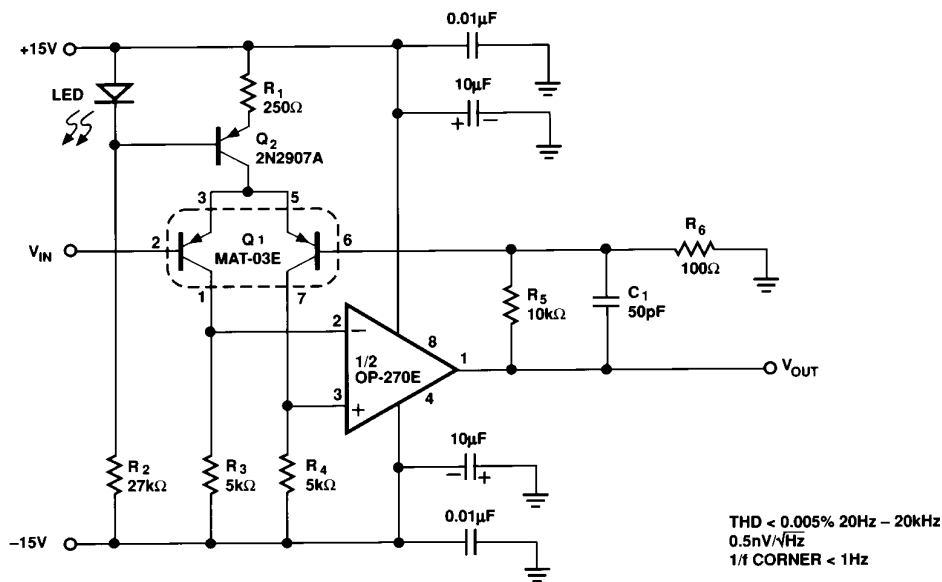


Figure 15. Low Noise Microphone Preamplifier



$Q_2$  and  $Q_3$  are in series and operate at the same current levels so the total output impedance is:

$$R_O = h_{FE} r_{OQ3} @ (160)(1 M\Omega) = 160 M\Omega.$$

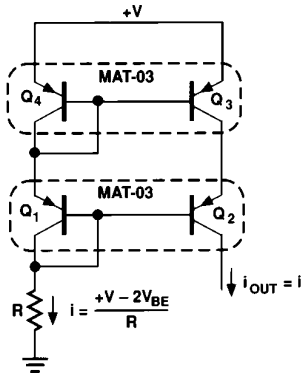


Figure 16. Cascode Current Source

Since  $Q_2$  buffers  $Q_3$ , both transistors in the MAT03,  $Q_1$  and  $Q_3$ , maintain the same collector current.  $D_2$  and  $D_3$  form a Baker clamp which prevents  $Q_2$  from turning off, thereby improving the switching speed of the current mirror. The feedback serves to increase the output impedance and improves accuracy by reducing the base-width modulation which occurs with varying collector-emitter voltages. Accuracy and linearity performance of the current pump is summarized in Figure 19.

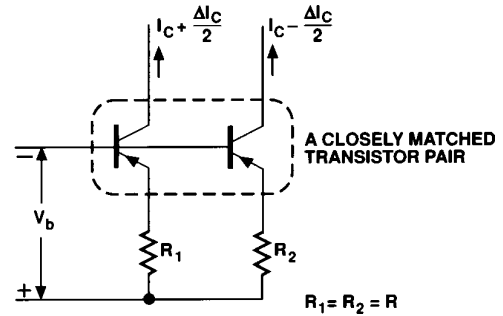


Figure 17a. Current Matching Circuit

**CURRENT MATCHING**

The objective of current source or mirror design is generation of currents that are either matched or must maintain a constant ratio. However, mismatch of base-emitter voltages cause output current errors. Consider the example of Figure 17a. If the resistors and transistors are equal and the collector voltages are the same, the collector currents will match precisely. Investigating the current-matching errors resulting from a nonzero  $V_{OS}$ , we define  $\Delta I_C$  as the current error between the two transistors.

Graph 17b describes the relationship of current matching errors versus offset voltage for a specified average current  $I_C$ . Note that since the relative error between the currents is exponentially proportional to the offset voltage, tight matching is required to design high accuracy current sources. For example, if the offset voltage is 5 mV at 100  $\mu$ A collector current, the current matching error would be 20%. Additionally, temperature effects such as offset drift (3  $\mu$ V/ $^{\circ}$ C per mV of  $V_{OS}$ ) will degrade performance if  $Q_1$  and  $Q_2$  are not well matched.

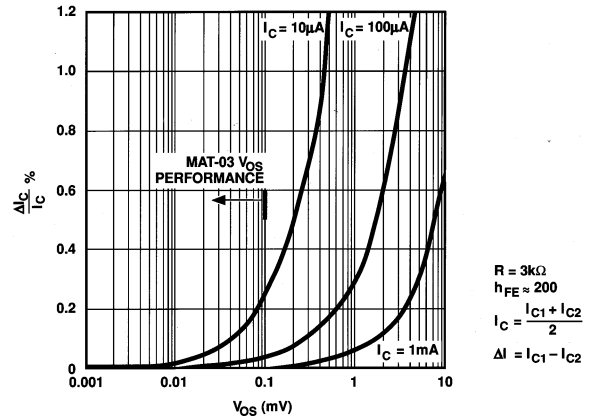


Figure 17b. Current Matching Accuracy % vs. Offset Voltage

**DIGITALLY PROGRAMMABLE BIPOLAR CURRENT PUMP**

The circuit of Figure 18 is a digitally programmable current pump. The current pump incorporates a DAC08, and a fast Wilson current source using the MAT03. Examining Figure 18, the DAC08 is set for 2 mA full-scale range so that bipolar current operation of  $\pm 2$  mA is achieved. The Wilson current mirror maintains linearity within the LSB range of the 8-bit DAC08 ( $\pm 2$  mA/256 = 15.6  $\mu$ A resolution) as seen in Figure 19. A negative feedback path established by  $Q_2$  regulates the collector current so that it matches the reference current programmed by the DAC08.

Collector-emitter voltages across both  $Q_1$  and  $Q_3$  are matched by  $D_1$ , with  $Q_3$ 's collector-emitter voltage remaining constant, independent of the voltage across the current source output.

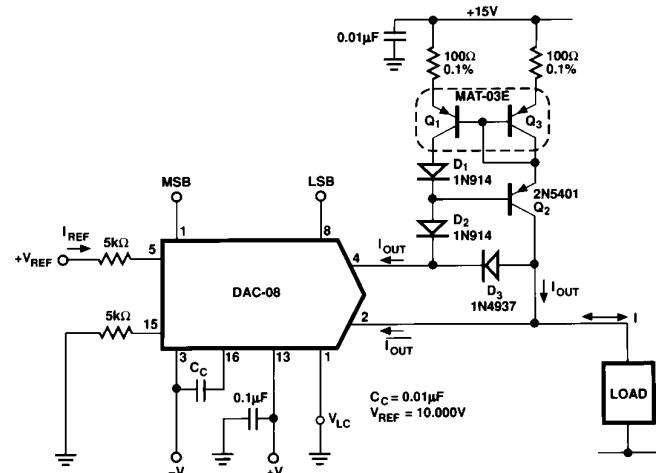


Figure 18. Digitally Programmable Bipolar Current Pump

# MAT03

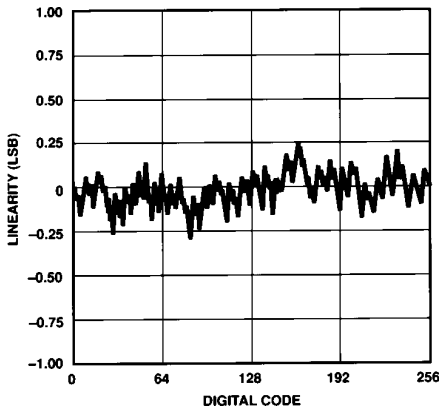


Figure 19. Digitally Programmable Current Pump—INL Error as Digital Code

The full-scale output of the DAC08,  $I_{OUT}$ , is a linear function of  $I_{REF}$

$$I_{FR} = \frac{256}{256} \times I_{REF}, \text{ and } I_{OUT} + \overline{I_{OUT}} = I_{REF} \frac{256}{256}$$

The current mirror output is  $I_{OUT} - \overline{I_{OUT}} = 1$ , so that if

$$I_{REF} = 2 \text{ mA:}$$

$$I = 2 I_{OUT} - 1.992 \text{ mA}$$

$$= 2 \left( \frac{\text{Input Code}}{256} \right) (2 \text{ mA}) - 1.992 \text{ mA.}$$

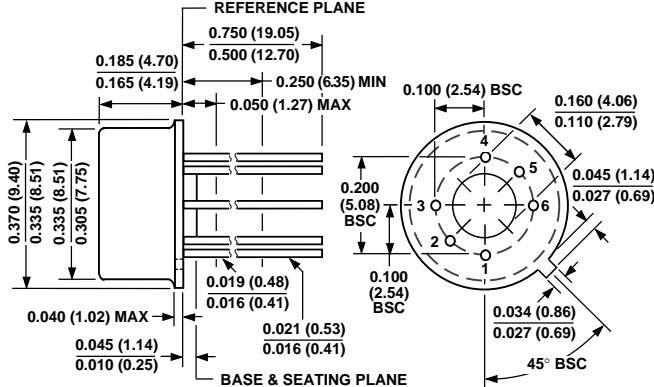
### DIGITAL CURRENT PUMP CODING

	Digital Input B1 . . . B8	Output Current
FULL RANGE	1111 1111	I = 1.992 mA
HALF-RANGE	1000 0000	I = 0.008 mA
ZERO-SCALE	0000 0000	I = -1.992 mA

**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

**TO-78 Metal Can**



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