

## ML144110 ML144111 Digital-to-Analog Converters with Serial Interface

CMOS LSI

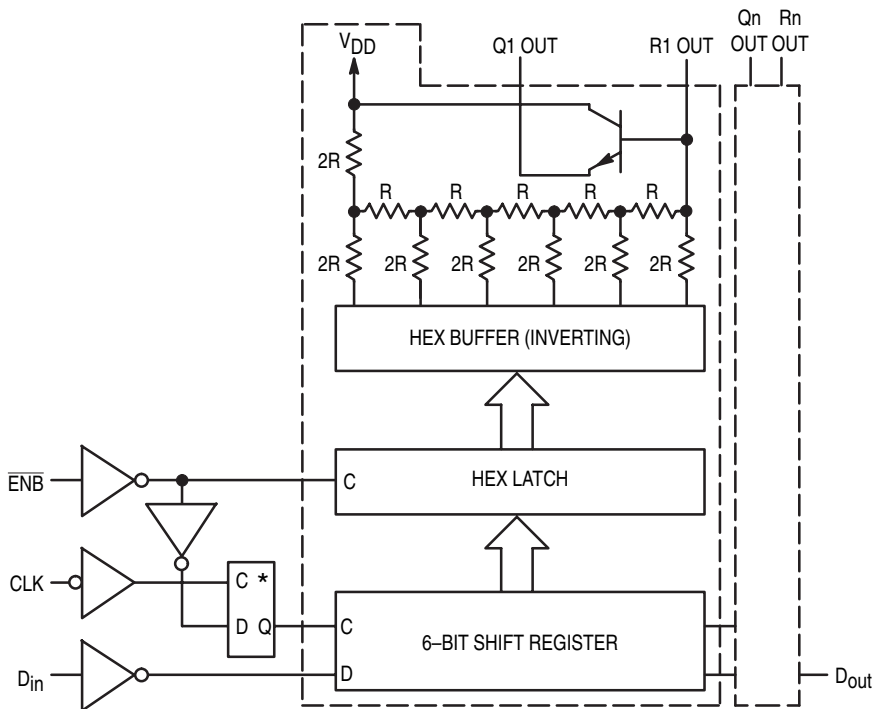
**Legacy Device:** Motorola/Freescale MC144110, MC144111

The ML144110 and ML144111 are low-cost 6-bit D/A converters with serial interface ports to provide communication with CMOS microprocessors and microcomputers. The ML144110 contains six static D/A converters; the ML144111 contains four converters.

Due to a unique feature of these DACs, the user is permitted easy scaling of the analog outputs of a system. Over a 5 to 15 V supply range, these DACs maybe directly interfaced to CMOS MPUs operating at 5 V.

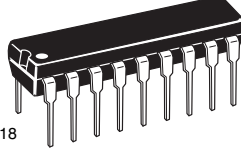
- Direct R-2R Network Outputs
- Buffered Emitter-Follower Outputs
- Serial Data Input
- Digital Data Output Facilitates Cascading
- Direct Interface to CMOS  $\mu$ P
- Wide Operating Voltage Range: 4.5 to 15 V
- Wide Operating Temperature Range:  $T_A = 0$  to  $85^\circ\text{C}$
- Software Information is Contained in Document M68HC11RM/AD

### BLOCK DIAGRAM

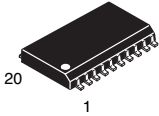


\* Transparent Latch

**MC144110**

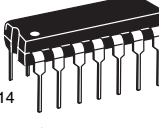


**P DIP 18 = VP**  
PLASTIC DIP  
CASE 707

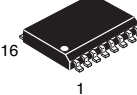


**SO 20W = -6P**  
SOG PACKAGE  
CASE 751D

**MC144111**



**P DIP 14 = CP**  
PLASTIC DIP  
CASE 646



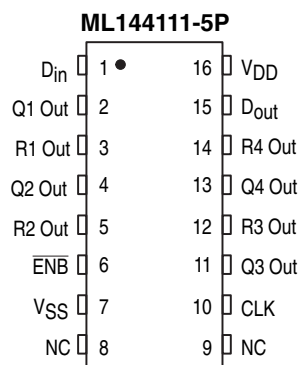
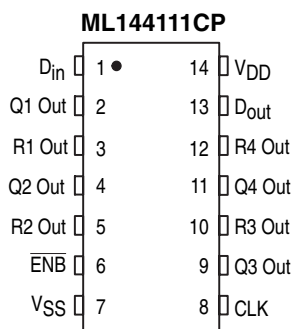
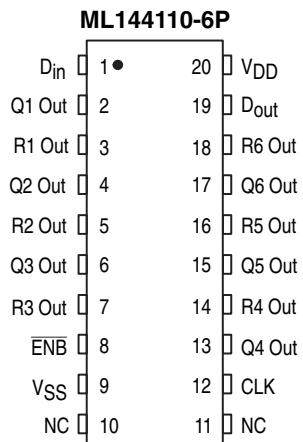
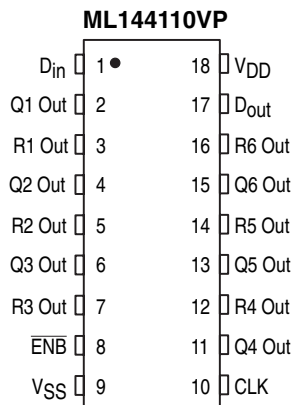
**SO 16W = -5P**  
SOG PACKAGE  
CASE 751G

PACKAGE	MOTOROLA	LANSDALE
P DIP 18	MC144110P	ML144110VP
SO 20W	MC144110DW	ML144110-6P
P DIP 14	MC144111P	ML144111CP
SO 16W	MC144111DW	ML144111-5P

**CROSS REFERENCE/ORDERING INFORMATION**

**Note:** Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

PIN ASSIGNMENTS



NC = NO CONNECTION

**MAXIMUM RATINGS\*** (Voltages referenced to V<sub>SS</sub>)

Parameter	Symbol	Value	Unit
DC Supply Voltage	V <sub>DD</sub>	- 0.5 to + 18	V
Input Voltage, All Inputs	V <sub>in</sub>	- 0.5 to V <sub>DD</sub> + 0.5	V
DC Input Current, per Pin	I	± 10	mA
Power Dissipation (Per Output) T <sub>A</sub> = 70°C, MC144110 MC144111 T <sub>A</sub> = 85°C, MC144110 MC144111	P <sub>OH</sub>	30 50 10 20	mW
Power Dissipation (Per Package) T <sub>A</sub> = 70°C, MC144110 MC144111 T <sub>A</sub> = 85°C, MC144110 MC144111	P <sub>D</sub>	100 150 25 50	mW
Storage Temperature Range	T <sub>stg</sub>	- 65 to + 150	°C

\* Maximum Ratings are those values beyond which damage to the device may occur.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields; however, it is advised that precautions be taken to avoid application of voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V<sub>in</sub> and V<sub>out</sub> be constrained to the range V<sub>SS</sub> ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>DD</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>).

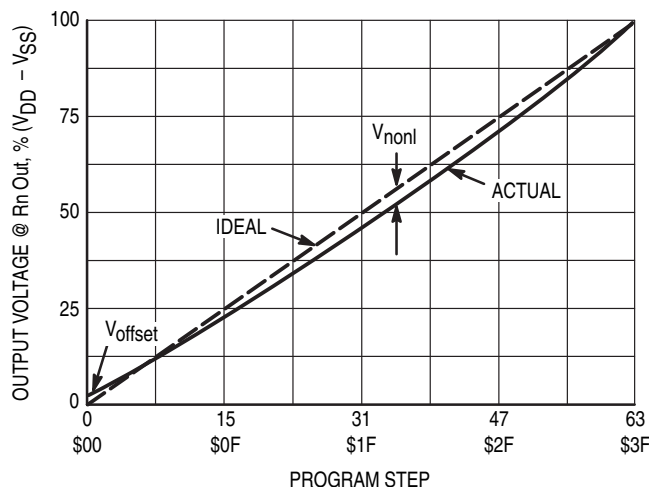
**ELECTRICAL CHARACTERISTICS** (Voltages referenced to V<sub>SS</sub>, T<sub>A</sub> = 0 to 85°C unless otherwise indicated)

Symbol	Parameter	Test Conditions	V <sub>DD</sub>	Min	Max	Unit
V <sub>IH</sub>	High-Level Input Voltage (D <sub>in</sub> , $\overline{\text{ENB}}$ , CLK)		5 10 15	3.0 3.5 4	— — —	V
V <sub>IL</sub>	Low-Level Input Voltage (D <sub>in</sub> , $\overline{\text{ENB}}$ , CLK)		5 10 15	— — —	0.8 0.8 0.8	V
I <sub>OH</sub>	High-Level Output Current (D <sub>out</sub> )	V <sub>out</sub> = V <sub>DD</sub> - 0.5 V	5	- 200	—	μA
I <sub>OL</sub>	Low-Level Output Current (D <sub>out</sub> )	V <sub>out</sub> = 0.5 V	5	200	—	μA
I <sub>DD</sub>	Quiescent Supply Current ML144110 ML144111	I <sub>out</sub> = 0 μA	15 15	— —	12 8	mA
I <sub>in</sub>	Input Leakage Current (D <sub>in</sub> , $\overline{\text{ENB}}$ , CLK)	V <sub>in</sub> = V <sub>DD</sub> or 0 V	15	—	± 1	μA
V <sub>nonl</sub>	Nonlinearity Voltage (Rn Out)	See Figure 1	5 10 15	— — —	100 200 300	mV
V <sub>step</sub>	Step Size (Rn Out)	See Figure 2	5 10 15	19 39 58	137 274 411	mV
V <sub>offset</sub>	Offset Voltage from V <sub>SS</sub>	D <sub>in</sub> = \$00, See Figure 1	—	—	1	LSB
I <sub>E</sub>	Emitter Leakage Current	V <sub>Rn Out</sub> = 0 V	15	—	10	μA
h <sub>FE</sub>	DC Current Gain	I <sub>E</sub> = 0.1 to 10.0 mA T <sub>A</sub> = 25°C	—	40	—	—
V <sub>BE</sub>	Base-to-Emitter Voltage Drop	I <sub>E</sub> = 1.0 mA	—	0.4	0.7	V

**SWITCHING CHARACTERISTICS**

(Voltages referenced to  $V_{SS}$ ,  $T_A = 0$  to  $85^\circ\text{C}$ ,  $C_L = 50$  pF, Input  $t_r = t_f = 20$  ns unless otherwise indicated)

Symbol	Parameter	$V_{DD}$	Min	Max	Unit
$t_{wH}$	Positive Pulse Width, CLK (Figures 3 and 4)	5	2	—	$\mu\text{s}$
		10	1.5	—	
		15	1	—	
$t_{wL}$	Negative Pulse Width, CLK (Figure 3 and 4)	5	5	—	$\mu\text{s}$
		10	3.5	—	
		15	2	—	
$t_{su}$	Setup Time, $\overline{\text{ENB}}$ to CLK (Figures 3 and 4)	5	5	—	$\mu\text{s}$
		10	3.5	—	
		15	2	—	
$t_{su}$	Setup Time, $D_{in}$ to CLK (Figures 3 and 4)	5	1000	—	ns
		10	750	—	
		15	500	—	
$t_h$	Hold Time, CLK to $\overline{\text{ENB}}$ (Figures 3 and 4)	5	5	—	$\mu\text{s}$
		10	3.5	—	
		15	2	—	
$t_h$	Hold Time, CLK to $D_{in}$ (Figures 3 and 4)	5	5	—	$\mu\text{s}$
		10	3.5	—	
		15	2	—	
$t_r, t_f$	Input Rise and Fall Times	5 – 15	—	2	$\mu\text{s}$
$C_{in}$	Input Capacitance	5 – 15	—	7.5	pF



**LINEARITY ERROR** (integral linearity). A measure of how straight a device's transfer function is, it indicates the worst-case deviation of linearity of the actual transfer function from the best-fit straight line. It is normally specified in parts of an LSB.

**Figure 1. D/A Transfer Function**

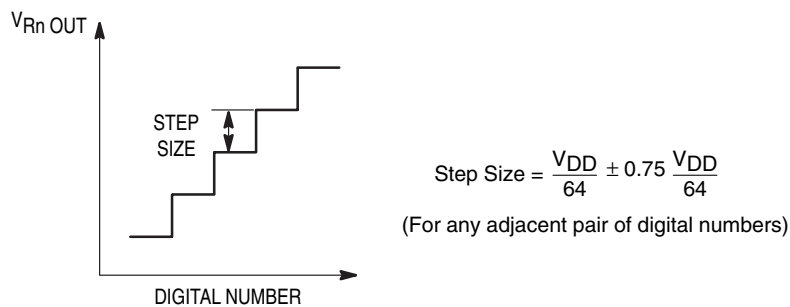


Figure 2. Definition of Step Size

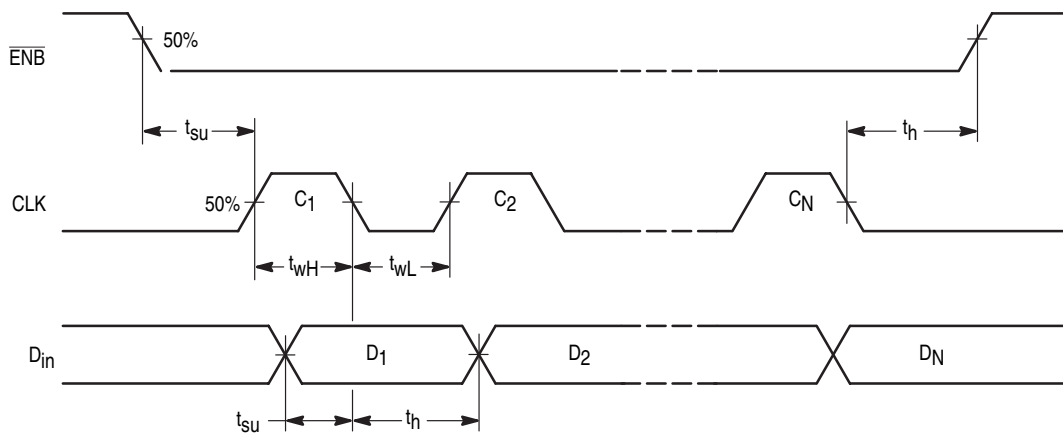


Figure 3. Serial Input, Positive Clock

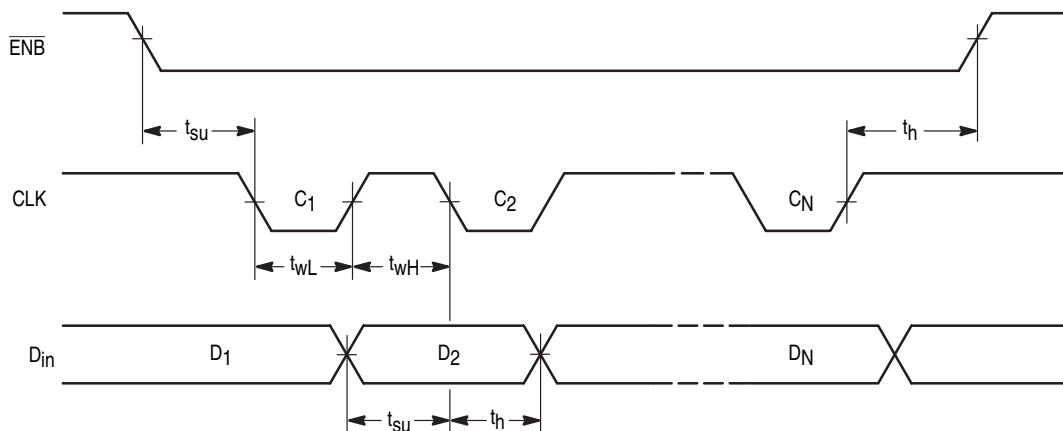


Figure 4. Serial Input, Negative Clock

## PIN DESCRIPTIONS

### INPUTS

#### **D<sub>in</sub>** **Data Input**

Six-bit words are entered serially, MSB first, into digital data input, D<sub>in</sub>. Six words are loaded into the ML144110 during each D/A cycle; four words are loaded into the ML144111.

The last 6-bit word shifted in determines the output level of pins Q1 Out and R1 Out. The next-to-last 6-bit word affects pins Q2 Out and R2 Out, etc.

#### **$\overline{\text{ENB}}$** **Negative Logic Enable**

The  $\overline{\text{ENB}}$  pin must be low (active) during the serial load. On the low-to-high transition of  $\overline{\text{ENB}}$ , data contained in the shift register is loaded into the latch.

#### **CLK** **Shift Register Clock**

Data is shifted into the register on the high-to-low transition of CLK. CLK is fed into the D-input of a transparent latch, which is used for inhibiting the clocking of the shift register when  $\overline{\text{ENB}}$  is high.

The number of clock cycles required for the ML144110 is usually 36. The ML144111 usually uses 24 cycles. See Table 1 for additional information.

### OUTPUTS

#### **D<sub>out</sub>** **Data Output**

The digital data output is primarily used for cascading the DACs and may be fed into D<sub>in</sub> of the next stage.

#### **R1 Out through R<sub>n</sub> Out** **Resistor Network Outputs**

These are the R-2R resistor network outputs. These outputs may be fed to high-impedance input FET op amps to bypass the on-chip bipolar transistors. The R value of the resistor network ranges from 7 to 15 k $\Omega$ .

#### **Q1 Out through Q<sub>n</sub> Out** **NPN Transistor Outputs**

Buffered DAC outputs utilize an emitter-follower configuration for current-gain, thereby allowing interface to low-impedance circuits.

### SUPPLY PINS

#### **V<sub>SS</sub>** **Negative Supply Voltage**

This pin is usually ground.

#### **V<sub>DD</sub>** **Positive Supply Voltage**

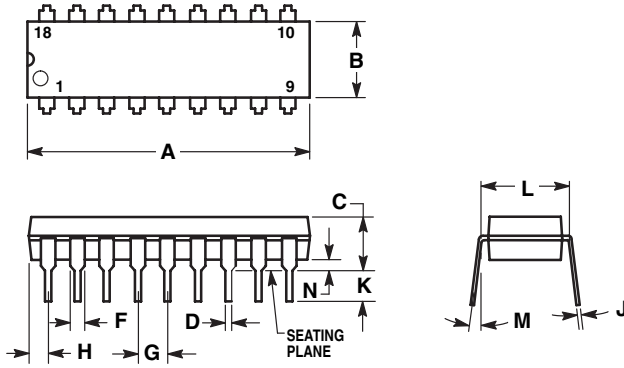
The voltage applied to this pin is used to scale the analog output swing from 4.5 to 15 V p-p.

Table 1. Number of Channels vs Clocks Required

Number of Channels Required	Number of Clock Cycles	Outputs Used on ML144110	Outputs Used on ML144111
1	6	Q1/R1	Q1/R1
2	12	Q1/R1, Q2/R2	Q1/R1, Q2/R2
3	18	Q1/R1, Q2/R2, Q3/R3	Q1/R1, Q2/R2, Q3/R3
4	24	Q1/R1, Q2/R2, Q3/R3, Q4/R4	Q1/R1, Q2/R2, Q3/R3, Q4/R4
5	30	Q1/R1, Q2/R2, Q3/R3, Q4/R4, Q5/R5	Not Applicable
6	36	Q1/R1, Q2/R2, Q3/R3, Q4/R4, Q5/R5, Q6/R6	Not Applicable

OUTLINE DIMENSIONS

P DIP 18 = VP  
(ML144110VP)  
PLASTIC DIP  
CASE 707-02

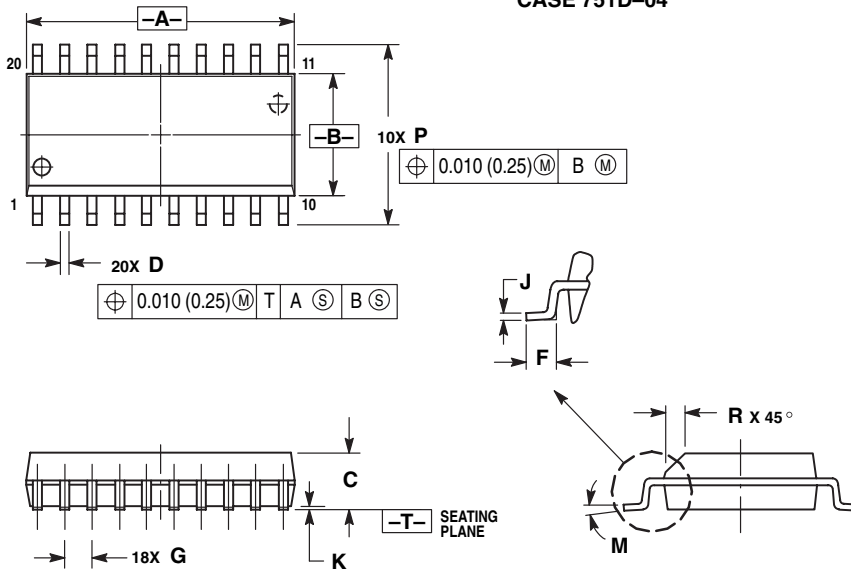


NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

SO 20W = -6P  
(ML144110-6P)  
SOG PACKAGE  
CASE 751D-04



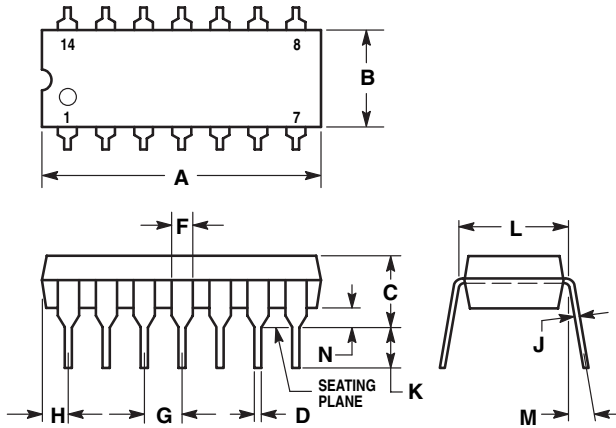
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

OUTLINE DIMENSIONS

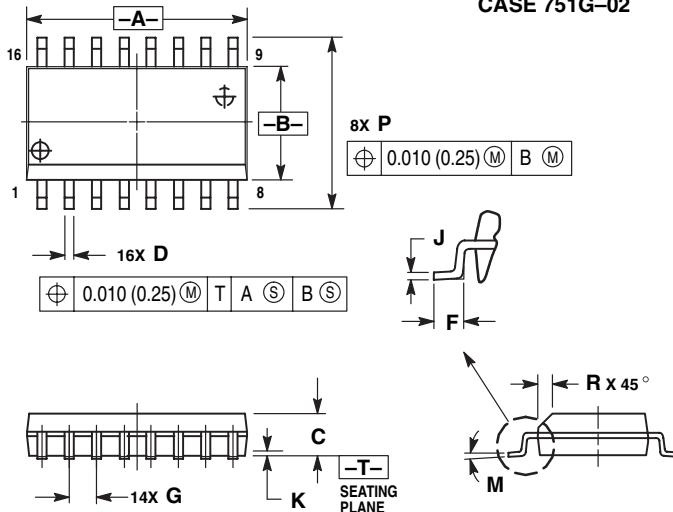
P DIP 14 = CP  
(ML144111CP)  
PLASTIC DIP  
CASE 646-06



- NOTES:
- LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
  - DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  - DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  - ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

SO 16W = -5P  
(ML144111-5P)  
SOG PACKAGE  
CASE 751G-02



- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: MILLIMETER.
  - DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  - MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  - DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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