

SXGA Flat Panel Controller

FEATURES

General

- Auto configuration of sampling clock frequency, phase, H/V center, as well as white balance.
- Auto detection of present or non-present or over range sync signals and their polarities.
- Composite sync separation and odd/even field detection of interlaced video.
- On-chip output PLL provide clock frequency fine-tune (inverse, duty cycle and delay).
- Selection of serial 2-wire I²C or 8-bit direct host interface to 8-bit MCU.
- 3.3V supplier, 5V I/O tolerance in 256-pin PQFP or 272-pin BGA package.

Input Processor

- Single RGB (24-bit) or Dual RGB (48-bit) input rates up to 160MHz.
- Support both non-interlaced and interlaced RGB graphic input signals.
- YUV 4:2:2 or YUV 4:1:1 (CCIR601) interlaced video input.
- Glue-less connection to Philips SAA711x digital video decoder.
- Built-in YUV to RGB color space converter.
- Compliant with digital LVDS/PanelLink TMDS input interface.
- PC input resolution up to SXGA 1280x1024 @85Hz.

Video Processor

- Independent programmable Horizontal and Vertical scaling ratios from 1/32 to 32
- Flexible de-interlacing unit for digital YUV video input data.
- Zoom to full screen resolution of de-interlaced YUV video data stream.
- Built-in programmable gain control for white balance alignments.
- Built-in programmable 8-bit or 10-bit gamma correction table.
- Built-in programmable temporal color dithering.
- Built-in programmable interpolation look-up table.
- Support smooth panning under viewing window change.

Output Processor

- Single pixel (18/24-bit) or Dual pixel (36/48-bit) per clock digital RGB output.
- Built-in output timing generator with programmable clock and H/V sync.
- Support VGA/SVGA/XGA/SXGA display resolution.
- Overlay input interface with external OSD controller.
- Double scan capability for interlaced input.

Memory Interface

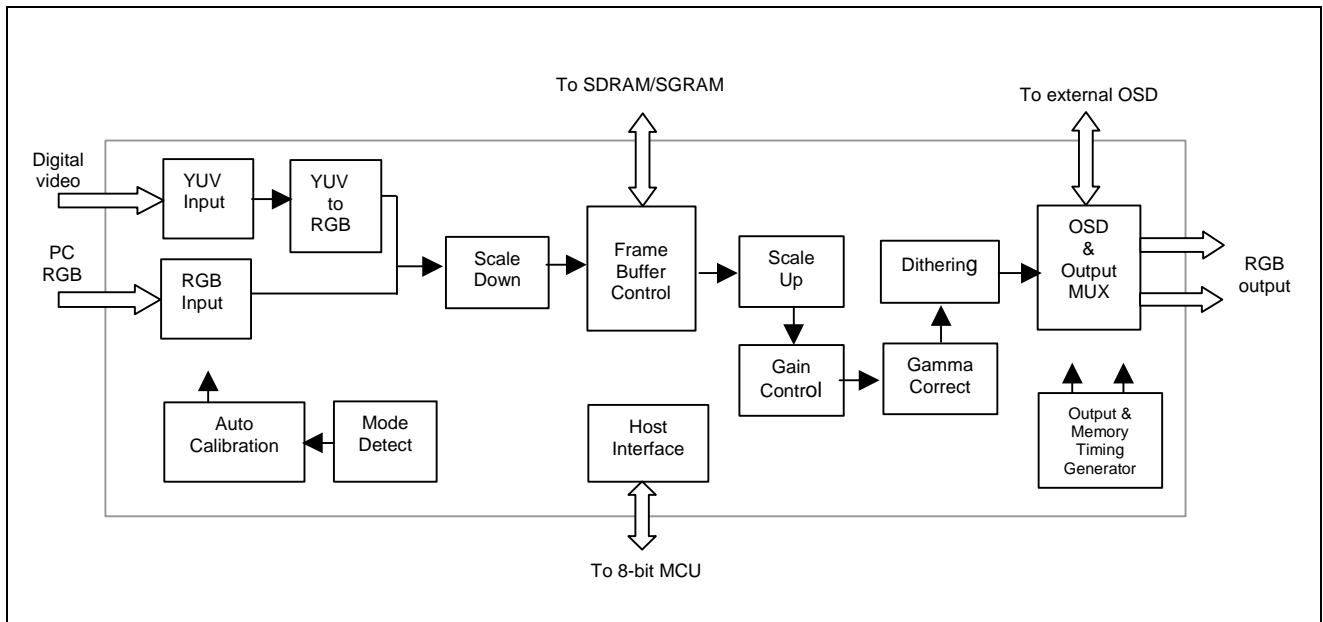
- Support 48/32/24 bit bus width, SDRAM/SGRAM x2 or x3 configuration.
- Optional display through internal line buffer without external frame-buffer memory.
- Support power down mode.

GENERAL DESCRIPTION

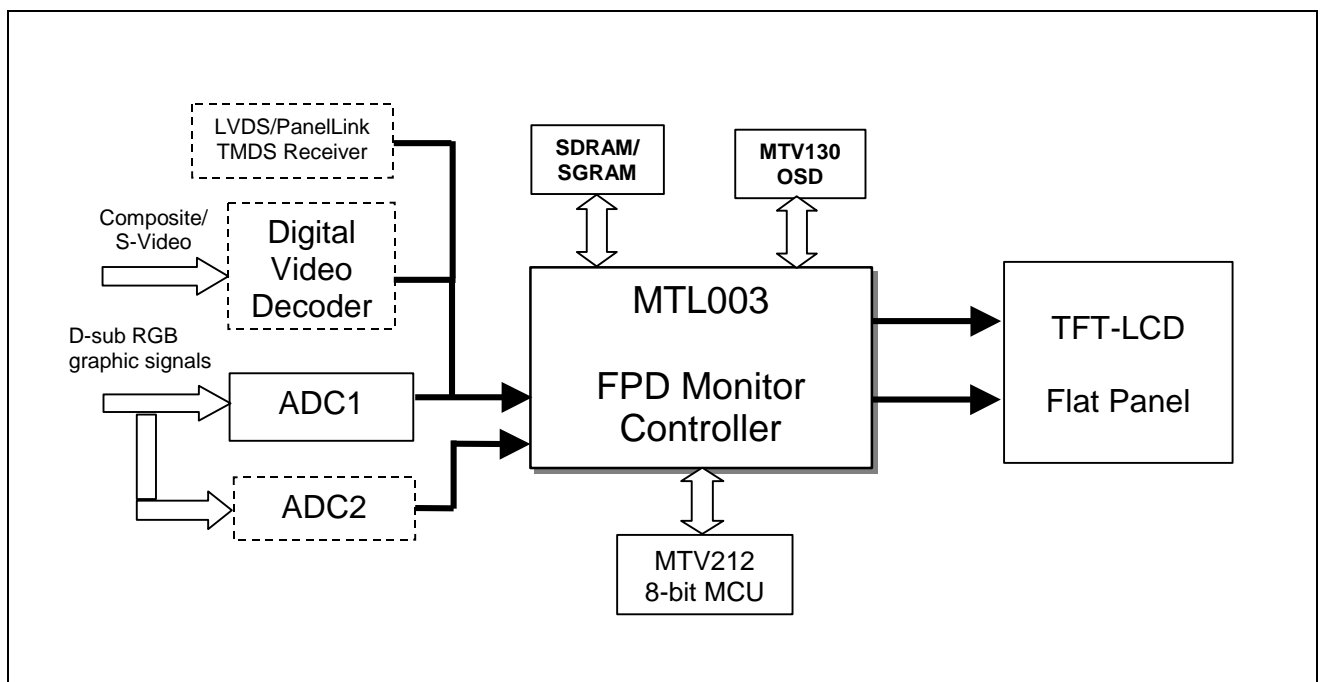
The MTL003 Flat Panel Display (FPD) Controller is an input format converter for TFT-LCD Monitor or LCD TV application which accepts 15-pin D-sub RGB graphic signals (through ADC), YUV signals from digital video decoder or digital RGB graphic signals from PanelLink TMDS receiver. It includes a RGB/YUV input processor, configurable frame-buffer memory interface, video scaling up/down processor, OSD input interface and output display processor in 256-pin PQFP or 272-pin BGA package.



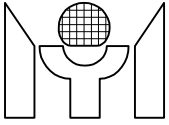
BLOCK DIAGRAM



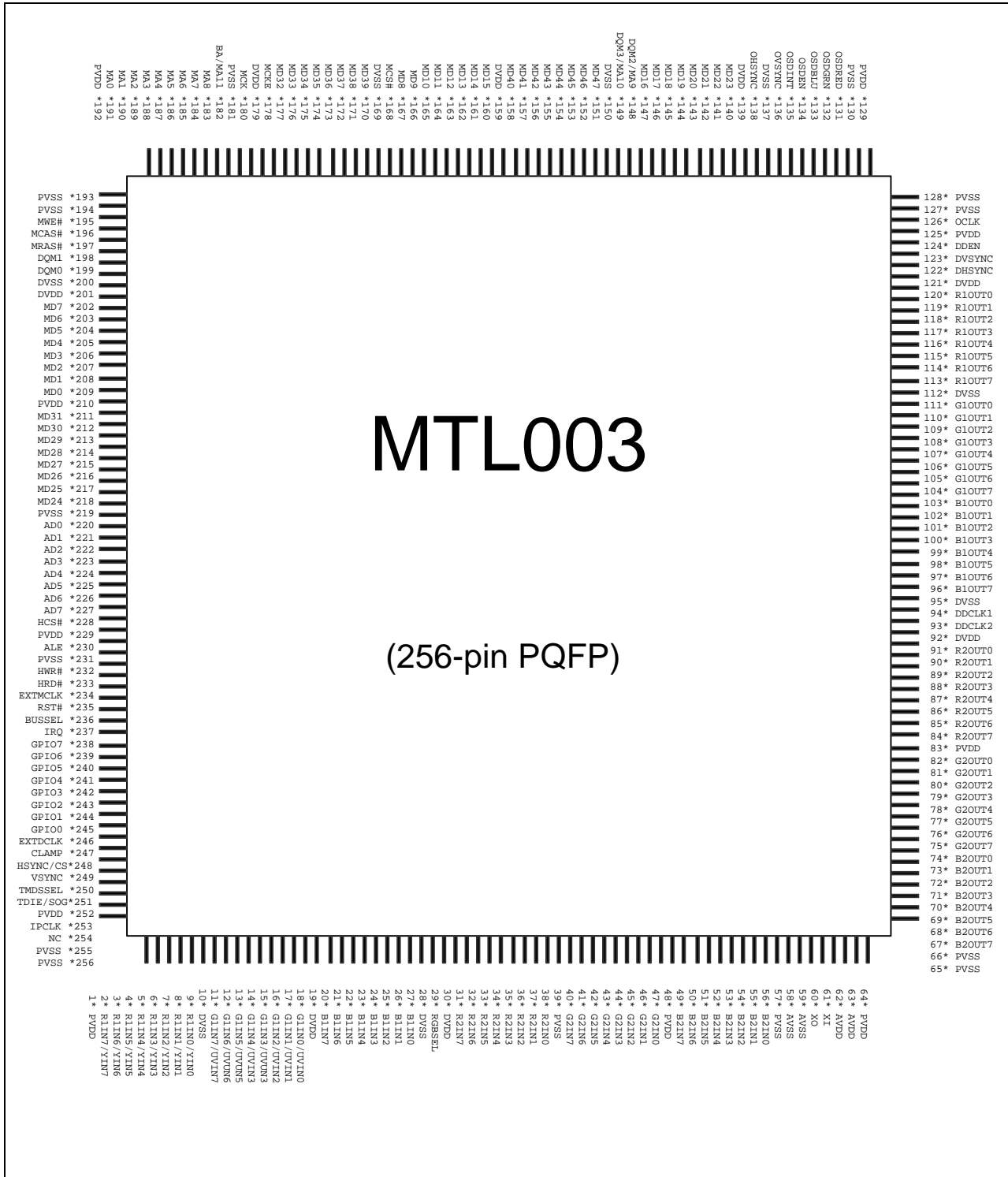
APPLICATIONS



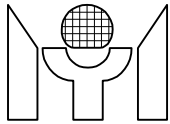
This datasheet contains new product information. Myson Technology reserves the rights to modify the product specification without notice. No liability is assumed as a result of the use of this product. No rights under any patent accompany the sale of the product.



1. PIN CONNECTION



Note: Pin connection of 272-pin BGA to be defined later



2. PIN DESCRIPTION

ADC1 Input Interface (YUV or RGB or TMDS Input Data)

| Name | Type | Pin# | Description |
|---------------------|------|-------|--|
| VSYNC | I | 249 | Vertical sync input |
| HSYNC/CS | I | 248 | Horizontal or Composite sync input |
| RGBSEL | O | 29 | Input select. 1:RGB input, 0:YUV input |
| TMDSSEL | O | 250 | TMDS input select, active high |
| CLAMP | O | 247 | Clamp pulse output for ADC |
| IPCLK | I | 253 | Input pixel clock |
| R1IN[7:0]/YIN[7:0] | I | 2-9 | Red or Y channel or TMDS input data (Single/Dual ADC) |
| G1IN[7:0]/UVIN[7:0] | I | 11-18 | Green or UV channel or TMDS input data (Single/Dual ADC) |
| B1IN[7:0] | I | 20-27 | Blue channel or TMDS input data (Single/Dual ADC) |
| TDIE | I | 251 | TMDS digital input enable |

ADC2 Input Interface (RGB Data)

| Name | Type | Pin# | Description |
|-----------|------|-------|--|
| R2IN[7:0] | I | 31-38 | Red channel input data (Dual ADC) or Control bit for YUV video input Bit 4: VPHREF, Video input Horizontal reference signal Bit 3: VPVS, Video input VSYNC signal Bit 2: VPODD, Video input ODD/EVEN field signal Bit 1: VPHS, Video input HSYNC signal Bit 0: VPCLK, Video input clock signal |
| G2IN[7:0] | I | 40-47 | Green channel input data (Dual ADC) |
| B2IN[7:0] | I | 49-56 | Blue channel input data (Dual ADC) |

Display Output Interface

| Name | Type | Pin# | Description |
|------------|------|---------|---|
| DDEN | O | 124 | Display data output enable for LCD panel |
| DVSYNC | O | 123 | Display Vertical sync output |
| DHSYNC | O | 122 | Display Horizontal sync output |
| DDCLK1 | O | 94 | Display output clock for odd data |
| DDCLK2 | O | 93 | Display output clock for even data |
| R1OUT[7:0] | O | 113-120 | Red output even data , bit[7:2] for 6-bit panel |
| G1OUT[7:0] | O | 104-111 | Green output even data , bit[7:2] for 6-bit panel |
| B1OUT[7:0] | O | 96-103 | Blue output even data , bit[7:2] for 6-bit panel |
| R2OUT[7:0] | O | 84-91 | Red output odd data , bit[7:2] for 6-bit panel |
| G2OUT[7:0] | O | 75-82 | Green output odd data , bit[7:2] for 6-bit panel |
| B2OUT[7:0] | O | 67-74 | Blue output odd data , bit[7:2] for 6-bit panel |

Memory Interface

| Name | Type | Pin# | Description |
|-----------|------|---------|---|
| MCK | O | 180 | Memory output clock |
| MCKE | O | 178 | Memory clock enable |
| MCS# | O | 168 | Memory chip select, active low. |
| MRAS# | O | 197 | Memory row address strobe, active low |
| MCAS# | O | 196 | Memory column address strobe, active low |
| MWE# | O | 195 | Memory write enable, active low |
| DQM[1:0] | O | 198-199 | Memory data mask byte enable |
| BA/MA11 | O | 182 | Memory bank address or Memory address line |
| DQM3/MA10 | O | 149 | SGRAM data mask byte enable or SDRAM address line |
| DQM2/MA9 | O | 148 | SGRAM data mask byte enable or SDRAM address line |
| MA[8:0] | O | 183-191 | Memory address line |



| | | | |
|-----------|-----|---------|------------------------|
| MD[47:40] | I/O | 151-158 | Memory Blue (B1) data |
| MD[39:32] | I/O | 170-177 | Memory Green (G1) data |
| MD[31:24] | I/O | 211-218 | Memory Red (R1) data |
| MD[23:16] | I/O | 140-147 | Memory Blue (B0) data |
| MD[15:8] | I/O | 160-167 | Memory Green (G0) data |
| MD[7:0] | I/O | 202-209 | Memory Red (R0) data |

Host Interface

| Name | Type | Pin# | Description |
|---------|------|---------|---|
| RST# | I | 235 | System reset input, active low. |
| AD[7:0] | I/O | 227-220 | The address and data bus of 8-bit direct interface or 2-wire I ² C series bus Bit 1: SDA, serial bus data Bit 0: SCK, serial bus clock |
| HWR# | I | 232 | Host write strobe, active low |
| HRD# | I | 233 | Host read strobe, active low |
| ALE | I | 230 | Host address latch enable for 8-bit direct bus |
| HCS# | I | 228 | Host chip select |
| BUSSEL | I | 236 | Bus mode selection. 0: I ² C bus, 1: 8-bit direct bus |
| IRQ | O | 237 | Interrupt request output |

OSD Interface

| Name | Type | Pin# | Description |
|--------|------|------|----------------------------------|
| OCLK | O | 126 | Clock for external OSD |
| OVSYNC | O | 136 | Vertical sync for external OSD |
| OHSYNC | O | 138 | Horizontal sync for external OSD |
| OSDRED | I | 131 | OSD red input |
| OSDGRN | I | 132 | OSD green input |
| OSDBLU | I | 133 | OSD blue input |
| OSDINT | I | 135 | OSD intensity input |
| OSDEN | I | 134 | OSD overlay enable |

Other Interface

| Name | Type | Pin# | Description |
|-----------|------|---------|--|
| XI | I | 61 | Oscillator frequency input |
| XO | O | 60 | Oscillator frequency output |
| EXTDCLK | I | 246 | External display clock input |
| EXTMCLK | I | 234 | External memory clock input |
| GPIO[7:0] | I/O | 238-245 | General purpose I/O or Bit 7: ADVS, Vertical sync for A/D converter Bit 6: ADHS, Horizontal sync for A/D converter Bit 2: MA9_SGRAM, Memory address 9 for SGRAM Bit 0: RAWHS/SOG, Input source HSYNC or Input Sync On Green Default: Bit[7:2]: Output direction Bit[1:0]: Input direction |
| NC | - | 254 | No connection |

3.3V Power and Ground

| Name | Pin# | Description |
|------|---|--------------------|
| DVDD | 19, 30, 92, 121, 139, 159, 179, 201 | Digital power 3.3V |
| DVSS | 10, 28, 95, 112, 137, 150, 169, 200 | Digital ground |
| PVDD | 1, 48, 64, 83, 125, 129, 192, 210, 229, 252 | Pad power 3.3V |
| PVSS | 39, 57, 65, 66, 127, 128, 130, 181, 193, 194, | Pad ground |



| | | |
|------|--------------------|-------------------|
| | 219, 231, 255, 256 | |
| AVDD | 62, 63 | Analog power 3.3V |
| AVSS | 58, 59 | Analog ground |



3. FUNCTIONAL DESCRIPTION

3.1 Input Processor

General Description

The function of Input Interface is to provide the interface between MTL003 and external input devices. It can process both non-interlaced and interlaced RGB graphic input, YUV video input, and digital RGB input compliant with digital LVDS/PanelLink TMDS interface. It also contains the Decimation circuit to scale down the input image with arbitrary ratios down to 1/32 and the built-in YUV to RGB color space converter.

3.1.1 RGB Input Format

The RGB input port can work in two modes: Single Pixel mode (24 bits) and Double Pixel mode (48 bits). For Single Pixel mode, only the ports R1IN[7:0], G1IN[7:0], and B1IN[7:0] are internally sampled. For Double Pixel mode, besides the ports R1IN[7:0], G1IN[7:0], and B1IN[7:0], the ports R2IN[7:0], G2IN[7:0], and B2IN[7:0] are needed additionally. The R/G/B1IN ports are sampled at the rising edge of the RGB input clock, and the R/G/B2IN ports are sampled at the falling edge.

3.1.2 TMDS Input Format

The Digital RGB input port works just in the same way as Sec 3.1.1 except that pin "Digital Input Enable DIEN" is needed.

With a flexible single or double pixel input interface, the supported format is up to true color, including the 18 bit/pixel or 24 bit/pixel in 1 or 2 pixels/clock mode.

3.1.3 YUV Input Format

The YUV input port supports interlaced video data from the most common video decoder ICs like SAA711x. The 16 bit data bus is shared with the ports R1IN[7:0] and G1IN[7:0]. The 5 bit control signals are shared with the port R2IN[4:0]. The 16 bit data is sampled at the rising edge of the shared video clock VPCLK when the shared data enable HREF is active. The supported formats are YUV4:1:1 and YUV4:2:2 with CCIR601 standard.

3.1.4 YUV to RGB Converter

Is used to convert YCbCr format into RGB format. The basic equations are as follows:

$$\begin{aligned}R &= Y + 1.371(Cr - 128) \\G &= Y - 0.698(Cr - 128) - 0.336(Cb - 128) \\B &= Y + 1.732(Cb - 128)\end{aligned}$$

3.1.5 De-interlace mode

For interlace input, MTL003 features several de-interlacing algorithms for processing interlaced video data depending on the type of input images.

Ā Static Mode

In this mode, the first and second fields are put together without any filtering. Memory for two fields is needed. It is commonly used in still image input.

Ā Toggle Mode

In this mode, only one field is displayed at a time. First field and second field is toggled displayed. The missing lines are calculated from duplicating the neighboring lines. For moving picture, it has a good quality.

Ā Spatial Mode

In this mode, two fields are toggled displayed, just like Toggle mode. The missing lines are calculated from interpolating the neighboring lines. This mode has a generally good quality for still and moving pictures.

3.1.6 Sync Processor

The V/H SYNC processing block performs the functions of Composite signal separation/insertion, SYNC inputs the presence check, frequency counting, polarity detection and control. It contains a de-glitch circuit to filter out any pulse shorter than one OSC period which is treated as noise among V/H SYNC pulses.



Ā **V/H SYNC Frequency Counter**

MTL003 measures VSYNC/HSYNC frequency counted in the proper clock and using the following formulae:

$$f_{\text{vsync}} = f_{\text{osc}} / N_{\text{vsync}} \quad F \ 1/256$$

$$f_{\text{hsync}} = f_{\text{osc}} / N_{\text{hsync}} \quad F \ 8$$

Where

- f_{vsync} : VSYNC frequency
- f_{hsync} : HSYNC frequency
- f_{osc} : oscillator clock with 14.31818 MHz
- N_{vsync} : counted number of VSYNC
- N_{hsync} : counted number of HSYNC

Ā **V/H SYNC Presence Check**

This function checks the input VSYNC, where Vpre flag is set when VSYNC is over 40Hz or cleared when VSYNC is under 10Hz and the input is HSYNC, where Hpre flag is set when HSYNC is over 10KHz or cleared when HSYNC is under 10Hz.

Ā **V/H Polarity Detect**

This function detects the input VSYNC/HSYNC high and low pulse duty cycle. If the high pulse duration is longer than that of low pulse, the negative polarity is asserted; otherwise, positive polarity is asserted.

Ā **Composite SYNC separation/insertion**

MTL003 continuously monitors the input HSYNC. If the input VSYNC can be extracted from it, a CVpre flag is set. MTL003 can insert HSYNC pulse during Composite VSYNC's active time and the insertion frequency can adapt to original HSYNC's.

3.1.7 Auto Tune

Auto Tune function consists of Auto Position that automatically centering the screen and Auto Calibration which contains Phase Calibration, Histogram, Min/Max Value, and Pixel Grab described as below. With this auto adjustment support it is possible to measure the correct phase, frequency, gain, and offset of ADC. The horizontal and vertical back porches of input image and the horizontal and vertical active regions can also be measured. Firmware can adjust input image registers automatically by reading Auto Tune's registers in single or burst mode.

Ā **Auto Position**

MTL003 provides Horizontal/Vertical back porch and active region values. Users can use these values to set input sample registers to aid in centering the screen automatically.

Ā **Phase Calibration**

MTL003 provides Auto Calibration registers to measure the quality of current ADC's phase and frequency. The biggest Auto Calibration registers value means the right value of ADC's phase and frequency. MTL003 has two kinds of algorithms to calculate Auto Calibration's value. One is the traditional Difference method, the other is MYSON's proprietary method; the latter one is recommended for a better performance.

Ā **Histogram**

Histogram means the total number of input pixels below/above one threshold value, for individual R/G/B colors. This advanced function helps the firmware to analyze ADC performance. Usually the firmware can use this information to measure ADC's noise margin, and adjust its offset and gain, or even aid in the mode detection.

Ā **Min/Max Value**

Min/Max value means minimum or maximum pixel value within the specified input active image region for each RGB channel. This information is usually used to adjust ADC's offset and gain.

Ā **Pixel Grab**

Pixel Grab means users can grab a single input pixel at any one point. The position of the point can be programmed by users. This is another traditional method to measure ADC's phase and frequency.



3.2 Video Processor

General Description

MTL003 possesses a powerful and programmable video processor by providing the following functions: Scaling Up/Down, Gain Control, Brightness Control, Gamma Correction, and Dithering Control.

The block diagram of Video Processor is as follows:

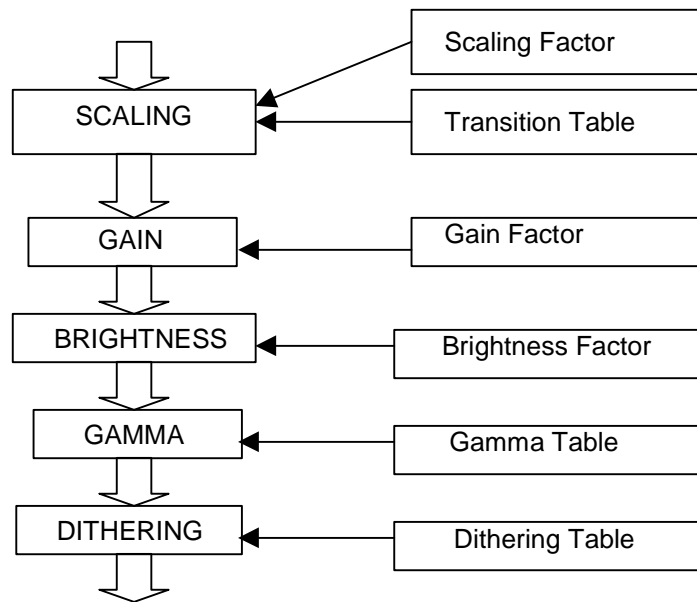


Fig. 3.2.1 Video Processor Block Diagram

3.2.1 Scaling

MTL003 provides scaling function ranging from 1/32 to 32 for both up and down scaling, and for both horizontal and vertical processing. Note that the up and down scaling cannot operate in the same time, because they share the same line buffers.

For scaling up, both horizontal and vertical processing, MTL003 provides four methods:

- ⌘ **Pass Mode:** Image will be passed through without considering any scaling factor.
- ⌘ **Duplicate Mode:** Image will be scaled up/down based on scaling factor. Every point of output image comes from the input. In this method, Output image will have the good contrast but may be non-uniformed.
- ⌘ **Bilinear Mode:** Image will be scaled up/down based on scaling factor. Every point of output image data will be filtered by bilinear filter. In this method, output image will have the good scaling quality but may be blurred.
- ⌘ **Interpolation Table Mode:** Image will be scaled up/down based on scaling factor. Every point of output image data will be filtered by the user defined filter.

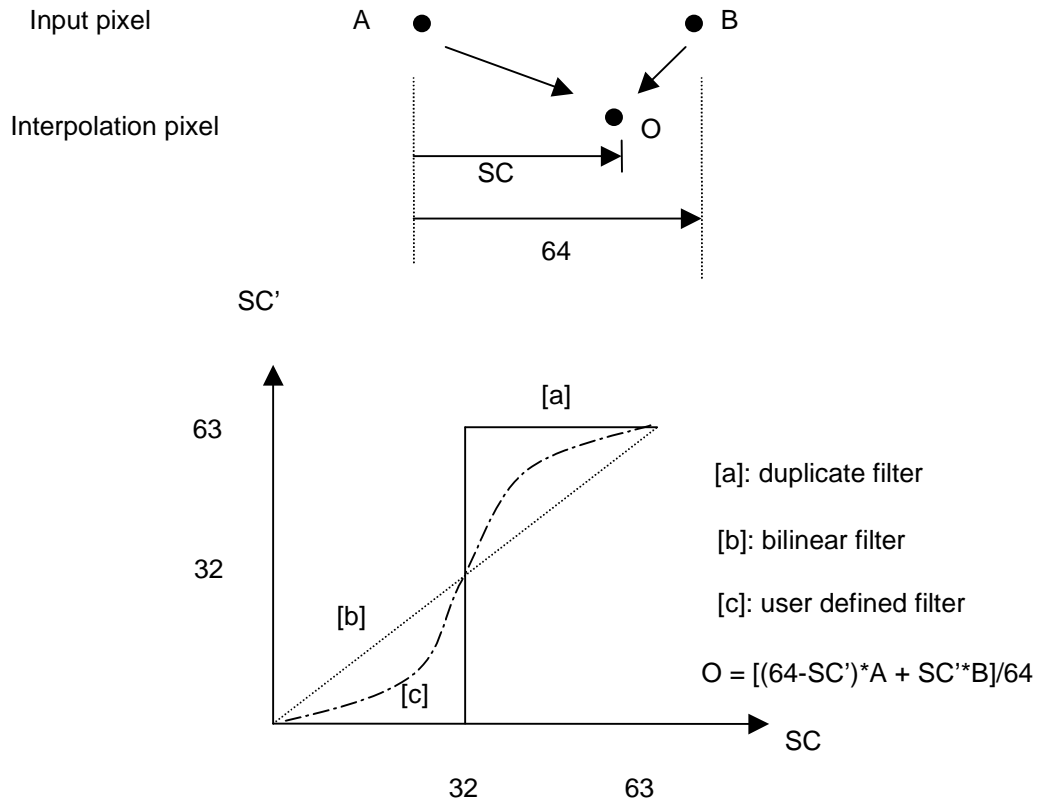


Fig. 3.2.2 Scaling filter

Note: For scaling down, for both horizontal and vertical processing, MTL003 provides three methods: Pass mode, Duplicate mode, and Bilinear mode.

3.2.2 Gain/Brightness Control

MTL003 provides Gain and Brightness control to adjust the contrast and brightness of output color by programming the gain and brightness coefficients. This adjustment is applied to RGB colors individually. Auto-white balance can be achieved by using this function.

3.2.3 Gamma Correction

Gamma Correction is used to compensate the non-linearity of LCD display panel. MTL003 contains an 8/10-bit Gamma table to fix this phenomenon. The 10-bit Gamma Table performs a better output quality, and is commonly used together with dithering function. A traditional 8-bit Gamma correction table can also be used.

3.2.4 Color Dithering

MTL003 supports true color (8 bits per color) or high color (6 bits per color) display. In the latter case, users can turn on dithering function to avoid artificial contour due to truncation. The dithering function works in two modes:

- ⌘ **Static dithering:** Dithering coefficient is fixed.
- ⌘ **Temporal dithering:** Dithering coefficient is time dependent.



3.3 Output Processor

General Description

Output processor provides the interface for both LCD panel and OSD controller. MTL003 can work for frame-buffer or non-frame-buffer mode. When in frame-buffer mode, there is no restriction between the timing of input and output. When in non-frame-buffer mode, output frame rate must be equal to input frame rate and output display time must be equal to input display time due to the absence of frame buffer. Some features based on using the frame buffer do not work in non-frame-buffer mode, for example the screen write, static mode in de-interlace etc.

3.3.1 Display Timing Generation

There are three display timing modes:

- ̂ **Frame-buffer Mode:** is used for frame rate conversion. External frame buffer is needed.
- ̂ **Non-frame-buffer Mode:** performs a low cost version of solution where the external frame buffer is not needed. This mode is used in the condition that output frame rate is equal to input frame; some features are disabled in this mode.
- ̂ **Frame SYNC Mode:** is used for video input. In this mode, output frame is synchronized to input frame, gives the moving picture a smooth change.

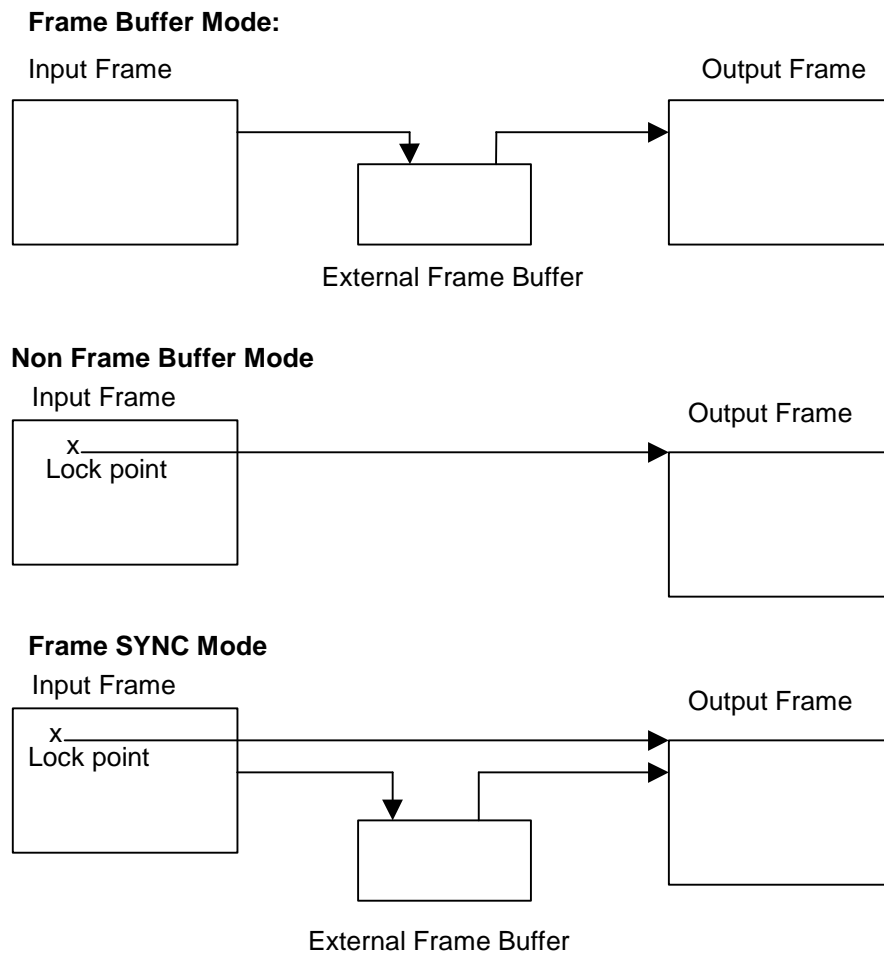


Fig. 3.2.3 Display Timing modes



3.3.2 OSD Overlay

MTL003 allows the integration of overlay data with the scaled output pixel stream. It provides a fully compatible OSD interface. Individual OSD clock, OSD HSYNC and OSD VSYNC are sent to external OSD device. MTL003 receives OSD Enable, OSD Red, OSD Green, OSD Blue, and OSD Intensity from external OSD device.

3.3.3 RGB Output Format

MTL003 output interface consists of two pixel ports, each containing Red, Green, and Blue color information with a resolution of 6/8 bits per color. These two ports are PORT1 and PORT2 respectively. The control signals for output port are the display horizontal sync signal (DHSYNC), the display vertical sync signal (DVSYNC) and the display data enable signal (DDEN).

All the signals mentioned above are synchronous to the output clock. The output timing relative to the active edge of the output clock is programmable.

There are two RGB output formats:

Single Pixel Mode

Is designed to support TFT panels with single pixel input. Only PORT1 is active. The frequency of DCLK1 is equal to the internal display clock.

Dual Pixel Mode

Is designed to support TFT panels with dual pixel input. PORT1 and PORT2 are used. The first pixel is at PORT1, and the second at PORT2.

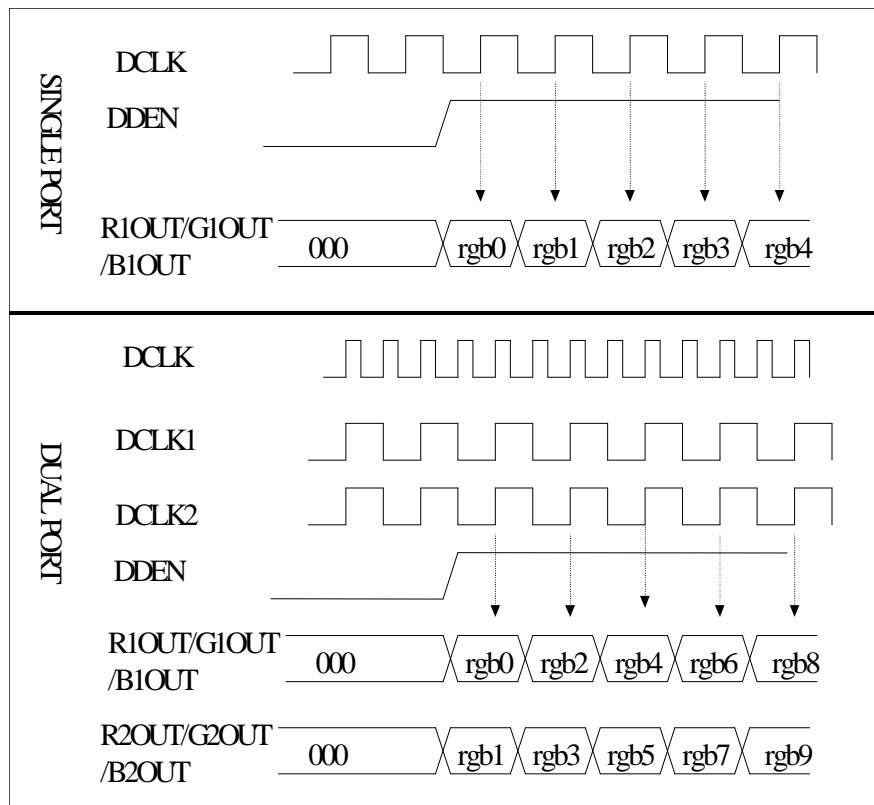


Fig. 3.2.4 Display Data Timing



3.4 Memory Interface

General Description

In frame buffer mode, the MTL003 connects to the external frame buffers by means of memory interface. The external frame memory can be made for 1MF 16bits SDRAM, 256KF 32bits or 512KF 32bits SGRAM devices. Due to different applications such as VGA, SVGA, XGA as well as SXGA, the image resolution of input and output will be limited resulting from the bandwidth of memory interface. Two configurations with 24, 32 and 48 bits bus modes will be supported to resolve the bandwidth constraint in most of applications. The clock for external frame memory devices can be provided from the internal PLL circuit or the external clock applied to pin EXTMCLK and its frequency can be up to 118 MHz. The MTL003 also supplies a simple and complete memory self-testing mechanism for SDRAM and SGRAM, which can be used to detect memory cell status and to check connection in memory interface.

3.4.1 SDRAM Configuration

In current applications, the most popular organization of SDRAM is 1MF 16bits. To achieve the desired bandwidth in memory interface, 2 or 3 devices have to be constructed in parallel. The memory clock range is from 50Mhz to 118Mhz by tuning the appropriate parameters for the internal PLL circuit. In two devices configuration, the 24 and 32 bits bus modes are supported. By these modes, the maximum input image resolution can be supported up to 1024F 768 @ 60Hz and 1024F 768 @ 85Hz respectively. The 48 bits bus mode in 3 devices will provide the maximum input image resolution up to 1280F 1024 @ 75Hz. Table 3.4.1 gives the configuration for different input and output image format. Figure 3.4.1 shows the connection between the MTL003 and SDRAM devices in 2 configurations.

Unit: device

| Output Resolution Input Resolution | SVGA | XGA | SXGA |
|---------------------------------------|------|-----|------|
| YUV | 2 | 2 | 2 |
| VGA (640F 480) | 2 | 2 | 2 |
| SVGA (800F 600) | 2 | 2 | 2 |
| XGA (1024F 768) | 2 | 2 | 2 |
| SXGA (1280F 1024) | 3 | 3 | 3 |

Table 3.4.1 SDRAM configuration in different input and output modes

3.4.2 SGRAM Configuration

The SGRAM devices in 256KF 32bits and 512KF 32bits constructions are usually used to feature the wide data bus for high speed applications. In case of SGRAM usage, the 32 bits data bus of each device is divided into 2 parts to store input image data. The memory clock is able to be set the desired range as SDRAM case as well. In two devices(512KF 32bits) configuration, the 24 and 32 bits bus modes are supported. By these modes, the maximum input image resolution can be supported up to 1024F 768 @ 60Hz and 1024F 768 @ 85Hz respectively. The 48 bits bus mode in 3 devices(512KF 32bits) will provide the maximum input image resolution up to 1280F 1024 @ 75Hz. Table 3.4.2 provides the configuration for different input and output image format. Figure 3.4.2 and 3.4.3 show the connection between the MTL003 and SGRAM devices in 2 configurations by 256KF 32bits and 512KF 32bits constructions respectively..

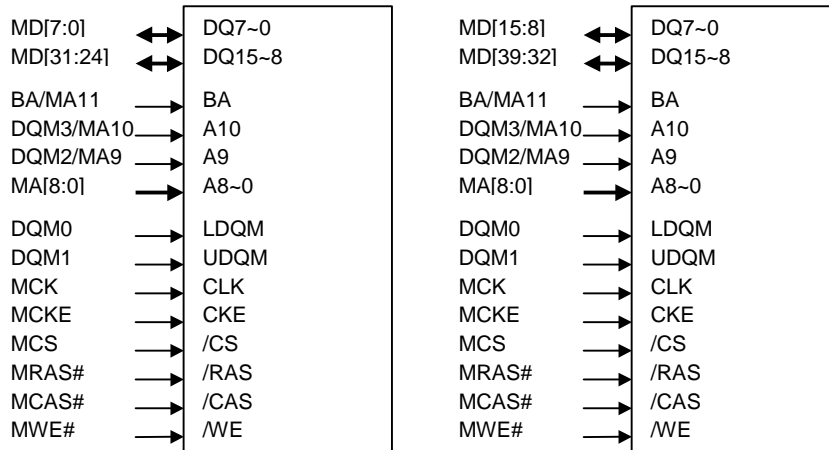
Unit: device

| Output Resolution Input Resolution | SVGA | XGA | SXGA |
|--|-------|-------|-------|
| YUV | 2 | 2 | 2 |
| VGA (640F 480) | 2 | 2 | 2 |
| SVGA (800F 600) | 2 | 2 | 2 |
| XGA (1024F 768) (512Kx32bits / 256Kx32bits) | 2 / 3 | 2 / 3 | 2 / 3 |
| SXGA (1280F 1024) (512KF 32bits only) | 3 | 3 | 3 |

Table 3.4.2 SGRAM configurations in different input and output modes



SDRAM(1MF 16bits) F 2



SDRAM(1MF 16bits) F 3

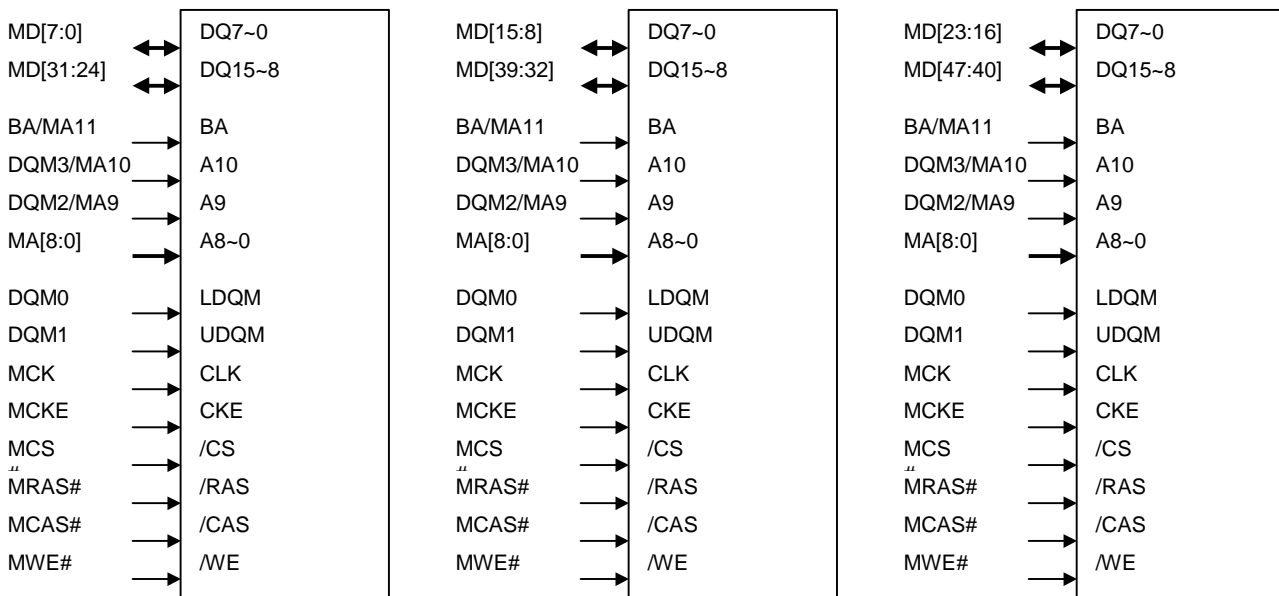
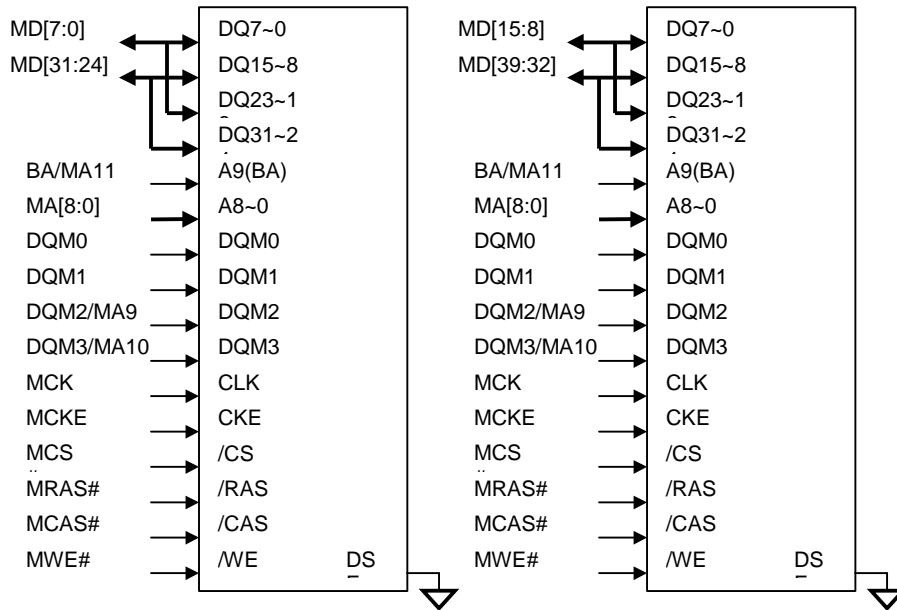


Fig. 3.4.1 The interface between MTL003 and 1Mx16 bits SDRAM



SGRAM(128KF 32bitsF 2) F 2



SGRAM(128KF 32bitsF 2) F 3

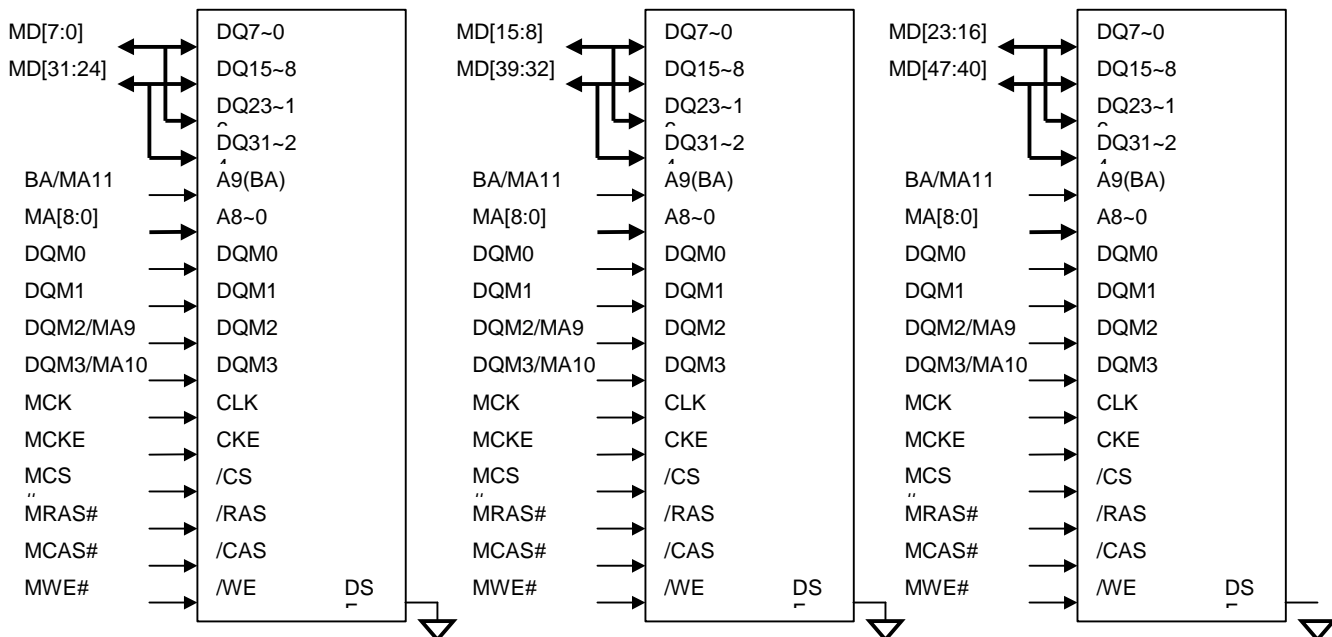
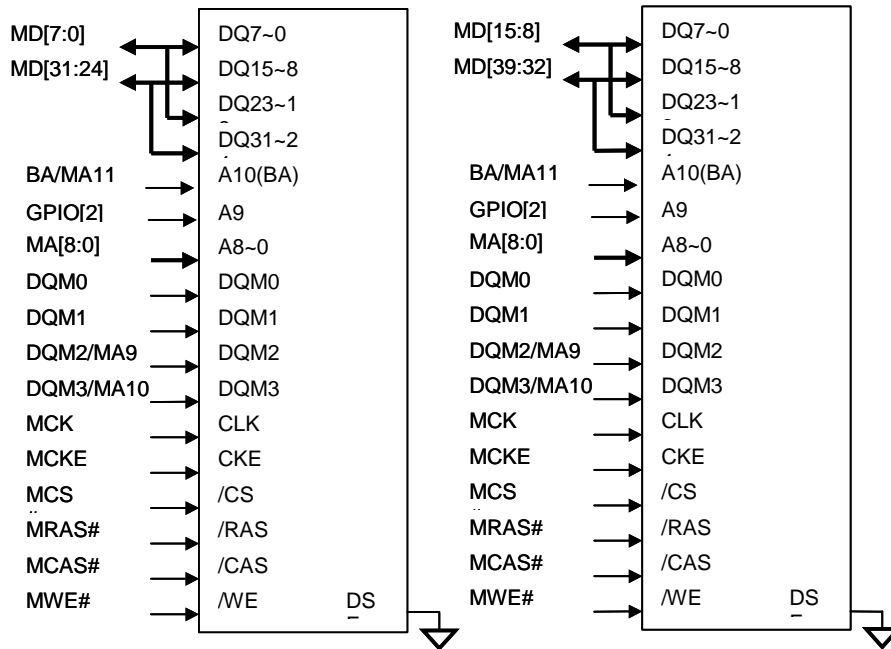


Fig. 3.4.2 The interface between MTL003 and 256Kx32 bits SGRAM



SGRAM(256KF 32bitsF 2) F 2



SGRAM(256KF 32bitsF 2) F 3

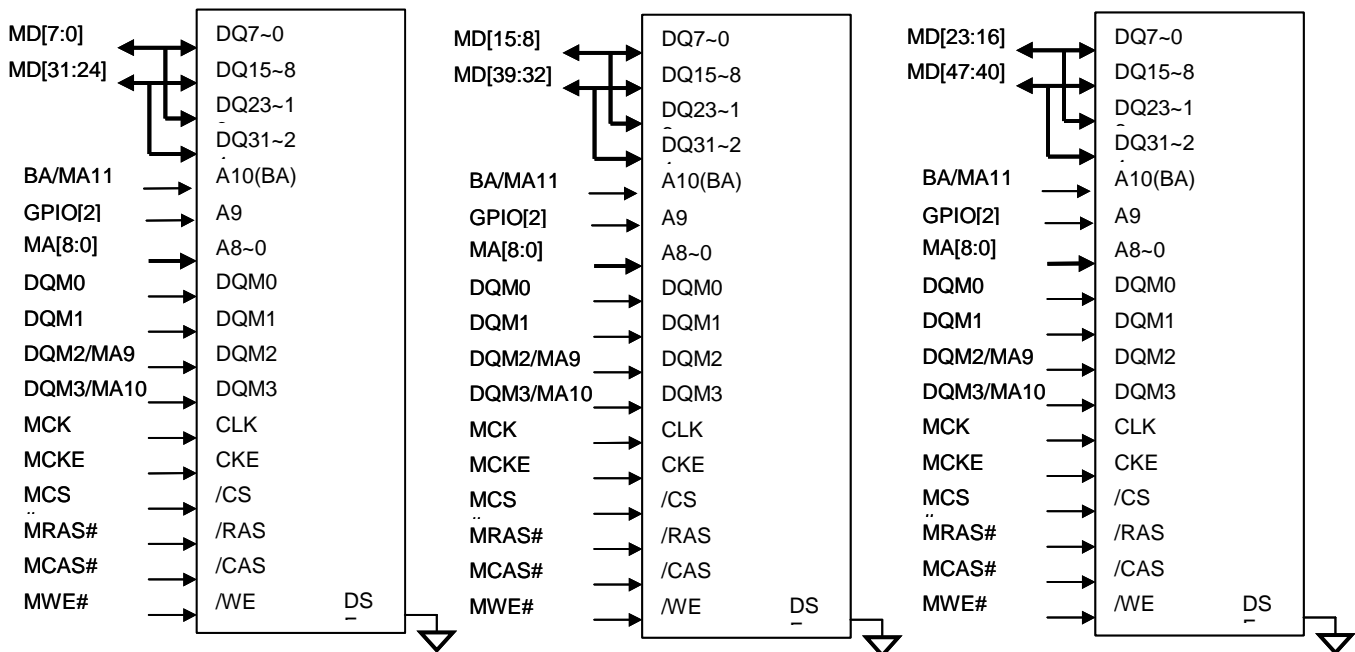


Fig. 3.4.3 The interface between MTL003 and 512Kx32 bits SGRAM



3.5 Host Interface

General Description

The primary function of Host Interface is to provide the interface between MTL003 and external CPU by 2-wire I²C Bus or Direct Bus selected by the input pin BUSSEL. It can generate all the I/O decoded control timing to control all the registers in MTL003. The other function is Screen Write, which allows users to clear frame buffer, and display output as well.

3.5.1 I²C Serial Bus

The I²C serial interface use 2 wires, SCK (clock) and SDA(data I/O). The SCK is used as the sampling clock and SDA is a bi-directional signal for the data. The communication must be started with a valid START condition, concluded with STOP condition and acknowledged by ACK condition by the receiver.

The I²C bus device address of MTL003 is 0111010x.

- AD[0] SCK, serial bus clock.
- AD[1] SDA, bi-directional serial bus data.

The START condition means a HIGH to LOW transition of SDA when SCK is high, the STOP condition means a LOW to HIGH transition of SDA when SCK is high. Data of SDA only changes when SCK is low. Ref. Fig.3.5.1.

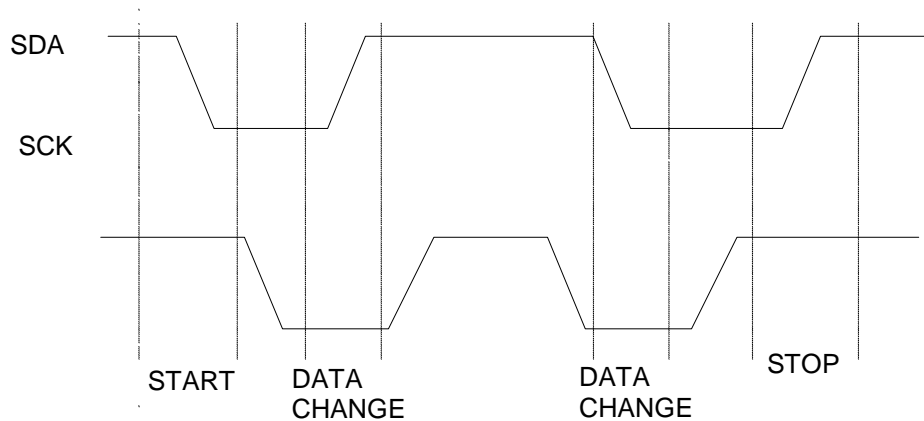


Fig. 3.5.1 START, STOP ,and DATA definition

The I²C interface supports Random Write, Sequential Write, Current Address Read, Random Read and Sequential Read operations.

Å Random Write

For Random Write operation, it contains the slave address with R/W bit set to 0 and the word address which is comprised of 8 bits that provides the access to any one of the 256 bytes in the selected memory range. Upon receipt of the word address, MTL003 responds with an Acknowledge and waits for the next eight bits of data again, responding with an Acknowledge, and then the master generates a stop condition. Ref. Fig.3.5.2.

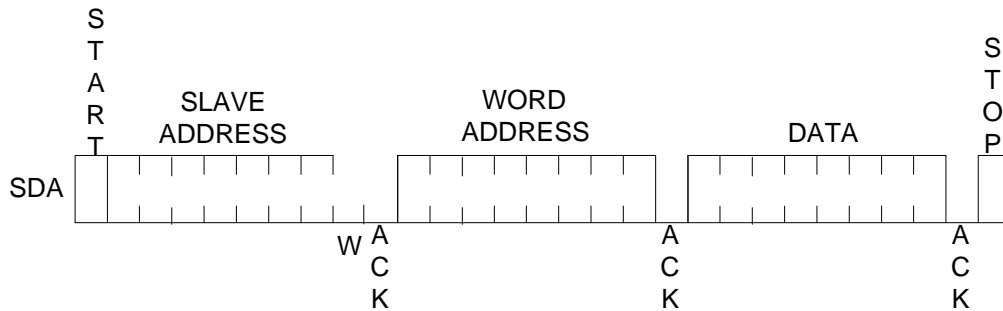


Fig. 3.5.2 Random Write

Sequential Write

The initial step of Sequential Write is the same as Random Write, after the receipt of each word data, MTL003 will respond with an Acknowledge and then internal address counter will increment by one for next data write. If the master stops writing data, it will generate stop condition. Ref. Fig. 3.5.3.

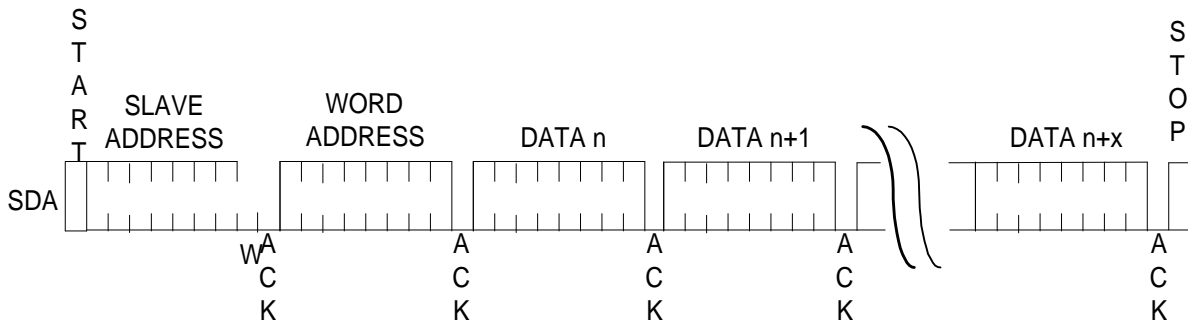


Fig. 3.5.3 Sequential Write

Current Address Read

MTL003 contains an address counter which maintains the last access address incremented by one. If the last access address is n, the read data should access from address n+1. Upon receipt of the slave address with R/W bit set to 1, MTL003 generates an Acknowledge and transmits the eight bits data. After receiving data the master will generate a stop condition instead of an Acknowledge. Ref. Fig. 3.5.4.

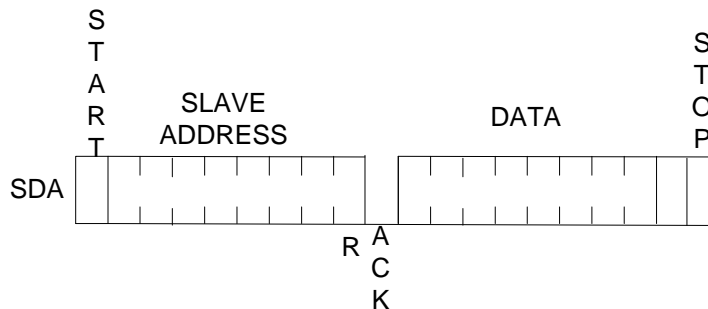
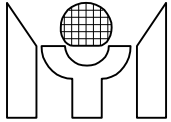


Fig. 3.5.4 Current Address Read



Random Read

The operation of Random Read allows access to any address. Before the reading data operation, it must issue a “dummy write” operation — the master issues the start condition, slave address and then the word address it is to read. After the word address acknowledge, the master generating a start condition again and slave address with R/W bit is set to 1. MTL003 then transmits the 8 bits of data. Upon the completion of receiving data, the master will generate a stop condition instead of an Acknowledge. Ref. Fig 3.5.5.

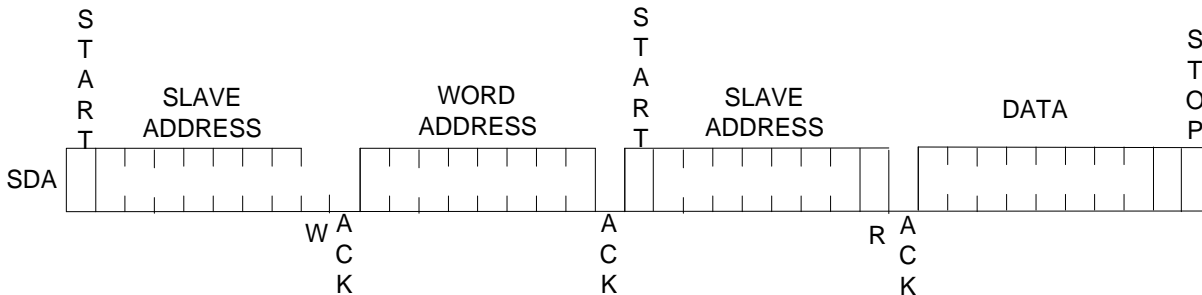


Fig. 3.5.5 Random Read

Sequential Read

The initial step can be as either Current Address Read or Random Read. The first read data is transmitted in the same manner as other read methods. However, the master generates an Acknowledge indicating that it requires more data to read. MTL003 continues to output data for each Acknowledge received. The output data is sequential and the internal address counter increments by one for next read data. Ref. Fig. 3.5.6.

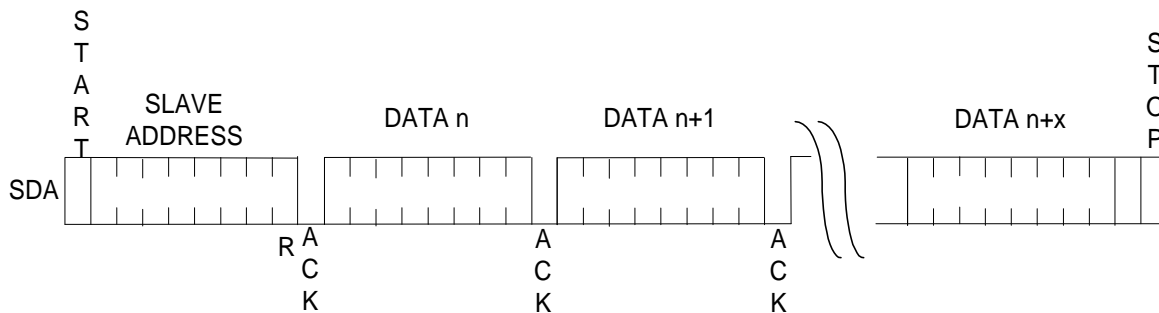


Fig. 3.5.6 Sequential Read

3.5.2 8-bit Direct Bus

The Direct Bus use AD[7:0], HWR#, HRD#, ALE, HCS# as the interface with host. ALE is used to latch read or write address from AD[7:0] and HRD#, HWR# to access data. Ref. Fig. 3.5.7.

- AD[7:0] Address and data multiplex bus.
- HRD# CPU read data strobe, Active Low.
- HWR# CPU write data strobe, Active Low.
- ALE ALE =1 latch read or write address, ALE=0 represents I/O data.
- HCS# Enable signal for CPU access, Active Low.

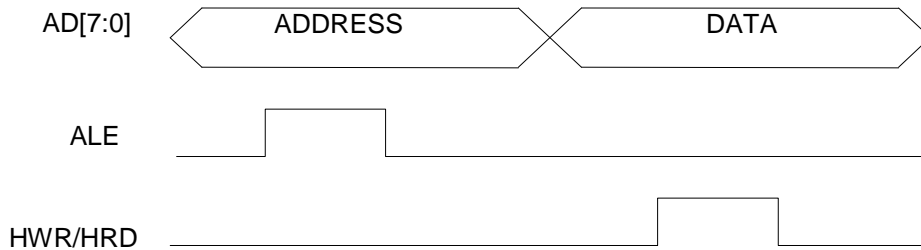


Fig. 3.5.7 Direct Bus Timing

3.5.3 Interrupt

MTL003 supports one interrupt output signal (IRQ) which can be programmed to provide SYNC related or function status related interrupts to the system. Upon receiving the interrupt request, Firmware needs to firstly check the interrupt event by reading the Interrupt Flag Control registers (Reg. E8h and E9h) to decide what events are happening. After the operation is completed, Firmware needs to clear interrupt status by writing the same registers Reg. E8h and E9h. Furthermore, by using the Interrupt Flag Enable registers (Reg. EAh and EBh), each interrupt event can be masked.

3.5.4 Screen Write

Screen Write function can be used to clear frame buffer memory and display output by a fixed value defined in Reg. C6h, C7h, C8h.

3.5.5 Bi-directional GPIO

MTL003 supports eight General Purpose Input and Output (GPIO) pins GPIO[7:0] on chip. The GPIO[5:0] pins are bi-directional GPIO pins, and the GPIO[7:6] pins are output only GPIO pins. There are two functions for GPIO[7:6] pins. One is to set them as output only GPIO pins, and the other is to set them as Composite decoded VSYNC/HSYNC for A/D converters in VGA input path. The data and I/O direction of GPIO[7:0] pins are controlled by Reg. F4h and F5h respectively, and each bit in the register is mapped to GPIO[7:0] correspondingly. The following description is the process to control GPIO[0] and GPIO[6] in detail, and the control processes of GPIO[4:1] and GPIO[7] also follows in the same manner.

Ā Bi-directional GPIO control process

- ” Setting Reg. F5h/D0 = 0 or 1 to assign GPIO[0] as output or input.
- ” Writing data to Reg. F4h/D0 when GPIO[0] is assigned to output status, otherwise reading data from Reg. F4h/D0 when GPIO[0] is input.

Ā Output only GPIO control process

- ” Setting Reg. F5h/D6 = 0 or 1 to assign GPIO[6] as output or tri-state.
- ” Setting Reg. F6h/D0 = 0 to select output source from Reg. F4h/D6 or setting it as 1 to make GPIO[6] pin to output ADHS which is HSYNC signal decoded from VGA input Composite signal by the MTL003.
- ” Writing data to F4h/D6 when GPIO[6] is assigned to output only GPIO pin, that is, F6h/D0 = 0 and F5h/D6 = 0. If F6h/D0 is set to 1, the GPIO[6] pin outputs ADHS for AD converters in VGA input path.

3.5.6 Update Register Contents

I/O write operation to some consecutive register set can have the “Double Buffer” effect by setting the Reg. C1h/D4. Written data is first stored in an intermediate bank of latches and then transferred to the active register set by setting Reg. C1h/D1-0.



3.6 On-Chip PLL

General Description

The MTL003 needs three clock sources to drive synchronous circuits on chip. These clocks are generated from the internal Phase Lock Loop (PLL) circuits with reference to the oscillator clock which is applied to pin XI and XO by an external quartz crystal at 14.31818 MHz. The first one is the same as to the oscillator clock at frequency (14.31818 MHz) to detect and measure graphic vertical and horizontal SYNC Frequency, Polarity as well as Presence. The second is memory clock to synchronize memory controller with the external frame buffers. The third is the display clock for display controller on chip and output signals to LCD panel.

3.6.1 Reference Clock

It is the counting basis of counter values in SYNC Processor such as VS and HS period count registers; that is, the read back values from these registers must multiply the period of this clock to estimate VS and HS frequency. Incorporating with polarity and frequency information of VS and HS, it can show the input graphic image mode and pixel clock frequency.

3.6.2 Memory Clock

This clock is the synchronous clock for the external frame buffer. To accomplish the different DRAM types, configuration and bandwidth needed for various applications, the memory clock can be set from 50 MHz to 118 MHz by means of adjusting a set of appropriate values for M, N and R. The formula for calculating the desired frequency of the memory clock is as follows:

$$f_{mclk} = f_{osc} F (M+2)/(N+2) F 1/R$$

Where

| | |
|------------|--------------------------------------|
| f_{mclk} | : the desired memory clock |
| f_{osc} | : oscillator clock with 14.31818 MHz |
| M | : post-divider ratio |
| N | : pre-divider ratio |
| R | : optional divider ratio |

3.6.3 Display Clock

This clock is the synchronous clock for LCD panel. According to the LCD panel resolution of applications, the display clock range is from 50 MHz to 160 MHz by means of choosing a set of appropriate values for M, N as well as R. The computing formula is exactly the same as for the memory clock.



4. REGISTER DESCRIPTION

INPUT CONTROL REGISTERS

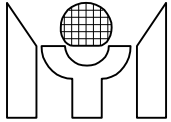
| Address | Mode | Registers | Reset value |
|---------|------|--|-------------|
| 00h | R/W | Input Image Vertical Active Line Start - Low | 00h |
| 01h | R/W | Input Image Vertical Active Line Start - High | 00h |
| 02h | R/W | Input Image Vertical Active Lines - Low | 00h |
| 03h | R/W | Input Image Vertical Active Lines - High | 00h |
| 04h | R/W | Input Image Horizontal Active Pixel Start - Low | 00h |
| 05h | R/W | Input Image Horizontal Active Pixel Start - High | 00h |
| 06h | R/W | Input Image Horizontal Active Pixels - Low | 00h |
| 07h | R/W | Input Image Horizontal Active Pixels - High | 00h |
| 10h | R/W | Input Image Control Register 0 | 00h |
| 11h | R/W | Input Image Control Register 1 | 00h |
| 12h | R/W | Input Image Control Register 2 | 00h |
| 13h | R/W | Input Image Control Register 3 | 00h |
| 14h | R/W | Input Image Control Register 4 | 00h |
| 15h | R/W | Input Image Control Register 5 | 00h |
| 16h | R/W | Input Image Control Register 6 | 00h |
| 1Ah | R/W | Input Delay Control 2 | 00h |
| 1Ch | R/W | HS1 Sample Window Forward Extend | 00h |
| 1Dh | R/W | HS1 Sample Window Backward Extend | 00h |
| 1Fh | RO | Input Image Status Register | - |
| 20h | R/W | Input Image Back Porch Guard Band | 00h |
| 21h | R/W | Input Image Front Porch Guard Band | 00h |

FRAME SYNC REGISTERS

| Address | Mode | Registers | Reset value |
|---------|------|---|-------------|
| 28h | R/W | Frame Sync Control | 00h |
| 2Ch | R/W | Input Image Vertical Lock Position - Low | 00h |
| 2Dh | R/W | Input Image Vertical Lock Position - High | 00h |
| 2Eh | R/W | Input Image Horizontal Lock Position - Low | 00h |
| 2Fh | R/W | Input Image Horizontal Lock Position - High | 00h |

AUTO CALIBRATION REGISTERS

| Address | Mode | Registers | Reset value |
|---------|------|---------------------------------------|-------------|
| 30h | R/W | Auto Calibration Control 0 | 80h |
| 31h | R/W | Auto Calibration Control 1 | 00h |
| 34h | RO | Auto Calibration RED Value - Byte 0 | - |
| 35h | RO | Auto Calibration RED Value - Byte 1 | - |
| 36h | RO | Auto Calibration RED Value - Byte 2 | - |
| 37h | RO | Auto Calibration RED Value - Byte 3 | - |
| 38h | RO | Auto Calibration GREEN Value - Byte 0 | - |
| 39h | RO | Auto Calibration GREEN Value - Byte 1 | - |
| 3Ah | RO | Auto Calibration GREEN Value - Byte 2 | - |
| 3Bh | RO | Auto Calibration GREEN Value - Byte 3 | - |
| 3Ch | RO | Auto Calibration BLUE Value - Byte 0 | - |
| 3Dh | RO | Auto Calibration BLUE Value - Byte 1 | - |
| 3Eh | RO | Auto Calibration BLUE Value - Byte 2 | - |
| 3Fh | RO | Auto Calibration BLUE Value - Byte 3 | - |



| | | | |
|-----|-----|--|-----|
| 40h | R/W | Pixel Grab V Reference Position - Low | 00h |
| 41h | R/W | Pixel Grab V Reference Position - High | 00h |
| 42h | R/W | Pixel Grab H Reference Position - Low | 00h |
| 43h | R/W | Pixel Grab H Reference Position - High | 00h |
| 44h | R/W | Histogram Reference Color - RED | 00h |
| 45h | R/W | Histogram Reference Color - GREEN | 00h |
| 46h | R/W | Histogram Reference Color - BLUE | 00h |

SYNC PROCESSOR REGISTERS

| Address | Mode | Registers | Reset value |
|---------|------|---|-------------|
| 48h | R/W | SYNC Processor Control | 00h |
| 49h | R/W | Auto Position Control | 00h |
| 4Ah | R/W | Auto Position Reference Color - RED | 00h |
| 4Bh | R/W | Auto Position Reference Color - GREEN | 00h |
| 4Ch | R/W | Auto Position Reference Color - BLUE | 00h |
| 4Eh | R/W | Clamp Pulse Control 0 | 00h |
| 4Fh | R/W | Clamp Pulse Control 1 | 00h |
| 50h | RO | Input VS Period Count by REFCLK - Low | - |
| 51h | RO | Input VS Period Count by REFCLK - High | - |
| 52h | RO | Input V Back Porch Count by Input HS - Low | - |
| 53h | RO | Input V Back Porch Count by Input HS - High | - |
| 54h | RO | Input V Active Lines Count by Input HS - Low | - |
| 55h | RO | Input V Active Lines Count by Input HS - High | - |
| 56h | RO | Input V Total Lines Count by Input HS - Low | - |
| 57h | RO | Input V Total Lines Count by Input HS - High | - |
| 58h | RO | Input HS Period Count by REFCLK - Low | - |
| 59h | RO | Input HS Period Count by REFCLK - High | - |
| 5Ah | RO | Input H Back Porch Count by Input Pixel Clock - Low | - |
| 5Bh | RO | Input H Back Porch Count by Input Pixel Clock - High | - |
| 5Ch | RO | Input H Active Pixels Count by Input Pixel Clock - Low | - |
| 5Dh | RO | Input H Active Pixels Count by Input Pixel Clock - High | - |
| 5Eh | RO | Input H Total Pixels Count by Input Pixel Clock - Low | - |
| 5Fh | RO | Input H Total Pixels Count by Input Pixel Clock - High | - |

DISPLAY CONTROL REGISTERS

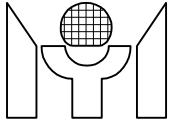
| Address | Mode | Registers | Reset value |
|---------|------|--------------------------------------|-------------|
| 60h | R/W | Display Vertical Total - Low | 00h |
| 61h | R/W | Display Vertical Total - High | 00h |
| 62h | R/W | Display Vertical SYNC End- Low | 00h |
| 63h | R/W | Display Vertical SYNC End - High | 00h |
| 64h | R/W | Display Vertical Active Start - Low | 00h |
| 65h | R/W | Display Vertical Active Start - High | 00h |
| 66h | R/W | Display Vertical Active End - Low | 00h |
| 67h | R/W | Display Vertical Active End - High | 00h |
| 68h | R/W | Display Vertical Border Start - Low | 00h |
| 69h | R/W | Display Vertical Border Start - High | 00h |
| 6Ah | R/W | Display Vertical Border End - Low | 00h |
| 6Bh | R/W | Display Vertical Border End - High | 00h |
| 70h | R/W | Display Horizontal Total - Low | 00h |



| | | | |
|------|-----|---|-----|
| 71h | R/W | Display Horizontal Total - High | 00h |
| 72h | R/W | Display Horizontal SYNC End - Low | 00h |
| 73h | R/W | Display Horizontal SYNC End - High | 00h |
| 74h | R/W | Display Horizontal Active Start - Low | 00h |
| 75h | R/W | Display Horizontal Active Start - High | 00h |
| 76h | R/W | Display Horizontal Active End - Low | 00h |
| 77h | R/W | Display Horizontal Active End - High | 00h |
| 78h | R/W | Display Horizontal Border Start - Low | 00h |
| 79h | R/W | Display Horizontal Border Start - High | 00h |
| 7Ah | R/W | Display Horizontal Border End - Low | 00h |
| 7Bh | R/W | Display Horizontal Border End - High | 00h |
| | | | |
| 88h | R/W | Output Image Control Register 0 | 00h |
| 89h | R/W | Output Image Control Register 1 | 00h |
| 8Ah | R/W | Output Image Control Register 2 | 00h |
| | | | |
| 90h | R/W | Color Gain Control - RED | 80h |
| 91h | R/W | Color Gain Control - GREEN | 80h |
| 92h | R/W | Color Gain Control - BLUE | 80h |
| 93h | R/W | Brightness Control - RED | 00h |
| 94h | R/W | Brightness Control - GREEN | 00h |
| 95h | R/W | Brightness Control - BLUE | 00h |
| 96h | R/W | Border Window Color - RED | 00h |
| 97h | R/W | Border Window Color - GREEN | 00h |
| 98h | R/W | Border Window Color - BLUE | 00h |
| 9Eh | R/W | Dithering Table Data Port | - |
| 9Fh | R/W | Gamma Table Data Port | - |
| | | | |
| A0h | R/W | OSD Control Register 0 | 08h |
| A1h | R/W | OSD Control Register 1 | 00h |
| A2h | R/W | OSD Control Register 2 | 00h |
| A4h | R/W | Output Invert Control | 00h |
| A5h | R/W | Output Tri-State Control | 00h |
| A6h | R/W | Output Clocks Delay Adjustment | 00h |
| A7h | R/W | Output Clocks Duty Cycle Adjustment | 00h |
| A9h | R/W | Output Miscellaneous Control | 00h |
| AAh | R/W | Output Vertical Line Number - Low | FFh |
| ABh | R/W | Output Vertical Line Number - High | 02h |
| ACh | RO | Output Horizontal Total Pixel Number – Low | - |
| ADh | RO | Output Horizontal Total Pixel Number – High | - |
| A Eh | RO | Output Horizontal Total Residue Number – Low | - |
| AFh | RO | Output Horizontal Total Residue Number - High | - |

ZOOM CONTROL REGISTERS

| Address | Mode | Registers | Reset value |
|---------|------|------------------------------------|-------------|
| B0h | R/W | Zoom Control Register 0 | 00h |
| B1h | R/W | Zoom Control Register 1 | 00h |
| | | | |
| B2h | R/W | Zoom Vertical Scale Down Integer | 00h |
| B3h | R/W | Zoom Horizontal Scale Down Integer | 00h |
| B4h | R/W | Zoom Vertical Scale Ratio - Low | 00h |
| B5h | R/W | Zoom Vertical Scale Ratio - High | 00h |
| B6h | R/W | Zoom Horizontal Scale Ratio - Low | 00h |
| B7h | R/W | Zoom Horizontal Scale Ratio - High | 00h |



| | | | |
|-----|-----|-------------------------------|---|
| BFh | R/W | Interpolation Table Data Port | - |
|-----|-----|-------------------------------|---|

HOST CONTROL REGISTERS

| Address | Mode | Registers | Reset value |
|---------|------|--------------------------------------|-------------|
| C0h | R/W | Host Control Register 0 | 00h |
| C1h | R/W | Host Control Register 1 | 00h |
| | | | |
| C4h | R/W | Host Screen Write Line Length - Low | 00h |
| C5h | R/W | Host Screen Write Line Length - High | 03h |
| C6h | R/W | Host Fill Color - RED | 00h |
| C7h | R/W | Host Fill Color - GREEN | 00h |
| C8h | R/W | Host Fill Color - BLUE | 00h |
| | | | |
| CBh | RO | Host Access Mode Status | - |

MEMORY CONTROL REGISTERS

| Address | Mode | Registers | Reset value |
|---------|------|---|-------------|
| D0h | R/W | Memory Type Control | 00h |
| D2h | R/W | Memory Self Test Control | 00h |
| D4h | R/W | Memory Line Offset - Low | 00h |
| D5h | R/W | Memory Line Offset - High | 04h |
| | | | |
| DBh | RO | Memory Self-Test Compare Error Address – Low | - |
| DCh | RO | Memory Self-Test Compare Error Address – Middle | - |
| DDh | RO | Memory Self-Test Compare Error Address – High | - |

CLOCK CONTROL REGISTERS

| Address | Mode | Registers | Reset value |
|---------|------|-----------------------------------|-------------|
| E0h | R/W | Clock Control Register | 00h |
| | | | |
| E1h | WO | Clock Synthesizer Value Load | - |
| E2h | R/W | Display Clock Synthesizer N Value | 0Bh |
| E3h | R/W | Display Clock Synthesizer M Value | 32h |
| E4h | R/W | Memory Clock Synthesizer N Value | 0Bh |
| E5h | R/W | Memory Clock Synthesizer M Value | 32h |
| E6h | R/W | Clock Synthesizer R Value | 00h |

INTERRUPT CONTROL REGISTERS

| Address | Mode | Registers | Reset value |
|---------|------|---------------------------------------|-------------|
| E8h | R/W | SYNC Interrupt Flag Control | 00h |
| E9h | R/W | General Interrupt Flag Control | 00h |
| EAh | R/W | SYNC Interrupt Enable | 00h |
| EBh | R/W | General Interrupt Enable | 00h |
| ECh | R/W | HS Frequency Change interrupt Compare | 00h |

MISCELLANEOUS REGISTERS

| Address | Mode | Registers | Reset value |
|---------|------|--------------------------|-------------|
| F1h | R/W | Power Management Control | 00h |
| F4h | R/W | GPIO Control Register | 00h |
| F5h | R/W | GPIO Direction Control | 00h |
| F6h | R/W | GPIO Misc Control | 00h |

Input Image Vertical Active Line Start - Low (Address 00h) (R/W)

It defines the low byte of the start position of the Vertical Active Window.



D7-0 IV_ACT_START[7:0]

Input Image Vertical Active Line Start - High (Address 01h) (R/W)

It defines the high byte of the start position of the Vertical Active Window.

D7-3 Reserved

D2-0 IV_ACT_START[10:8]

Input Image Vertical Active Lines - Low (Address 02h) (R/W)

It defines the low byte of the number of active lines of the Vertical Active Window.

D7-0 IV_ACT_LEN[7:0]

Input Image Vertical Active Lines - High (Address 03h) (R/W)

It defines the high byte of the number of active lines of the Vertical Active Window.

D7-3 Reserved

D2-0 IV_ACT_LEN[10:8]

Input Image Horizontal Active Pixel Start - Low (Address 04h) (R/W)

It defines the low byte of the start position of the Horizontal Active Window.

D7-0 IH_ACT_START[7:0]

Input Image Horizontal Active Pixel Start - High (Address 05h) (R/W)

It defines the high byte of the start position of the Horizontal Active Window.

D7-3 Reserved

D2-0 IH_ACT_START[10:8]

Input Image Horizontal Active Pixels - Low (Address 06h) (R/W)

It defines the low byte of the number of active pixels of the Horizontal Active Window.

D7-0 IH_ACT_WIDTH[7:0]

Input Image Horizontal Active Pixels - High (Address 07h) (R/W)

It defines the high byte of the number of active pixels of the Horizontal Active Window.

D7-3 Reserved

D2-0 IH_ACT_WIDTH[10:8]

Input Image Control Register 0 (Address 10h) (R/W)

D7 Horizontal Sampling Point Reference
0: from Input HSYNC.



1: from Input HREF (only for Video Decoder).

| | |
|----|--|
| D6 | Input YCBCR Format 0: 4-2-2 1: 4-1-1 |
| D5 | Digital RGB 6 bit Mode 0: 8 bits 1: 6 bits |
| D4 | Digital RGB Mode Select 0: RGB Input from ADC 1: RGB Input from Panel Link |
| D3 | Input Image Format 0: RGB888 1: YCBCR |
| D2 | Input Clock Source 0: from Graphic PLL clock. 1: from Video Decoder clock. |
| D1 | Input Image Source 0: from Graphic source through ADC. 1: from Video source through Video Decoder like SAA7111A. |
| D0 | ADC Configuration 0: Double Pixel mode 1: Single Pixel mode |

Input Image Control Register 1 (Address 11h) (R/W)

| | |
|------|---|
| D7 | Reserved |
| D6-4 | De-interlace mode Select 000: All Fields write mode 001: Toggle Field write mode 010: Spatial Filtering write mode |
| D3 | Input YUV CCIR656 Format 0: Disable 1: Enable |
| D2-1 | Reserved |
| D0 | Still mode Enable 0: Live mode 1: Still mode |

Input Image Control Register 2 (Address 12h) (R/W)

| | |
|----|---|
| D7 | Input ODD Field Invert 0: Normal 1: Invert |
| D6 | External Input Interlace Select 0: Non-interlace |



1: Interlace

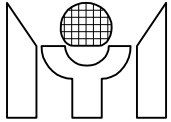
- D5 External Input VSYNC Polarity
0: Active Low
1: Active High
- D4 External Input HSYNC Polarity
0: Active Low
1: Active High
- D3 Input ODD Field Source
0: from Internal Detection
1: from External pin.
- D2 Input Interlace Source
0: from Internal detection
1: from Register setting (D6)
- D1 Input VSYNC Polarity Source
0: from Internal detection
1: from Register setting (D5)
- D0 Input HSYNC Polarity Source
0: from Internal detection
1: from Register setting (D4)

Input Image Control Register 3 (Address 13h) (R/W)

- D7 Active Position Area for Auto Position in TMDS
0: from Internal Detection
1: from External Data Enable (TDIE)
- D6-3 Reserved
- D2 Sync On Green Select
0: Select Normal HSYNC/ Composite Sync
1: Select Sync On Green
- D1 Input Vertical Timing based on VSYNC
0: Leading Edge
1: Trailing Edge
- D0 Input Horizontal Timing based on HSYNC
0: Leading Edge
1: Trailing Edge

Input Image Control Register 4 (Address 14h) (R/W)

- D7 Input ODD Field Detection Point
0: at the start of VSYNC pulse.
1: at the end of VSYNC pulse.
- D6 Input Image Port A, B Data and Clocks Swap
0: Normal
1: Swap
- D5 Reserved



D4 Input Image CBCR Order Swap
0: Normal
1: Swap

D3-0 Reserved

Input Image Control Register 5 (Address 15h) (R/W)

D7 Horizontal Pixel Valid Select
0: from Internal Programming
1: from External HREF/TDIE

D6-0 Reserved

Input Image Control Register 6 (Address 16h) (R/W)

D7-3 Reserved

D2 ADC HS Polarity Invert when D1=1
0: Active Low
1: Active High

D1 Raw HS path Enable
0: Disable
1: Enable

D0 Reserved

Input Delay Control 2 (Address 1Ah) (R/W)

D7-4 Input VSYNC Delay Adjustment
1111: 7 IDCLKs delay
1110: 6 IDCLKs delay
1101: 5 IDCLKs delay
1100: 4 IDCLKs delay
1011: 3 IDCLKs delay
1010: 2 IDCLKs delay
1001: 1 IDCLK delay
1000: Reserved
0111: 7ns gate delay
0110: 6ns gate delay
0101: 5ns gate delay
0100: 4ns gate delay
0011: 3ns gate delay
0010: 2ns gate delay
0001: 1ns gate delay
0000: No delay

D3-0 Input HSYNC Delay Adjustment
16 steps to change, each of them is 1ns delay/step.

Input HS Pulse Width Forward Extend (Address 1Ch) (R/W)

D7-0 Input HS Pulse Width Forward Extend by IDCLK
HS1FWEXT[7:0]: Used when Interlace First/Second Field Detection.



Input HS Pulse Width Backward Extend (Address 1Dh) (R/W)

D7-0 Input HS Pulse Width Backward Extend by IDCLK
HS1BWEXT[7:0]: Used when Interlace First/Second Field Detection.

Input Image Status Register (Address 1Fh) (RO)

D7 Display VSYNC Monitor
Show Display VSYNC signal directly.

D6 Input VSYNC Monitor
Show Input VSYNC signal directly.

D5 External Input Interlace Status
0: Non-interlace
1: Interlace

D4 Extracted CVSINC Present Status
0: Not Present
1: Present

D3 External Input VSYNC Present Status
0: Not Present
1: Present

D2 External Input HSYNC Present Status
0: Not Present
1: Present

D1 External Input VSYNC Polarity Status
0: Active Low
1: Active High

D0 External Input HSYNC Polarity Status
0: Active Low
1: Active High

Input Image Back Porch Guard Band (Address 20h) (R/W)

D7-0 Input Image Back Porch Guard Band by IDCLK
HBPGB[7:0]: Used in Auto Position detection to mask out unwanted data.

Input Image Front Porch Guard Band (Address 21h) (R/W)

D7-0 Input Image Front Porch Guard Band by IDCLK
HFPGB[7:0]: Used in Auto Position detection to mask out unwanted data.

Frame Sync Control 0 (Address 28h) (R/W)

D7-5 Reserved

D1 Frame Sync Select in Frame Buffer mode
0: Normal
1: Frame Sync

D0 Frame Buffer mode Select
0: Frame Buffer mode



1: Non Frame Buffer mode

Input Image Vertical Lock Position - Low (Address 2Ch) (R/W)

It defines the low byte of the number of input lines where Display image timing synchronizes the input image source.

D7-0 IPV_LOCK_POS[7:0]

Input Image Vertical Lock Position - High (Address 2Dh) (R/W)

It defines the high byte of the number of input lines where Display image timing synchronizes the input image source.

D7-3 Reserved

D2-0 IPV_LOCK_POS[10:8]

Input Image Horizontal Lock Position - Low (Address 2Eh) (R/W)

It defines the low byte of the number of input pixel clocks where Display image timing synchronizes the input image source.

D7-0 IPH_LOCK_POS[7:0]

Input Image Horizontal Lock Position - High (Address 2Fh) (R/W)

It defines the high byte of the number of input pixel clocks where Display image timing synchronizes the input image source.

D7-3 Reserved

D2-0 IPH_LOCK_POS[10:8]

Auto Calibration Control 0 (Address 30h) (R/W)

D7 Pixel Grab Ready Flag (**RO**)
0: Ready
1: Not Ready

D6 Pixel Grab Update Enable
0: Stop updating
1: Continue updating

D5 Threshold Select
Used in Histogram mode or MIN/MAX mode.
0: High bound / MAX
1: Low bound / MIN

D4 Phase Calibration Method Select
0: MYSON proprietary method
1: Difference Value method

D3-2 Auto Calibration Modes Select
The measured value is available one item at a time,
selected as shown:
00: Phase Calibration Mode



01: Histogram Mode
10: MIN/MAX Mode
11: Pixel Grab Mode

D1 Auto Calibration Burst Mode Enable
(except Pixel Grab Mode)
0: Single Mode
1: Burst Mode

D0 Auto Calibration Enable **(W)**
(except Pixel Grab Value)
0: Disable
1: Enable
Auto Calibration Ready Flag **(R)**
0: Ready
1: Not Ready

Auto Calibration Control 1 (Address 31h) (R/W)

D7-3 Reserved

D2-0 Mask LSBs of Input Image Select
It is used only for Phase Calibration to mask noise.
000: No Mask
001: Mask bit0
010: Mask bit0,1
011: Mask bit0,1,2
100: Mask bit0,1,2,3
101: Mask bit0,1,2,3,4
110: Mask bit0,1,2,3,4,5
111: Mask bit0,0,1,2,3,4,5,6

Auto Calibration RED Value - Byte 0 (Address 34h) (RO)

It states the byte 0 of the number of Phase Calibration RED value in one frame or the byte 0 of the number of Histogram Red value in one frame or the Pixel Grab RED value in one frame of Non_interlace mode or FIRST field of Interlace mode.

D7-0 CALVAL_R[7:0]

Auto Calibration RED Value - Byte 1 (Address 35h) (RO)

It states the byte 1 of the number of Phase Calibration RED value in one frame or the byte 1 of the number of Histogram Red value in one frame or the Pixel Grab GREEN value in one frame of Non_interlace mode or FIRST field of Interlace mode.

D7-0 CALVAL_R[15:8]

Auto Calibration RED Value - Byte 2 (Address 36h) (RO)

It states the byte 2 of the number of Phase Calibration RED value in one frame or the byte 2 of the number of Histogram Red value in one frame or the Pixel Grab BLUE value in one frame of Non_interlace mode or FIRST field of Interlace mode.

D7-0 CALVAL_R[23:16]

Auto Calibration RED Value - Byte 3 (Address 37h) (RO)



It states the byte 3 of the number of Phase Calibration RED value in one frame.

D7-6 Reserved

D5-0 CALVAL_R[29:24]

Auto Calibration GREEN Value - Byte 0 (Address 38h) (RO)

It states the byte 0 of the number of Phase Calibration GREEN value in one frame or the byte 0 of the number of Histogram GREEN value in one frame or the Pixel Grab RED value in SECOND field of Interlace mode.

D7-0 CALVAL_G[7:0]

Auto Calibration GREEN Value - Byte 1 (Address 39h) (RO)

It states the byte 1 of the number of Phase Calibration GREEN value in one frame or the byte 1 of the number of Histogram GREEN value in one frame or the Pixel Grab GREEN value in SECOND field of Interlace mode.

D7-0 CALVAL_G[15:8]

Auto Calibration GREEN Value - Byte 2 (Address 3Ah) (RO)

It states the byte 2 of the number of Phase Calibration GREEN value in one frame or the byte 2 of the number of Histogram GREEN value in one frame or the Pixel Grab BLUE value in SECOND field of Interlace mode.

D7-0 CALVAL_G[23:16]

Auto Calibration GREEN Value - Byte 3 (Address 3Bh) (RO)

It states the byte 3 of the number of Phase Calibration GREEN value in one frame.

D7-6 Reserved

D5-0 CALVAL_G[29:24]

Auto Calibration BLUE Value - Byte 0 (Address 3Ch) (RO)

It states the byte 0 of the number of Phase Calibration BLUE value in one frame or the byte 0 of the number of Histogram BLUE value in one frame or the MIN/MAX RED value in one frame.

D7-0 CALVAL_B[7:0]

Auto Calibration BLUE Value - Byte 1 (Address 3Dh) (RO)

It states the byte 1 of the number of Phase Calibration BLUE value in one frame or the byte 1 of the number of Histogram BLUE value in one frame or the MIN/MAX GREEN value in one frame.

D7-0 CALVAL_B[15:8]

Auto Calibration BLUE Value - Byte 2 (Address 3Eh) (RO)



It states the byte 2 of the number of Phase Calibration BLUE value in one frame or the byte 2 of the number of Histogram BLUE value in one frame or the MIN/MAX BLUE value in one frame.

D7-0 CALVAL_B[23:16]

Auto Calibration BLUE Value - Byte 3 (Address 3Fh) (RO)

It states the byte 3 of the number of Phase Calibration BLUE value in one frame.

D7-6 Reserved

D5-0 CALVAL_B[29:24]

Pixel Grab V Reference Position - Low (Address 40h) (R/W)

It states the low byte of Vertical Reference Position in Pixel Grab Mode.

D7-0 VGRAB_POS[7:0]

Pixel Grab V Reference Position - High (Address 41h) (R/W)

It states the high byte of Vertical Reference Position in Pixel Grab Mode.

D7-3 Reserved

D2-0 VGRAB_POS[10:8]

Pixel Grab H Reference Position - Low (Address 42h) (R/W)

It states the low byte of Horizontal Reference Position in Pixel Grab Mode.

D7-0 HGRAB_POS[7:0]

Pixel Grab H Reference Position - High (Address 43h) (R/W)

It states the high byte of Horizontal Reference Position in Pixel Grab Mode.

D7-3 Reserved

D2-0 HGRAB_POS[10:8]

Histogram Reference Color - RED (Address 44h) (R/W)

It states the Histogram Reference RED Color in Histogram Mode.

D7-0 HIST_R[7:0]

Histogram Reference Color - GREEN (Address 45h) (R/W)

It states the Histogram Reference GREEN Color in Histogram Mode.

D7-0 HIST_G[7:0]

Histogram Reference Color - BLUE (Address 46h) (R/W)

It states the Histogram Reference BLUE Color in Histogram Mode.



D7-0 HIST_B[7:0]

SYNC Processor Control (Address 48h) (R/W)

D7-2 Reserved

D1-0 SYNC Source
00: from H/V SYNC
01: from CVSYNC (Composite SYNC)
1x: Auto switch to CVSYNC when CVSYNC is present, but VSYNC not.

Auto Position Control (Address 49h) (R/W)

D7-2 Reserved

D1 Auto Position Burst Mode Enable
0: Single Mode
1: Burst Mode

D0 Auto Position Enable (**W**)
0: Disable
1: Enable
Auto Position Ready Flag (**R**)
0: Ready
1: Not Ready

Auto Position Reference Color - RED (Address 4Ah) (R/W)

It defines the red component color for selecting between black and non-black pixels.

D7-0 REF_COLOR_RED[7:0]

Auto Position Reference Color - GREEN (Address 4Bh) (R/W)

It defines the green component color for selecting between black and non-black pixels.

D7-0 REF_COLOR_GREEN[7:0]

Auto Position Reference Color - BLUE (Address 4Ch) (R/W)

It defines the blue component color for selecting between black and non-black pixels.

D7-0 REF_COLOR_BLUE[7:0]

Clamp Pulse Control 0 (Address 4Eh) (R/W)

D7 Clamp Pulse Mask
0: Normal
1: Mask out Clamp Pulse

D6 Clamp Pulse Start Reference Edge
0: From Input HSYNC trailing edge.
1: From Input HSYNC leading edge.

D5 Clamp Pulse output Polarity
0: Active High



1: Active Low

D4-0 Clamp Pulse Start
Start of Clamp Pulse after the selected edge of Input HSYNC by Input DCLK.

Clamp Pulse Control 1 (Address 4Fh) (R/W)

D7-5 Reserved

D4-0 Clamp Pulse Width
To adjust Clamp Pulse Width by input DCLK.

Input VS Period Count by REFCLK - Low (Address 50h) (RO)

It states the low byte of the number of REFCLK of the Vertical Sync period measurement.

D7-0 VSPRD[7:0]

Input VS Period Count by REFCLK - High (Address 51h) (RO)

It states the high byte of the number of REFCLK of the Vertical Sync period measurement.

D7-4 Reserved

D3-0 VSPRD[11:8]

Input V Back Porch Count by Input HS - Low (Address 52h) (RO)

It states the low byte of the number of lines between the end of VSYNC and the active image.

D7-0 VBPW[7:0]

Input V Back Porch Count by Input HS - High (Address 53h) (RO)

It states the high byte of the number of lines between the end of VSYNC and the active image

D7-3 Reserved

D2-0 VBPW[10:8]

Input V Active Image Count by Input HS - Low (Address 54h) (RO)

It states the low byte of the number of the active image lines.

D7-0 VACTW[7:0]

Input V Active Image Count by Input HS - High (Address 55h) (RO)

It states the high byte of the number of the active image lines

D7-3 Reserved

D2-0 VACTW[10:8]

Input V Total Image Count by Input HS - Low (Address 56h) (RO)

It states the low byte of the number of the total image lines.



D7-0 VTOTW[7:0]

Input V Total Image Count by Input HS - High (Address 57h) (RO)

It states the high byte of the number of the total image lines.

D7-3 Reserved

D2-0 VTOTW[10:8]

Input HS Period Count by REFCLK - Low (Address 58h) (RO)

It states the low byte of the number of REFCLKs of the Horizontal Sync period measurement.

D7-0 HSPRD[7:0]

Input HS Period Count by REFCLK - High (Address 59h) (RO)

It states the high byte of the number of REFCLKs of the Horizontal Sync period measurement.

D7-5 Reserved

D4-0 HSPRD[12:8]

Input H Back Porch Count by Input Pixel Clock -Low (Address 5Ah) (RO)

It states the low byte of the number of pixels between the end of HSYNC and the active image.

D7-0 HBPW[7:0]

Input H Back Porch Count by Input Pixel Clock -High (Address 5Bh) (RO)

It states the high byte of the number of pixels between the end of HSYNC and the active image.

D7-3 Reserved

D2-0 HBPW[10:8]

Input H Active Image Count by Input Pixel Clock-Low(Address 5Ch) (RO)

It states the low byte of the number of the Horizontal active image pixels.

D7-0 HACTW[7:0]

Input H Active Image Count by Input Pixel Clock-High(Address 5Dh)(RO)

It states the high byte of the number of the Horizontal active image pixels.

D7-3 Reserved

D2-0 HACTW[10:8]

Input H Total Image Count by Input Pixel Clock- Low (Address 5Eh) (RO)

It states the low byte of the number of the Horizontal total image pixels.



D7-0 HTOTW[7:0]

Input H Total Image Count by Input Pixel Clock- High (Address 5Fh) (RO)

It states the high byte of the number of the Horizontal total image pixels.

D7-3 Reserved

D2-0 HTOTW[10:8]

Display Vertical Total - Low (Address 60h) (R/W)

It defines the low byte of the number of lines per display frame.

D7-0 DV_TOTAL[7:0]

Display Vertical Total - High (Address 61h) (R/W)

It defines the high byte of the number of lines per display frame.

D7-3 Reserved

D2-0 DV_TOTAL[10:8]

Display Vertical SYNC End - Low (Address 62h) (R/W)

It defines the low byte of Vertical SYNC end position in lines.

D7-0 DV_SYNC_END[7:0]

Display Vertical VSYNC End - High (Address 63h) (R/W)

It defines the high byte of Vertical SYNC end position in lines.

D7-3 Reserved

D2-0 DV_SYNC_END[10:8]

Note: Display Vertical SYNC Start is always equal 0.

Display Vertical Active Start - Low (Address 64h) (R/W)

It defines the low byte of Vertical Active region start position in lines.

D7-0 DV_ACT_START[7:0]

Display Vertical Active Start - High (Address 65h) (R/W)

It defines the high byte of Vertical Active region start position in lines.

D7-3 Reserved

D2-0 DV_ACT_START[10:8]

Display Vertical Active End - Low (Address 66h) (R/W)

It defines the low byte of Vertical Active region end position in lines.



D7-0 DV_ACT_END[7:0]

Display Vertical Active End - High (Address 67h) (R/W)

It defines the high byte of Vertical Active region end position in lines.

D7-3 Reserved

D2-0 DV_ACT_END[10:8]

Display Vertical Border Start - Low (Address 68h) (R/W)

It defines the low byte of Vertical Border start position in lines.

D7-0 DV_BOR_START[7:0]

Display Vertical Border Start - High (Address 69h) (R/W)

It defines the high byte of Vertical Border start position in lines.

D7-3 Reserved

D2-0 DV_BOR_START[10:8]

Display Vertical Border End - Low (Address 6Ah) (R/W)

It defines the low byte of Vertical Border end position in lines.

D7-0 DV_BOR_END[7:0]

Display Vertical Border End - High (Address 6Bh) (R/W)

It defines the high byte of Vertical Border end position in lines.

D7-3 Reserved

D2-0 DV_BOR_END[10:8]

Display Horizontal Total - Low (Address 70h) (R/W)

It defines the low byte of the number of display clock cycles per display line.

D7-0 DH_TOTAL[7:0]

Display Horizontal Total - High (Address 71h) (R/W)

It defines the high byte of the number of display clock cycles per display line.

D7-3 Reserved

D2-0 DH_TOTAL[10:8]

Display Horizontal SYNC End - Low (Address 72h) (R/W)

It defines the low byte of Horizontal SYNC end position in display clock cycles.



D7-0 DH_SYNC_END[7:0]

Display Horizontal SYNC End - High (Address 73h) (R/W)

It defines the high byte of Horizontal SYNC end position in display clock cycles.

D7-3 Reserved

D2-0 DH_SYNC_END[10:8]

Note: Display Horizontal SYNC Start is always equal 0.

Display Horizontal Active Start - Low (Address 74h) (R/W)

It defines the low byte of Horizontal Active region start position in display clock cycles.

D7-0 DH_ACT_START[7:0]

Display Horizontal Active Start - High (Address 75h) (R/W)

It defines the high byte of Horizontal Active region start position in display clock cycles.

D7-3 Reserved

D2-0 DH_ACT_START[10:8]

Display Horizontal Active End - Low (Address 76h) (R/W)

It defines the low byte of Horizontal Active region end position in display clock cycles.

D7-0 DH_ACT_END[7:0]

Display Horizontal Active End - High (Address 77h) (R/W)

It defines the high byte of Horizontal Active region end position in display clock cycles.

D7-3 Reserved

D2-0 DH_ACT_END[10:8]

Display Horizontal Border Start - Low (Address 78h) (R/W)

It defines the low byte of Horizontal Border start position in display clock cycles.

D7-0 DH_BOR_START[7:0]

Display Horizontal Border Start - High (Address 79h) (R/W)

It defines the high byte of Horizontal Border start position in display clock cycles.

D7-3 Reserved

D2-0 DH_BOR_START[10:8]

Display Horizontal Border End - Low (Address 7Ah) (R/W)

It defines the low byte of Horizontal Border end position in display clock cycles.



D7-0 DH_BOR_END[7:0]

Display Horizontal Border End - High (Address 7Bh) (R/W)

It defines the high byte of Horizontal Border end position in display clock cycles.

D7-3 Reserved

D2-0 DH_BOR_END[10:8]

Output Image Control Register 0 (Address 88h) (R/W)

D7-3 Reserved

D2 Output Pixel 18 bit RGB Mode Select
0: 24 bit RGB
1: 18 bit RGB

D1 Output Dual Pixel Data Exchange
0: Normal
1: Exchange

D0 Output Dual Pixel Select
0: Dual Pixel
1: Single Pixel

Output Image Control Register 1 (Address 89h) (R/W)

D7-6 Reserved

D5 RGB Brightness Control Enable
0: Disable
1: Enable

D4 RGB Gain Control Enable
0: Disable
1: Enable

D3-2 Reserved

D1 Border Window Function
0: OFF
1: ON

D0 Output Blank Screen
0: Normal
1: Output Pixel masked as BLACK color

Output Image Control Register 2 (Address 8Ah) (R/W)

D7 Reserved

D6 Temporal Dithering Enable
0: Static Dithering
1: Temporal Dithering



| | |
|----|--|
| D5 | Dithering Table R/W Access Enable 0: Disable 1: Enable |
| D4 | Dithering Enable 0: Disable 1: Enable |
| D3 | Reserved |
| D2 | 10 bit Gamma Table Enable 0: 8 bit Gamma Table 1: 10 bit Gamma Table |
| D1 | Gamma Table R/W Access Enable 0: Disable 1: Enable |
| D0 | Gamma Correction Function 0: OFF 1: ON |

Color Gain Control - RED (Address 90h) (R/W)

It can be used to adjust the gain of RED component of the Display Image.

D7-0 RGAIN[7:0]
0(00h) ~ x1(80h) ~ x1.992185(FFh)

Color Gain Control - GREEN (Address 91h) (R/W)

It can be used to adjust the gain of GREEN component of the Display Image.

D7-0 GGAIN[7:0]
0(00h) ~ x1(80h) ~ x1.992185(FFh)

Color Gain Control - BLUE (Address 92h) (R/W)

It can be used to adjust the gain of BLUE component of the Display Image.

D7-0 BGAIN[7:0]
0(00h) ~ x1(80h) ~ x1.992185(FFh)

Color Brightness Control - RED (Address 93h) (R/W)

It can be used to adjust the brightness of RED component of the Display Image.

D7-0 RBRIGHT[7:0]
-128(80h) ~ 0(00h) ~127(7Fh)

Color Brightness Control - GREEN (Address 94h) (R/W)

It can be used to adjust the brightness of GREEN component of the Display Image.

D7-0 GBRIGHT[7:0]
-128(80h) ~ 0(00h) ~127(7Fh)



Color Brightness Control - BLUE (Address 95h) (R/W)

It can be used to adjust the brightness of BLUE component of the Display Image.

D7-0 BBRIGHT[7:0]
 -128(80h) ~ 0(00h) ~127(7Fh)

Border Window Color - RED (Address 96h) (R/W)

When the Display Image is not expanded to full screen, it can be specified as the RED component of the border color.

D7-0 BCR[7:0]

Border Window Color - GREEN (Address 97h) (R/W)

When the Display Image is not expanded to full screen, it can be specified as the GREEN component of the border color.

D7-0 BCG[7:0]

Border Window Color - BLUE (Address 98h) (R/W)

When the Display Image is not expanded to full screen, it can be specified as the BLUE component of the border color.

D7-0 BCB[7:0]

Dithering Table Data Port (Address 9Eh) (R/W)

Since the Dithering Table is downloadable, this data port is the entry address.

D7-0 DITHER_PORT[7:0]

Gamma Table Data Port (Address 9Fh) (R/W)

Since the Gamma Table is downloadable, this data port is the entry address.

D7-0 GAMMA_PORT[7:0]

OSD Control Registers (Address A0h) (R/W)

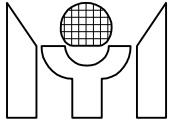
D7 OSD Output Clock Select
 0: from Internal Display Dot Clock
 1: from Internal Display Dot Clock x 2

D6 OSD Output VS Invert
 0: Normal
 1: Invert

D5-4 Reserved

D3 OSD Function
 0: OFF
 1: ON

D2 OSD Intensity Enable (For MOTOROLA)



0: Disable
1: Enable

D1-0 OSD TYPE Select
00: OSDRGB = {R0000000, G0000000, B0000000}
01: OSDRGB = {RR000000, GG000000, BB000000}
10: OSDRGB = {RRRR0000, GGGG0000, BBBB0000}
11: OSDRGB = {RRRRRRRR, GGGGGGGG, BBBBBBBB}
R = OSDR, G = OSDG, B = OSDB

OSD Control Register 1 (Address A1h) (R/W)

D7 OSD Output HS Invert
0: Normal
1: Invert.

D6 OSD Output DCLK Invert
0: Normal
1: Invert.

D5-4 OSD Output HS Delay
4 steps to change, each of them is 1ns delay/step.

D3 OSD Input Data Sample Clock Invert
0: Normal.
1: Invert.

D2-0 OSD Input Data Sample Clock Delay
8 steps to change, each of them is 1ns delay/step.

OSD Control Register 2 (Address A2h) (R/W)

D7-4 Reserved

D3-0 OSD Output Clock Delay
16 steps to change, each of them is 1ns delay/step.

Output Invert Control (Address A4h) (R/W)

D7 Reserved

D6 RGB Data Invert Enable
0: Disable
1: Enable

D5 Display DCLK2 Invert
0: Normal
1: Invert

D4 Display DCLK1 Invert
0: Normal
1: Invert

D3 Reserved

D2 Display Data Enable (DDEN) Invert
0: Normal



1: Invert

D1 Display VSYNC Invert
0: Normal
1: Invert

D0 Display HSYNC Invert
0: Normal
1: Invert

Output Tri_state Control (Address A5h) (R/W)

D7 Display Data R2OUT, G2OUT, B2OUT Output Disable
0: Normal
1: Tri_stated

D6 Display Data R1OUT, G1OUT, B1OUT Output Disable
0: Normal
1: Tri_stated

D5 Display DCLK2 Output Disable
0: Normal
1: Tri_stated

D4 Display DCLK1 Output Disable
0: Normal
1: Tri_stated

D3 OSD OCLK / OVSYNC / OHSYNC Output Disable
0: Normal
1: Tri_stated

D2 Display Data Enable (DDEN) Output Disable
0: Normal
1: Tri_stated

D1 Display VSYNC Output Disable
0: Normal
1: Tri_stated

D0 Display HSYNC Output Disable
0: Normal
1: Tri_stated

Output Clocks Delay Adjustment (Address A6h) (R/W)

D7-4 Display DCLK2 delay adjustment
16 steps to adjust, Typical 1ns delay/step

D3-0 Display DCLK1 delay adjustment
16 steps to adjust, Typical 1ns delay/step

Output Clocks Duty Cycle Adjustment (Address A7h) (R/W)

D7 Display DCLK2 duty cycle Increase/Decrease
0: Decrease
1: Increase



- D6-4 Display DCLK2 duty cycle adjustment
8 steps to adjust, Typical 0.5ns delay/step
- D3 Display DCLK1 duty cycle Increase/Decrease
0: Decrease
1: Increase
- D2-0 Display DCLK1 duty cycle adjustment
8 steps to adjust, Typical 0.5ns delay/step

Output Miscellaneous Control (Address A9h) (R/W)

- D7 Second field Line Buffer Overflow status for Interlace input **(RO)**
0: Not Overflow
1: Overflow
- D6 Second field Line Buffer Underflow status for Interlace input **(RO)**
0: Not Underflow
1: Underflow
- D5 First field Line Buffer Overflow status for Interlace input or
Line buffer Overflow status for Non-interlace input **(RO)**
0: Not Overflow
1: Overflow
- D4 First field Line Buffer Underflow status for Interlace input or
Line Buffer Overflow status for Non-interlace input **(RO)**
0: Not Underflow
1: Underflow
- D3 Auto Output Horizontal Total Calculation Start **(W)**
0: Disable
1: Enable
Auto Output Horizontal Total Calculation Ready Flag **(R)**
0: Ready
1: Not Ready
- D2-0 Reserved

Output Vertical Active Line Number - Low (Address AAh) (R/W)

It defines the low byte of Output Vertical Active Line Number only used for getting the values of Reg. ACh and ADh.

- D7-0 OVDE[7:0]

Output Vertical Active Line Number - High (Address ABh) (R/W)

It defines the high byte of Output Vertical Active Line Number only used for getting the values of Reg. ACh and ADh.

- D1-0 OVDE[9:8]

Output Horizontal Total Pixel Number - Low (Address ACh) (RO)

It states the low byte of Output Horizontal Total Pixel Number.



D7-0 OHTOT[7:0]

Output Horizontal Total Pixel Number - High (Address ADh) (RO)

It states the high byte of Output Horizontal Total Pixel Number.

D2-0 OHTOT[10:8]

Output Horizontal Total Residue Number - Low (Address AEh) (RO)

It states the low byte of Output Horizontal Total Pixel Residue Number.

D7-0 OHTOT_RES[7:0]

Output Horizontal Total Residue Number - High (Address AFh) (RO)

It states the high byte of Output Horizontal Total Pixel Residue Number.

D7-2 Reserved

D1-0 OHTOT_RES[9:8]

Zoom Control Register 0 (Address B0h) (R/W)

D7 Vertical Scale Mode
0: Scale Up
1: Scale Down

D6-4 Vertical Scale Select
0XX: PASS mode
10X: DUPLICATE mode
110: BILINEAR mode
111: INTERPOLATION TABLE mode (only for Scale Up)

D3 Horizontal Scale Mode
0: scale up
1: scale down

D2-0 Horizontal Scale Select
0xx: PASS mode
10x: DUPLICATE mode
110: BILINEAR mode
111: INTERPOLATION TABLE mode

Zoom Control Register 1 (Address B1h) (R/W)

D7-1 Reserved

D0 Interpolation Table R/W Access Enable
0: Disable
1: Enable

Zoom Vertical Scale Down Integer Ratio Region (Address B2h) (R/W)

It defines vertical scale down integer ratio value region



| | |
|------|--|
| D7-3 | Reserved |
| D2-0 | ZVDIV[2:0] 0 : scale down ratio = 1-1/2(exclude 1) 1 : scale down ratio = 1/2-1/4(exclude 1/2) 2: scale down ratio = 1/4-1/8(exclude 1/4) 3: scale down ratio = 1/8-1/16(exclude 1/8) 4: scale down ratio = 1/16-1/32(exclude 1/16) |

Zoom Horizontal Scale Down Integer Ratio Region (Address B3h) (R/W)

It defines horizontal scale down integer ratio value region.

| | |
|------|--|
| D7-3 | Reserved |
| D2-0 | ZHDIV[2:0] 0 : scale down ratio = 1-1/2(exclude 1) 1 : scale down ratio = 1/2-1/4(exclude 1/2) 2: scale down ratio = 1/4-1/8(exclude 1/4) 3: scale down ratio = 1/8-1/16(exclude 1/8) 4: scale down ratio = 1/16-1/32(exclude 1/16) |

Zoom Vertical Scale Ratio – Low (Address B4h) (R/W)

It defines the low byte of vertical scale ratio value for scale up and down.

| | |
|------|-----------|
| D7-0 | ZVSF[7:0] |
|------|-----------|

Zoom Vertical Scale Ratio - High (Address B5h) (R/W)

It defines the low byte of vertical scale ratio value for scale up and down.

| | |
|------|------------|
| D7-0 | ZVSF[15:8] |
|------|------------|

For Scale Up $ZVSF = \text{CEIL}[(\text{input_height} - 1) / (\text{output_height} - 1) * 2^{16}]$
For Scale Down $ZVSF = \text{CEIL}\{[(\text{input_height}' - 1) / (\text{output_height} - 1) - 1] * 2^{16}\}$
,where $\text{input_height}' = \text{input_height} / 2^{\text{ZVDIV}}$. The means of ZVDIV is referenced to Reg. B2h.

Zoom Horizontal Scale Ratio - Low (Address B6h) (R/W)

It defines the low byte of horizontal scale ratio value for scale up and down.

| | |
|------|-----------|
| D7-0 | ZHSF[7:0] |
|------|-----------|

Zoom Horizontal Scale Ratio - High (Address B7h) (R/W)

It defines the high byte of horizontal scale ratio value for scale up and down.

| | |
|------|------------|
| D7-0 | ZHSF[15:8] |
|------|------------|

For Scale Up $ZHSF = \text{ROUND}[(\text{input_width} - 1) / (\text{output_width} - 1) * 2^{16}]$
For Scale Down $ZVSF = \text{ROUND}\{[(\text{input_width}' - 1) / (\text{output_width} - 1) - 1] * 2^{16}\}$
,where $\text{input_width}' = \text{input_width} / 2^{\text{ZHDIV}}$. The means of ZHDIV is referenced to Reg. B3h.

Interpolation Table Data Port (Address BFh) (R/W)

It defines the entry address of the Interpolation table data port.



D7-0 TFPORT[7:0]

Host Control Register 0 (Address C0h) (R/W)

D7 Host Screen Write Stop Enable **(WO)**
0: Disable
1: Enable

D6-1 Force to 001010

D0 Host Screen Write Start Enable **(W)**
0: Disable
1: Enable
Host Screen Write Ready Flag **(R)**
0: Ready
1: Not Ready

Host Control Register 1 (Address C1h) (R/W)

D7 Reserved

D6 I²C Bus Address No Increment
0: Normal
1: No Increment

D5 Double Buffer load Select
0: Immediately
1: Delay to Display VSYNC

D4 Registers Double Buffer function Enable
0: Disable
1: Enable

D3-2 Reserved

D1 Display Registers Double Buffer Load **(WO)**

D0 Input Registers Double Buffer Load **(WO)**

Host Screen Write Line Length - Low (Address C4h) (R/W)

It defines the low byte of the vertical line length for Host Screen Write.

D7-0 HS_LEN[7:0]

Host Screen Write Line Length - High (Address C5h) (R/W)

It defines the high byte of the vertical line length for Host Screen Write.

D7-3 Reserved

D2-0 HS_LEN[10:8]

Host Fill RED Color (Address C6h) (R/W)

It defines Fill Red color for Host Screen Write.



D7-0 HFR[7:0]

Host Fill GREEN Color (Address C7h) (R/W)

It defines Fill Green color for Host Screen Write.

D7-0 HFG[7:0]

Host Fill BLUE Color (Address C8h) (R/W)

It defines Fill Blue color for Host Screen Write.

D7-0 HFB[7:0]

Host Access Mode Status (Address CBh) (RO)

D7-1 Reserved

D0 Host Access Mode
0: 2-wire Serial mode (IIC)
1: 8-bit Parallel mode

Memory Type Control (Address D0h) (R/W)

D7-5 Reserved

D4 32 bits Memory Bus (Only for X2 Memory Configuration)
0: Disable
1: Enable

D3 Reserved

D2-0 000: 16M SDRAM X 3
001: 16M SDRAM X 2
010: 8M SGRAM X 3
011: 8M SGRAM X 2
10x: Reserved
110: 16M SGRAM X 3
111: 16M SGRAM X 2

Memory Self Test Control (Address D2h) (R/W)

It controls the operation of Memory Self Test Mode.

D7-3 Reserved

D2 Memory Self Test mode Result Status (RO)
0: Success
1: Fail

D1 Memory Self Test mode Finish Status (RO)
0: Finish
1: Not Finish

D0 Memory Self Test mode Enable
0: Disable



1: Enable

Memory Line Offset – Low (Address D4h) (R/W)

It defines the low byte of Memory Line Offset Address Length for Memory Read/Write.

D7-0 Line_offset[7:0]

Memory Line Offset – High (Address D5h) (R/W)

It defines the high byte of Memory Line Offset Address Length for Memory Read/Write.

D7-3 Reserved

D2-0 Line_offset[10:8]

Memory Self-Test Compare Error Address – Low (Address DBh) (RO)

It defines the low byte of Memory Base Address for Memory Self-Test comparing error report.

D7-0 MSFTBA [7:0]

Memory Self-Test Compare Error Address – Middle (Address DCh) (RO)

It defines the middle byte of Memory Base Address for Memory Self-Test comparing error report.

D7-0 MSFTBA [15:8]

Memory Self-Test Compare Error Address – High (Address DDh) (RO)

It defines the high byte of Memory Base Address for Memory Self-Test comparing error report and Patterns Number.

D7 Reserved

D6-5 Memory Self-Test Patterns Number when Comparing Error
00: Pattern Constructed by Linear Memory Address
01: 48 Bits Pattern Toggled between 55 and AA
10: 48 Bits Pattern Toggled between AA and 55
11: Reserved

D4-0 MSFTBA [20:16]

Clock Synthesizer Control Register (Address E0h) (R/W)

D7-4 Reserved

D3 Memory Clock Source
0: Internal Memory Clock
1: External Memory Clock from pin EXTMCLK

D2 Display Clock Source
0: Internal Display Clock
1: External Display Clock from pin EXTDCLK

D1 Memory Clock Synthesizer Enable
0: Enable



1: Disable

D0 Display Clock Synthesizer Enable
0: Enable
1: Disable

Clock Synthesizer Value Load (Address E1h) (WO)

D7-2 Reserved
D1 Memory Clock Synthesizer Value Load (WO)
D0 Display Clock Synthesizer Value Load (WO)

Display Clock Synthesizer N Value (Address E2h) (R/W)

D7-0 Display Clock Synthesizer N value

Display Clock Synthesizer M Value (Address E3h) (R/W)

D7-0 Display Clock Synthesizer M value

Memory Clock Synthesizer N Value (Address E4h) (R/W)

D7-0 Memory Clock Synthesizer N value

Memory Clock Synthesizer M Value (Address E5h) (R/W)

D7-0 Memory Clock Synthesizer M value

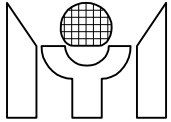
Clock Synthesizer R Value (Address E6h) (R/W)

D7-4 Reserved
D3-2 Memory Clock Synthesizer R value
00: No divided
01: Divided by 2
1x: Divided by 4
D1-0 Display Clock Synthesizer R value
00: No divided
01: Divided by 2
1x: Divided by 4

SYNC Interrupt Flag Control (Address E8h) (R)

It contains the status of SYNC Interrupts.

D7 Display VSYNC Pulse Interrupt Status
0: No Display VSYNC pulse detected
1: Any Display VSYNC pulse detected
D6 Input VSYNC Pulse Interrupt Status
0: No Input VSYNC pulse detected
1: Any Input VSYNC pulse detected
D5 VSYNC Presence Change Status



0: No Change
1: Change

- D4 HSYNC Presence Change Status
0: No Change
1: Change
- D3 VSYNC Polarity Change Status
0: No Change
1: Change
- D2 HSYNC Polarity Change Status
0: No Change
1: Change
- D1 VSYNC Frequency Change Status
0: No Change
1: Change
- D0 HSYNC Frequency Change Status
0: No Change
1: Change

SYNC Interrupt Flag Control (Address E8h) (W)

It is used to clear the corresponding SYNC interrupt signal when Software finishes serving the interrupt service routine.

- D7 Clear Display VSYNC Pulse Interrupt Enable
0: Disable
1: Enable
- D6 Clear Input VSYNC Pulse Interrupt Enable
0: Disable
1: Enable
- D5 Clear VSYNC Presence Change Interrupt Enable
0: Disable
1: Enable
- D4 Clear HSYNC Presence Change Interrupt Enable
0: Disable
1: Enable
- D3 Clear VSYNC Polarity Change Interrupt Enable
0: Disable
1: Enable
- D2 Clear HSYNC Polarity Change Interrupt Enable
0: Disable
1: Enable
- D1 Clear VSYNC Frequency Change Interrupt Enable
0: Disable
1: Enable
- D0 Clear HSYNC Frequency Change Interrupt Enable
0: Disable



1: Enable

General Interrupt Flag Control (Address E9h) (R)

It contains the status of General Interrupts.

| | |
|------|---|
| D7-2 | Reserved |
| D1 | Auto Position Finish Status (valid for Single mode only) 0: Not Finish 1: Finish |
| D0 | Auto Calibration Finish Status (valid for Single mode only) 0: Not Finish 1: Finish |

General Interrupt Flag Control (Address E9h) (W)

It is used to clear the corresponding general interrupt signal when Software finishes serving the interrupt service routine.

| | |
|------|---|
| D7-2 | Reserved |
| D1 | Clear Auto Position Finish Interrupt Enable 0: Disable 1: Enable |
| D0 | Clear Auto Calibration Finish Interrupt Enable 0: Disable 1: Enable |

SYNC Interrupt Flag Enable (Address EAh) (R/W)

It is used to enable SYNC Interrupt function.

| | |
|----|---|
| D7 | Display VSYNC Pulse Interrupt Enable 0: Disable 1: Enable |
| D6 | Input VSYNC Pulse Interrupt Enable 0: Disable 1: Enable |
| D5 | VSYNC Presence Change Interrupt Enable 0: Disable 1: Enable |
| D4 | HSYNC Presence Change Interrupt Enable 0: Disable 1: Enable |
| D3 | VSYNC Polarity Change Interrupt Enable 0: Disable 1: Enable |
| D2 | HSYNC Polarity Change Interrupt Enable 0: Disable |



1: Enable

D1 VSYNC Frequency Change Interrupt Enable
0: Disable
1: Enable

D0 HSYNC Frequency Change Interrupt Enable
0: Disable
1: Enable

General Interrupt Flag Enable (Address EBh) (R/W)

It is used to enable General Interrupt functions.

D7 Interrupt Output Polarity Invert
0: Active Low
1: Active High

D6-2 Reserved

D1 Auto Position Finish Interrupt Enable
0: Disable
1: Enable

D0 Auto Calibration Finish Interrupt Enable
0: Disable
1: Enable

HS Frequency Change Interrupt Compare (Address ECh) (R/W)

It is used to control Interrupt generation by comparing the frequency change value when Input HS Frequency Changes.

D7-0 HSCMPREG[7:0]

Power Management Control (Address F1h) (R/W)

D7 Reserved

D6 Power Down Gamma & Interpolation Table
0: Normal
1: Power Down

D5 Power Down Output Line Buffers
0: Normal
1: Power Down

D4 Power Down Input Line Buffers
0: Normal
1: Power Down

D3-2 Reserved

D1 Power Down all the clocks except REFCLK
0: Normal
1: Power Down



D0 Software Reset Enable
 0: Disable
 1: Enable

GPIO Control Register (Address F4h) (R/W)

It controls the data of the GPIO pins.

D7-0 GPIO[7:0]

GPIO Direction Control (Address F5h) (R/W)

It controls the In/Out direction of the GPIO pins, where “0” means Output, and “1” means Tri_state or Input.

D7-6 GPIO[7:6] Output Enable
 0: Output
 1: Tri_state

D5-0 GPIO[5:0] In/Out Select
 0: Output
 1: Input

GPIO Misc Control (Address F6h) (R/W)

It defines the GPIO pins miscellaneous control.

D7-1 Reserved

D0 GPIO[7:6] Output Pins Source
 0: from Reg. F4h/D7-6
 1: from ADVS/ADHS



5. ELECTRICAL CHARACTERISTICS

5.1 DC CHARACTERISTICS

Table 5.1 Recommended Operating Conditions

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|--------|-------------------------------|-----|-----|-----|------|
| Vcc | Operation Voltage | 3.0 | 3.3 | 3.6 | V |
| Tamb | Operating Ambient Temperature | 0 | | 70 | °C |
| Tstg | Storage Temperature | -55 | | 150 | °C |

Table 5.2 DC Electrical Characteristics for 3.3 V Operation

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|--------|--|--------------------------|-----|-----|-----|------|
| VIL | Input Low Voltage | | | | 0.8 | V |
| VIH | Input High Voltage | | 2.0 | | | V |
| Vt- | Input Schmitt Trigger Low Voltage at pins SDA and SCK | | | 1.0 | | |
| Vt+ | Input Schmitt Trigger High Voltage at pins SDA and SCK | | | 1.7 | | |
| VOL | Output Low Voltage | | | | 0.4 | V |
| VOH | Output High Voltage | | 2.4 | | | V |
| RI | Input Pull-up/Down Resistance | VIL = 0v or VIH = VCC | | 75 | | Kohm |
| ILI | Input Leakage Current | | -10 | | 10 | uA |
| ILO | Output Leakage Current | | -20 | | 20 | uA |



5.2 AC CHARACTERISTICS

À Input Interface Timing

Figure 5.2.1 Input Interface Timing

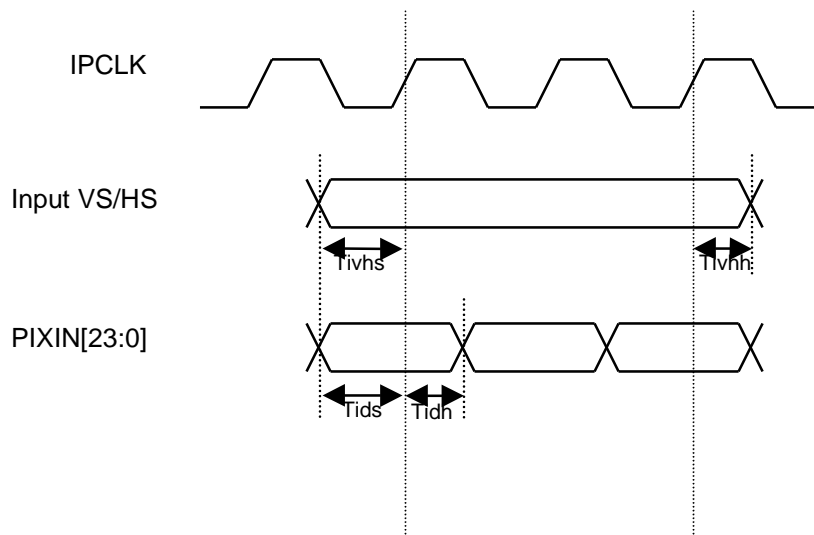


Table 5.2.1 Input Interface Timing

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|--------|---|-----|-----|------|
| Tids | Input Image Signal Setup Time for IPCLK | 2 | | ns |
| Tidh | Input Image Signal Hold Time for IPCLK | 3 | | ns |
| Tivhs | Input VSYNC/HSYNC Setup Time for IPCLK | 2 | | ns |
| Tivhh | Input VSYNC/HSYNC Hold Time for IPCLK | 3 | | ns |



Ā **Output Interface Timing**

Figure 5.2.2 Output Interface Timing

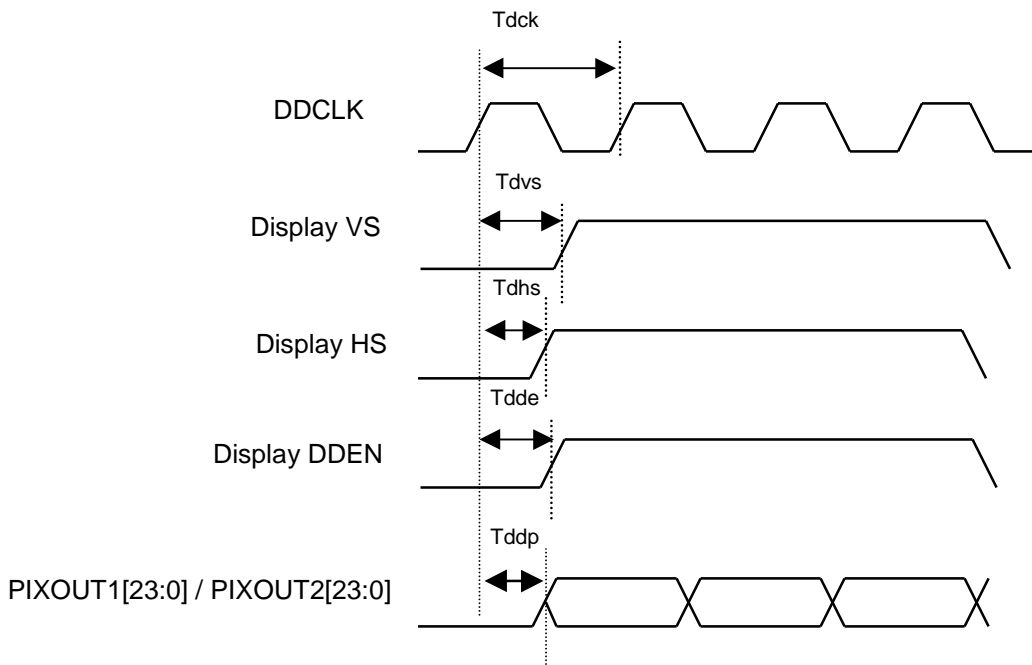


Table 5.2.2 Output Interface Timing

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|--------|-------------------------------------|-----|-----|------|
| Tdck | Display Clock DDCLK Frequency | 9 | | ns |
| Tdvs | Display VSYNC Output Delay to DDCLK | 2 | | ns |
| Tdhs | Display HSYNC Output Delay to DDCLK | 0.5 | | ns |
| Tdde | Display DDEN Output Delay to DDCLK | 1 | | ns |
| Tddp | Display Data Output Delay to DDCLK | 1.5 | | ns |

Note: DDCLK phase can be adjusted relative to data and control outputs using the DDCLK_INV (Reg. A4h/D5-4) and DDCLK_DELAY[2:0] (Reg. A6h/D7-0) programming controls.



Ā **OSD Interface Timing**

Figure 5.2.3 OSD Interface Timing

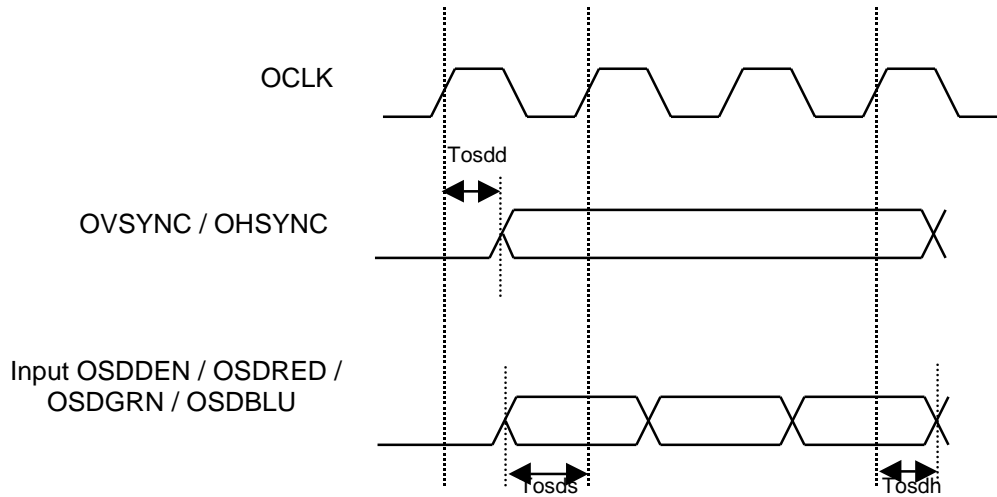


Table 5.2.3 OSD Interface Timing

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|---------------|--------------------------------------|------------|------------|-------------|
| Tosdd | OSD VS / HS Output Delay to OCLK | 2 | | ns |
| Tosds | OSD Signal Input Setup Time for OCLK | 5.5 | | ns |
| Tosdh | OSD Signal Input Hold Time for OCLK | 0 | | ns |

Note: OCLK phase can be adjusted using OCLK_INV (Reg. A1h/D3) programming control and OHSYNC phase can be adjusted using OHSYNC_DELAY[1:0] (Reg. A1h/D5-4) programming control.



Ā I²C Host Interface Timing

Figure 5.2.4 I²C Host Interface Timing

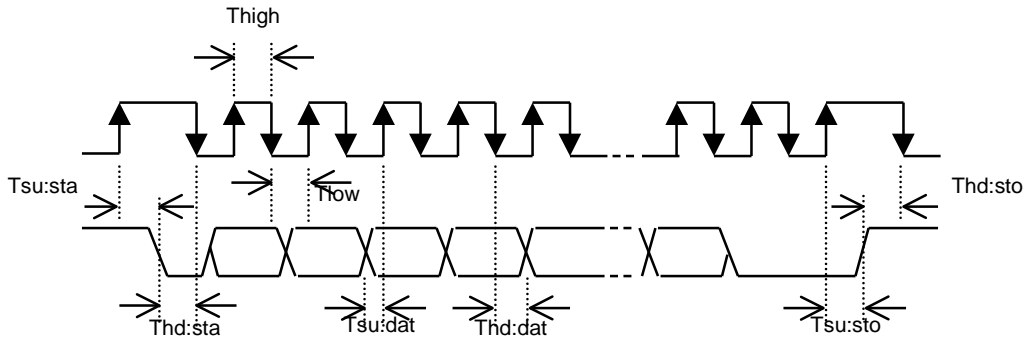


Table 5.2.4 I²C Host Interface Timing

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|--------------|----------------------------|-----|-----|------|
| T_{high} | Clock High Period | 500 | | ns |
| T_{low} | Clock Low Period | 500 | | ns |
| $T_{su:dat}$ | Data in Setup Time | 200 | | ns |
| $T_{hd:dat}$ | Data in Hold Time | 100 | | ns |
| $T_{su:sta}$ | Start condition Setup Time | 500 | | ns |
| $T_{hd:sta}$ | Start condition Hold Time | 500 | | ns |
| $T_{su:sto}$ | Stop condition Setup Time | 500 | | ns |
| $T_{hd:sto}$ | Stop condition Hold Time | 500 | | ns |



Ā **8-bit Direct Host Interface Timing**

Figure 5.2.5 8-bit Direct Host Interface Timing

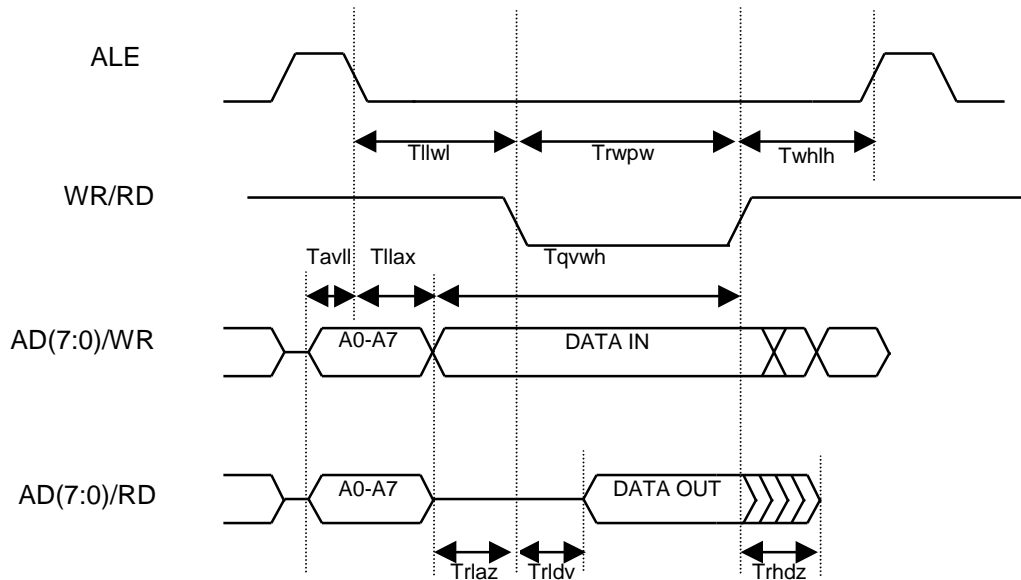


Table 5.2.5 8-bit Direct Host Interface Timing

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|--------|----------------------------|-----|-----|------|
| Tavll | Address Valid to ALE Low | 3 | | ns |
| Tllax | Address Hold After ALE Low | 5 | | ns |
| Trwpw | WR/RD Pulse Width | 35 | | ns |
| Tllwl | ALE Low to WR/RD Low | 5 | | ns |
| Tqvwh | Data Valid to WR High | 3 | | ns |
| Twhqx | Data Hold After WR | 10 | | ns |
| Twhlh | WR/RD High to ALE High | 0 | | ns |
| Trlaz | RD Low to Address Float | -5 | | ns |
| Trldv | RD Low to Valid Data In | | 30 | ns |
| Trhdz | Data Float after RD High | 0 | 15 | ns |



Ā **Memory Interface (SDRAM/SGRAM) Timing**

Figure 5.2.6 Memory Interface Timing

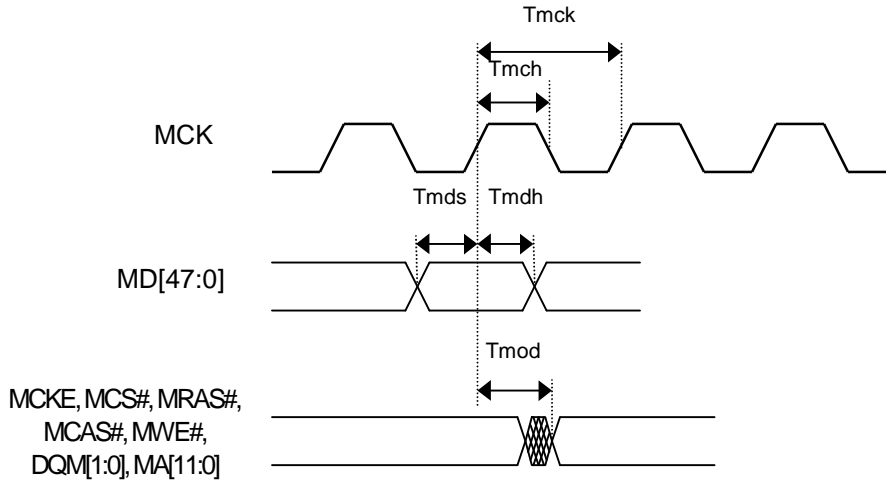


Table 5.2.6 Memory Interface Timing

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|-------------------|----------------------------|-----|-----|------|
| T_{mck} | Memory Clock Cycle Time | 8.5 | | ns |
| T_{mch}/T_{mck} | Memory Clock Duty Cycle | 0.4 | 0.6 | ns |
| T_{mds} | Data-in Setup Time for MCK | 1 | | ns |
| T_{mdh} | Data-in Hold Time for MCK | 2 | | ns |
| T_{mod} | Memory Output Delay to MCK | 2 | 8.5 | ns |

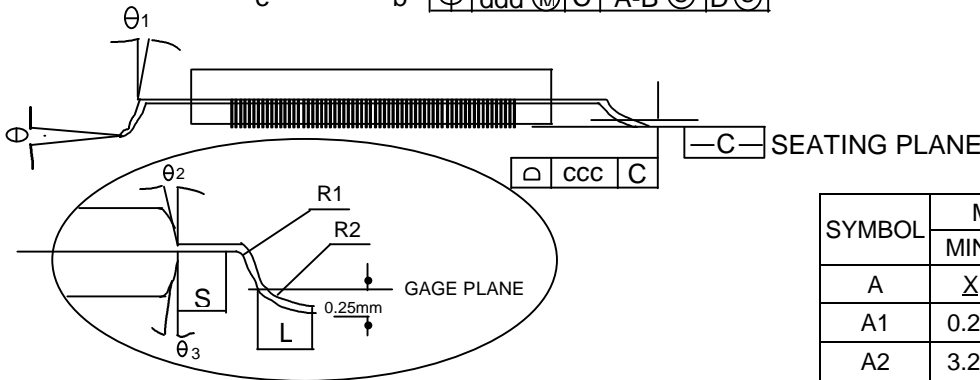
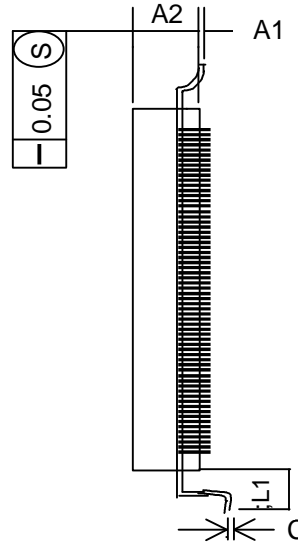
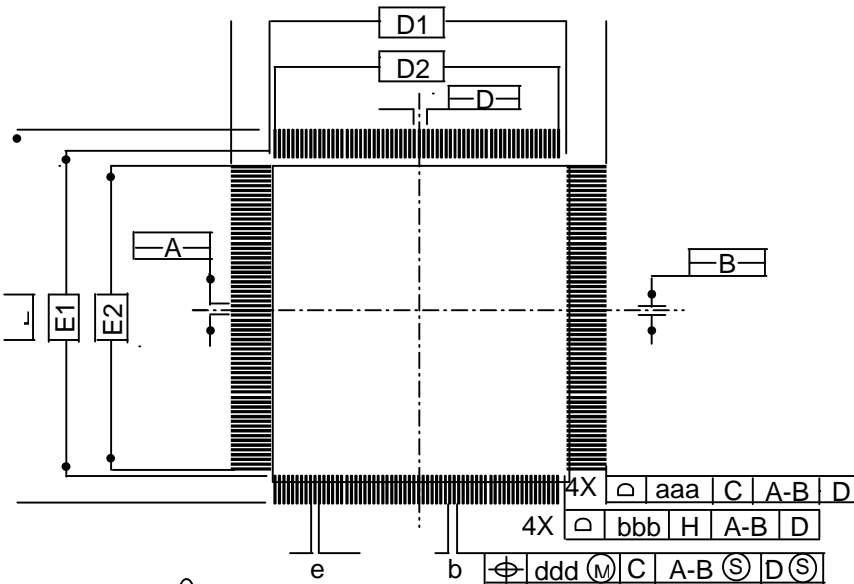


6. PACKAGE DIMENSION

120/128/132/144/160/184/208/256L OFP

28 X 28 X 3.32 mm

2.6mm FOOTPRINT



| MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
|---------------------------------|------|------|------------|-------|-------|
| 0.13 | 0.16 | 0.23 | 0.005 | 0.006 | 0.009 |
| 0.40 BSC. | | | 0.016 BSC. | | |
| 25.20 | | | 0.992 | | |
| 25.20 | | | 0.992 | | |
| TOLERANCES OF FORM AND POSITION | | | | | |
| 0.20 | | | 0.008 | | |
| 0.20 | | | 0.008 | | |
| X | 0.08 | X | X | 0.003 | X |
| X | 0.07 | X | X | 0.003 | X |

| SYMBOL | MILLIMETER | | | INCH | | |
|--------|------------|------|------|-----------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | X | X | 4.10 | X | X | 0.161 |
| A1 | 0.25 | X | X | 0.010 | X | X |
| A2 | 3.20 | 3.32 | 3.60 | 0.126 | 0.131 | 0.142 |
| D | 30.60 BSC | | | 1.205 BSC | | |
| D1 | 28.00 BSC | | | 1.102 BSC | | |
| E | 30.60 BSC | | | 1.205 BSC | | |
| E1 | 28.00 BSC | | | 1.102 BSC | | |
| R2 | 0.08 | X | 0.25 | 0.003 | X | 0.010 |
| R1 | 0.08 | X | | 0.003 | X | X |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ 1 | 0° | X | X | 0° | X | X |
| θ 2 | 8° REF | | | 8° REF | | |
| θ 3 | 8° REF | | | 8° REF | | |
| C | 0.09 | 0.15 | 0.20 | 0.004 | 0.005 | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.30 | | | 0.051 REF | | |
| S | 0.20 | X | X | 0.008 | X | X |

NOTES:

- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
- SIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. THE MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
- THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE.