

Ultra High Efficiency DC-DC Controller

FEATURES

- DC-DC SMPS controller with integrated drivers
- Constant ripple-current control allows
 optimum inductor size
- High Efficiency up to 94%
- High light load efficiency (>85% at 100mA)
- V_{OUT} accuracy 1%
- Input voltage from 3V to 30V
- Output voltage adjustable from 0.5V to 2.75V
- Output current up to 30A
- User adjustable operating frequency
- Dynamic voltage change support
- Voltage Feed-Forward Compensation Output Protection:
 - Latched Over Voltage Protection
 - Latched Under Voltage Protection
 - Valley type Over Current Protection
- Input Protection:
 - Under Voltage Lock Out on VDDA
 - Under Voltage Lock Out on VIN
- Power Good signal
- ON/SKIP signal
- Soft-Start at start-up with OCT protection
- Soft-Stop at shutdown

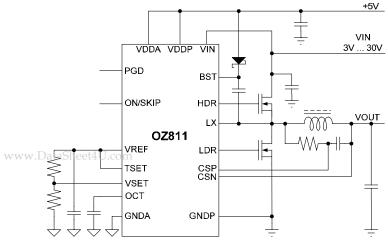
APPLICATIONS

Power Supplies for Notebook CPU and Peripherals

ORDERING INFORMATION

Part Number	Temp Range	Package	
OZ811LN	0°C to 85°C	QFN16 (4x4) Lead- Free	

SIMPLIFIED APPLICATION DIAGRAM



GENERAL DESCRIPTION

OZ811 is a DC/DC controller for the next generation of microprocessor power supplies, their peripherals and chipsets. OZ811 steps down the high battery voltage to low output voltages in the range of 0.5V to 2.75V. High efficiency, DC accuracy and excellent transient response make OZ811 the perfect choice for supplying low voltage CPU peripherals, chipset cores, and graphics processors. OZ811 is a constant ripple-current buck controller with powerful integrated drivers able to drive output currents up to 30A.

Voltage Feed-Forward compensation assures high rejection of input voltage transients typically occurring when the AC adapter is plugged in or removed.

Over Voltage Protection (OVP) acts when the output voltage exceeds the set voltage by more than 125mV. This protection condition is latched and initiates a ramp down of the output voltage.

Under Voltage Protection (UVP) acts when the output voltage falls below the set voltage by more than 133mV. This protection condition is latched and initiates a ramp down of the output voltage.

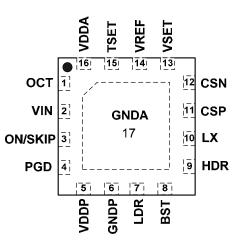
After OVP or UVP are triggered, the ON/SKIP pin should be toggled or VDDA/VIN cycled to restart the circuit.

The output is protected against overload by valley current type, cycle-by-cycle Over Current Protection (OCP) circuits.

The Under Voltage Lock Out circuit monitors both, VDDA and VIN and allows controller operation only if VDDA > 4.3V and VIN > 2.5V.

The Power Good signal is high as long as the output voltage is within +125mV/-133mV of the set voltage. At startup the output voltage ramps up in a controlled manner with a typical slew rate of 2V/ms and at shutdown the output voltage is ramped down in a controlled manner with the same slew rate, recovering the energy stored on the output capacitor and extending battery life.

PIN DIAGRAM



PIN DESCRIPTION

QFN	Name	I/O	Туре	Description
1	ОСТ	Р	Analog	Over Current Time-out. Time-out for Power Good assertion during startup. A capacitor setting the time-out should be connected between this pin and GNDA.
2	VIN	I	Analog	Input voltage sense. Used for feed-forward compensation. Also monitored by the Under Voltage Lock Out circuit. Enables controller only if VIN > 2.5V.
3	ON/SKIP	I	Digital	Enables operation. If V _{ON/SKIP} > 1.2V, the V _{OUT} voltage ramps up to the voltage set on VSET pin with a slew rate of 2V/ms. If V _{ON/SKIP} > 2.1V the controller enters skip mode of operation. If ON/SKIP is < 0.4V the chip is disabled and enters a very low consumption mode < 1 μ A. To re-enable the controller, the voltage on ON/SKIP pin needs to exceed 1V.
4	PGD	О	Digital	Power Good output for V_{OUT} . Open drain output asserted high when the output voltage V_{OUT} is within +125mV/-133mV of the set value.
5	VDDP	Р	Power	Positive supply for the low side driver. A 1µF capacitor should be placed from VDDP to GNDP.
6	GNDP	Р	Power	Power Ground.
7	LDR	0	Digital	Output of the low side driver.
8	BST	Р	Power	Positive supply for the high side driver. A 0.1μ F capacitor should be placed between BST and LX.
9	HDR	0	Digital	Output of the high side driver.
10	LX	Р	Power	Inductor switching node.
11	CSP		Analog	Non-inverting current sense pin.
12	CSN		Analog	Inverting current sense pin.
13	VSET	I	Analog	Sets the output voltage (V_{OUT}) of the controller. Uses a resistor divider from the reference voltage.
14	VREF	0	Analog	2.75V \pm 1% precision reference voltage. A 0.1µF should be placed from VREF to GNDA.
15	TSET	I	Analog	Adjust the T_{ON} of the controller according to the formula: $T_{ON} = \frac{1.6 \mu s \times V_{TSET}}{V_{IN} - V_{OUT}}$ A 0.1 μ F capacitor must be placed from TSET to GNDA.
16	VDDA	Р	Power	+5V supply for the controller analog circuits. A 1μF capacitor should be placed from VDDA to GNDA.
17	GNDA	Р	Power	Ground for the controller analog circuits.

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TYPICAL APPLICATION SCHEMATIC

+5\ +VDC +VIN +VIN M1 2x(BSC119N03S GNDP ____ CIN1 3x(10uF_25V) D3 L C1 0.22uF U1 15MQ040N 0.47uH_40A L1 RL=1mR R15 HDR SW VSET R1 22 >vout LDR Q1 2N7002_ R4 100k R5 300k 120k CSP CSP LX HDR BS R2 C2 R3 :470pF 120k 100k R13 ÷ D1 VSET VREF TSET VDDA **OZ811** DVC 🗌 14 15 /DDA 16 MBR0540 ӡ イ C3 4.7nF 51 R14 100k CSP ╢ C4 M2 2x(BSC022N03S) . C5 1uF CSN 17 GNDA PGD SOLT \checkmark R9 5 C10 VIN +VDC _____C9 _____1nF \sim _____C6 ____0.1uF C11 15k _____ 22nF \leftrightarrow COUT1 4x(150uF/4V イ 4 ON/SKIP (1.5V/1V)@30A R8 +3.3V D +3V3 \downarrow ÷ 0 R12 Signal Ground Power Ground 1k9 PGD Single point ground connection PGD 🔶

Figure 1: Typical Chipset Power Supply Schematic – OZ811LN

BILL OF MATERIALS

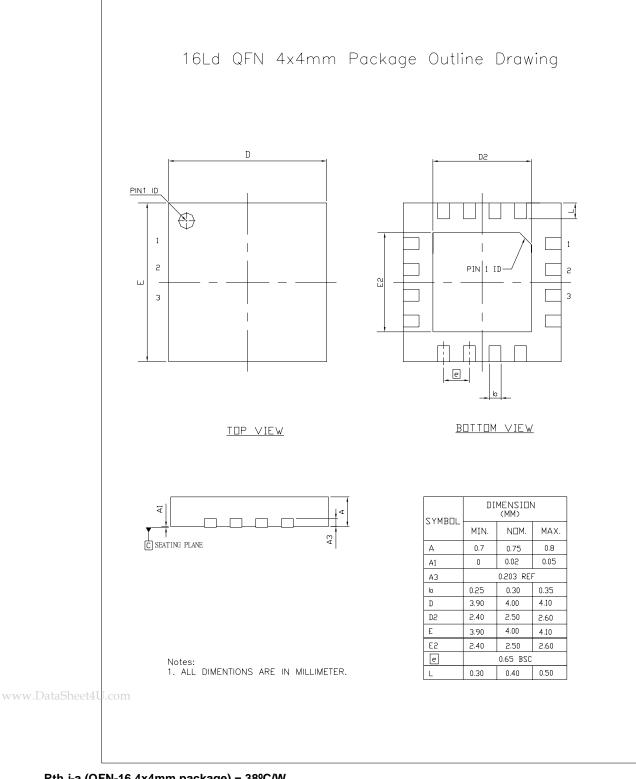
ltem	Qty	Reference	Value	Vendor	Part Number	PCB Footprint	
1 3		CIN1	10µ/25V	TDK	C4532X7R1E106M	1812	
1			10µ/23V	Johanson Dielectrics	250S43X106M		
2	4	COUT1	150µF/4V	Panasonic	EEFUE0J151R	D2E	
3	1	C6	0.1uF/10V	Any	Ceramic – X7R or X5R	0603	
4	1	C1	0.22µF	Any	Ceramic – X7R or X5R	0603	
5	2	C4, C5	1µF/10V	TDK	C1608X5R1A105K	0603	
5	2	04, 05	1μ17100	Johanson Dielectrics	100R14X105M		
6	1	C2	470pF				
7	1	C9	1nF/25V	Any	Ceramic – X7R or X5R	0603	
8	1	C10	22pf/25V	Any	Ceramic – X7R or X5R	0603	
9	1	C3	4.7nF/25V	Any	Ceramic – X7R or X5R	0603	
10	1	C11	22nF/10V	Any	Ceramic – X7R or X5R	0603	
11	1	R8	0Ω	Any	NONE	0603	
12	1	R13	51Ω	Any	NONE	0603	
13	1	R1	22Ω	Any	NONE	0603	
14	1	R12	1.9kΩ	Any	NONE	0603	
15	3	R3, R4, R14	100kΩ 1%	Any	NONE	0603	
16	2	R2, R15	120kΩ 1%	Any	NONE	0603	
17	1	R5	300kΩ	Any	NONE	0603	
18	1	D1	NONE	Vishay	MBR0540	SOD-123	
19	1	D3	NONE	Vishay	15MQ040N	SMA1	
20	1	Q1	NONE	Any	2N7002	SOT23	
21	2	M1	NONE	Infineon	BSC119N03S	PPAK SO-8	
22	2	M2	NONE	Infineon	BSC022N03S	PPAK SO-8	
23	1	L1	0.47µH/41A/1mΩ	Vishay	IHLP5050FDER0R47M01	-	
24	1	U1	NONE	O2Micro, Inc.	OZ811	QFN16	
#	24						

COMPONENT SUPPLIERS

Manufacturer	Contact Information			
Manufacturer	Phone	Website		
Power MOSFETs				
Infineon	+49 89 234 65555	www.infineon.com		
Inductors				
Vishay	1-402-563-6866	www.vishay.com		
TOKO	1-408-432-8281	www.toko.com		
Diode				
Vishay	1-402-563-6866	www.vishay.com		
Fairchild	1-703-478-5800	www.fairchildsemi.com		
Capacitors				
Vishay	1-847-803-6100	www.vishay.com		
Johanson Dielectrics	1-818-364-9800	www.johansondielectrics.com		
TDK	1-800-344-2112	www.tdk.com		
SANYO	N/A	http://www.sanyo.com/components		
Resistors				
Vishay	1-402-563-6866	www.vishay.com		
toShoot/IITDK	1-800-344-2112	www.tdk.com		

PACKAGE INFORMATION

Exposed pad is GNDA (pin 17) and must be fully soldered to PCB



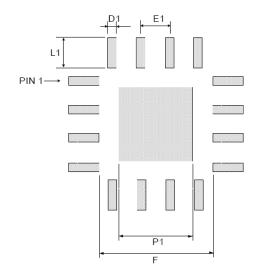
Rth j-a (QFN-16 4x4mm package) = 38°C/W Rth j-c (QFN-16 4x4mm package) = 4.8°C/W

DIMENSION TABLE

(16L QFN 4mmX4mm BODY)

SYMBOL	SPECIFICATION		
STWDOL	Min	Nom	Max
D1		0.32	
E1		0.65	
L1		0.80	
P1		2.50	
F		3.20	

LANDING PATTERN

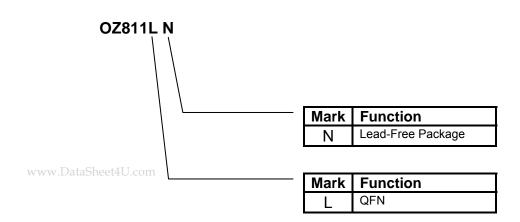


PACKAGE MARKING

Notes:

Controlling dimensions are in millimeters (mm).
 Pin #1 count orientation shall be in a

counterclockwise direction as viewed in live-bug position.



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