DATA SHEET

OM5193H
Disk drive spindle and VCM with servo controller

Product specification
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1 FEATURES

1.1 Servo control

- 10-bit VCM Digital-to-Analog Converter (DAC)
- 7-channel 10-bit Analog-to-Digital Converter (ADC)
- Programmable spindle commutation control logic
- 3-wire serial interface
- Two stand-alone operational amplifiers (op-amps) with outputs connected to the ADC
- Analog multiplexer with two inputs used to select VCM seek mode or track-following mode.

1.2 Motor control

1.2.1 SPINDLE MOTOR DRIVER

- 3-phase output motor driver
- 1.9 A maximum available start-up current
- Total $R_{ds(on)}$ = 0.6 Ω (typical) at 25 °C
- Back ElectroMotive Force (BEMF) processing for sensorless motor commutation
- Linear current control
- External current sense resistor
- External current control loop compensation
- Adjustable slew rate control
- Short-circuit brake
- Adjustable brake-after-park delay time.

1.2.2 VOICE COIL MOTOR DRIVER

- 1.5 A maximum current capability
- Total $R_{ds(on)}$ = 0.8 Ω (typical) at 25 °C
- Linear class AB output with low cross-over distortion delay
- Precision current control loop with external current sense resistor
- Programmable seek and track-following mode with adjustable current loop gain
- External current control loop compensation
- Precharge during brake mode
- 20 kHz current control loop bandwidth
- Parking function
- Adjustable park voltage with limiter.

1.3 Miscellaneous items

- Precision low voltage 5 and 12 V power monitor with hysteresis
- Precision internal voltage reference for servo and power control circuits
- Thermal sense circuit with over-temperature shutdown sensor
- Internal charge pump voltage generator
- Automatic brake-after-park at power-down, thermal shutdown or sleep mode
- Sleep mode: low power consumption mode.

2 APPLICATIONS

- 12 V hard disk drive products.

3 GENERAL DESCRIPTION

3.1 Overview

The OM5193H is a combination of a voice coil motor and a spindle motor driver with embedded servo controller designed for use in disk drives. Configuration and control registers are set via a 3-wire serial port running up to 30 MHz to interface commonly to a microcontroller or a digital signal processor.

The device operates at 5 and 12 V power supplies and integrates safety functions such as power stages overvoltage protection, power and temperature monitor, over-temperature shutdown and dynamic brake-after-park.

The device is contained in a QFP80 package with 18 pins connected to the leadframe thus providing low thermal resistance.

3.2 Servo controller

The servo controller includes the following circuits:

- 3-wire serial interface
- Spindle commutation logic
- A 10-bit ADC with 7 inputs selected by an internal multiplexer
- A 10-bit VCM DAC with 1.5, 2.5 and 3.5 V voltage references
- Two low-offset stand-alone op-amps
- Analog multiplexer with 2 inputs.

The serial interface is used:

- To adjust the timing parameters for proper spindle commutation sequence
- To accurately adjust head positioning via the 10-bit VCM DAC
- To set VCM seek or track-following mode via the low-impedance switch
- To select and process analog signals via a 7-channel multiplexer connected to the 10-bit ADC.

The spindle commutation logic circuit ensures proper spindle start-up (no reverse rotation) and commutation sequence for the spindle driver by processing BEMF sensing circuit output signals.

The two stand-alone op-amps, with the inputs connected to the read channel IC, provide servo track signals processed by the microcontroller to perform accurate track-following mode.

3.3 Spindle and voice coil motor

The OM5193H drives a 3-phase brushless, sensorless DC spindle motor and a voice coil motor.

Spindle and voice coil motor power stages with low $R_{ds(on)}$ and high current capability are suitable for mid-end and low-end 12 V disk drives. Power stages are designed in such a way that external Schottky diodes are not needed.

Spindle current is sensed by an external resistor and monitored by the external signal SPCC (SPindle Current Control). Spindle speed is regulated by the microcontroller via the ZCROSS signal (Zero CROSSing detection frequency output). BEMF comparators provide the digital zero crossing signals. These are processed by the commutation logic circuit to properly switch-on and switch-off spindle power drivers thus ensuring the rotation of the motor.

The control of the heads positioning is accomplished by the internal 10-bit VCM DAC. Seek and track-following VCM current loop gain is set by external resistors. VCM zero current is referenced to the 2.5 V internal voltage reference.

An internal precharge of the actuator (magnetic latch) during brake mode guarantees total control of the current when VCM starts running without current spikes.

3.4 Safety functions

The OM5193H is protected against transient voltage spikes that are generated by the inductive loads of spindle and VCM.

Power supplies and temperature are monitored in order to guarantee data reliability and self-protection of the device in case of power loss or temperatures beyond maximum rating.

Park and brake functions secure heads and disk media in case of power-down or high temperature failure. This function is also activated by the sleep mode.

An internal temperature monitor is available to monitor the chip temperature and thus prevents over-temperature shutdown. Internally connected to the ADC channel 4, it can be used by the microcontroller as an early ‘temperature-too-high’ warning during a long VCM seek sequence.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply voltage					
V_{DDA1}	5 V analog supply voltage	4.5	5.0	5.5	V
V_{DDD}	5 V digital supply voltage	4.5	5.0	5.5	V
V_{DDA2}	12 V analog supply voltage	10.8	12.0	13.2	V
Drivers					
I_{SPOUT}	spindle start-up current	–	–	1.9	A
I_{VCMRUN}	VCM current	–	–	1.5	A

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OM5193H	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body $14 \times 20 \times 2.8$ mm	SOT318-2

6 BLOCK DIAGRAMS

Figures 1, 2, 3 and 4 provide block diagrams of the OM5193H servo and motor control (top level diagram, servo controller, spindle motor driver and voice coil motor driver).

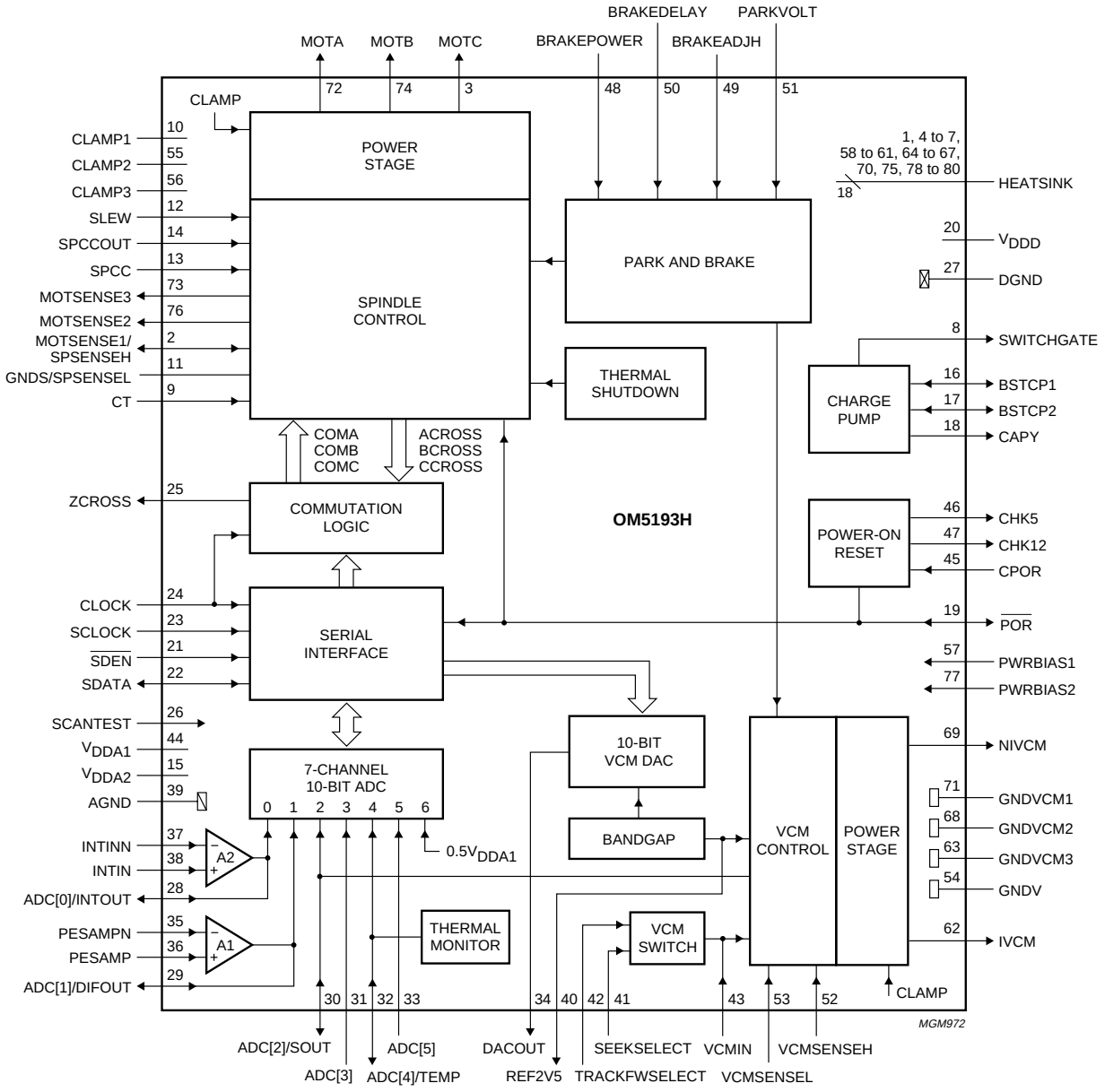


Fig.1 Block diagram, top level.

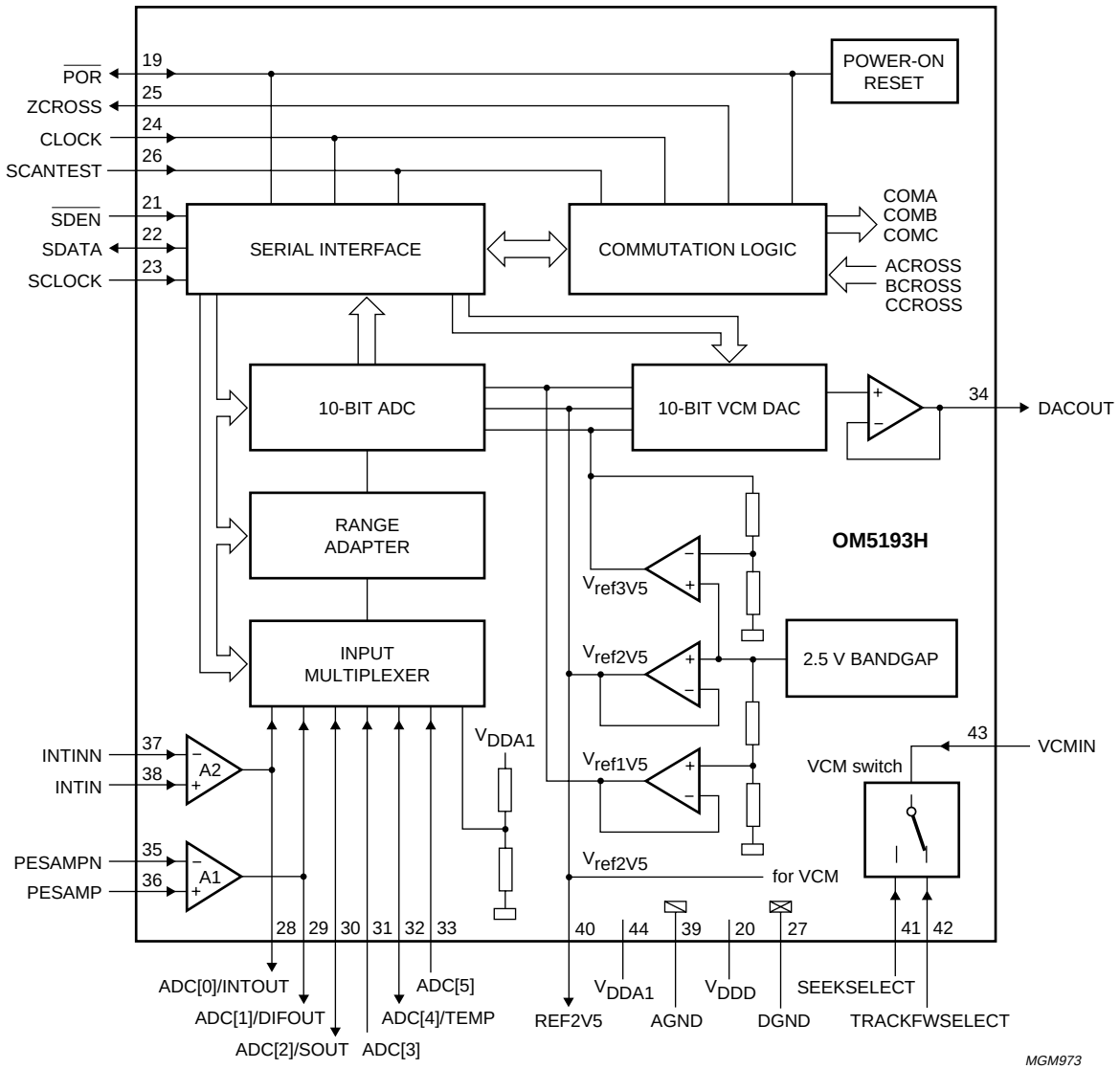


Fig.2 Block diagram, servo controller.

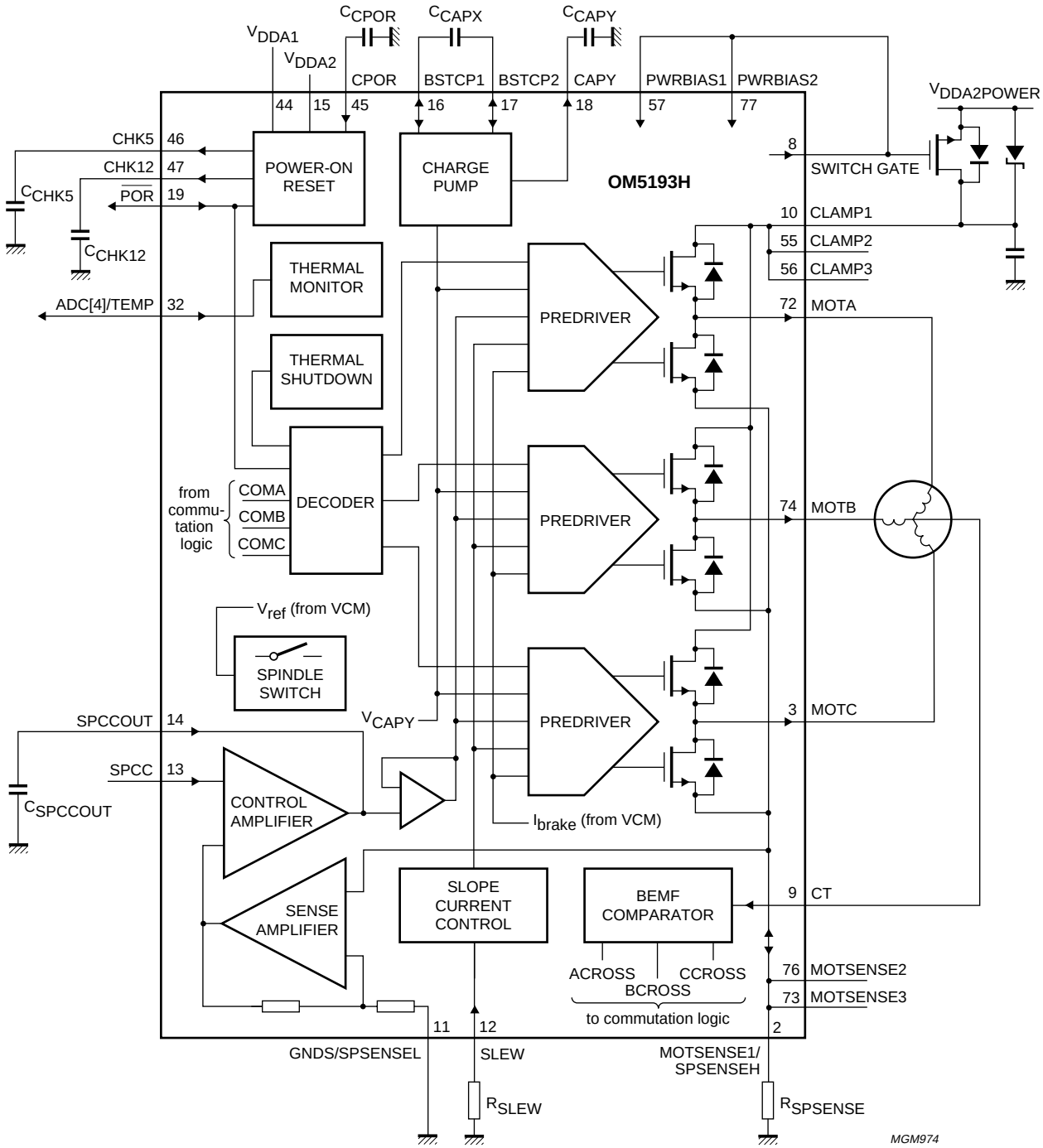


Fig.3 Block diagram, spindle motor driver.

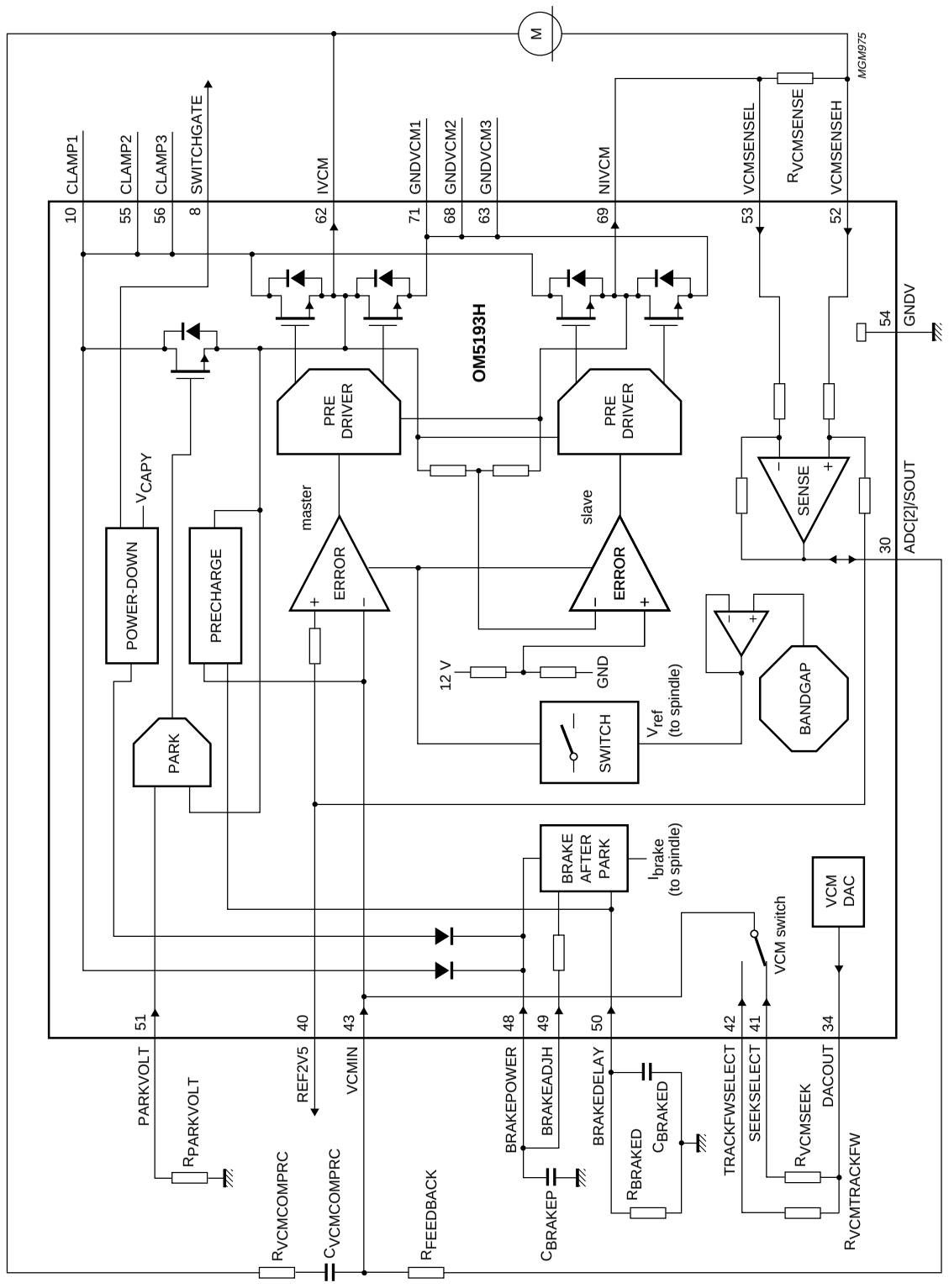


Fig.4 Block diagram, voice coil motor driver.

7 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
HEATSINK	1	–	dissipation pin; internally connected to the leadframe
MOTSENSE1/SPSENSEH	2	analog I/O	sense line of the spindle/spindle sense amplifier input
MOTC	3	analog output	spindle motor power output
HEATSINK	4	–	dissipation pin; internally connected to the leadframe
HEATSINK	5	–	dissipation pin; internally connected to the leadframe
HEATSINK	6	–	dissipation pin; internally connected to the leadframe
HEATSINK	7	–	dissipation pin; internally connected to the leadframe
SWITCHGATE	8	analog output	isolation FET driver
CT	9	analog input	centre tap of the spindle
CLAMP1	10	supply	power stage supply voltage
GNDS/SPSENSEL	11	ground	spindle ground connection/spindle sense amplifier ground
SLEW	12	analog input	spindle motor slope control
SPCC	13	analog input	spindle current control
SPCCOUT	14	analog input	compensation point of the spindle current control loop
V_{DDA2}	15	supply	12 V analog supply voltage
BSTCP1	16	analog I/O	booster capacitor 1
BSTCP2	17	analog I/O	booster capacitor 2
CAPY	18	analog output	DC-to-DC converter output (19 V)
$\overline{POR}$	19	digital I/O	power-on reset signal; active LOW
V_{DDD}	20	supply	5 V digital supply voltage
$\overline{SDEN}$	21	digital input	serial interface data enable; active LOW
SDATA	22	digital I/O	serial interface data line
SCLOCK	23	digital input	serial interface clock line
CLOCK	24	digital input	clock input
ZCROSS	25	digital output	zero crossing detection signal
SCANTEST	26	digital input	scantest mode control; at LOW-level in normal conditions
DGND	27	ground	servo digital ground
ADC[0]/INTOUT	28	analog I/O	ADC channel 0 input/output of the A2 amplifier
ADC[1]/DIFOUT	29	analog I/O	ADC channel 1 input/output of the A1 amplifier
ADC[2]/SOUT	30	analog I/O	ADC channel 2 input/VCM sense amplifier output
ADC[3]	31	analog input	ADC channel 3 input
ADC[4]/TEMP	32	analog I/O	ADC channel 4 input/temperature monitor, thermal shutdown
ADC[5]	33	analog input	ADC channel 5 input
DACOUT	34	analog output	10-bit VCM DAC output
PESAMPN	35	analog input	inverting input of the A1 amplifier.
PESAMP	36	analog input	non-inverting input of the A1 amplifier
INTINN	37	analog input	inverting input of the A2 amplifier
INTIN	38	analog input	non-inverting input of the A2 amplifier
AGND	39	ground	servo analog ground
REF2V5	40	analog output	2.5 V bandgap reference voltage

SYMBOL	PIN	I/O	DESCRIPTION
SEEKSELECT	41	analog input	input for the seek mode
TRACKFWSELECT	42	analog input	input for the track-following mode
VCMIN	43	analog input	VCM control input
V_{DDA1}	44	supply	5 V analog supply voltage
CPOR	45	analog input	set the $\overline{POR}$ delay time
CHK5	46	analog output	set the V_{DDA1} POR threshold
CHK12	47	analog output	set the V_{DDA2} POR threshold
BRAKEPOWER	48	analog input	brake power capacitor
BRAKEADJH	49	analog input	adjust current consumption during park mode
BRAKEDELAY	50	analog input	set the brake-after-park delay time
PARKVOLT	51	analog input	set the park voltage
VCMSENSEH	52	analog input	positive input of the VCM sense amplifier
VCMSENSEL	53	analog input	negative input of the VCM sense amplifier
GNDV	54	ground	VCM ground connection
CLAMP2	55	supply	power stage supply voltage
CLAMP3	56	supply	power stage supply voltage
PWRBIAS1	57	analog input	power stages isolation bias; externally connected to the clamp
HEATSINK	58	–	dissipation pin; internally connected to the leadframe
HEATSINK	59	–	dissipation pin; internally connected to the leadframe
HEATSINK	60	–	dissipation pin; internally connected to the leadframe
HEATSINK	61	–	dissipation pin; internally connected to the leadframe
IVCM	62	analog output	inverted output of the VCM (master stage)
GNDVCM3	63	ground	VCM power stage ground
HEATSINK	64	–	dissipation pin; internally connected to the leadframe
HEATSINK	65	–	dissipation pin; internally connected to the leadframe
HEATSINK	66	–	dissipation pin; internally connected to the leadframe
HEATSINK	67	–	dissipation pin; internally connected to the leadframe
GNDVCM2	68	ground	VCM power stage ground
NIVCM	69	analog output	non-inverted VCM output (slave stage)
HEATSINK	70	–	dissipation pin; internally connected to the leadframe
GNDVCM1	71	ground	VCM power stage ground
MOTA	72	analog output	spindle motor power output
MOTSENSE3	73	analog output	sense line of the spindle
MOTB	74	analog output	spindle motor power output
HEATSINK	75	–	dissipation pin; internally connected to the leadframe
MOTSENSE2	76	analog output	sense line of the spindle
PWRBIAS2	77	analog input	power stages isolation bias; externally connected to the clamp
HEATSINK	78	–	dissipation pin; internally connected to the leadframe
HEATSINK	79	–	dissipation pin; internally connected to the leadframe
HEATSINK	80	–	dissipation pin; internally connected to the leadframe

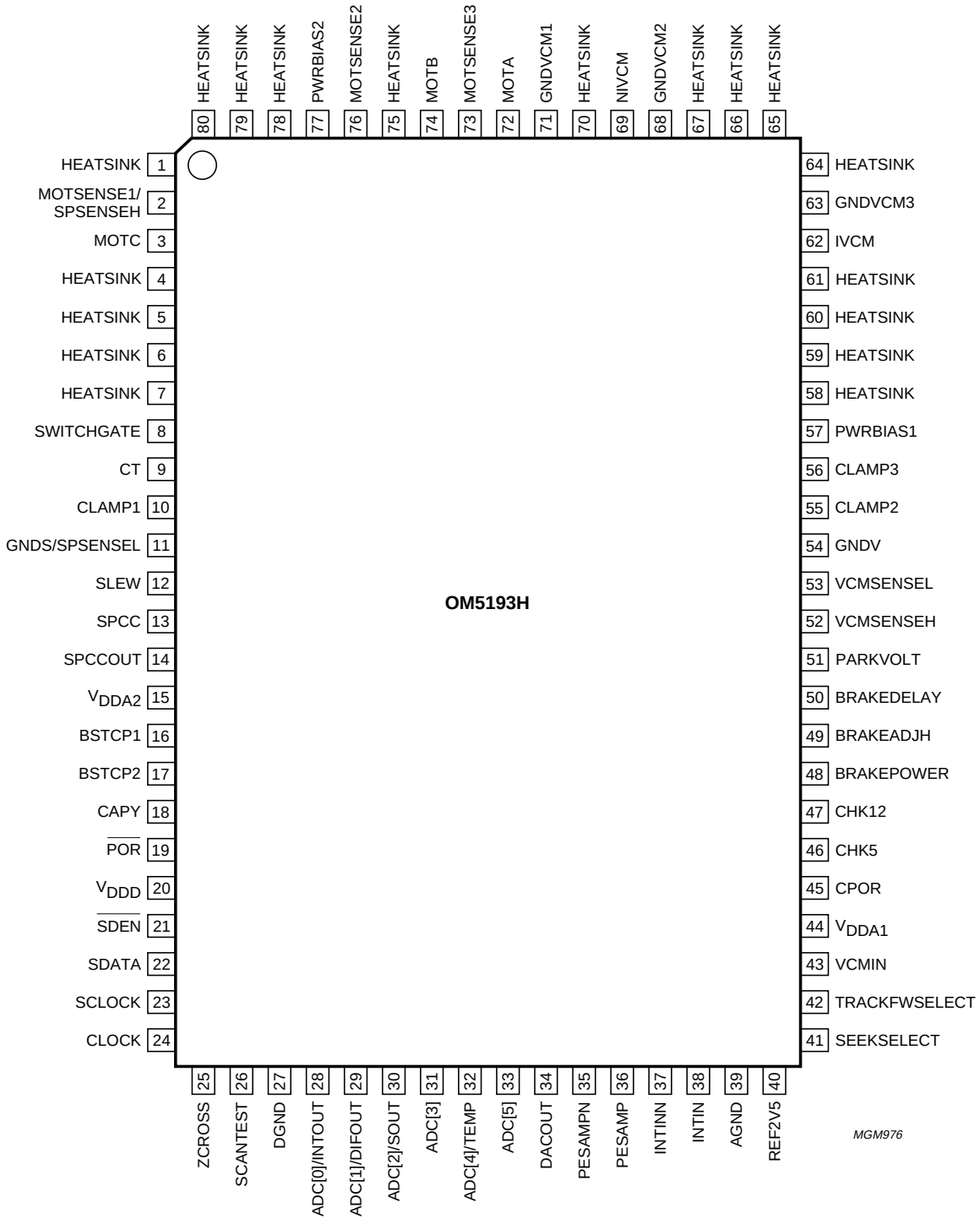


Fig.5 Pin configuration.

8 FUNCTIONAL DESCRIPTION

8.1 Serial interface

The serial interface is a 3-wire bidirectional port for writing and reading data to and from the internal registers of the OM5193H. Each read or write will be composed of 16 bits. For data transfer $\overline{SDEN}$ is brought LOW, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLOCK pin. After the $\overline{SDEN}$ pin goes LOW, the first 16 pulses applied to the SCLOCK pin shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock pulse. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when $\overline{SDEN}$ goes HIGH. If less than 16 clock pulses are provided before $\overline{SDEN}$ goes HIGH, the data transfer is aborted.

All transfers are shifted into the serial port with the MSB first. The first 4 bits of the transfer contain address and instruction information. The MSB is the R/$\overline{W}$ bit which determines if the transfer is a read (logic 1) or a write (logic 0).

The remaining 3 bits determine the internal register to be accessed. The other 12 bits contain the programming data. In the read mode (R/$\overline{W}$ = 1), the OM5193H outputs the register contents of the selected address. In the write mode (R/$\overline{W}$ = 0), the OM5193H loads the selected register with the data presented on the SDATA pin. During sleep mode, the serial port remains active and register programmed data is retained.

SCLOCK is driven by the microcontroller. When the microcontroller drives the SDATA line, the data is valid on the rising edge of SCLOCK. When the OM5193H is driving the SDATA line (in read mode after the R/$\overline{W}$ bit and 3 bits) the data is valid on the falling edge of SCLOCK.

$\overline{SDEN}$ marks the end of the serial transfer. When the $\overline{SDEN}$ pin goes HIGH, the shift register data is latched into the addressed register of the OM5193H.

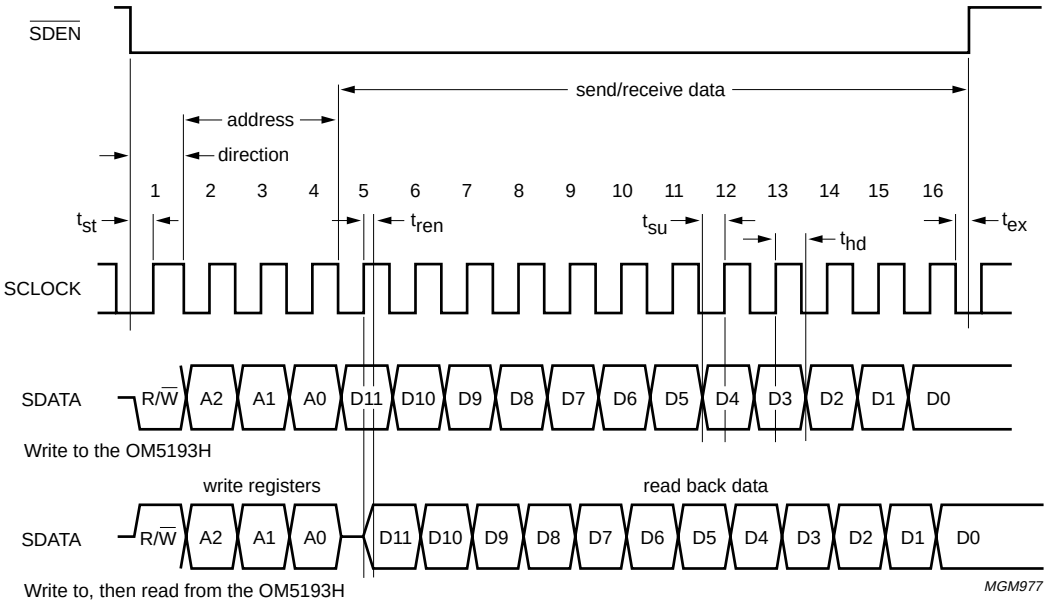


Fig.6 Serial port timing information.

Table 1 Timing information for the serial interface

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
f_{clk}	clock frequency	–	30	MHz
t_{st}	chip select to first active clock edge	$\frac{1}{2}T_{clk}$	–	ns
t_{su}	data to clock set-up time	12	–	ns
t_{hd}	clock to data hold time	12	–	ns
t_{rd}	time data line is driven after 5th negative clock	–	5	ns
t_{ren}	time from positive clock for data line to be driven	0	–	ns
t_{rhd}	receive data hold time	0	–	ns
t_{rsu}	receive data set-up time	12	–	ns
t_{exW}	last active clock to chip select; inactive on write	0	–	ns
t_{exR}	last active clock to chip select; inactive on read	10	–	ns
T_{bpa}	time between successive serial port accesses	5	–	clock cycles

Table 2 Writeable registers of the serial interface

REG	BITS											
	11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	not used		opamp Select_N	increm. Channel	auto Conv. select	range Select	test Mode_N	not used		ADC MUX address		
1	reverse break	not used	seek/ trackfw	not used		sleep_N	spindiv	manual	run/ stop	comC	comB	comA
2	not used		DAC (9)	DAC (8)	DAC (7)	DAC (6)	DAC (5)	DAC (4)	DAC (3)	DAC (2)	DAC (1)	DAC (0)
3	not used											
4	not used											
5	Watchdog						Blank 1					
6	high Clock_N	Comdelim										
7	Start-up						Blank 2					

Table 3 Readable registers of the serial interface

REG	BITS											
	11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0		ADC status	ADC (9)	ADC (8)	ADC (7)	ADC (6)	ADC (5)	ADC (4)	ADC (3)	ADC (2)	ADC (1)	ADC (0)
1										Ccross	Bcross	Across

Table 4 Address of registers

R/$\overline{W}$	A2	A1	A0	REG.	DESCRIPTION
0	0	0	0	0	ADC channel and programmable options
1	0	0	0	0	ADC status and value
0	0	0	1	1	commutation, sleep, and VCM switch controls
1	0	0	1	1	commutation state in manual mode
0	0	1	0	2	10-bit DAC
0	0	1	1	3	not used
0	1	0	0	4	not used
0	1	0	1	5	Blank 1 and Watchdog delays
0	1	1	0	6	commutation delay limit (11 bits), internal clock divider factor
0	1	1	1	7	Start-up and Blank 2 delays

8.2 Commutation and sleep mode

Spindle control and sleep mode are controlled by writing or reading on register#1.

- Register#1 (0, 1 and 2) control the spindle commutations in manual mode when run/stop, manual and sleep bits are correctly set. The commutation sequence is described in Section “Spindle driver” (see also Table 16 and Fig.12).
- Register#1 (3) is the run/stop bit. After the power is turned on and $\overline{POR}$ is HIGH, the motor will not start spinning until register#1 (3) has been set to logic 1. The motor stops spinning when this bit is set to logic 0.
- Register#1 (4) is the manual commutation mode bit. When this bit is set to logic 1 and register#1 (3) set to logic 1, the commutation logic in the OM5193H will be disabled so that the spindle will not automatically go to the next commutation.

  When register#1 (3 and 4) are set to logic 1, the microcontroller is expected to generate the different commutation states for the motor. The OM5193H will still provide the coil status which will be available by reading register#1. The different waveforms are shown in Section “Spindle driver” (see also Fig.12). Note that depending on the coil status acquisition moment, transient states (due to the flyback pulses) can be read.

  When register#1 (4) is set to logic 0, the manual mode is disabled and the OM5193H will automatically commutate the motor each time a zero crossing is detected. The time between the zero crossing and the next commutation is half the time between the two preceding zero crossings. This is explained in the detailed description in Section “Commutation control”.
- Register#1 (5) is the spindiv bit. This bit together with register#6 (11) enables the selection of a divider factor for both converter clock and spindle clock. Clock configurations are described in Section “Commutation control” (see also Table 6).
- Register#1 (6) is the sleep mode bit. When it is set to logic 0, the OM5193H will enter the low power mode. Then the commutation control generates (101) output codes on commutation signals to set spindle and VCM head into sleep mode. This causes the OM5193H to go into the brake-after-park mode. The only operating circuits are the power monitor, the voltage reference generator, the VCM precharge circuit and the serial interface. The OM5193H is in sleep mode when $\overline{POR}$ is LOW.

  When the power is first turned on, the $\overline{POR}$ signal goes HIGH after the POR delay. The OM5193H is then automatically set in sleep mode and thus in low power consumption mode. The VCM DAC output is in high-impedance mode, the spindle is in the brake mode and the VCM is in the precharge mode. Only after $\overline{POR}$ is HIGH and register#1 (6) is set to logic 1, OM5193H is ready to be functional. When register#1 (6) goes HIGH, the VCM DAC outputs the 2.5 V reference voltage.
- Register#1 (11) is dedicated to brake the spindle motor without going in ‘brake-after-park’ mode.
  The commutation sequence is shifted in order to efficiently brake the motor. This brake, called reverse brake, is activated when register#1 (11) bit is set to logic 1. Note that there is no action on the VCM input signal when the reverse brake is used. When this bit is set to logic 0, the spindle motor starts again with normal spindle commutations.

Reading register#1 will read the state of the 3 coils coming from the spindle control block (ACROSS, BCROSS and CCROSS). The 3 input lines will be in bits 0, 1, and 2. The different waveforms are shown in Section “Spindle driver” (see also Fig.12). Note that depending on the coil status acquisition moment, transient states (due to the flyback pulses) can be read.

Table 5 Writing register#1

BIT	DEFAULT VALUE	NAME	DESCRIPTION
0	0	comA	drives COMA when in manual commutation
1	0	comB	drives COMB when in manual commutation
2	0	comC	drives COMC when in manual commutation
3	0	run/stop	0 = motor to brake-after-park mode 1 = motor spinning; VCM active
4	0	manual	0 = automatic commutation mode with run/stop = 1 1 = manual commutation mode with run/stop = 1
5	0	spindiv	0 = the internal spindle clock frequency is controlled by register#6 (11) (bit highClock_N) 1 = an additional divider by 4 is added on the internal spindle clock
6	0	sleep_N	0 = sleep mode: low power mode, serial interface active, power stages in brake-after-park mode 1 = fully functional mode: sleep_N has higher priority than run/stop if both are active
7	0	–	not used
8	0	–	not used
9	1	seek/trackfw	0 = VCMIN connected to SEEKSELECT 1 = VCMIN connected to TRACKFWSELECT
10	1	–	not used
11	0	reverse break	1 = active brake control 0 = normal commutations as defined by bits above

8.3 Commutation control

The commutation logic block generates the six different states to rotate the spindle motor. The spindle driver block provides the BEMF zero crossing information.
The commutation block interprets the zero crossing information and determines the commutation delay time and the next coil state. The commutation block must take into account the following situations:

- Start-up
- No start
- Reverse rotating
- Run
- Manual commutation.

The commutation logic keeps the motor spinning by commutating the motor after each detected zero crossing. It measures the time between two successive BEMF zero crossings and then determines the next commutation. The delay (commutation delay) between a zero crossing and the next commutation is half the time between the two preceding zero crossings. The commutation delay (Comdelim) can be limited to guarantee a faster lock after the motor has gone out of lock. A maximum commutation delay can be set via the serial port. The time is a function of both the external clock frequency, the individual register prescalers and the time programmed into the registers. Figure 7 shows a typical motor commutation timing diagram.

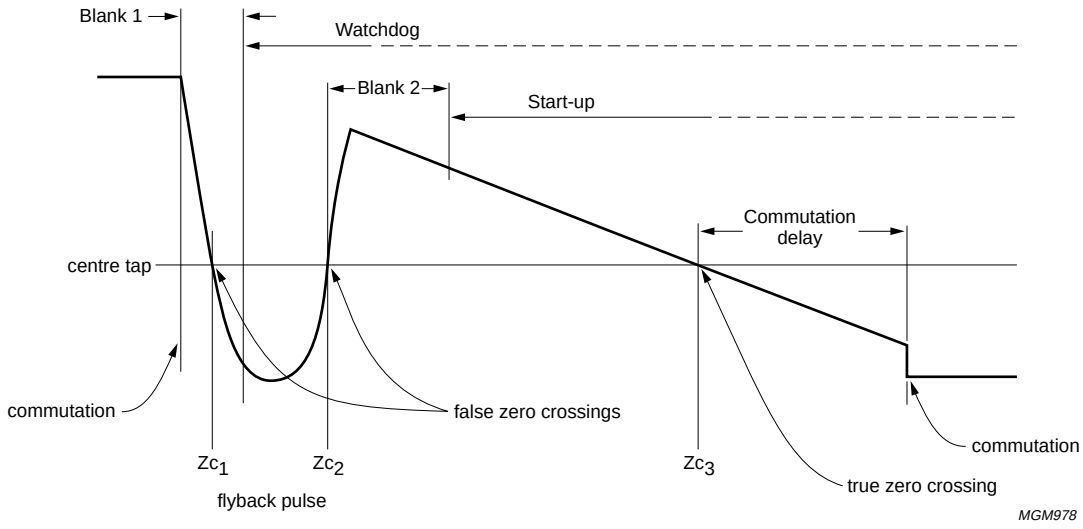


Fig.7 A typical motor commutation diagram.

- Blank 1
  After a commutation occurs, the leading edge of the flyback pulse has a zero crossing (Zc_1). Blank 1 timer is used to ignore this zero crossing by masking it while the timer initialized at Blank 1 value is counting. The state associated to Blank 1 down-counter will end when the counter reaches the zero value.
- Blank 2
  The Blank 2 timer starts counting as soon as the second zero crossing occurs (Zc_2). After the second flyback pulse zero crossing, all extra zero crossings are ignored during the Blank 2 time. This allows the ringing of the coil voltage without causing a commutation advance. The state associated to Blank 2 down-counter will end when the counter reaches the zero value.
- Watchdog
  The Watchdog timer makes sure the motor is running in forward direction. If the motor is rotating in reverse direction, the BEMF voltage is inverted and the second crossing of the flyback pulse (Zc_2) will not occur until the true BEMF zero crossing is detected. Therefore, if the Watchdog timer expires before a zero crossing occurs, the motor is assumed to be rotating backwards.
  The commutation is advanced by one step to correct this condition. The Watchdog time must be set to a value that is greater than the flyback pulse duration, measured when the spindle motor stands still.
  The state associated to the Watchdog timer will start when the one associated to Blank 1 timer is finished and will end when Zc_2 occurs or when the Watchdog counter expires.
- Start-up
  If the motor is not spinning, the BEMF zero crossings will not occur. The Start-up timer detects this if it expires before the true zero crossing (Zc_3) has occurred. It will advance the commutation by one step if this happens. The state associated to Start-up timer will start when the one associated to Blank 2 timer is finished and will end when Zc_3 occurs or when Start-up expires.
- Comdelim
  The timer associated to Comdelim value allows to control the maximum commutation delay (between zero crossing and next commutation). When the true zero crossing is detected (Zc_3), the timer will count until it expires and then will commutate the motor to the next step. This commutation delay time is equal to half the measured value between 2 zero crossings.
  The Comdelim value should be set to the maximum allowable delay value. If ΔZc_{meas} is lower than the programmed Comdelim value, the next timer value will be ΔZc_{meas} divided by 2. If ΔZc_{meas} is higher than the programmed Comdelim value, the next timer value will be the programmed Comdelim value divided by 2.

The clock used in the commutation logic block is obtained by dividing the master clock of the chip (f_{CLOCK}) by a clock divider (Prescaler). This internal clock will be named internalSpindleClock. Internal spindle clock configurations are described in Table 6.

All the delays described above (Blank 1, Watchdog, Blank 2, Start-up and Comdelim) are generated by one down-counter (called TIMER 1), see Fig.8 and one up-counter (called TIMER 2), see Fig.9. Each of them uses internalSpindleClock signal.

Table 6 Spindle clock configurations

spindiv REGISTER#1 (5)	highClock_N REGISTER#6 (11)	internalSpindleClock
0	0	$1/16 f_{CLOCK}$
0	1	$1/32 f_{CLOCK}$
1	0	$1/64 f_{CLOCK}$
1	1	$1/128 f_{CLOCK}$

8.3.1 Blanks, Watchdog and Start-up delays

An internal down-counter called TIMER 1 is used to generate Blank 1, Blank 2, Watchdog and Start-up delays. It loads one of these programmed values and counts down till it reaches zero.

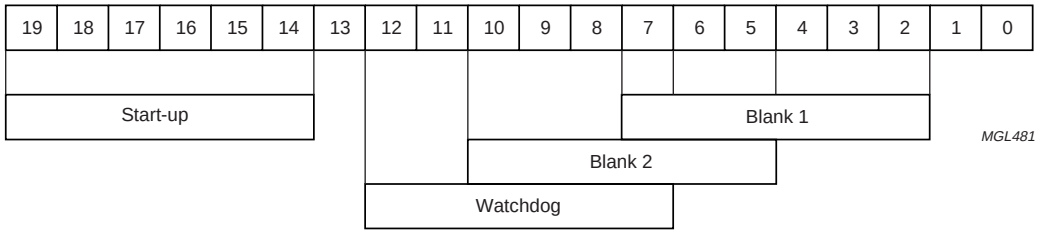


Fig.8 Down-counter TIMER 1.

The actual delay time will be:

$$Delay = value \times step \quad (1)$$

Value is the decimal representation of the binary code programmed in one of the 6 bit registers.

$$Step = \frac{2^{LSB}}{internalSpindleClock} \quad (2)$$

$$maxValue = \frac{\left(2^{(MSB+1)} - 1\right) - \left(2^{LSB} - 1\right)}{internalSpindleClock} = \frac{2^{(MSB+1)} - 2^{LSB}}{internalSpindleClock} \quad (3)$$

We have to subtract ($2^{LSB} - 1$) to obtain maxValue because all the bits from 0 to (LSB – 1) are set internally to zero by design.

Table 7 Delays used for TIMER 1

DELAY	LSB	MSB	BITS
Blank 1	2	7	6
Blank 2	5	10	6
Watchdog	7	12	6
Start-up	14	19	6

Table 8 Numerical application with f_{CLOCK} = 30 MHz

DELAYS	internalSpindleClock							
	$^1/_{16}f_{CLOCK}$		$^1/_{32}f_{CLOCK}$		$^1/_{64}f_{CLOCK}$		$^1/_{128}f_{CLOCK}$	
	STEP	MAX.	STEP	MAX.	STEP	MAX.	STEP	MAX.
Blank 1; note 1	2.13 µs	134 µs	4.27 µs	269 µs	8.53 µs	538 ms	17.1 µs	1.08 ms
Blank 2; note 2	17.1 µs	1.08 ms	34.1 µs	2.15 ms	68.3 µs	4.30 ms	137 µs	8.60 ms
Watchdog; note 3	68.3 µs	4.30 ms	137 µs	8.60 ms	273 µs	17.2 ms	546 µs	34.4 ms
Start-up; note 4	8.74 ms	550 ms	17.5 ms	1.101 s	35 ms	2.202 s	70 ms	4.404 s

Notes

1. The first zero crossing of the flyback should occur within this time.
2. The real zero crossing should not come within this time after the second zero crossing of the flyback pulse.
3. The time should be larger than the duration of the flyback pulse measured when the motor stands still.
4. The actual zero crossing should occur within this time after the Blank 2 time has expired.

8.3.2 COMDELIM DELAY

An internal up-counter called TIMER 2 is used to measure the time between two zero crossings and also to set the maximum commutation delay through Comdelim delay.

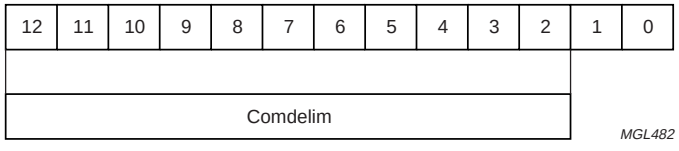


Fig.9 Up-counter TIMER 2.

Comdelim is the maximum value that can be reached by TIMER 2. So, this is the maximum time between 2 zero crossings (ΔZc). The maximum commutation delay (Comdelim delay) is then half this value.

The actual delay will be:

$$\Delta Zc = value \times step + Offset \quad (4)$$

$$ComdelimDelay = \frac{\Delta Zc}{2} \quad (5)$$

Value is the decimal representation of the binary code programmed in the 11-bit register.

$$Step = \frac{2^{LSB}}{internalSpindleClock} \quad (6)$$

$$Offset = \frac{3}{internalSpindleClock} \quad (7)$$

(we have to add this offset because bits 0 and 1 are set internally to logic 1 by design).

$$maximum\Delta Zc = \frac{2^{(MSB+1)} - 1}{internalSpindleClock} \quad (8)$$

$$maximumComdelimDelay = \frac{2^{(MSB)} - \frac{1}{2}}{internalSpindleClock} \quad (9)$$

Table 9 Delay used for TIMER 2

DELAY	LSB	MSB	BITS
Comdelim	2	12	11

Table 10 Numerical application with f_{CLOCK} = 30 MHz

DELAYS	CLOCKOUT/PRESCALER											
	$^1/_{16}f_{CLOCK}$			$^1/_{32}f_{CLOCK}$			$^1/_{64}f_{CLOCK}$			$^1/_{128}f_{CLOCK}$		
	STEP (μs)	OFFSET (μs)	MAX. (ms)	STEP (μs)	OFFSET (μs)	MAX. (ms)	STEP (μs)	OFFSET (μs)	MAX. (ms)	STEP (μs)	OFFSET (μs)	MAX. (ms)
ΔZc	2.13	1.6	4.37	4.27	3.2	8.74	8.53	6.4	17.48	17.1	12.8	35
Comdelim delay	1.07	0.8	2.18	2.13	1.6	4.37	4.27	3.2	8.74	8.53	6.4	17.48

The commutation delay counter, which starts counting at a zero crossing, has two operating modes:

- In the adaptive mode, the next zero crossing is detected before the commutation delay counter has reached its programmed value. In this mode, the next commutation will occur at the measured t_{Zcross} divided by 2 after the last zero crossing.
- In the forced mode, the next zero crossing is detected after the commutation delay counter reaches its programmed value. In this mode, the counter is stopped and the commutation logic block waits until the next zero crossing occurs. After it occurs, the next commutation will be forced at the programmed commutation delay divided by 2.

8.4 10-bit ADC with 7 analog inputs

The ADC is a signed 10-bit converter which uses the successive approximation conversion technique.
The overall accuracy is 2% absolute error not including contribution of the reference voltage and guaranteed monotonicity.

8.4.1 INPUT CHANNELS

7 analog input channels can be sampled and converted:

- Channel 0: conversion of the op-amp A2 output
- Channel 1: conversion of the op-amp A1 output
- Channel 2: conversion of the VCM sense amplifier output
- Channel 3: conversion of an analog external signal
- Channel 4: conversion of the temperature monitor + temperature shutdown signal
- Channel 5: conversion of an analog external signal
- Channel 6: conversion of an internal signal, controlling analog supply voltage over two ranges.

Channels 0 and 1 can be used as external inputs by deactivating the 2 stand-alone op-amps A1 and A2 (op-amps are put in sleep mode), that means by putting register#0 (9) at logic 1.

The ADC does not include input filtering. If this is required in the application then it must be implemented externally.

8.4.2 INPUT RANGES

Two analog input ranges are possible: either between 1.5 and 3.5 V or between 0 and 5 V. The input range is selected with register#0 (6):

- Register#0 (6) = 0: means input analog value between 1.5 and 3.5 V
- Register#0 (6) = 1: means input analog value between 0 and 5 V.

Table 11 Input analog voltage and corresponding output code

BIT	MIN. OUTPUT = 200H	MIDDLE OUTPUT = 000H	MAX. OUTPUT = 1FFH
register#0 (6) = 0	minimum input value = 1.5 V	middle input value = 2.5 V	maximum input value = 3.5 V
register#0 (6) = 1	minimum input value = 0 V	middle input value = 2.5 V	maximum input value = 5 V

8.4.3 CONVERSION MODES

Three different conversion modes are possible depending on the states of register#0 (7) and register#0 (8):

- Auto conversion and input channel auto incrementation mode.

  This mode is obtained with register#0 (7) = 1 and register#0 (8) = 1. The conversion sequence works as follows: the first A/D conversion is started by writing to serial port register#0. The address of the channel is decoded from the three LSBs in register#0 [2 to 0]. Then the OM5193H selects the addressed analog channel, samples and holds the analog input and starts the analog to digital conversion. The conversion result is obtained by reading the serial port register#0. Register#0 (10) provides the status of the conversion: it is set to 0 as long as the conversion is running and indicates that the low 10 bits of register#0 are invalid. Register#0 (10) going HIGH means the conversion is complete and guarantees the validity of the data in register#0 [9 to 0].

- Auto conversion on the same channel.

  This input channel automatic incrementation option can be deactivated by setting register#0 (8) to logic 0 with register#0 (7) at logic 1. So the behaviour of the ADC is the same as explained above, except that all the conversions are made on the channel specified by the last write access on register#0.

- Single conversion mode.

  The automatic conversion mode can also be deactivated by setting register#0 (7) to logic 0. In this mode, a write access on register#0 will start a conversion on the specified channel and a read access will not launch any other conversion.

8.4.4 PROGRAMMING REGISTER#0

Table 12 Writing register#0

BIT	DEFAULT VALUES	NAME	DESCRIPTION
0		ADC MUX address; note 1	ADC MUX address 0
1			ADC MUX address 1
2			ADC MUX address 2
3		not used	
4		not used	should be at logic 0 under normal operating conditions
5	0	testMode_N	dedicated for test purposes of the DAC in ADC or DAC mode; should be at logic 0 under normal operating conditions
6	0	rangeSelect	selects the analog input range of the ADC: 0 = range 1.5 to 3.5 V 1 = range 0 to 5 V
7	0	autoConvSelect	selects the automatic conversion option; see details in Table 13
8	0	incrementChannel	selects the automatic channel increment option; see details in Table 13
9	0	opampSelect_N	selects the stand-alone op-amps: 0 = op-amps activated 1 = op-amps deactivated
10		not used	
11		not used	

Note

1. Possible addresses:
   a) ADC MUX address = 000: channel 0 selected;
   b) ADC MUX address = 001: channel 1 selected;
   c) ADC MUX address = 010: channel 2 selected;
   d) ADC MUX address = 011: channel 3 selected;
   e) ADC MUX address = 100: channel 4 selected;
   f) ADC MUX address = 101: channel 5 selected;
   g) ADC MUX address = 110: channel 6 selected;
   h) ADC MUX address = 111 is an illegal address. No analog input will be selected if a conversion is asked in this channel and the ADC will convert a random analog value.

For a correct initialization of the converter just after power up, when $\overline{\text{POR}}$ is HIGH (before using the ADC or the DAC), the register#0 has to be programmed as follows: write 020H and then write 000H. A read of register#0 between the 2 write accesses is not necessary.

Table 13 Truth table for bits 7 and 8 on register#0 in write mode; conversion mode options; note 1

autoConvSelect REGISTER#0 (7)	incrementChannel REGISTER#0 (8)	DESCRIPTION
0	0	Default state: no auto channel incrementation, no A/D conversion started automatically after each read of the result.
1	0	Starts automatically an A/D conversion on the same channel (no channel incrementation) after each read of the result.
1	1	Starts automatically an A/D conversion on the next channel (increment the channel by 1) after each read of the result.
0	1	No auto channel incrementation, no A/D conversion started automatically after each read of the result (similar to the default state '00').

Note

1. The autoConvSelect bit has priority over the incrementChannel bit.

8.4.5 Converter clock frequency values

The ADC internal clock named converterClock can have two different frequency values by programming register#6 (11) (bit highClock_N):

Register#6 (11) = 1: means converterClock = Master clock (f_{CLOCK}) divided by 8 (clockDivider = 8)

Register#6 (11) = 0: means converterClock = Master clock (f_{CLOCK}) divided by 4 (clockDivider = 4)

$$\text{conversionTime} = \frac{13 \times \text{clockDivider}}{f_{CLOCK}} \quad (10)$$

Table 14 Numerical application

TIME	MASTER CLOCK = 10 MHz		MASTER CLOCK = 20 MHz		MASTER CLOCK = 30 MHz	
	DIVISION BY 8	DIVISION BY 4	DIVISION BY 8	DIVISION BY 4	DIVISION BY 8	DIVISION BY 4
Conversion time	10.4 µs	5.2 µs	5.2 µs	2.6 µs	3.4 µs	1.7 µs

8.5 10-bit VCM DAC

The VCM DAC is a signed 10-bit digital-to-analog convertor. It will start the conversion when register#2 is written. The lowest 10 bits contain the value to be converted.

Table 15 Input code and corresponding output analog voltage

INPUT CODE	OUTPUT VOLTAGE
200H	1.5 V
000H	2.5 V
1FFH	3.5 V

The overall accuracy is 2% absolute error not including the contribution of the reference voltage and guaranteed monotonicity.

8.6 Reference voltage

V_{ref2V5} is a 2.5 V bandgap reference used as the reference voltage for the VCM circuit. Stable voltages of 1.5 and 3.5 V are generated from the 2.5 V reference and used as reference voltages for the VCM DAC and for the ADC. The 1.5 and 3.5 V voltages are only available inside the IC and are not connected to external pins.

8.7 Stand-alone op-amps

This block is composed of two low-offset stand-alone op-amps (A1 and A2) with outputs connected to the ADC channels 0 and 1.

The stand-alone op-amps can be deactivated if they are not used in the application. When deactivated, they are put in sleep mode and outputs are in high-impedance. In that case, ADC channels 0 and 1 can be used as input signals. The op-amps are controlled by writing to the serial port on register#0 (9); bit opampSelect_N:

Register#0 (9) = 0: means the op-amps are selected and put in normal mode

Register#0 (9) = 1: means the op-amps are not selected and put in sleep mode.

8.8 Analog switch

This block is composed of a 2 input analog multiplexer used to select the seek mode or the track-following mode. It is controlled by writing to serial port register#1 (9); bit seek/trackfw:

Register#1 (9) = 0: means input SEEKSELECT is selected and connected to VCMIN

Register#1 (9) = 1: means input TRACKFWSELECT is selected and connected to VCMIN.

8.9 Charge pump voltage

The charge pump voltage circuit (voltage doubler) generates a power supply voltage higher than V_{DDA2} (12 V) power supply. This voltage is used to:

- Drive the upper N-channel FETs of the power stages
- Drive an optional external FET (see Section 8.18)
- Set a voltage independent of the power supply and temperature for the functions BRAKEPOWER and BRAKEDELAY.

Two external capacitors are used to generate the higher voltage on pin CAPY. The capacitor between BSTCP1 and BSTCP2 is charged and discharged with a frequency, which is a function of the charge pump output current and an internal oscillator frequency. The voltage on pin CAPY is typically 19.2 V. Figure 10 illustrates the charge pump block diagram.

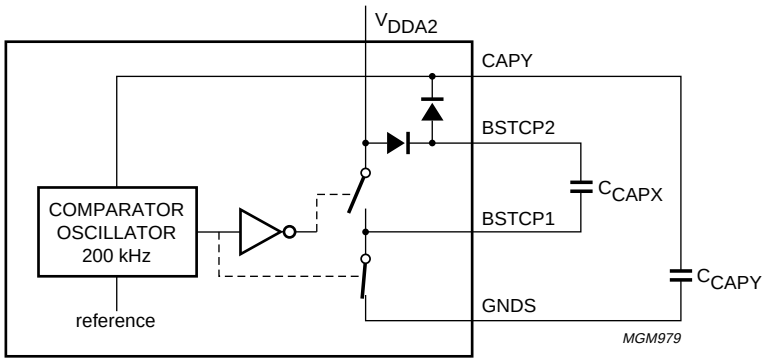


Fig.10 Charge pump voltage generator.

8.10 Spindle driver

The spindle block contains both the low-side and high-side drivers configured as a H-bridge for a 3-phase DC brushless, sensorless motor. In each of the six possible states, two outputs are active, one sourcing current and one sinking current. The third output presents a high impedance to the motor which enables measurement of the BEMF in the corresponding motor coil. The BEMF zero crossing comparator outputs (xCROSS) are processed by the commutation logic circuit to calculate the correct moment for the next commutation, so the change to the next output state. The commutation logic circuit provides proper commutation commands for the spindle drivers thus ensuring the rotation of the motor. The commutation logic circuit also controls the spindle motor driver during start-up (no reverse rotation).

The spindle should be set in the high-impedance mode (see Table 16) between the sleep mode (brake-after-park mode) and the normal running mode. Register#1 should be programmed as follows:

- Write 00x001x11010 to activate the manual mode during typically less than 1 ms (time discharge of low-side power FETs)
- Write 00x001x01xxx to activate the automatic running mode. The 'x' states concern the seek or track-following mode register#1 (9) and the spindle prescaler value used on the application register#1 (5). Their states are specific to the application needs.

The ZCROSS signal is a combination of the xCROSS signals. It can be used by the microcontroller as a tacho information for the spindle speed control loop.

The external SPCC signal is used to control the spindle current. The external SPCCOUT capacitor is connected to the spindle current control amplifier to ensure the stability of the spindle current control loop.

The short-circuit brake mode is entered if power-down, thermal shutdown or sleep mode occurs.

A Miller network is used to obtain soft switching on the low-side and high-side drivers.

The slew rate of the driver stage that is switched-off can be controlled by means of a resistor connected to the pins SLEW and GND. The slew rate is calculated using the following equation:

$$SR = \frac{3\ \mu A + \frac{2.55}{4 \times (1\ k\Omega + R_{SLEW})}}{20\ pF} \quad (11)$$

R_{SLEW} is in Ω and SR in V/s. Without a resistor, SR is typical 0.15 V/μs and with a resistor of 90 kΩ, the typical value is 0.5 V/μs. The maximum slew rate depends on the limit for stability of the spindle loop.

The spindle current I_{SPRUN} is sensed by an external resistor $R_{SPSENSE}$ connected to a sense amplifier providing the internal signal SPOUT. The gain G_v of the sense amplifier is typical 10.

$$V_{SPOUT} = G_v \times R_{SPSENSE} \times I_{SPRUN} = G_v \times V_{SPSENSEH} \quad (12)$$

The transconductance gain of the spindle loop is given by the following equation:

$$g_s = \frac{I_{SPRUN}}{V_{SPOUT}} = \frac{1}{R_{SPSENSE}} \times \frac{V_{SPSENSEH}}{V_{SPOUT}} = \frac{1}{R_{SPSENSE} \times G_v} \quad (13)$$

The control amplifier differentiates the control signal on pin SPCC from the signal SPOUT. A 0.25 V offset is subtracted from the input voltage on pin SPCC to ensure that the current command includes the zero current. With the spindle loop closed, the voltage SPOUT is given by the following equation:

$$V_{SPOUT} = V_{SPCC} - V_{OFFSET} \quad (14)$$

The control signal $V_{CONTROL}$ provided by the control amplifier is then applied to the spindle drivers. The spindle drivers control the voltage on the gate of the low-side power drivers. One of the three high-side drivers is fully on. The charge pump voltage is applied to the gate. One of the three low-side drivers is controlled by the control amplifier. Purpose is to adjust the voltage on the gate to adjust the total output resistance $R_{ds(on)}$ at the specified running current.

The current in the spindle loop is given by the following formula:

$$I_{SPRUN} = g_s \times (V_{SPCC} - V_{OFFSET}) \quad (15)$$

With $R_{SPSENSE}$ = 0.25 Ω:

$$I_{SPRUN} = 0.4 \times (V_{SPCC} - 0.25) \quad (16)$$

The maximum start-up current is I_{SPRUN} = 1.9 A with SPCC signal at 5 V.

Figure 11 illustrates the spindle current control loop.

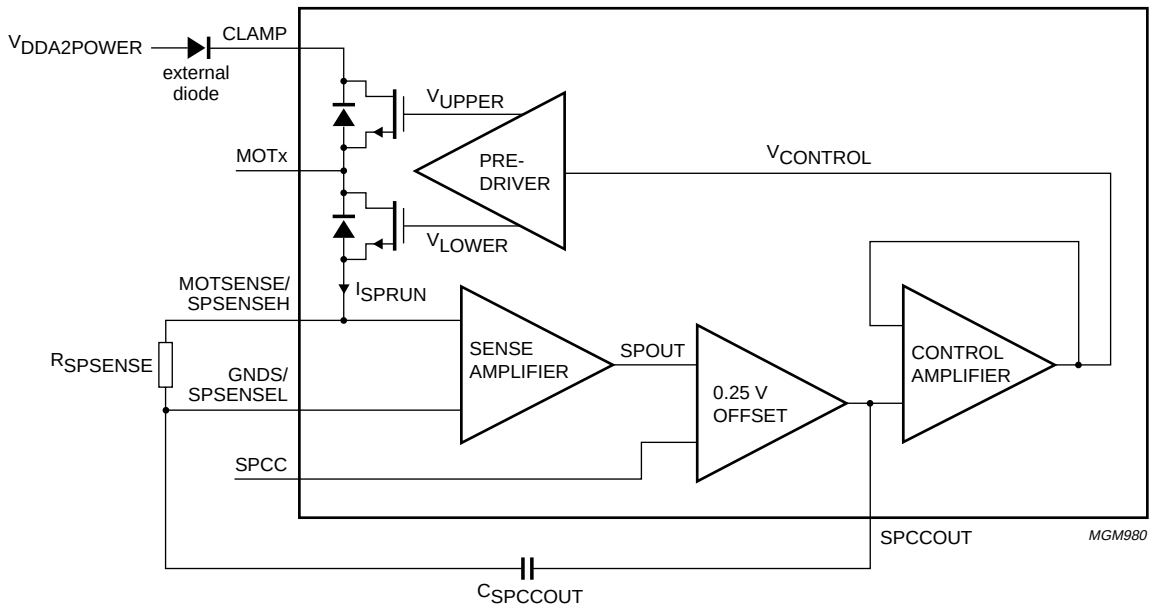


Fig.11 Spindle transconductance loop schematic.

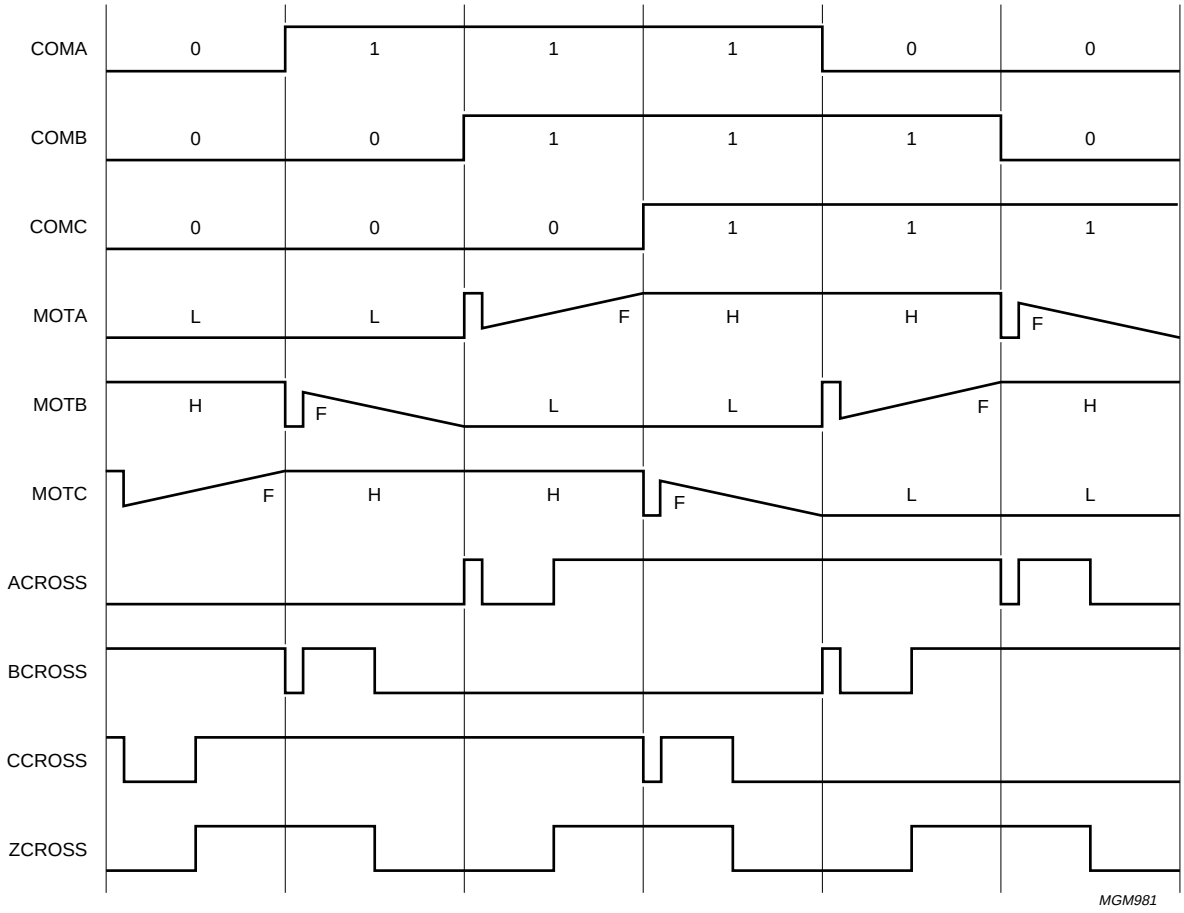
Table 16 and Fig.12 illustrate the relationship between the commutation signals and the associated output drivers and output comparators.

Table 16 Input commutations to output drivers

COMA	COMB	COMC	MOTA	MOTB	MOTC	STATE
0	0	0	LOW	HIGH	float	1
1	0	0	LOW	float	HIGH	2
1	1	0	float	LOW	HIGH	3
1	1	1	HIGH	LOW	float	4
0	1	1	HIGH	float	LOW	5
0	0	1	float	HIGH	LOW	6
1	0	1	F_L(1)	F_L(1)	F_L(1)	SLEEP
0	1	0	float	float	float	Spindle high-impedance

Note

1. F_L is for float-and-then-LOW (brake-after-park mode).



L = LOW.
H = HIGH.
F = Floating.

Fig.12 Input commutations to output drivers.

8.11 VCM driver

The VCM driver is a linear, class AB amplifier with both low-side and high-side drivers configured as an H-bridge.

The zero-current reference voltage for the VCM loop is internally set at 2.5 V. The sense resistor $R_{VCMSENSE}$ enables the VCM current (I_{VCMRUN}) to be measured through the sense amplifier. The gain G_v of the sense amplifier is typically 4. The output voltage (V_{sout}) on pin ADC[2]/SOUT is given by the following equation:

$$V_{sout} = G_v \times R_{VCMSENSE} \times I_{VCMRUN} + V_{ref2V5} \quad (17)$$

$$= G_v \times (V_{VCMSENSEH} - V_{VCMSENSEL}) + V_{ref2V5}$$

Figure 13 presents the VCM sense amplifier.

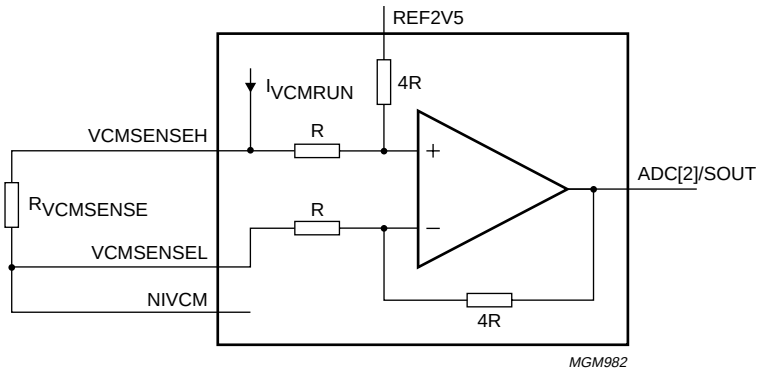


Fig.13 VCM sense amplifier.

The error amplifier (see Fig.14) compares the DACOUT input command and the output signal V_{sout} of the sense amplifier to generate the control voltage of the power drivers.

$$\frac{V_{ref2V5} - V_{DACOUT}}{R_i} = \frac{V_{sout} - V_{ref2V5}}{R_o} = \frac{G_v \times R_{VCMSENSE} \times I_{VCMRUN}}{R_o} \quad (18)$$

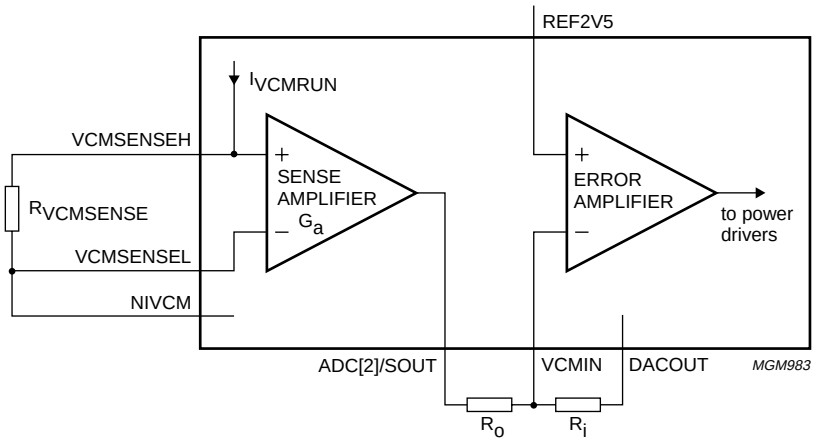
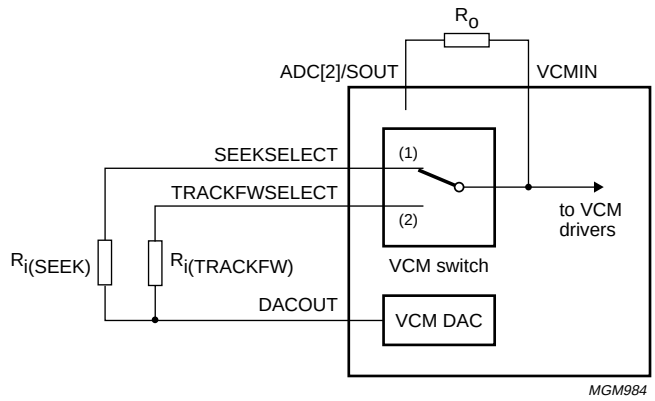


Fig.14 VCM transconductance gain schematic.

Finally, the transconductance gain of the VCM loop is given by the following equation:

$$g_v = \frac{I_{VCMRUN}}{V_{ref2V5} - V_{DACOUT}} = \frac{R_o}{R_i} \times \frac{1}{G_v \times R_{VCMSENSE}} \quad (19)$$

The VCM loop gain is set through external resistors. The seek (high gain) or the track-following (low gain) mode is controlled with the serial bus. Purpose is to set the appropriate gain by selecting the R_i resistor through the low impedance analog 2 input switch.



(1) High gain.
(2) Low gain.

Fig.15 VCM selectable loop gain.

8.12 Park the VCM

A VCM park sequence is initiated any time a power-down, a thermal shutdown and/or a sleep mode situation occurs. The fault signal (FAULT) initiates the VCM park sequence.

This secure function is accomplished even in case of power loss. In this case, the energy provided by the rectified BEMF of the spindle motor coils is used to supply the park circuit and park the heads above a landing area. Otherwise, the energy is provided by the V_{DDA2} power supply through an external diode or power FET.

To accomplish this function, the spindle power stage is automatically set in a high-impedance mode. The NIVCM low-side power driver is fully on while the remaining power drivers of the VCM power stage are off.

The current flowing in the PARKVOLT resistor sets the voltage on the PARKVOLT pin. The voltage across the VCM load is internally regulated by the voltage on the PARKVOLT pin. An internal circuit clamps the voltage on PARKVOLT at $3V_{BE}$. Without resistor, the voltage on PARKVOLT is $3V_{BE}$. The park current $I_{coilpark}$ is applied to the VCM coil. The $I_{coilpark}$ park current is given by the following equation:

$$I_{coilpark} = \frac{V_{PARKVOLT}}{R_{VCMSENSE} + R_{coil} + R_{ds(on)(sink)}} \quad (20)$$

An RC network is connected to pin BRAKEDELAY. During the normal functioning, the voltage on the BRAKEDELAY pin is typically V_{BDC} = 12.55 V. This value is independent of the power supply and the temperature. During park mode, the RC network discharges with a time constant τ.

The park mode is activated as long as the voltage on the BRAKEDELAY pin is greater than the internal brake delay threshold voltage V_{BDT} of typically 2.2 V.

The t_{BDT} park time duration (or brake delay time duration) is set by the following equation:

$$t_{BDT} = \tau \times \ln\left(\frac{V_{BDC}}{V_{BDT}}\right) \quad (21)$$

where

$$\tau = C_{BRAKED} \times R_{BRAKED} \quad (22)$$

C_{BRAKED} and R_{BRAKED} are respectively the capacitor and the resistor connected to the BRAKEDELAY pin.

Typically, with C_{BRAKED} = 330 nF and R_{BRAKED} = 650 kΩ, t_{BDT} = 400 ms.

Figure 16 shows the equivalent park circuit.

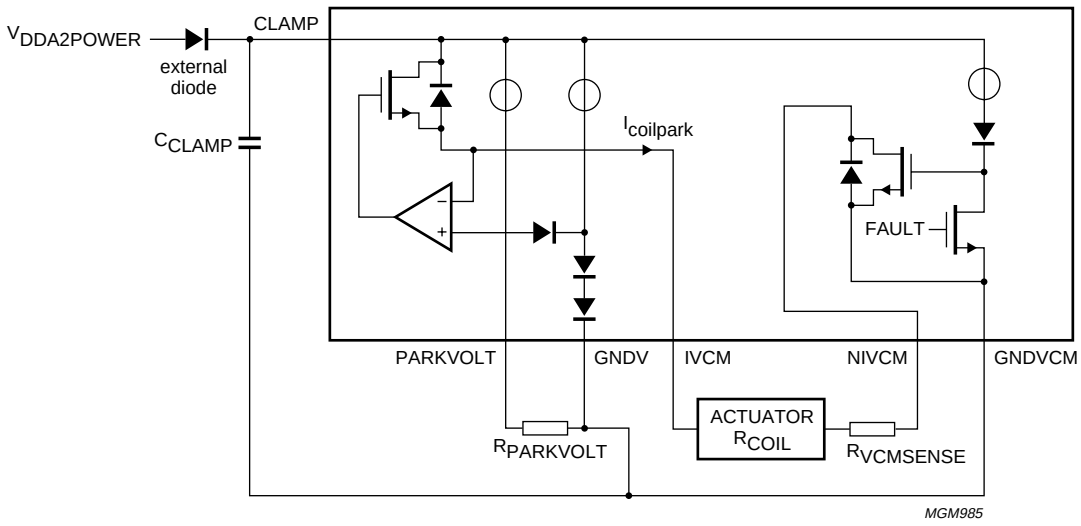


Fig.16 Park circuit.

8.13 Precharge the VCM

When the voltage on the BRAKEDELAY pin goes below the brake delay threshold voltage V_{BDT}, the BRAKEDELAY pin is short-circuited to ground. While the brake mode is activated, the VCM outputs are precharged to $V_{DDA1} - V_{BE}$ while pin VCMIN is short-circuited to ground.

This function precharges the external RC compensation network.

The NIVCM low-side power driver is set off during VCM precharge. This is convenient for actuators with a magnetic latch.

The park circuit is powered off during VCM precharge with the actuator latched.

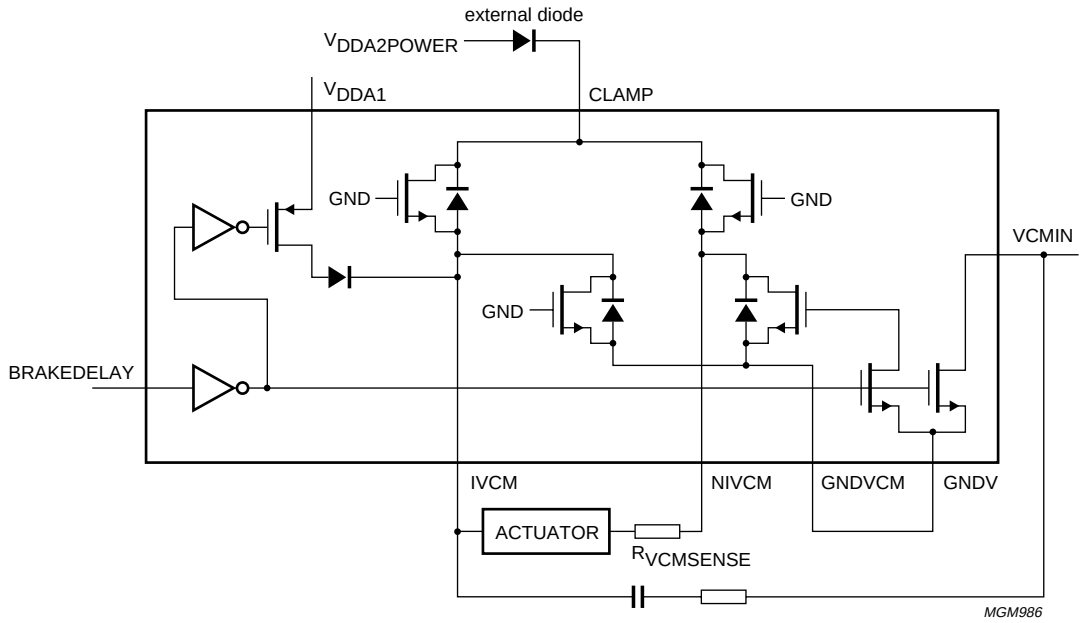


Fig.17 Precharge circuit.

8.14 Brake the motor

A spindle brake sequence is initiated any time a power-down, a thermal shutdown and/or a sleep mode situation occurs. The fault signal activates the brake-after-park sequence.

When the heads are parked, the motor has to be braked in order to guarantee heads reliability. During the brake sequence, the heads land on a dedicated area of the disk.

The OM5193H integrates a highly efficient, low cost brake circuit. It is guaranteed to be functional in case of power loss and thermal shutdown with a short time brake duration thus minimizing friction of the heads on the landing zone.

The energy stored by an external capacitor connected to the BRAKEPOWER pin supplies the brake circuit during the brake-after-park sequence.

The brake of the motor is accomplished by turning on the spindle low-side power components while high-side power drivers are off. This causes a short-circuit of the spindle motor coils and thus reversing the current and torque of the motor.

During normal operation, the voltage V_{BDC} on the BRAKEPOWER pin is typically V_{BDC} = 12.55 V. This value is independent of the power supply and the temperature. During the park sequence, the discharge of the BRAKEPOWER capacitor is set by an internal resistor, with or without an optional external resistor between BRAKEPOWER and BRAKEADJUST. The typical value of the internal resistor is 4 MΩ.

The brake sequence is started when the voltage on BRAKEDELAY goes below the brake delay threshold voltage V_{BDT} of 2.2 V. The gates of the three spindle low-side power drivers are charged by the energy stored in the BRAKEPOWER capacitor and thus braking the motor.

The OM5193H will stay in the brake-after-park mode until register#1 (3) bit run/stop is set to logic 1.

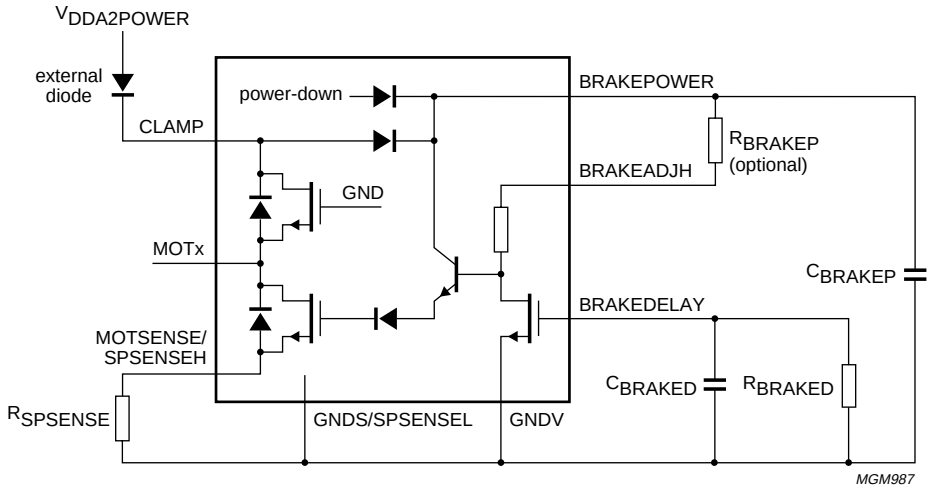


Fig.18 Brake circuit.

The typical value for the BRAKEPOWER capacitor is 1 µF. An optional resistance could be added between the BRAKEPOWER and BRAKEADJUST pins. The values of the capacitor and the resistor are depending on the application.

Without resistor, the BRAKEADJH pin must be connected to the BRAKEPOWER pin.

8.15 Power-on reset

The Power-On Reset (POR) circuit monitors the voltage level of both 5 and 12 V supply voltages as shown in Fig.19.

The $\overline{POR}$ active LOW logic line is set HIGH following the 5 and 12 V supply voltage rise above a specified voltage threshold plus a hysteresis, and delayed by a time t_C that is determined by the external CPOR capacitor.

This $\overline{POR}$ output remains HIGH until either the 5 or 12 V supplies drop below their voltage threshold, at which point the $\overline{POR}$ output becomes LOW.

The C_{CPOR} capacitor is charged with a typically 2.7 µA current. The voltage on CPOR is compared to the POR circuit voltage reference of 2.55 V. The t_C time is set by the following equation:

$$t_C = \frac{C_{CPOR} \times V_{PORREF}}{I_{CPOR}} \quad (23)$$

where V_{PORREF} = 2.55 V and I_{CPOR} = 2.5 µA typically.

The value of the t_C time is set by the C_{CPOR} capacitor value.

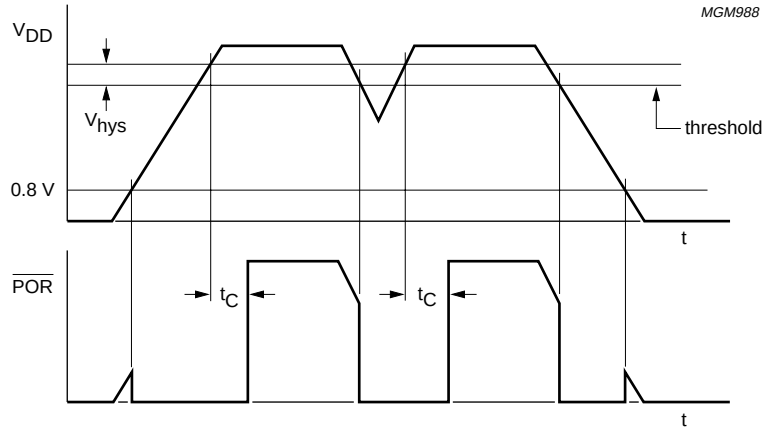


Fig.19 Power-on reset timing.

The values of the 5 and 12 V supply threshold voltages can be adjusted by adding external bridge resistors respectively on the CHK5 and CHK12 pins. Internally, the CHK5 and CHK12 pins are designed as described in Fig.20.

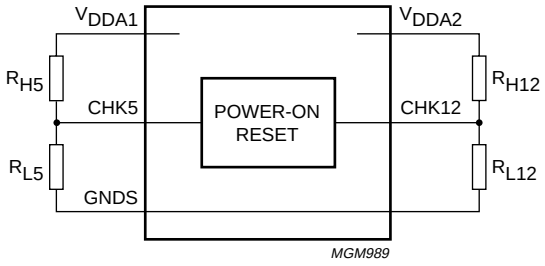


Fig.20 CHK5 and CHK12 pins.

A glitch monitor prevents premature $\overline{POR}$ signals due to voltage spikes on power supplies. An external capacitor has to be connected to the CHK5 and CHK12 pins to filter the noise on CHK5 and CHK12 pins caused by spikes on the power supplies; see Fig.21.

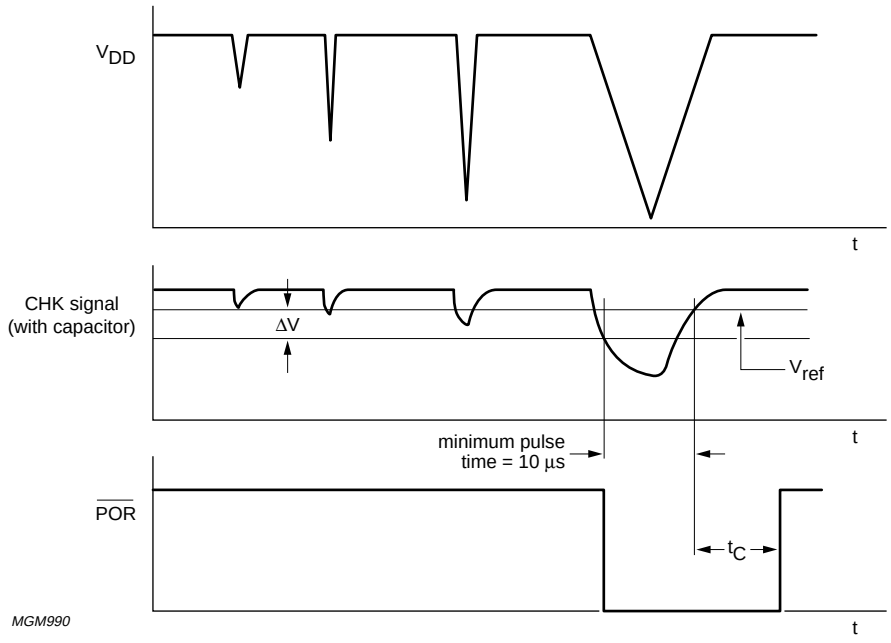


Fig.21 Glitch detector timing.

During a power-down situation, the POR circuit must not only generate an output $\overline{POR}$ signal, but must also activate the brake-after-park sequence. In doing so, the VCM driver draws power from the BEMF of the motor coils through the clamp line during spin-down, and uses this power to bias the VCM against one of the hard stops of the actuator. This prevents the heads from landing on data zones.

$\overline{POR}$ also controls the digital part of the chip.

When $\overline{POR}$ is LOW, the chip is automatically set in the brake-after-park mode.

When $\overline{POR}$ goes HIGH, the digital section is initialized forcing the brake-after-park sequence until a normal start is asked (by writing on register#1).

$\overline{POR}$ is considered as an asynchronous signal for the digital part and default values are loaded when $\overline{POR}$ goes HIGH. Default values for register#0 and register#1 are shown in Section “Commutation and sleep mode” (see also Table 5) and in Section “10-bit ADC with 7 analog inputs” (see also Table 12).

If default values have to be loaded when $\overline{POR}$ is LOW, at least one clock pulse is needed to load the registers with default values.

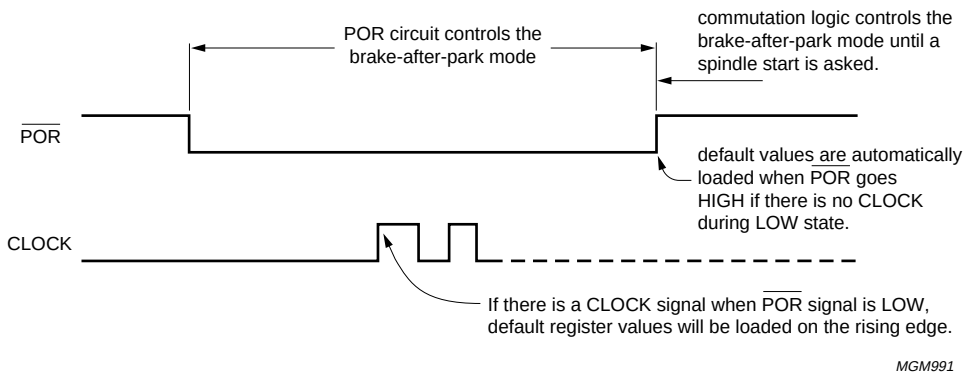


Fig.22 Initialization of the registers when $\overline{POR}$ is LOW.

8.16 Thermal monitor and shutdown

The OM5193H is provided with both a temperature monitor and a thermal shutdown circuit.

The device is protected against over-temperature by the thermal shutdown circuit. When the temperature of the chip exceeds 150 °C, the device is automatically set to the brake-after-park mode. Furthermore, the voltage V_{temp} on pin ADC[4]/TEMP goes HIGH. It remains in this mode until the temperature goes below the thermal shutdown temperature minus typically 10 °C.

During the normal operation, the signal V_{temp} provides a voltage as a function of the chip temperature.
The equation of the voltage versus the temperature is the following:

$$V_{temp} = 7.05 \times 10^{-3} \times T_j\,(°C) + 1.995 \quad (24)$$

Figure 23 presents the voltage V_{temp} on pin ADC[4]/TEMP during normal operation and the voltage on thermal shutdown with hysteresis.

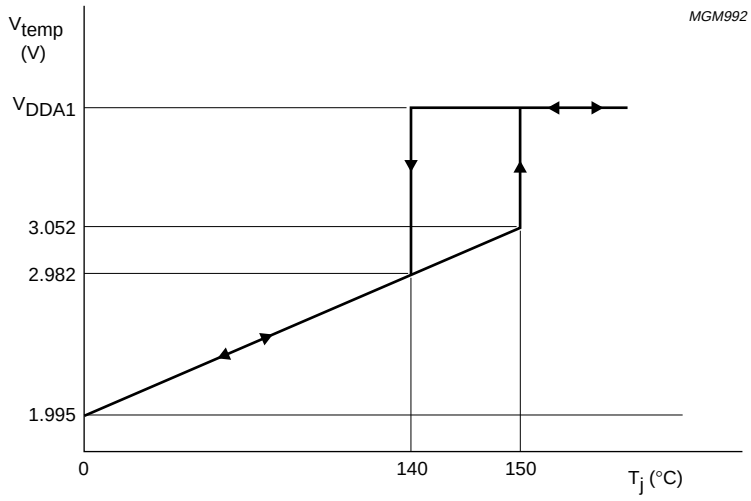


Fig.23 V_{temp} behaviour versus temperature.

The pin ADC[4]/TEMP is internally connected to channel 4 of the ADC. The data can be read and processed by the microcontroller to control the temperature of the device during the spindle start-up sequence and normal operation and to create an early high-temperature warning.

8.17 Power supply isolation

In case of power-down, the brake-after-park sequence must be supplied from the motor BEMF and the energy stored in the CLAMP capacitor. When the supply voltage for the spindle and the VCM is directly connected to the V_{DDA2}, the energy from the motor BEMF and the CLAMP capacitor will be lost in the V supply system instead that it is used for brake-after-park sequence. Therefore, the motor and VCM supply must be isolated from the V_{DDA2}. This can be done by means of a diode or a power FET between V_{DDA2} and the power supply line for the spindle and the VCM.

8.17.1 External isolation diode

A diode can be used when the motor current and the VCM current are low and the voltage drop over the diode does not limit the supply voltage range of the motor and the VCM. The diode can be either a normal diode or a Schottky diode. The type and electrical properties of the diode are determined by the load characteristics.

8.17.2 External power FET

For higher current applications, the diode can be replaced by a N-channel FET. The OM5193H contains an output to drive this N-channel FET. To prevent the brake and park currents from flowing back to V_{DDA2}, the source of the FET must be connected to V_{DDA2} and the drain to the CLAMP line. In this case, the back-gate diode of the FET is reverse biased.

The gate is connected to the SWITCHGATE pin. During normal operation, the voltage on the SWITCHGATE pin is about 19 V and the isolation transistor is conducting. When the brake-after-park sequence is activated, the gate is short-circuited to ground. The recirculation diode is used to isolate the power supply from the power stages.

8.18 Thermal behaviour

The OM5193H uses a dedicated leadframe to effectively drain the heat from the chip. Therefore 18 pins are connected to the leadframe and called HEATSINK.

These pins must be short-circuited together and connected to a large dissipating copper area on the printed-circuit board. The copper area has to be as thick as possible. The thermal resistance can also be decreased by placing the device close to a mounting screw used to fasten the printed-circuit board to the bare casting assembly.

Paths used to connect the power stages to the external components, ground and V_{DDA2} must be as large as possible to guarantee a minimal extra thermal resistance and a higher current capability.

9 LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134); note 1

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA1}	5 V analog supply voltage	–0.3	+6	V
V_{DDD}	5 V digital supply voltage	–0.3	+6	V
V_{DDA2}	12 V analog supply voltage	–0.3	+13.5	V
$V_{DDA2POWER}$				
V_{MOTA}	output voltage	–0.3	+18	V
V_{MOTB}				
V_{MOTC}				
V_{NIVCM}	output voltage	–0.7	+18	V
V_{IVCM}				
V_{UB}	voltage on pins BSTCP1, BSTCP2, CAPY and SWITCHGATE	–0.3	+20.5	V
V_{es}	ESD Human Body Model	–	2000	V
	except for BRAKEDELAY	–	500	V
	except for BRAKEPOWER	–	1500	V
	ESD Machine Model	–	200	V
T_{amb}	operating ambient temperature	0	70	°C
T_{stg}	storage temperature	–55	+125	°C
T_j	junction temperature	–	150	°C

Note

1. Stressing beyond these levels may cause permanent damage to the device. This is a stress rating only and functional operation of the device under this condition is not implied.
   a) OVS: one pin stressed by sample; square pulse time duration = 1 s, maximum current = 1 A.
   b) ESD Human Body Model: JEDEC specification EIA/JESD22-A114 February 1996.
   c) ESD Machine Model: JEDEC specification JC-14.1 July 07 1995.

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	note 1	26	K/W

Note

1. This is obtained with a thermally enhanced printed-circuit board tied to the bare casting assembly.

12 CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; note 1						
V_{DDA1}	5 V analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	5 V digital supply voltage		4.5	5.0	5.5	V
V_{DDA2}	12 V analog supply voltage		10.8	12.0	13.2	V
$V_{DDA2POWER}$	12 V analog supply voltage		10.8	12.0	13.2	V
I_{DDD}	5 V supply current	normal mode	–	40	70	mA
		stand-alone op-amps deactivated	–	25	55	mA
		sleep mode	–	1	3	mA
I_{DDA2}	12 V supply current	normal mode	–	15	25	mA
		sleep mode	–	1.5	5	mA
POWER BIAS VOLTAGE						
$I_{L(PWRBIAS)}$	power bias leakage current	$V_{PWRBIAS}$ = 20.5 V	–	–	200	nA
Servo control; note 2						
7 CHANNEL 10-BIT ADC						
RES_{ADC}	resolution	note 3	–	10	–	bits
t_{CONV}	conversion time	including the sample and hold time; relative to CLOCK signal				
		register#6 (11) = 0	–	–	104	clock cycles
		register#6 (11) = 1	–	–	52	clock cycles
V_I	input voltage	register#0 (6) = 0; V_{ref2V5} = 2.5 V	1.5	–	3.5	V
		register#0 (6) = 1; V_{ref2V5} = 2.5 V	0	–	5	V
OFF_{MID}	offsets for middle code	analog input at V_{ref2V5}				
		1.5 to 3.5 V range	–5	–	+5	LSB
		0 to 5 V range	–7	–	+7	LSB
$E_{i(max)}$	input error for maximum code	relative to 1.4V_I at 00H				
		1.5 to 3.5 V range	–40	–	+40	mV
		0 to 5 V range	–80	–	+80	mV
$E_{i(min)}$	input error for minimum code	relative to 0.6V_I at 00H				
		1.5 to 3.5 V range	–40	–	+40	mV
		0 to 5 V range	–80	–	+80	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INL	end-point integral non-linearity	note 4				
		1.5 to 3.5 V range	–4	–	+4	LSB
		0 to 5 V range	–8	–	+8	LSB
DNL	differential non-linearity	monotonic; no missing codes; for both ranges; note 4	–1	–	+1	LSB
$CODE_{C6}$	code value on channel 6	$\frac{1}{2}V_{DDA1}$ (internal analog value) is sampled and converted in this channel	–190	–	+190	LSB
E_{C6}	code error on channel 6	represents the difference between an external $\frac{1}{2}V_{DDA1}$ conversion result and a conversion made in channel 6	–30	–	0	LSB
$\lvert E_{tot} \rvert$	absolute error	includes integral non-linearity, offset and gain error	–	–	2	%
R_i	input resistance	0 to 5 V range; notes 5 and 6	40	50	60	kΩ
C_i	input capacitance	1.5 to 3.5 V range; note 6	–	20	25	pF
TC	temperature coefficient	combined temperature coefficient of gain error, integral non-linearity and offset				
		T > 25 °C	0	–	0.05	LSB/°C
		T < 25 °C	–0.05	–	0	LSB/°C
CC_{MATCH}	channel-to-channel matching	the same analog voltage is applied in each channel; note 6	–	–	1	LSB
α_{ct}	crosstalk attenuation	f_i = 1 MHz; note 7	66	–	–	dB
PSRR	power supply rejection ratio	note 6	50	–	–	dB
10-BIT VCM DAC						
RES_{DAC}	resolution		–	10	–	bits
t_{st}	settling time	to within 0.5 LSB	–	–	2.0	µs
DR_{DAC}	dynamic range		$0.6V_{ref}$	2.5 (±1.0)	$1.4V_{ref}$	V
$V_{OO(MID)}$	offsets for middle code	measured at code 00H: relative to V_{ref2V5}	–10	–	+10	mV
$E_{o(max)}$	maximum output error	relative to $1.4V_O$ at code 00H	–40	–	+40	mV
$E_{o(min)}$	minimum output error	relative to $0.6V_O$ at code 00H	–40	–	+40	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{OO(max)}$	maximum output offset voltage	relative to $V_{ref3V5(meas)}$; only tested on wafer	–10	–	+10	mV
$V_{OO(min)}$	minimum output offset voltage	relative to $V_{ref1V5(meas)}$; only tested on wafer	–10	–	+10	mV
INL	end-point integral non-linearity	note 4	–2	–	+2	LSB
DNL	differential non-linearity	guaranteed monotonic; note 4	–1	–	+1	LSB
$\lvert E_{tot} \rvert$	absolute error	includes integral non-linearity, offset and gain error	–	–	2	%
TC	temperature coefficient	combined temperature coefficient of gain error, integral non-linearity and offset				
		T > 25 °C	0	–	100	mV/°C
		T < 25 °C	–100	–	0	mV/°C
PSRR	power supply rejection ratio	note 6	50	–	–	dB
REFERENCE VOLTAGES						
V_{ref1V5}	1.5 V reference output voltage	$0.6V_{ref2V5(meas)}$; only tested on wafer	1.414	1.504	1.596	V
V_{ref2V5}	2.5 V reference output voltage	$-1\ mA \leq I_{ref} \leq 5\ mA$	2.397	2.507	2.617	V
V_{ref3V5}	3.5 V reference output voltage	$1.4V_{ref2V5(meas)}$; only tested on wafer	3.332	3.510	3.690	V
G_{1V5}	value of the gain used to generate V_{ref1V5}	$V_{ref1V5(meas)}$ divided by $V_{ref2V5(meas)}$; only tested on wafer	0.59	0.6	0.61	–
G_{3V5}	value of the gain used to generate V_{ref3V5}	$V_{ref3V5(meas)}$ divided by $V_{ref2V5(meas)}$; only tested on wafer	1.39	1.4	1.41	–
TC	temperature coefficient	note 6	–	–	200	µV/°C
PSRR	power supply rejection ratio	note 6	–	–	50	dB
C_L	load capacitance	note 6	0.01	–	0.1	nF
ANALOG SWITCH						
t_{sw}	switching time	note 6	–	–	0.5	µs
$R_{ds(on)}$	total output resistance (source + sink + isolation)	switch closed; value at 25 °C and nominal supply voltages	–	–	100	Ω
TC	temperature coefficient	T > 25 °C	–	–	0.3	%/°C
		T < 25 °C	–	–	–0.3	%/°C
I_L	off leakage current		–	–	100	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
STAND-ALONE OP-AMPS						
V_I	input voltage		1.4	–	V_{DDA1} – 0.5	V
$I_{i(bias)}$	input bias current		–	–	1	µA
V_{IO}	input offset voltage	relative to V_{ref2V5} value	–10	–	+10	mV
I_{IO}	input offset current	note 6	–	–	100	nA
V_O	output voltage	R_L = 10 kΩ to V_{ref2V5} level	0.9	–	V_{DDA1} – 0.5	V
SR	slew rate	R_L = 10 kΩ; C_L = 20 pF	5	–	–	V/µs
GB	gain bandwidth product		0.75	1.0	–	MHz
$G_{v(ol)}$	open-loop voltage gain	f = 1 kHz; R_L = 10 kΩ; note 6	50	60	–	dB
SVRR	supply voltage ripple rejection	f = 100 kHz; R_L = 10 kΩ; C_L < 20pF; note 6	60	70	–	dB
t_{ON}	power-on time	after sleep mode	–	–	1	µs
CMRR	common mode rejection ratio	note 6	60	70	–	dB
DIGITAL PINS						
C_{BIPIN}	bidirectional pins capacitance	CMOS level, high-drive, output stage, 8 mA 3-state				
		input capacitance	–	6	–	pF
		maximum output load	–	–	100	pF
C_{INPIN}	input pins capacitance	CMOS level, high-drive, protection to V_{DDD} and DGND	–	5	–	pF
C_{OUTPIN}	output pins capacitance	2 mA push-pull	–	–	25	pF
V_{IH}	HIGH-level input voltage		3	–	–	V
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{OH}	HIGH-level output voltage	I_O = 2 mA	V_{DDA1} – 0.5	–	–	V
V_{OL}	LOW-level output voltage	I_O = 2 mA	–	–	0.5	V
Motor control; note 1						
GENERAL						
Thermal protection: thermal shutdown						
$T_{sw(off)}$	switch-off temperature	note 8	143	150	157	°C
hys_T	thermal hysteresis	note 6	–	10	15	°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Thermal monitor						
$V_{O(LT)}$	output voltage at low temperature	T_j = 25 °C	–	2.171	–	V
$V_{O(HT)}$	output voltage at high temperature	T_j = 150 °C	–	3.052	–	V
G_T	temperature monitor thermal gain	note 6	6.8	7.05	7.30	mV/°C
Charge pump generator: CAPY, BSTCP1 and BSTCP2						
V_{CP}	charge pump voltage	running mode	18.2	19.2	20.2	V
$V_{SWITCHGATE}$	switchgate voltage	running mode	17.6	19	20	V
POWER-ON RESET						
Power monitor comparators: CHK12 and CHK5						
$V_{th(12)}$	12 V threshold voltage	CHK12 open-circuit	9.05	9.40	9.75	V
$V_{hys(12)}$	hysteresis on V_{DDA2}		80	115	150	mV
$V_{th(5)}$	5 V threshold voltage	CHK5 open-circuit	4.2	4.3	4.4	V
$V_{hys(5)}$	hysteresis on V_{DDD}		35	50	70	mV
R_{L12}	low internal bridge resistor on CHK12	CHK12 short-circuited to 2.55 V	20	27.5	35	kΩ
R_{H12}	high internal bridge resistor on CHK12	CHK12 short-circuited to ground	60	80	100	kΩ
R_{L5}	low internal bridge resistor on CHK5	CHK5 short-circuited to V_{DDA1}	37	46	55	kΩ
R_{H5}	high internal bridge resistor on CHK5	CHK5 short-circuited to ground	24	32	40	kΩ
Power-on reset generator: CPOR and $\overline{POR}$						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	–	–	0.5	V
R_{pu}	pull-up resistor	$\overline{POR}$ short-circuited to ground	10	15	20	kΩ
$I_{CPOR(source)}$	source current for CPOR		–3.5	–2.5	–1.5	μA
$V_{th(CPOR)}$	CPOR threshold voltage	functional test	–	2.55	–	V
SPINDLE DRIVER						
BEMF comparators: ACROSS, BCROSS and CCROSS						
$V_{I(CM)}$	common mode input voltage	running mode	–0.7	–	V_{DDA2} + 0.7	V
$I_{I(bias)}$	input bias current	note 6	–10	–	0	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{sw(comp)}$	comparator switching level	only tested on wafer	–20	–	+20	mV
$V_{sw(tol)}$	tolerance on the comparator switching level	only tested on wafer	–3	–	+3	mV
ΔV_{sw}	variation in comparator switching levels for one IC	note 6	–4.2	–	+4.2	mV
$V_{i(hys)}$	input voltage hysteresis	note 6	–	0.5	–	mV
V_{OL}	LOW-level output voltage	sink current = –40 μA; only tested on wafer	–	–	0.45	V
V_{OH}	HIGH-level output voltage	source current = 40 μA; only tested on wafer	V_{DDA1} – 0.5	–	–	V
Output drivers: MOTA, MOTB and MOTC						
$R_{ds(on)(source)}$	high-side driver output resistance	I_O = 1.0 A at T_{amb} = 25 °C	–	0.36	0.45	Ω
		I_O = 1.0 A at T_{amb} = 125 °C	–	0.56	0.65	Ω
$R_{ds(on)(sink)}$	low-side driver output resistance	I_O = 1.0 A at T_{amb} = 25 °C	–	0.24	0.35	Ω
		I_O = 1.0 A at T_{amb} = 125 °C	–	0.44	0.55	Ω
V_{SLEW}	slew rate voltage	I_{SLEW} = 20 μA	–	2.55	–	V
SR	slew rate	open-loop; note 9	0.09	–	0.23	V/μs
		I_{SLEW} = 30 μA; note 9	0.32	–	0.87	V/μs
I_{SPRUN}	spindle current control	V_{SPCC} = 1.25 V; R_{SENSE} = 0.25 Ω	380	400	420	mA
V_{CLP}	overvoltage protection circuit	I_{SVDMOS} > 10 mA	–	15.8	–	V
$I_{L(SP)}$	spindle power stage leakage current		–	–	1	mA
Sense amplifier: SPSENSEL and SPSENSEH						
I_I	input current on MOTSENSE	only tested on wafer	10	–	10	μA
V_{IO}	input offset voltage	note 6	–	3	–	mV
G_v	sense amplifier gain	only tested on wafer	9.8	10	10.2	V/V
TC	temperature coefficient of sense amplifier gain	note 6	–	200	–	ppm/°C
Control amplifier: SPCC and SPCCOUT						
V_{SPCC0}	spindle zero-current reference	only tested on wafer; T_{amb} = 25 °C	230	250	270	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$f_{cut(ol)}$	open-loop cut-off frequency at 0 dB	$C_{SPCCOUT}$ minimum value = 10 nF for stability when closed loop; note 10	–	–	3	kHz
Logic decoder: COMA, COMB and COMC						
I_{LI}	input leakage current	V_I = 0 to V_{DD}; only tested on wafer	–1	–	+1	µA
VOICE COIL MOTOR DRIVER						
VCM preamplifiers: VCMIN and REF2V5						
I_I	input current on VCMIN		1	–	0	µA
V_{IO}	input offset voltage	relative to V_{ref2V5} for zero output current	–10	–	+10	mV
f_G	unity gain frequency	note 6	2	3.5	–	MHz
VCM driver amplifiers						
t_{COD}	cross-over distortion delay	note 6	–	3	5	µs
SR_{VCM}	VCM slew rate	C_L = 10 pF; note 6	–	1	–	V/µs
f_G	unity gain frequency	note 6	1.5	–	–	MHz
$G_{v(SD)}$	slave driver voltage gain		1.05	1.15	1.25	
$R_{ds(on)(source)}$	high-side driver output resistance	I_O = 1.0 A at T_{amb} = 25 °C	–	0.45	0.55	Ω
		I_O = 1.0 A at T_{amb} = 125 °C	–	0.65	0.75	Ω
$R_{ds(on)(sink)}$	low-side driver output resistance	I_O = 1.0 A at T_{amb} = 25 °C	–	0.35	0.45	Ω
		I_O = 1.0 A at T_{amb} = 125 °C	–	0.55	0.65	Ω
V_{CLP}	overvoltage protection circuit	I_{SVDMOS} > 10 mA	–	15.1	–	V
$I_{LI(VCM)}$	VCM power stage leakage current		–	–	1	mA
VCM sense amplifier: VCMSENSEL and VCMSENSEH						
V_I	input voltage		–0.7	–	V_{DDA2} + 0.7	V
I_I	input current	V_{ref2V5} = 2.5 V	–100	–	+250	µA
G_v	sense amplifier gain	under all conditions	3.8	4.0	4.2	
$I_{O(sink)}$	output sink current	T_j = 0 to 140 °C; note 11	600	–	–	µA
$I_{O(source)}$	output source current	T_j = 0 to 140 °C; note 12	–	–	–500	µA
V_{OO}	output offset voltage	$V_{VCMSENSEH}$ = $V_{VCMSENSEL}$ = 6 V	–15	10	+35	mV
GB	gain-bandwidth product	note 6	5	8	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SR	slew rate	R_L = 10 kΩ; C_L = 60 pF; note 6	1.7	–	5.3	V/µs
$G_{v(ol)}$	open-loop voltage gain	note 6	75	80	–	dB
SVRR	supply voltage ripple rejection	f = 100 Hz; R_L = 10 kΩ; C_L < 60 pF; note 6	90	100	–	dB
CMRR	common mode rejection ratio	note 6	90	–	–	dB
BRAKE-AFTER-PARK DELAY MODE						
Park and brake power						
V_{NMBP}	normal mode voltage on brake power		12.0	12.55	12.9	V
V_{NMBD}	normal mode voltage on brake delay		12.0	12.55	12.9	V
I_{BPR}	brake power park current	$V_{BRAKEPOWER}$ = 12 V; $V_{BRAKEDELAY} > V_{BDT}$	1	3	5	µA
I_{BPB}	brake power brake current	$V_{BRAKEPOWER}$ = 12 V; $V_{BRAKEDELAY}$ = 0	–	–	1	µA
Park						
$V_{SWITCHGATE}$	voltage on SWITCHGATE during brake-after-park	brake-after-park mode	–	–	0.1	V
I_{brake}	park voltage current source	$V_{BRAKEPOWER}$ = 12 V; V_{CLAMP} = 8 V; $V_{BRAKEDELAY} > V_{BDT}$	–12	–9	–6	µA
$V_{IVCM(max)}$	maximum park voltage	pin PARKVOLT open-circuit; V_{CLAMP} = 8 V; $V_{BRAKEDELAY} > V_{BDT}$; T_{amb} = 25 °C; note 13	–	1.95	–	V
$V_{IVCM(park)}$	voltage on IVCM during park	$V_{PARKVOLT}$ = 1 V; $V_{BRAKEPOWER}$ = 12 V; V_{CLAMP} = 8 V; $V_{BRAKEDELAY} > V_{BDT}$	0.9	1	1.1	V
$V_{NIVCM(park)}$	voltage on NIVCM during park	$V_{PARKVOLT}$ = 1 V; $V_{BRAKEPOWER}$ = 12 V; V_{CLAMP} = 8 V; $V_{BRAKEDELAY} > V_{BDT}$	–	15	50	mV
$V_{MOTx(park)}$	voltage on MOTx during park (high impedance state)	$V_{BRAKEDELAY} > V_{BDT}$; note 14	3	6	9	V
$R_{ds(on)(park)}$	switch park resistor	R_L = 20.2 Ω; T_{amb} = 25 °C	–	0.35	2	Ω
$TC_{Rds(on)(park)}$	temperature coefficient	note 15	–	2	–	mΩ/°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Brake						
V_{BDT}	brake delay time threshold voltage	$V_{BRAKEPOWER}$ = 12 V	1.1	2.1	3.1	V
I_{LI}	brake delay leakage current		–500	–	+500	nA
$R_{ds(on)(brake)}$	lower DMOS resistor during a brake	I_{MOTx} = 200 mA; T_{amb} = 25 °C	–	0.24	0.5	Ω
$TC_{Rds(on)(brake)}$	temperature coefficient	note 16	–	2	–	mΩ/°C
Precharge						
V_{IVCM}	voltage on pin IVCM	$V_{BRAKEPOWER}$ = 12 V; $V_{BRAKEDELAY}$ = 0; note 17	–	$V_{DDD} - V_{BE}$	–	V
V_{NIVCM}	voltage on pin NIVCM	$V_{BRAKEPOWER}$ = 12 V; $V_{BRAKEDELAY}$ = 0; note 17	–	$V_{DDD} - V_{BE}$	–	V
V_{VCMIN}	voltage on pin VCMIN	$V_{BRAKEPOWER}$ = 12 V; $V_{BRAKEDELAY}$ = 0	–	–	0.2	V

Notes

1. V_{DDD} = 5 V ±10%; $V_{DDA2} = V_{DDA2POWER}$ = 12 V ±10%; T_{amb} = 0 to 70 °C; unless otherwise specified.
2. $V_{DDD} = V_{DDA1}$ = 5 V ±10%; T_{amb} = 0 to 70 °C.
3. LSB on the 1.5 to 3.5 V range is equal to $^{1}/_{512}$ V; LSB on the 0 to 5 V range is equal to $^{2.5}/_{512}$ V.
4. Integral non-linearity means the deviation of a code from a straight line passing through an actual end-point and the actual centre. INL and DNL are calculated by dividing the output transfer function in 2 parts: minimum value to centre value and centre value to maximum value.
5. The temperature dependency of the resistance is expressed as follows:

   $$R_{sh}(T) = R_{sh}(T_{ref}) \times \left[(1 + 1.1e{-}3 \times (T - T_{ref}) + 1.1e - 6 \times (T - T_{ref})^2 \right]$$

   where $R_{sh}(T)$ = resistance at desired temperature; $R_{sh}(T_{ref})$ = resistance at reference temperature; T = desired temperature and T_{ref} = 27 °C.
6. Guaranteed by design.
7. Channel-to-channel crosstalk is measured while driving one input and measuring the other open inputs.
8. In any case, it allows to go beyond the rated 150 °C limit.
9. The description of the spindle driver circuit is given in Section 8.10.
10. R_{SENSE} = 0.25 Ω. Model for a motor phase: RLC network in parallel (L_P = 1.5 mH, C_P = 100 pF, R_P = 4.6 kΩ) in series with a resistor R_S = 3.2 Ω. Guaranteed by design.
11. $V_{VCMSENSEL}$ = 0.4 V, $V_{VCMSENSEH}$ = 0 V, measured $V_{sout} = V_O$, force $V_{sout} = V_O$ + 10 mV.
12. $V_{VCMSENSEL}$ = 0 V, $V_{VCMSENSEH}$ = 0.4 V, measured $V_{sout} = V_O$, force $V_{sout} = V_O$ – 10 mV.
13. $V_{PARKVOLT(max)} = 3 \times V_{BE}$, $V_{PARKVOLT} = 3 \times 0.70 - 3 \times 2e - 3 \times (T - 25)$ without resistor.
14. Brake-after-park mode when in sleep, $\overline{POR}$ or over-temperature mode.
15. $R_{ds(on)T(park)} = R_{ds(on)(park)} + T_{Rds(on)(park)} \times (T - 25)$.
16. $R_{ds(on)T(break)} = R_{ds(on)(break)} + T_{Rds(on)(break)} \times (T - 25)$.
17. $V_{BE} = 0.65 + 2e - 3 \times (T - 25)$.

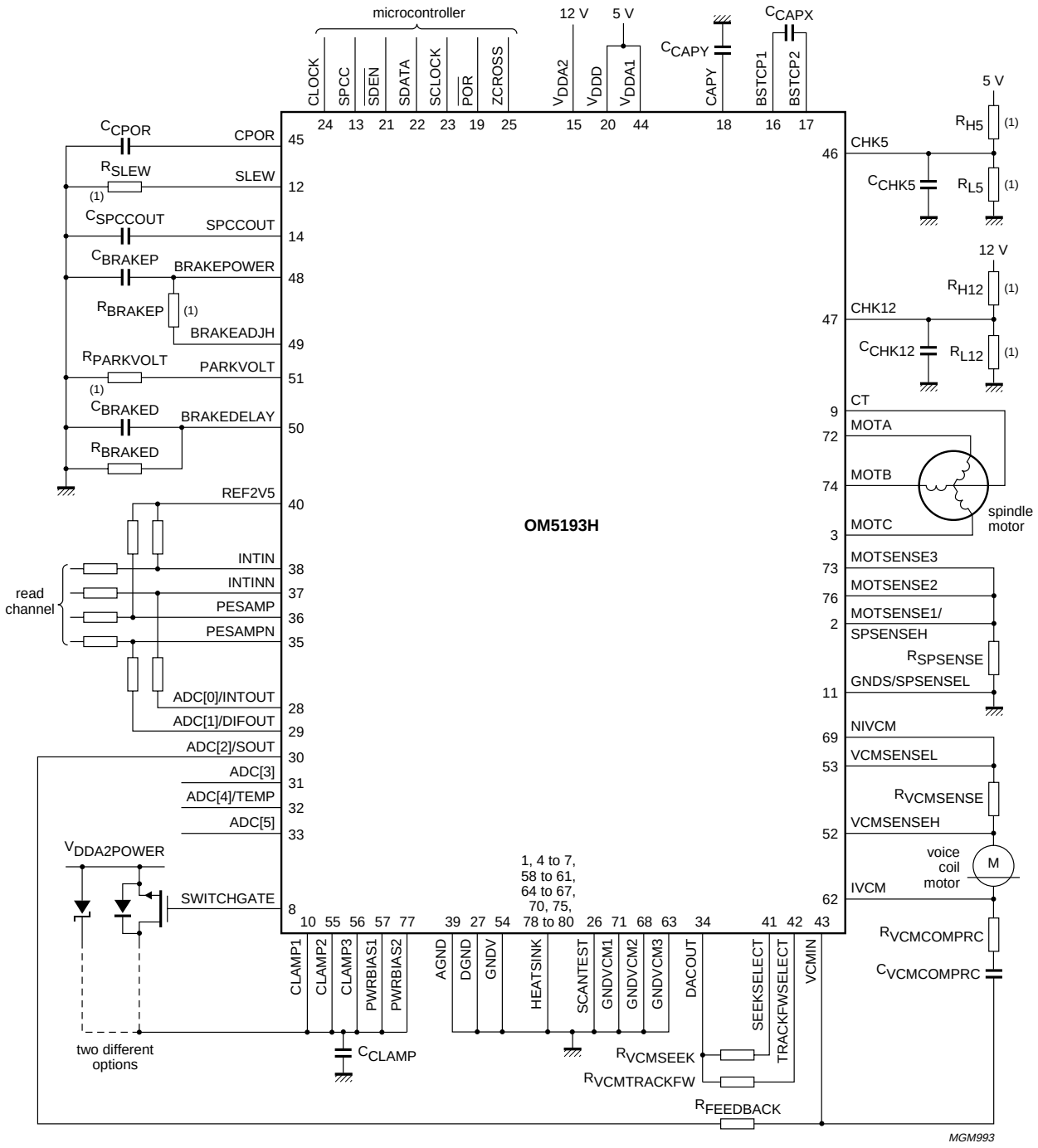
13 APPLICATION INFORMATION

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power supplies monitor						
C_{CPOR}	$\overline{POR}$ time capacitor (time t_C)	note 1	–	100	–	nF
C_{CHK5}	analog 5 V filter	between CHK5 and ground	–	1	–	nF
C_{CHK12}	analog 12 V filter	between CHK12 and ground	–	1	–	nF
Spindle driver						
$C_{SPCCOUT}$	spindle current control loop capacitor	function of the motor characteristics	–	10	–	nF
R_{SLEW}	slew up and down resistor	note 2	–	200	–	kΩ
$R_{SPSENSE}$	spindle sense resistor		–	0.25	–	Ω
VCM driver						
$R_{VCMCOMPRC}$	resistor of compensation RC network	function of the VCM characteristics	–	130	–	kΩ
$C_{VCMCOMPRC}$	capacitor of compensation RC network	function of the VCM characteristics	–	1	–	nF
$R_{VCMSENSE}$	VCM sense resistor		–	0.33	–	Ω
$R_{FEEDBACK}$	feedback resistor	function of the VCM characteristics	–	2.67	–	kΩ
$R_{VCMSEEK}$	seek mode resistor	function of the VCM characteristics	–	2.43	–	kΩ
$R_{VCMTRACKFW}$	track-following mode resistor	function of the VCM characteristics	–	10	–	kΩ
V_I	input voltage controlling the current		1.5	–	3.5	V
V_{ref2V5}	2.5 V reference voltage		–	2.5	–	V
Clamp line						
C_{CLAMP}	clamp capacitor between CLAMP line and ground		–	1	–	µF
Charge pump generator						
C_{CAPX}	pump capacitor between pins BSTCP1 and BSTCP2		–	10	–	nF
C_{CAPY}	storage capacitor between pin CAPY and ground		–	22	–	nF
Park and brake functions						
C_{BRAKEP}	BRAKEPOWER capacitor	brake time = 10 s; speed = 5400 RPM; R_{coil} = 5 Ω; BEMF = 8.2 V	–	1	–	µF
R_{BRAKEP}	resistor between BRAKEADJH and BRAKEPOWER	brake time = 10 s; speed = 5400 RPM; R_{coil} = 5 Ω; BEMF = 8.2 V	–	0	–	MΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{BRAKED}	BRAKEDELAY capacitor	brake delay = 400 ms	–	330	–	nF
R_{BRAKED}	BRAKEDELAY resistor	brake delay = 400 ms	–	650	–	kΩ
$R_{PARKVOLT}$	PARKVOLT resistor	$V_{PARKVOLT}$ = 1.25 V; V_{CLAMP} = 8 V	–	250	–	kΩ

Notes

1. The description of the Power-On Reset (POR) circuit is given in Section “Power-on reset”.
2. The description of the spindle driver circuit is given in Section “Spindle driver”.

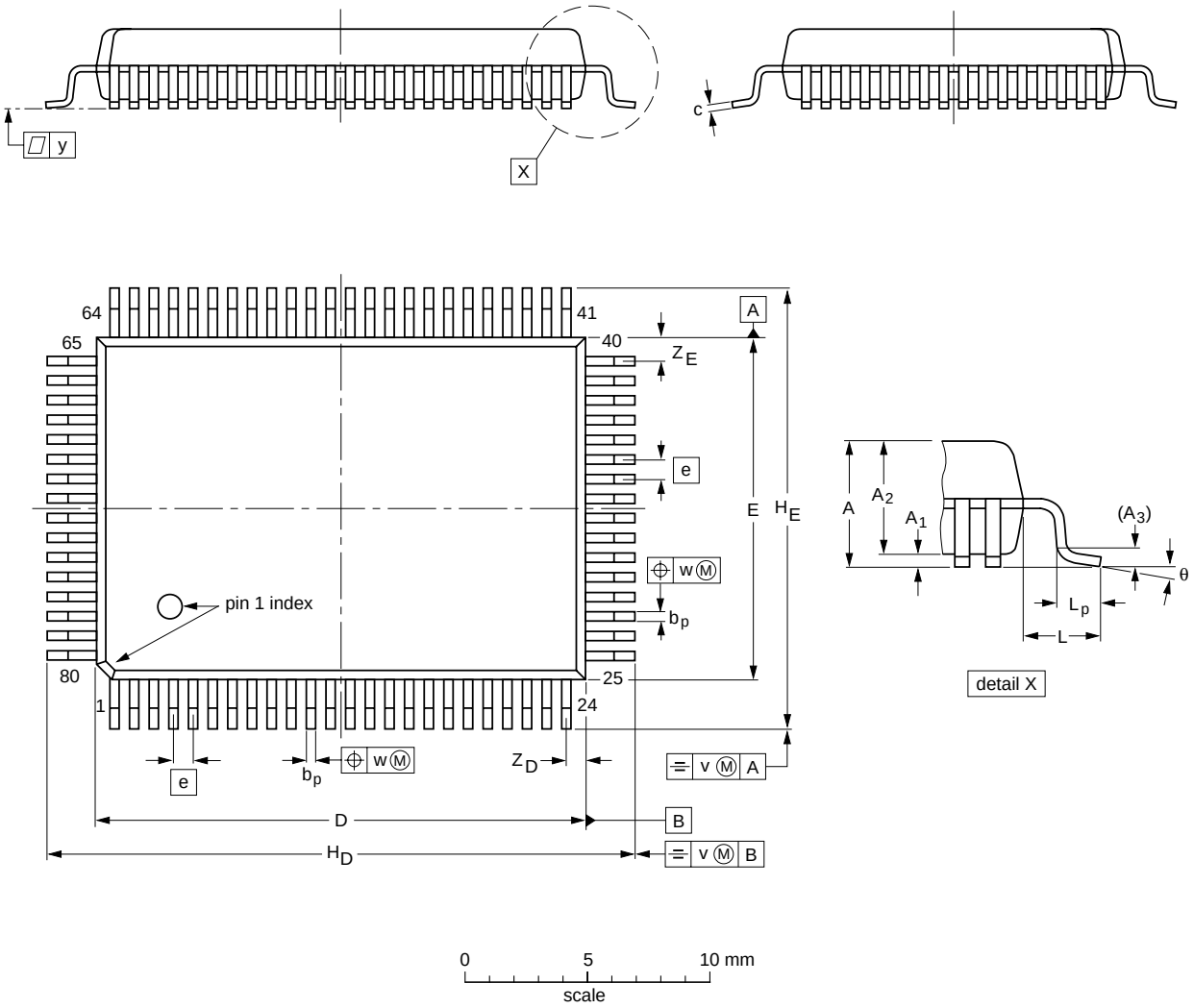


(1) Optional components.

Fig.24 Application diagram.

14 PACKAGE OUTLINE

QFP80: plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT318-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.2	0.25 0.05	2.90 2.65	0.25	0.45 0.30	0.25 0.14	20.1 19.9	14.1 13.9	0.8	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.2	0.1	1.0 0.6	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT318-2						~~95-02-04~~ 97-08-01

15 SOLDERING

15.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

15.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

15.3 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

CAUTION
Wave soldering is NOT applicable for all QFP packages with a pitch (e) equal or less than 0.5 mm.

If wave soldering cannot be avoided, for QFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

16 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

17 LIFE SUPPORT APPLICATIONS

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