Ordering number : ENA1525

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DATA SHEET

LV8064TT — Bi-CMOS IC Fan Motor Driver Single-Phase Full-Wave Driver

Overview

The LV8064TT is a single-phase bipolar fan motor driver IC. It features quiet operation that suppresses reactive current through BTL output system. The speed control range can be adjusted to desired values by the external application program, so that it can rotate fan at lower speeds than conventional drivers in the same driver voltage control range. It is optimal for use in applications that require low noise and power saving, including CPU coolers.

Functions

- Single-phase full-wave drive with BTL output (BTL amplifier gain = 43dB)
- Speed control gain adjusted by SET pin
- FG output pin (open collector output)
- Built-in thermal protection circuit
- Constant-voltage output pin for Hall bias (VREG = 1.05V typ)
- Lock protection and auto return circuits built-in

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		7	V
Output current	I_{OUT} max1	During steady state	0.7	A
	I_{OUT} max2	During lock protection	1	A
Output withstand voltage	V_{OUT} max		7	V
FG output withstand	V_{FG} max		7	V
FG output current	I_{FG} max		5	mA
REG output current	IREG max		10	mA
Allowable dissipation	Pd max1	Independent IC	0.2	W
	Pd max2	With specified substrate *	0.4	W
Junction temperature	Tj max		+150	°C
Operating temperature	Topr		-30 to +95	°C
Storage temperature	Tstg		-55 to +150	°C

* Specified substrate : 20mm × 10mm × 0.8mm, Paper phenol

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Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		2.2 to 6.0	V
Common-phase input voltage range of Hall input	VICM		0.3 to V_{CC}-1.5	V
SET pin input voltage range	VSETIN		0.3 to VREG	V

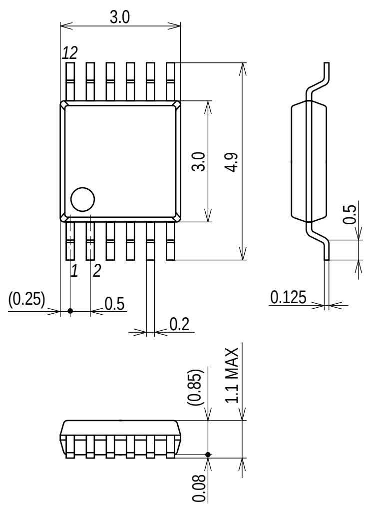
Electrical Characteristics at Ta = 25°C, V_{CC} = 5V, unless especially speified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current	I_{CC}			3	5	mA
REG pin output voltage	VREG	When IREG = 5mA	0.9	1.05	1.2	V
Hall input bias current	IHIN				1	μA
Output On voltage	V_O	I_O = 250mA, source + sink		0.44	0.54	V
Hall amplifier input offset voltage	$V_{IN}OFS$		-10		10	mV
Hall amplifier voltage gain	GH		40	43		dB
CPWM pin charge current	ICPC	VSET = 0.5V		4.5	8	μA
CPWM pin discharge current	ICPD	VSET = 0.5V		4.5	8	μA
CPWM pin charge/discharge current ratio	ICPRTO	ICPRTO = ICPC/ICPD	0.7	1	1.2	
CPWM pin high voltage	VCPH			1.3	1.5	V
CPWM pin oscillation amplitude	VCPA	VSET = 0.5V	0.4	0.5	0.6	V
SET pin input bias current	ISET				1	μA
FG output pin low voltag	V_{FG}	I_{FG} = 3mA			0.3	V
FG output pin leakage current	I_{FGL}	V_{FG} = 5V			10	μA
FG comparator hysteresis width	ΔV_{FG}		±5	±15	±20	mV
Output on time during lock protection	TACT	VSET = 0.5V, CPWM = 100pF	0.3	0.5	0.65	sec
Output off time during lock protection	TDET	VSET = 0.5V, CPWM = 100pF	3.0	5	6.5	sec
Lock protection on/off ratio	TRTO	TRTO = TDET/TACT	8	10	11	
Thermal shutdown operating temperature	TSD	Design guarantee *		180		°C
Thermal shutdown hysteresis width	ΔTSD	Design guarantee *		40		°C

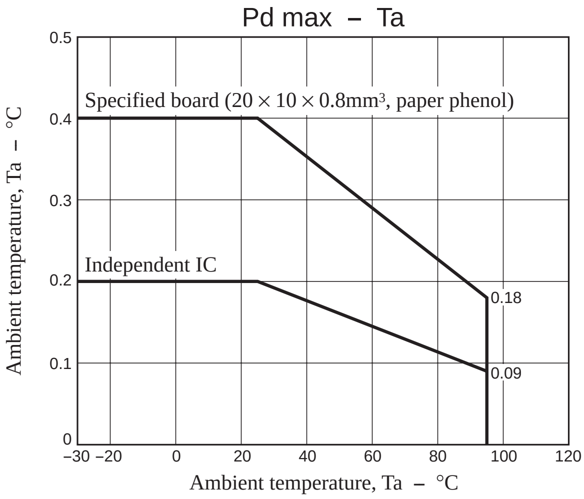
* Design guaranteed value (No measurement is performed.)

Package Dimensions

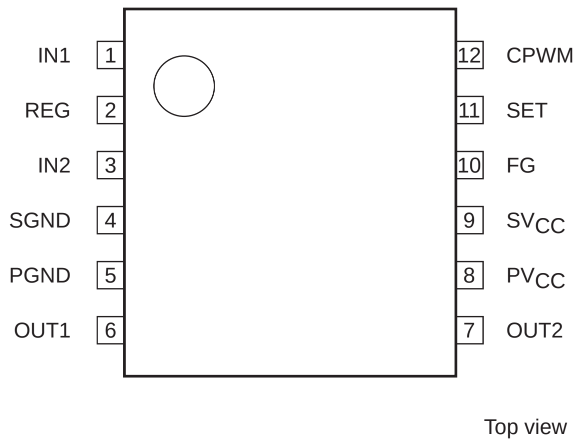
unit : mm (typ)
3375



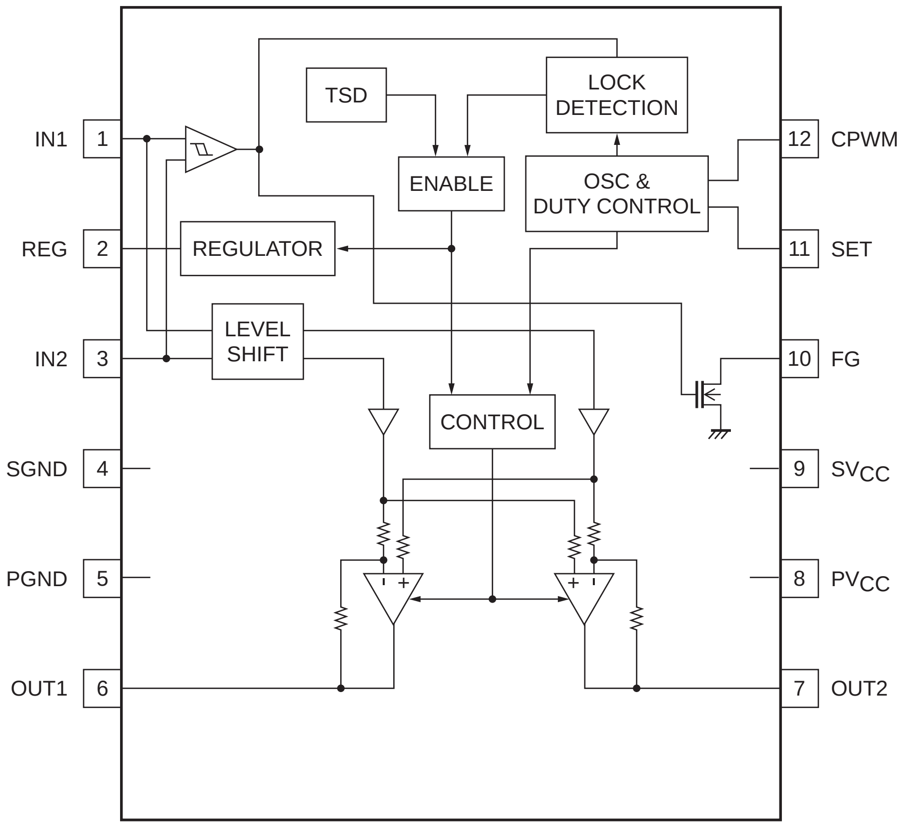
SANYO : MSOP12(150mil)



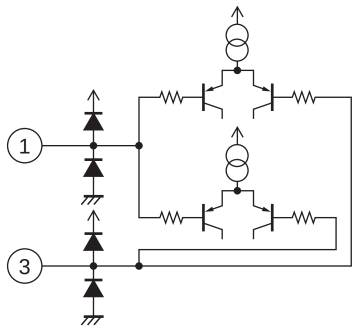
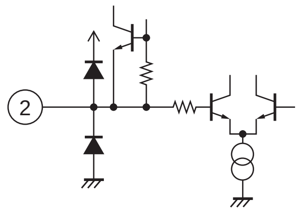
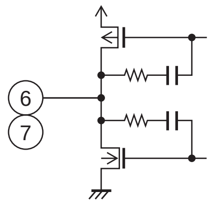
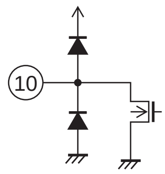
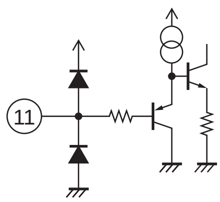
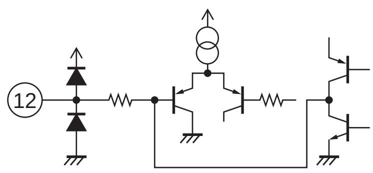
Pin Assignment



Block Diagram

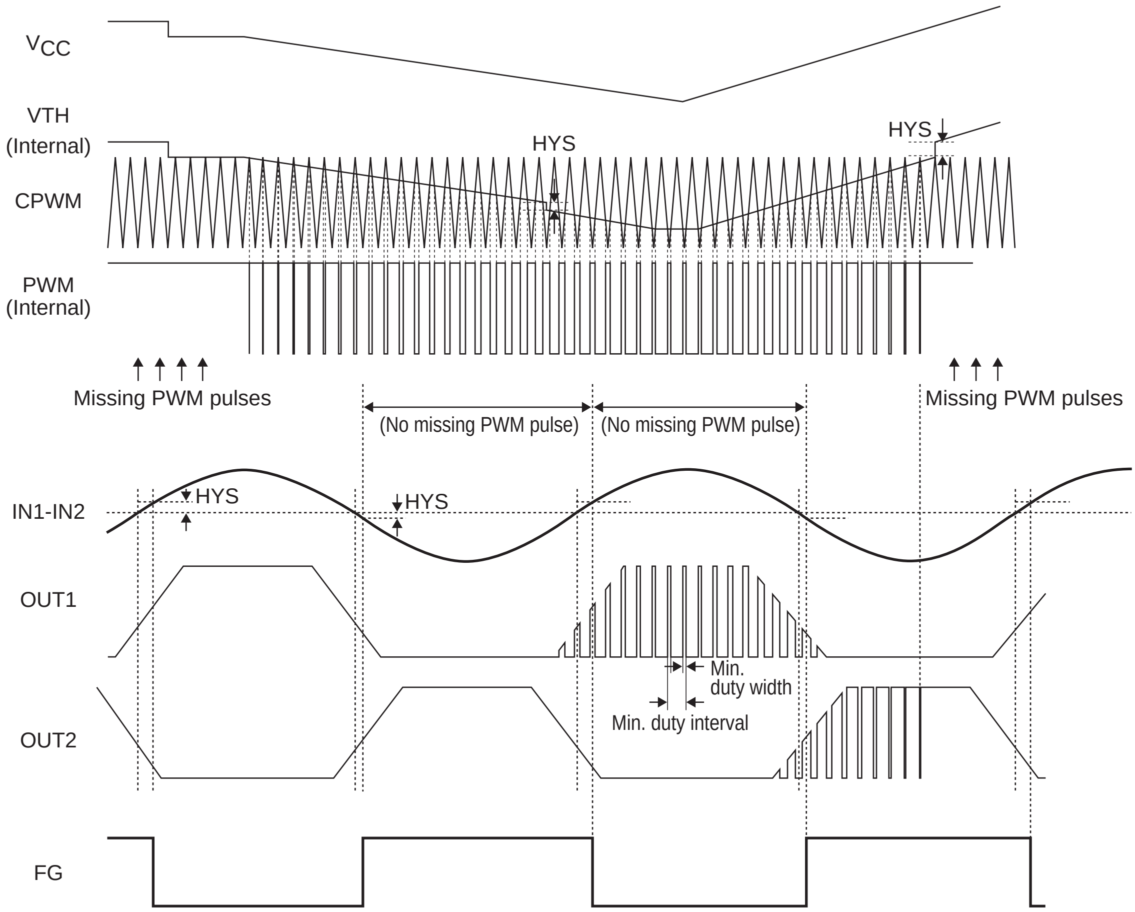


Pin Description

Pin No.	Pin name	Pin voltage	Description	Equivalent circuit
1	IN1	-	Hall input pin (+)	
3	IN2		Hall input pin (-)	
2	REG	1.05V (typ)	Hall bias output pin	
4	SGND	0V	Signal GND	
5	PGND		Power GND	
6	OUT1	-	Motor drive output pin	
7	OUT2			
8	SVCC	2.2V to 6.0V	Signal power source	
9	PVCC		Power source	
10	FG	-	FG pulse output pin	
11	SET	0.3V to VREG	PWM voltage control pin	
12	CPWM	-	PWM oscillator capacitor connection pin	

Timing Chart

When motor is steady-state rotation



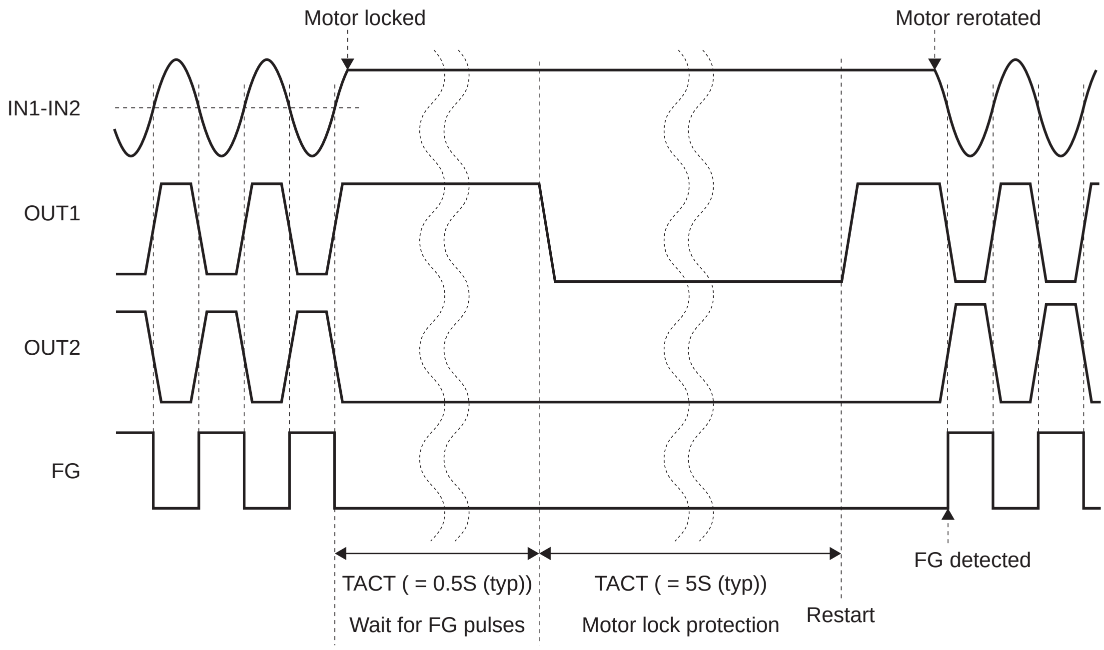
* VTH = 0.5V+V_{CC}/6 (typ)
* Check for the presence or absence of PWM pulses at intervals of 1/2 FG period, and if there are missing pulses, immediately turn off the PWM pulse output. If there are no missing pulses at 1/2 FG period intervals, restart generating PWM pulses at the next interval.

*Truth Table When Steady Rotation

IN1	IN2	*PWM	OUT1	OUT2	FG	Mode
H	L	H	H	L	L	During rotation - drive
		L	L	L		During rotation - regeneration
L	H	H	L	H	OFF	During rotation - drive
		L	L	L		During rotation - regeneration

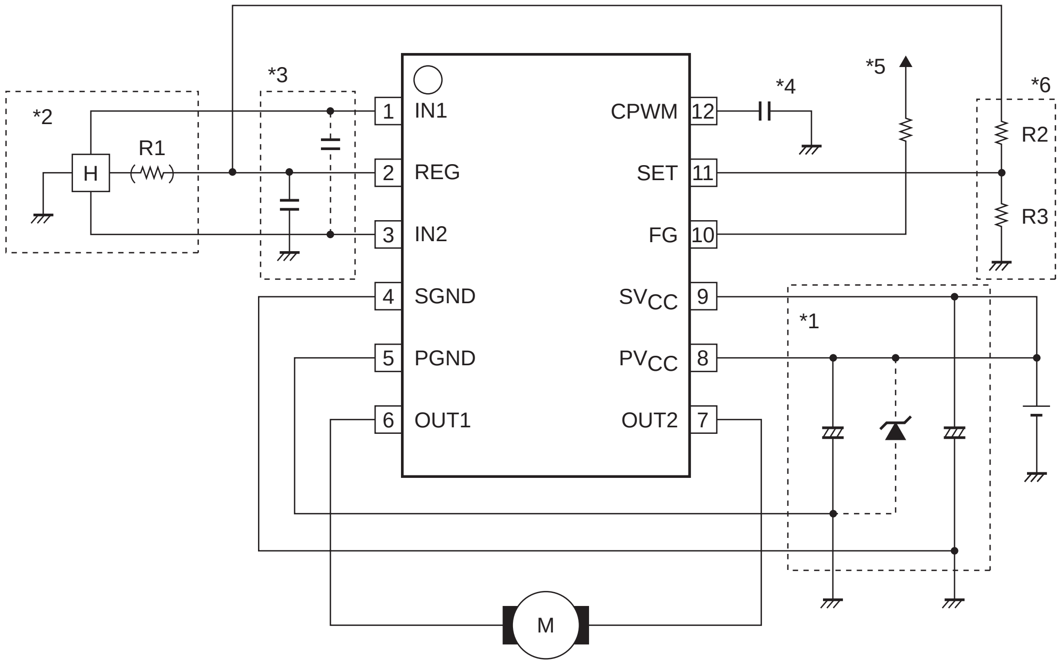
* IC's internal signal

When motor is locked



* When motor protection is activated, both OUT1 and OUT2 output low level.

Application Circuit Example



*1 Capacitors with capacitances adequate to tabilize the power-supply voltage must be inserted between the PV_{CC} pin and PGND pin and between the SV_{CC} pin and SGND pin as close as possible to each pin. An excessive increase of the power supply voltage due to the regeneration current of the motor can cause a fatal damage to the IC. Be sure to use a zener diode if such a condition is likely to occur.

*2 The REG pin outputs a constant voltage of 1.05V (typ). Stable Hall output of excellent temperature characteristics is obtained by providing a bias to the Hall element from the REG pin. Insert R1 when adjusting the Hall amplitude. When this pin is not to be used, pull it down to GND with a resistor of 1k to 10kΩ.

*3 Insert a capacitor of an adequate capacitance between the REG pin and GND pin to stabilize the Hall signal and SET pin input voltage. When the wiring from the Hall output to the Hall input is long, noise may be carried through the wiring. Insert a capacitor close to the IN1 and IN2 pins as shown in the figure.

*4 A capacitor for PWM oscillation. A 120pF capacitor provides an oscillation frequency of approx. 33kHz (typ).

*5 Must be held open when this pin is not to be used.

*6 The SET pin is used to determine the amplitude of the triangle waves generated at the CPWM pin. The same voltage level input to this pin determines the amplitude of the triangle wave. To make the amplitude of the triangle waves constant regardless of possible power voltage fluctuations, apply to the SET pin the register-divided voltage from the REG pin as shown in the figure.

This catalog provides information as of August, 2009. Specifications and information herein are subject to change without notice.