Ordering number : ENN7944

SANYO Semiconductors

DATA SHEET

Bi-CMOS IC

LV8041FN — Seven-Channel Motor Driver IC for Digital Cameras

Overview

The LV8041FN is a digital camera motor driver IC that integrates seven driver channels on a single chip.

Features

- Two PWM current control microstepping drive stepping motor driver channels
- One constant current forward/reverse motor driver
- Two PWM drive forward/reverse motor driver channels (one channel of which can be switched to function as a microstepping drive stepping motor driver)
- Stepping motor drivers 1 and 2 support 2-phase, 1-2 phase, 2W1-2 phase, and 4W1-2 phase drive.
- Stepping motor driver 3 operates in fixed 2W1-2 phase drive mode.
- Microstepping drive step advance can be controlled with a single clock input (stepping motor drivers 1, 2, and 3)
- The constant current control chopping frequency can be adjusted with an external resistor (stepping motor drivers 1, 2, and 3)
- Phase detection monitor pins provided (stepping motor drivers 1, 2, and 3)
- The states of all of the drivers can be set up and controlled over an 8-bit serial data interface.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	Vmmax		6	V
Supply voltage 2	V_{CC}max		6	V
Peak output current	$I_O$peak	1ch/2ch/3ch/4ch/5ch/6ch/7ch	600	mA
Continuous output current	$I_O$max	1ch/2ch/3ch/4ch/5ch/6ch/7ch	400	mA
Allowable power dissipation	Pd max1	Independent IC	0.35	W
	Pd max2	Mounted on a 30 × 50 × 0.8 mm glass epoxy PCB	2.2	W
Operating temperature	Topr		–20 to +85	°C
Storage temperature	Tstg		–55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range 1	VM		2 to 5.5	V
Supply voltage range 2	V_{CC}		2.7 to 5.5	V
Logic input voltage	V_{IN}		0 to V_{CC} +0.3	V
Chopping frequency	fchop	1ch, 2ch, 3ch, 4ch, 5ch, 6ch	50 to 200	KHz
Clock frequency	fCLK	CLK12, CLK34, CLK56	Up to 64	KHz
PWM frequency	fPWM	PWM5, PWM6	Up to 100	KHz

Electrical Characteristics at Ta = 25°C, VM = 5 V, V_{CC} = 5 V

Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Standby mode current drain		Istn	ST = low			1	μA
Current drain		IM	ST =high PWM5 = PWM6 = IN72 = high, No load		50	100	μA
		I_{CC}	ST =high PWM5 = PWM6 = IN72 =high, No load	3.5	4.5	5.5	mA
V_{CC} low-voltage cutoff voltage		VthV_{CC}		2.1	2.35	2.6	V
Low-voltage sensing hysteresis		VthHIS		100	150	200	mV
VG reference voltage		VGL		4.5	4.7	5.0	V
Charge pump step-up voltage		VGH		8.5	9	9.5	V
Charge pump startup time		tONG	C (VGH) = 0.1 μF		0.1	0.2	ms
Charge pump oscillator frequency		Fchg	R = 20 kΩ	100	125	150	kHz
Thermal shutdown temperature		TSD	Design guarantee value	150	160	170	°C
Thermal shutdown hysteresis		ΔTSD	Design guarantee value	5	10	20	°C
Stepping Motor Drivers (Channels 1, 2, 3, and 4)							
Output on-resistance		Ronu	Ta = 25°C, I_O = 400mA, Upper side on-resistance		0.45	0.55	Ω
		Rond	Ta = 25°C, I_O = 400mA, Lower side on-resistance		0.45	0.55	Ω
Output leakage current		$I_O$leak			1	50	μA
Diode forward voltage		VD1	ID = −400mA	0.6	0.9	1.2	V
Logic pin input current		I_{IN}L	V_{IN} = 0 V (ST, CLK12, CLK34)			1.0	μA
		I_{IN}H	V_{IN} = 5 V (ST, CLK12, CLK34)		50	70	μA
Logic high-level input voltage		V_{IN}H	ST, CLK12, CLK34	3.5			V
Logic low-level input voltage		V_{IN}L	ST, CLK12, CLK34			1.5	V
Current selection reference voltage levels	4W1-2 phase drive		Step 16 (Initial state, channel 1 comparator level)	0.188	0.2	0.218	V
			Step 15 (Initial state +1)	0.188	0.2	0.218	V
			Step 14 (Initial state +2)	0.188	0.2	0.218	V
			Step 13 (Initial state +3)	0.177	0.192	0.207	V
			Step 12 (Initial state +4)	0.170	0.185	0.200	V
			Step 11 (Initial state +5)	0.163	0.178	0.193	V
			Step 10 (Initial state +6)	0.156	0.171	0.186	V
			Step 9 (Initial state +7)	0.148	0.163	0.178	V
			Step 8 (Initial state +8)	0.133	0.148	0.163	V
			Step 7 (Initial state +9)	0.117	0.132	0.147	V
			Step 6 (Initial state +10)	0.100	0.115	0.130	V
			Step 5 (Initial state +11)	0.083	0.098	0.113	V
			Step 4 (Initial state +12)	0.065	0.080	0.095	V
			Step 3 (Initial state +13)	0.050	0.062	0.077	V
			Step 2 (Initial state +14)	0.030	0.043	0.058	V
			Step 1 (Initial state +15)	0.010	0.023	0.038	V
	2W1-2 phase drive		Step 16 (Initial state, channel 1 comparator level)	0.188	0.2	0.218	V
			Step 14 (Initial +1)	0.188	0.2	0.218	V
			Step 12 (Initial +2)	0.170	0.185	0.200	V
			Step 10 (Initial +3)	0.156	0.171	0.186	V
			Step 8 (Initial +4)	0.133	0.148	0.163	V
			Step 6 (Initial +5)	0.100	0.115	0.130	V
			Step 4 (Initial +6)	0.065	0.080	0.095	V
			Step 2 (Initial +7)	0.030	0.043	0.058	V
	1-2 phase drive		Step 16 (Initial state, channel 1 comparator level)	0.188	0.2	0.218	V
			Step 8 (Initial state + 1)	0.133	0.148	0.163	V
	2-phase drive		Step 8	0.188	0.2	0.218	V
Chopping frequency		Fchop	R = 20 kΩ	100	125	150	kHz
Monitor pin (MO pin) output voltage		VMOH	IMO = −50 μA, VM = 5V	4.5	4.9	V_{CC}	V
		VMOL	IMO = 50 μA	0	0.1	0.5	V

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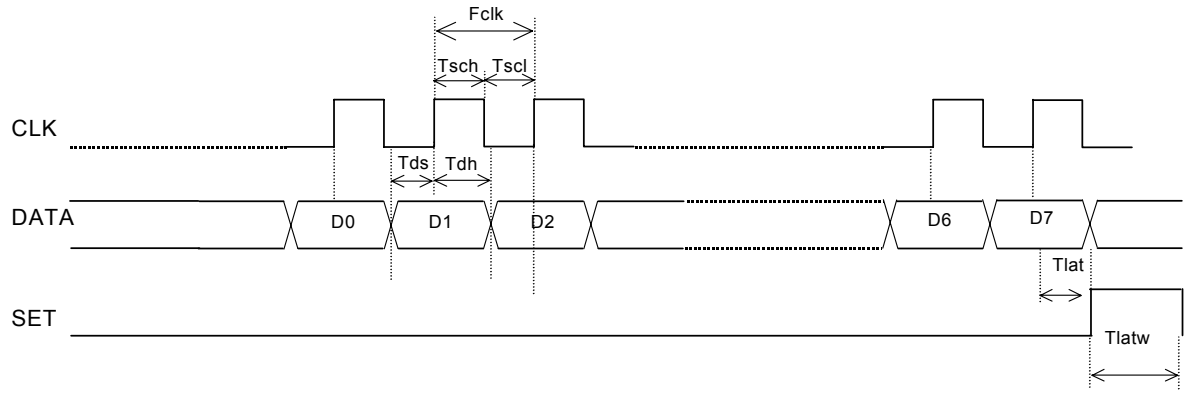
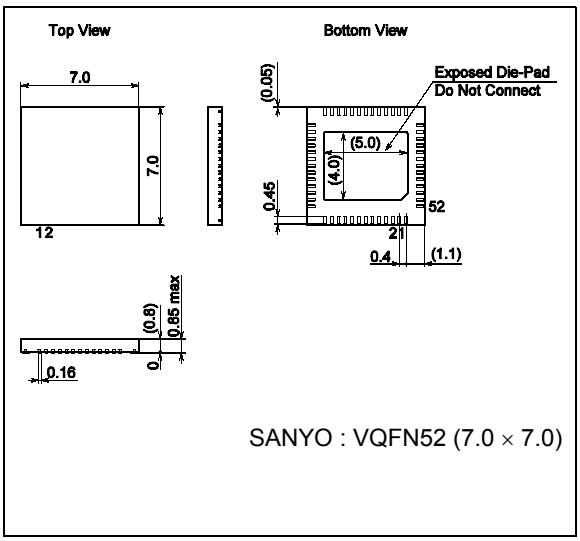
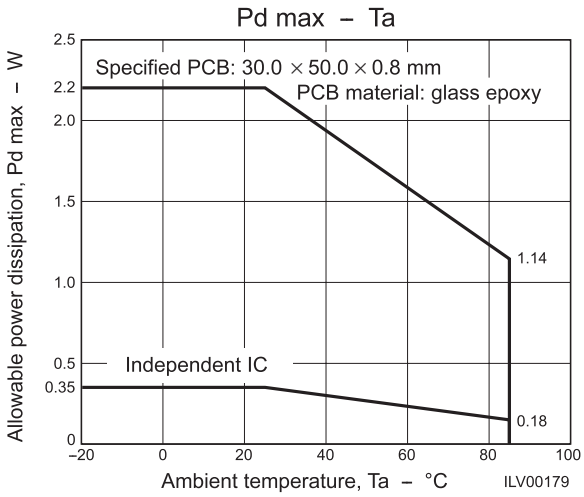
Parameter		Symbol	Conditions	Ratings			Unit
H Bridge Drivers (Channels 5 and 6)							
Output on-resistance		Ronu	Ta = 25°C, I_O = 400 mA, Upper side on-resistance		0.45	0.55	Ω
		Rond	Ta = 25°C, I_O = 400 mA, Lower side on-resistance		0.45	0.55	Ω
Output leakage current		$I_O$leak			1	50	μA
Diode forward voltage 1		VD1	ID = −400 mA	0.6	0.9	1.2	V
Logic pin input current		I_{IN}L	V_{IN} = 0 V (PWM5, PWM6)			1.0	μA
		I_{IN}H	V_{IN} = 5 V (PWM5, PWM6)		50	70	μA
Logic high-level input voltage		V_{IN}H	PWM5, PWM6	3.5			V
Logic low-level input voltage		V_{IN}L	PWM5, PWM6			1.5	V
Current selection reference levels when microstepping is selected	2W1-2 phase drive		Step 16 (Initial state, channel 5 comparator level)	0.188	0.2	0.218	V
			Step 14 (Initial state +1)	0.188	0.2	0.218	V
			Step 12 (Initial state +2)	0.170	0.185	0.200	V
			Step 10 (Initial state +3)	0.156	0.171	0.186	V
			Step 8 (Initial state +4)	0.133	0.148	0.163	V
			Step 6 (Initial state +5)	0.100	0.115	0.130	V
			Step 4 (Initial state +6)	0.065	0.080	0.095	V
			Step 2 (Initial state +7)	0.030	0.043	0.058	V
Monitor pin (MO56 pin) output voltage		VMOH	IMO = −50 μA, VM = 5 V	4.5	4.9	V_{CC}	V
		VMOL	IMO = 50 μA	0	0.1	0.5	V
Current control reference voltage		VSEN1	(D7, D6) = (0, 0)	0.188	0.2	0.218	V
		VSEN2	(D7, D6) = (0, 1)	0.119	0.134	0.149	V
		VSEN3	(D7, D6) = (1, 0)	0.085	0.1	0.115	V
		VSEN4	(D7, D6) = (1, 1)	0.051	0.066	0.081	V
Constant Current Forward/Reverse Motor Driver (Channel 7)							
Output on-resistance		Ronu	Ta = 25°C, I_O = 400 mA, Upper side on-resistance		0.5	0.6	Ω
		Rond	Ta = 25°C, I_O = 400 mA, Lower side on-resistance		0.5	0.6	Ω
Output leakage current		$I_O$leak			1	50	μA
Diode forward voltage 1		VD1	ID = −400 mA	0.6	0.9	1.2	V
Logic pin input current		I_{IN}L	V_{IN} = 0 V (IN71, IN72)			1.0	μA
		I_{IN}H	V_{IN} = 5 V (IN71, IN72)		50	70	μA
Logic high-level input voltage		V_{IN}H	IN71, IN72	3.5			V
Logic low-level input voltage		V_{IN}L	IN71, IN72			1.5	V
Constant current output		I_{OUT}	Rload = 3 Ω, RF = 0.5 Ω, LIM7 = 0.2 V	384	400	416	mA
VREF7 output voltage		VREF7		0.19	0.2	0.21	V
LIM7 input current		ILIM7	LIM7 = 0 V			1.0	μA
FC7 Rapid charge current		Irafc7		500	670	850	μA
FC7 steady-state charge current		Ichfc7		5	10	15	μA
FC7 steady-state discharge current		Idisfc7		5	10	15	μA
Serial Data Transfer Pins							
Logic pin input current		I_{IN}L	V_{IN} = 0 V (SCLK, DATA, STB)			1.0	μA
		I_{IN}H	V_{IN} = 5 V (SCLK, DATA, STB)		50	70	μA
Logic high-level input voltage		V_{IN}H	SCLK, DATA, STB	3.5			V
Logic low-level input voltage		V_{IN}L	SCLK, DATA, STB			1.5	V
Minimum SCLK high-level pulse width		Tsch		0.125			μs
Minimum SCLK low-level pulse width		Tscl		0.125			μs
Stipulated STB time		Tlat		0.125			μs
Minimum STB pulse width		Tlatw		0.125			μs
Data setup time		Tds		0.125			μs
Data hold time		Tdh		0.125			μs
Maximum CLK frequency		Fclk				4	MHz



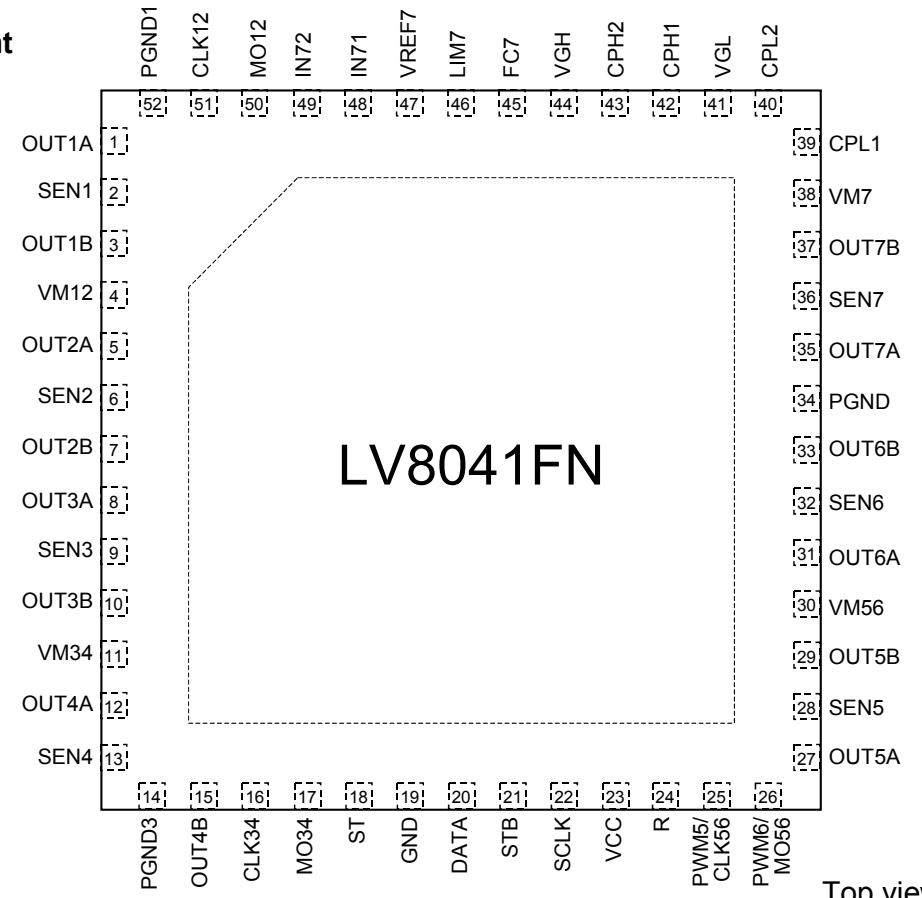
Package Dimensions

unit: mm
3305

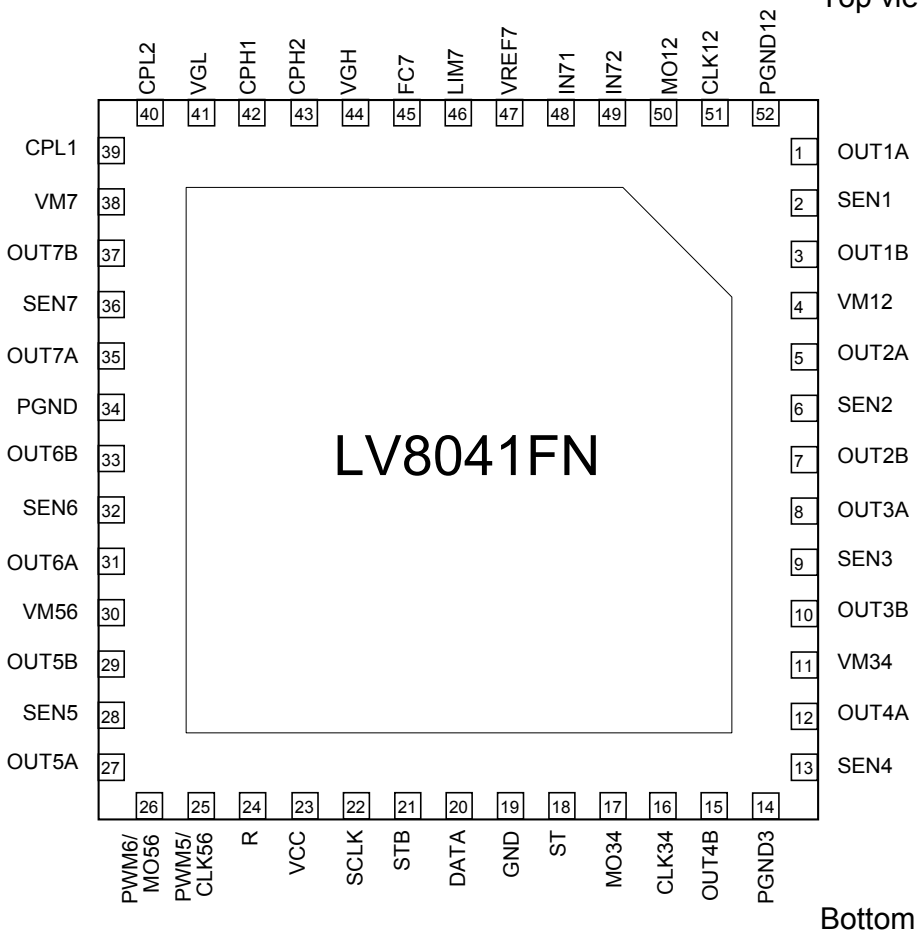




Pin Assignment

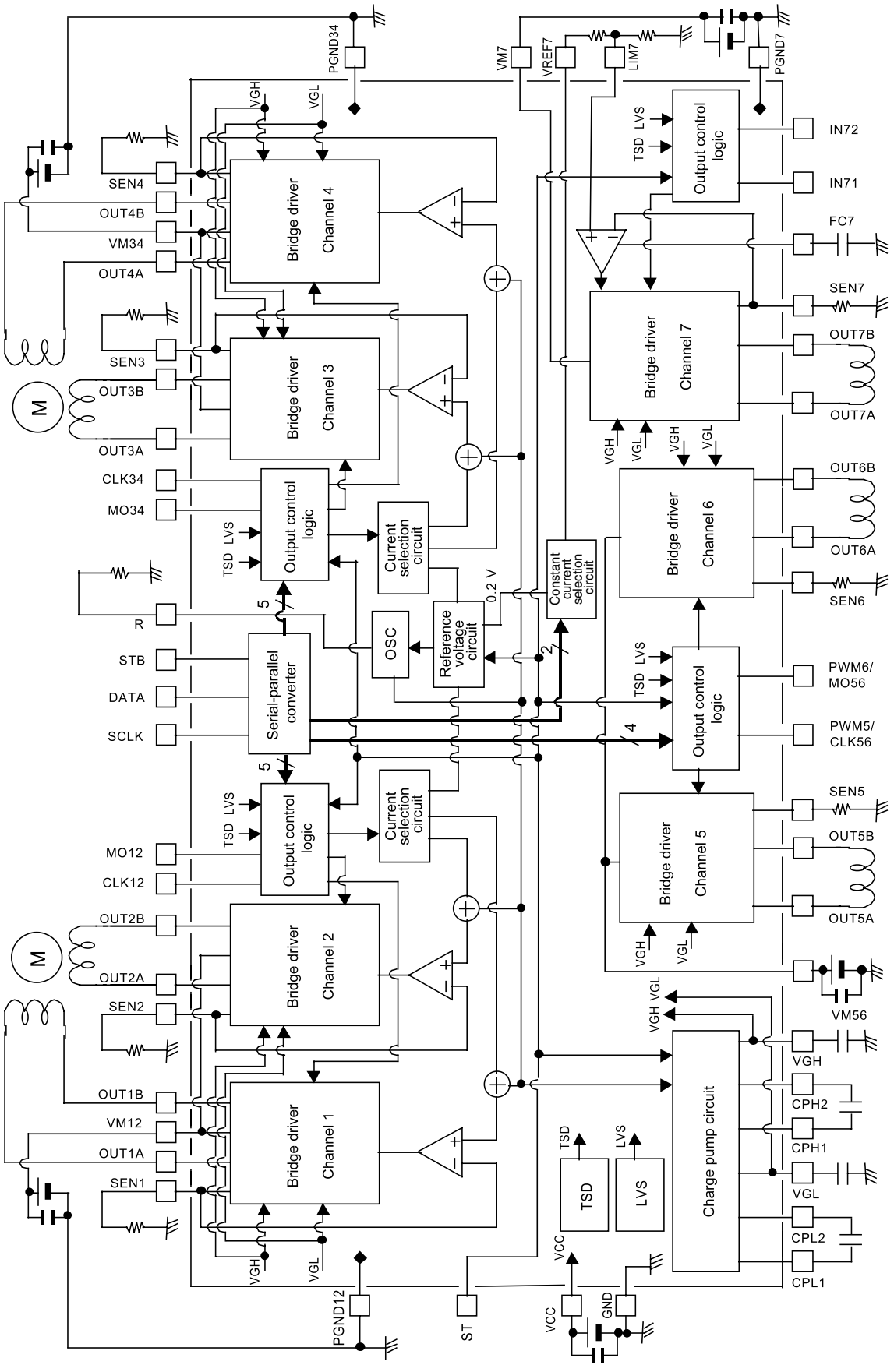


Top view



Bottom view

Block Diagram



Pin Functions

Pin No.	Symbol	Pin description
4	VM12	STP 1: Motor power supply
1	OUT1A	STP 1: Channel 1 OUTA output
3	OUT1B	STP 1: Channel 1 OUTB output
2	SEN1	STP 1: Channel 1 current sensing resistor connection
5	OUT2A	STP 1: Channel 2 OUTA output
7	OUT2B	STP 1: Channel 2 OUTB output
6	SEN2	STP 1: Channel 2 current sensing resistor connection
52	PGND12	STP 1: Power system ground
51	CLK12	STP 1: Clock signal input
50	MO12	STP 1: Phase detector monitor
22	SCLK	Serial data transfer clock input
20	DATA	Serial data input
21	STB	Serial data latch pulse input
24	R	Oscillator frequency setting resistor connection
11	VM34	STP 2: Motor power supply
8	OUT3A	STP 2: Channel 3 OUTA output
10	OUT3B	STP 2: Channel 3 OUTB output
9	SEN3	STP 2: Channel 3 current sensing resistor connection
12	OUT4A	STP 2: Channel 4 OUTA output
15	OUT4B	STP 2: Channel 4 OUTB output
13	SEN4	STP 2: Channel 4 current sensing resistor connection
14	PGND34	STP 2: Power system ground
16	CLK34	STP 2: Clock signal input
17	MO34	STP 2: Phase detector monitor
30	VM56	PWM: Channels 5 and 6 motor power supply
27	OUT5A	PWM: Channel 5 OUTA output STP 3: Channel 5 OUTA output
29	OUT5B	PWM: Channel 5 OUTB output STP 3: Channel 5 OUTB output
28	SEN5	STP 3: Channel 5 current sensing resistor connection
25	PWM5/CLK56	PWM: Channel 5 PWM signal input STP 3: Clock signal input
31	OUT6A	PWM: Channel 6 OUTA output STP 3: Channel 6 OUTA output
33	OUT6B	PWM: Channel 6 OUTB output STP 3: Channel 6 OUTB output
32	SEN6	STP 3: Channel 6 current sensing resistor connection
26	PWM6/MO56	PWM: Channel 6 PWM signal input STP 3: Phase detector monitor
38	VM7	Constant current drive: Channel 7 motor power supply
45	FC7	Constant current drive: Channel 7 phase compensation capacitor connection
36	SEN7	Constant current drive: Channel 7 current sensing resistor connection
35	OUT7A	Constant current drive: Channel 7 OUTA output
37	OUT7B	Constant current drive: Channel 7 OUTB output
48	IN71	Constant current drive: Channel 7 logic input 1
49	IN72	Constant current drive: Channel 7 logic input 2
34	PGND7	Constant current drive: Channel 7 power system ground
47	VREF7	Constant current drive: Channel 7 current control reference voltage output
46	LIM7	Constant current drive: Channel 7 constant current setting
39	CPL1	Charge pump capacitor connection
40	CPL2	Charge pump capacitor connection
42	CPH1	Charge pump capacitor connection
43	CPH2	Charge pump capacitor connection
41	VGL	Lower side DMOS gate voltage capacitor connection
44	VGH	Upper side DMOS gate voltage capacitor connection
18	ST	Chip enable
23	V_{CC}	Logic system power supply
19	GND	Signal system ground

Serial Data Input Specifications

• Register (D1, D0): Data transfer target register selection

D1	D0	Mode
0	0	Monitor/channels 5 and 6 drive mode settings
0	1	STP1 settings
1	0	STP2 settings
1	1	PWM/STP3 settings

The D1 and D0 bits in the serial data select the register used to set the motor driver state as shown above.

• Monitor/channel 5 and 6 drive mode settings

Register No.	Data	Symbol	Functions
D0	0	RG_SELECT1	Register selection 1
D1	0	RG_SELECT2	Register selection 2
D2	1 or 0	MO_SELECT1	MO12 output selection 1
D3	1 or 0	MO_SELECT2	MO12 output selection 2
D4	1 or 0	MO12_MD	MO12 output mode setting
D5	1 or 0	MO34_MD	MO34 output mode setting
D6	1 or 0	MO56_MD	MO56 output mode setting
D7	1 or 0	PWM/MICRO	Channel 5 and 6 drive mode setting

• STP1 Settings

Register No.	Data	Symbol	Functions	Channel
D0	1	RG_SELECT1	Register selection 1	
D1	0	RG_SELECT2	Register selection 2	
D2	1 or 0	F/R1	Forward/reverse setting	
D3	1 or 0	MS11	Microstep selection 1	
D4	1 or 0	MS12	Microstep selection 2	1ch, 2ch
D5	1 or 0	HOLD1	Step/hold setting	(STP1)
D6	1 or 0	RESET1	Logic reset	
D7	1 or 0	OUT ENABLE1	Output enable	

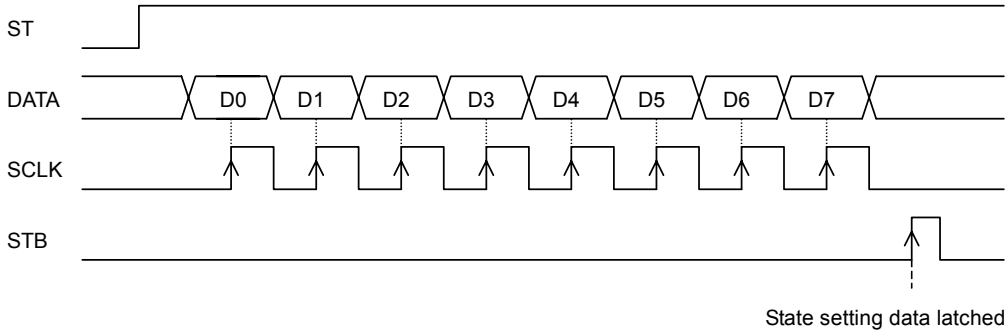
• STP2 Settings

Register No.	Data	Symbol	Functions	Channel
D0	0	RG_SELECT1	Register selection 1	
D1	1	RG_SELECT2	Register selection 2	
D2	1 or 0	F/R2	Forward/reverse setting	
D3	1 or 0	MS21	Microstep selection 1	
D4	1 or 0	MS22	Microstep selection 2	3ch, 4ch
D5	1 or 0	HOLD2	Step/hold setting	(STP2)
D6	1 or 0	RESET2	Logic reset	
D7	1 or 0	OUT ENABLE2	Output enable	

• Channel 5 and 6 Driver Settings

Register No.	Data	Symbol		Functions		Channel	
		Channel 5 and 6 drive mode setting register D7		PWM mode	STP3 mode		
		"0"	"1"				
D0	1	RG_SELECT1		Register selection 1			
D1	1	RG_SELECT2		Register selection 2			
D2	1 or 0	F/R5	F/R3	Forward/reverse setting	Forward/reverse setting	5ch PWM	5ch/6ch STP
D3	1 or 0	DECAY5	HOLD3	Current attenuation mode setting	Step/hold setting		
D4	1 or 0	F/R6	RESET3	Forward/reverse setting	Logic reset	6ch PWM	
D5	1 or 0	DECAY6	OUT ENABLE3	Current attenuation mode setting	Output enable		
D6	1 or 0	VSEN1		Current control reference voltage selection 1		5ch/6ch STP	
D7	1 or 0	VSEN2		Current control reference voltage selection 2			

Serial Data Input Settings



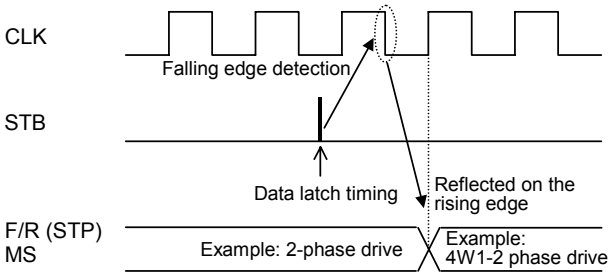
Data is input in order from data bit 0 to data bit 7. The data is transferred on the clock signal rising edge and after all the data has been transferred, it is latched on the rising edge of the STB signal.

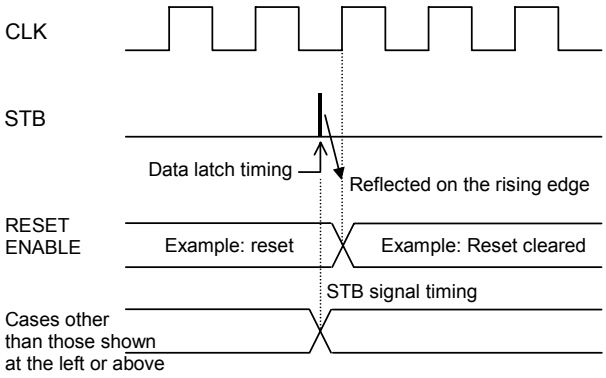
- Timing with which the serial data is reflected in the output

  Type 1: For the forward/reverse (FR) and drive mode (MS) settings in STP setting mode, after the data is latched, after the clock falling edge is detected, the new settings are reflected in the output on the next rising edge on the clock signal.

  Type 2: For the reset and output enable settings, after the data is latched, the new settings are reflected in the output on the next rising edge on the clock signal.

  Type 3: For settings other than those listed above, the new settings are reflected in the output at the same time as the data is latched with the STB signal.





Stepping Motor Drivers (STP1 (channels 1 and 2) and STP2 (channels 3 and 4))

Clock Function (STP1 (Items in parentheses refer to STP2))

Input		Operating mode	Charge pump circuit
ST	CLK12 (CLK34)		
Low	*	Standby mode	Stopped
High		Drive step operate	Operating
High		Drive step hold	

STP State Setting Serial Data Truth Table: Six bits (STP1/STP2 settings register)

D7 (OE)	D6 (RES)	D5 (HOLD)	D4 (MS2)	D3 (MS1)	D2 (F/R)	Operating mode
*	*	*	*	*	0	Clockwise (forward)
*	*	*	*	*	1	Counterclockwise (reverse)
*	*	*	0	0	*	2-phase drive
*	*	*	0	1	*	1-2 phase drive
*	*	*	1	0	*	2W1-2 phase drive
*	*	*	1	1	*	4W1-2 phase drive
*	*	0	*	*	*	Step/hold clear
*	*	1	*	*	*	Step/hold
*	0	*	*	*	*	Counter reset (Drive returns to the initial position)
*	1	*	*	*	*	Counter reset clear
0	*	*	*	*	*	Outputs set to the high-impedance state
1	*	*	*	*	*	Outputs set to the operating state

Note *: Don't Care

Initial Drive Position

Drive mode	1ch (3ch)	2ch (4ch)
2-phase	100%	−100%
1-2 phase	100%	0%
2W1-2 phase	100%	0%
4W1-2	100%	0%

Procedure for Calculating the Set Current

I_{OUT} = (reference voltage × set current ratio)/(sense resistor (SEN) value)

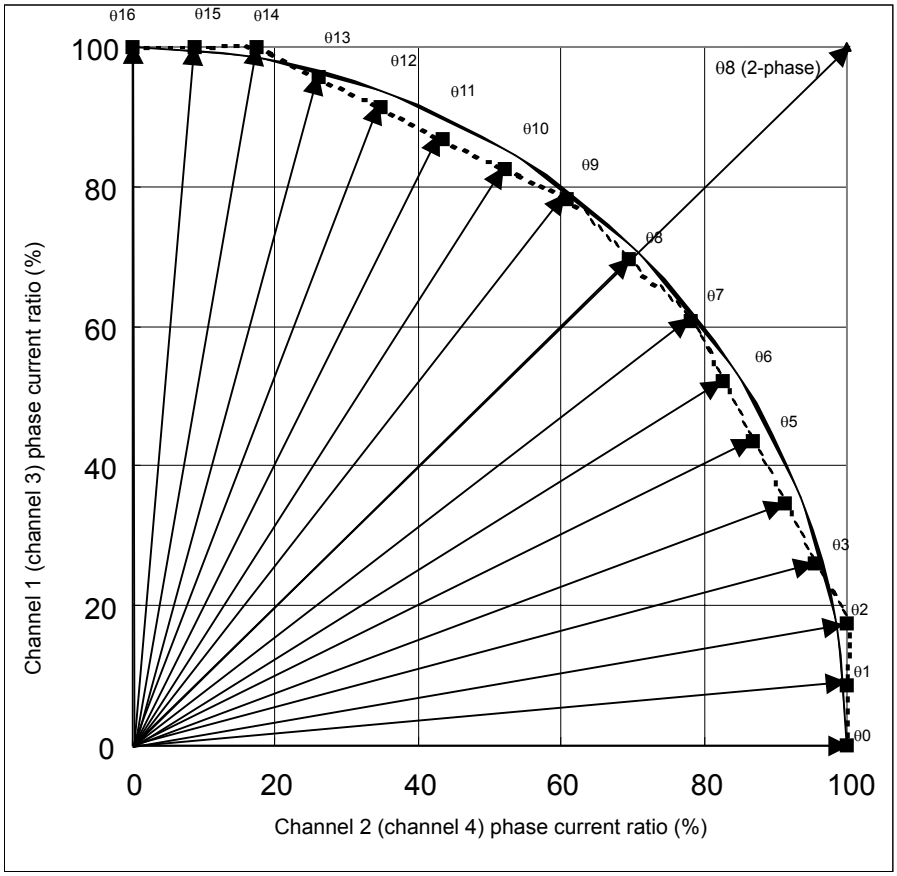
Since the reference voltage is 0.2 V, the following output current flows when the set current ratio is 100% and the sense resistor is 1 Ω.

I_{OUT} = 0.2 V × 100%/1 Ω

= 200 mA

Vary the value of the sense resistor (SEN) to vary the output current.

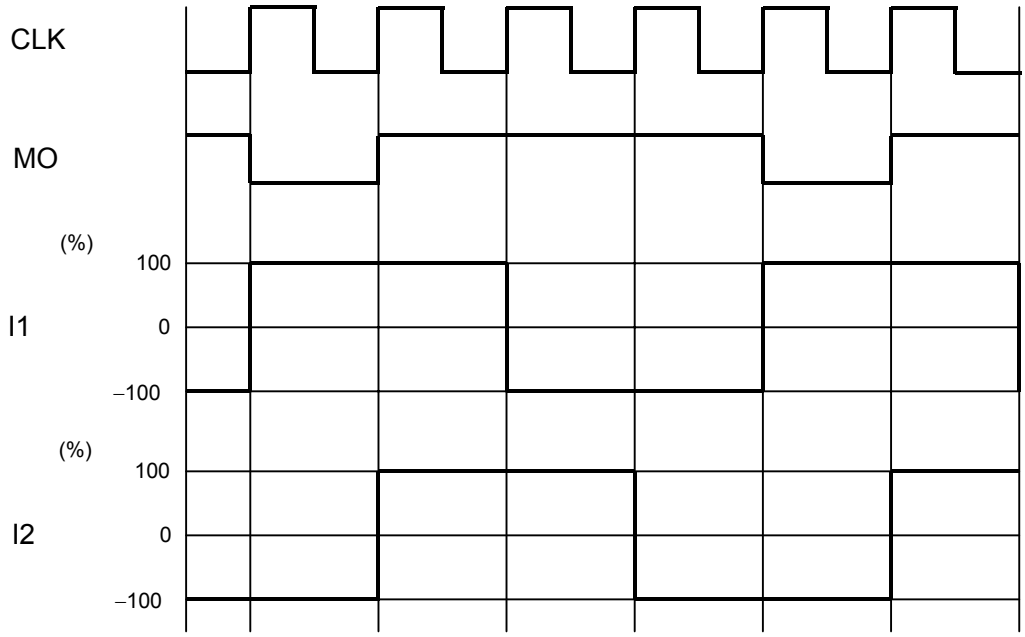
Output Current Vector Locus (One step is normalized to 90°)



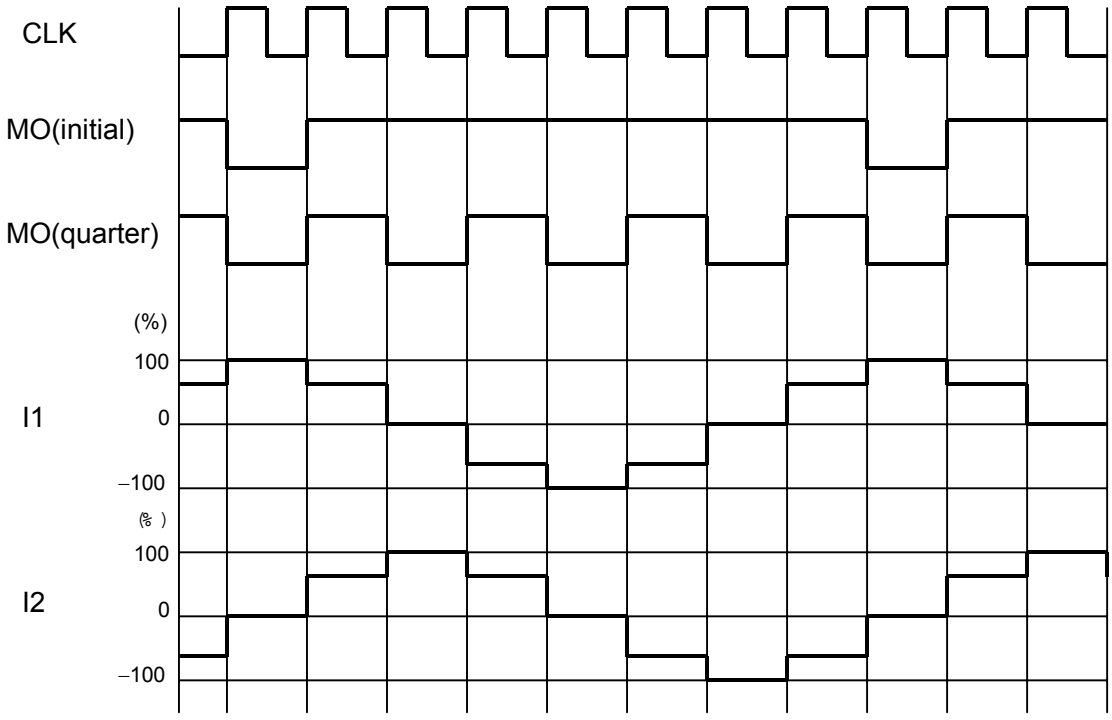
Set Current Ratios in the Various Drive Modes

STEP	4W1-2 phase (%)		2W1-2 phase (%)		1-2 phase (%)		2 phase (%)	
	1ch(3ch)	2ch(4ch)	1ch(3ch)	2ch(4ch)	1ch(3ch)	2ch(4ch)	1ch(3ch)	2ch(4ch)
θ0	0	100	0	100	0	100		
θ1	8.69	100						
θ2	17.39	100	17.39	100				
θ3	26.08	95.65						
θ4	34.78	91.3	34.78	91.3				
θ5	43.48	86.95						
θ6	52.17	82.61	52.17	82.61				
θ7	60.87	78.26						
θ8	69.56	69.56	69.56	69.56	69.56	69.56	100	100
θ9	78.26	60.87						
θ10	82.61	52.17	82.61	52.17				
θ11	86.95	43.48						
θ12	91.3	34.78	91.3	34.78				
θ13	95.65	26.08						
θ14	100	17.39	100	17.39				
θ15	100	8.69						
θ16	100	0	100	0	100	0		

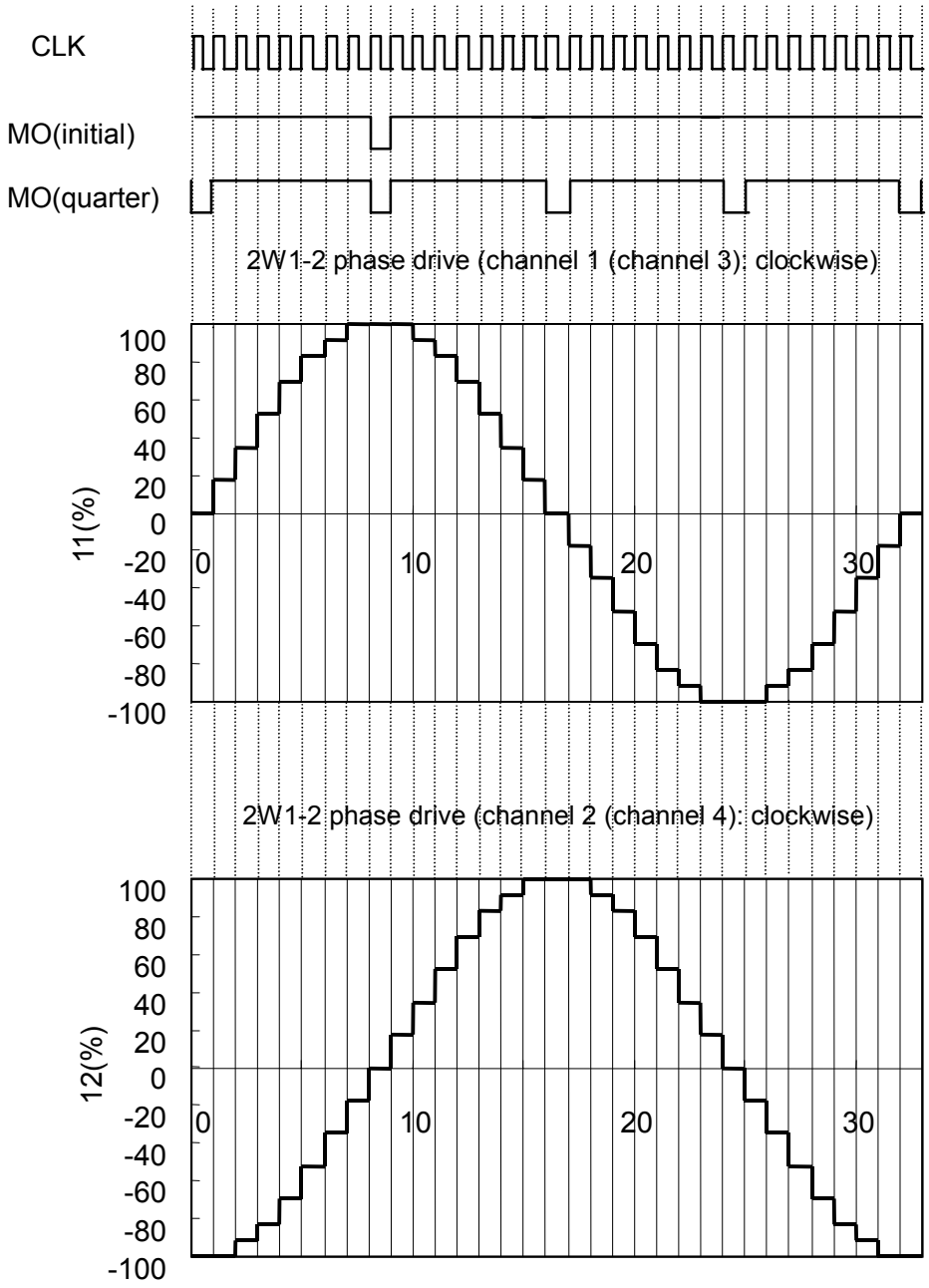
2-Phase Drive (D4 = 0, D3 = 0, D2 = 0: clockwise mode)



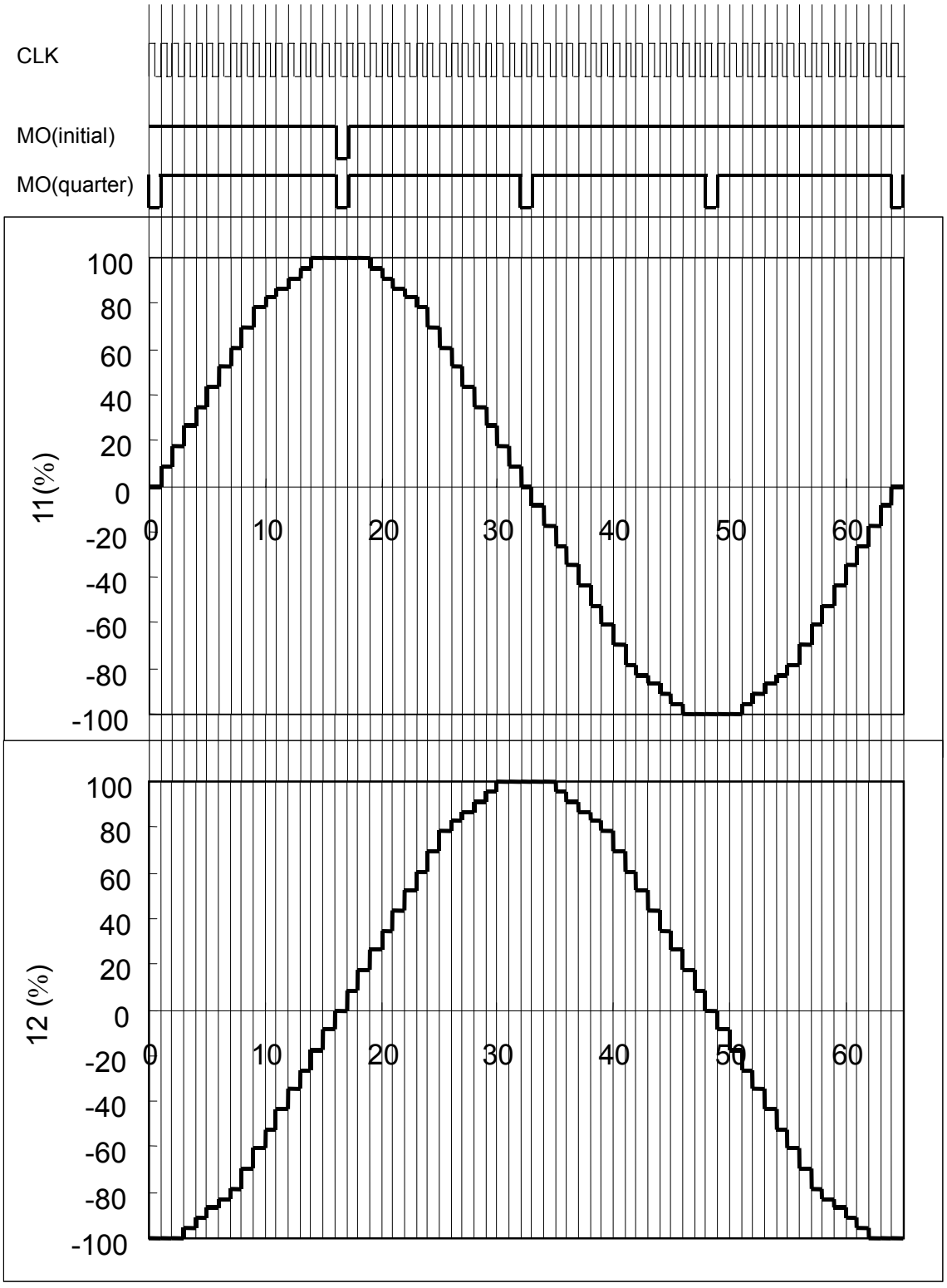
1-2 Phase Drive (D4 = 0, D3 = 1, D2 = 0: clockwise mode)



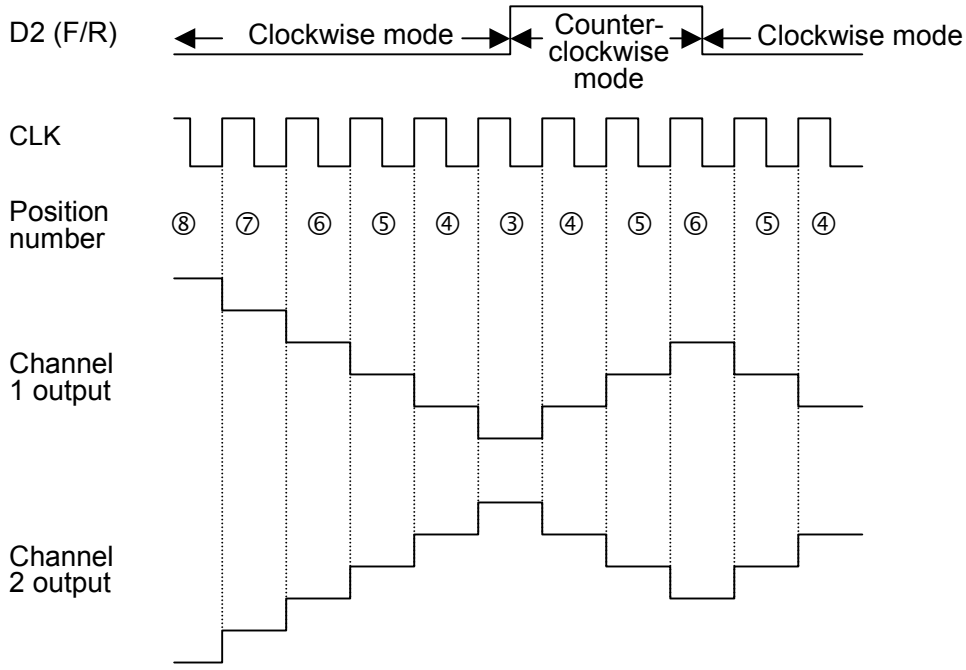
2W1-2 Phase Drive (D4 = 1, D3 = 0, D2 = 0: clockwise mode)



4W1-2 Phase Drive (D4 = 1, D3 = 1, D2 = 0: clockwise mode)

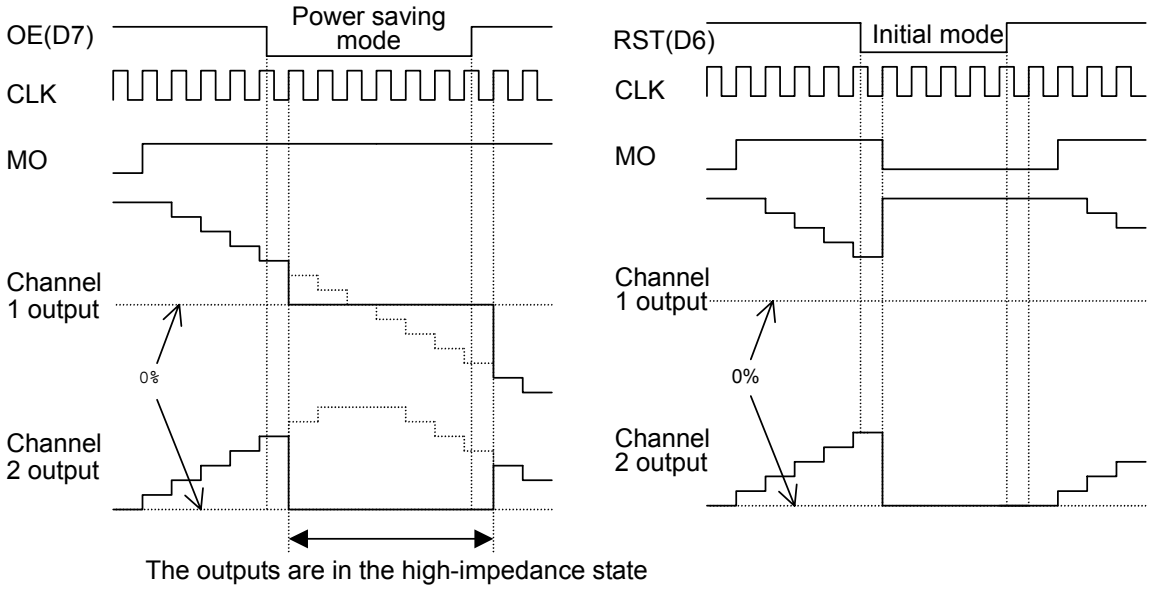


Set Current Step Switching (CLK pin), Forward/Reverse Switching (D2 (F/R)) Basic Operation



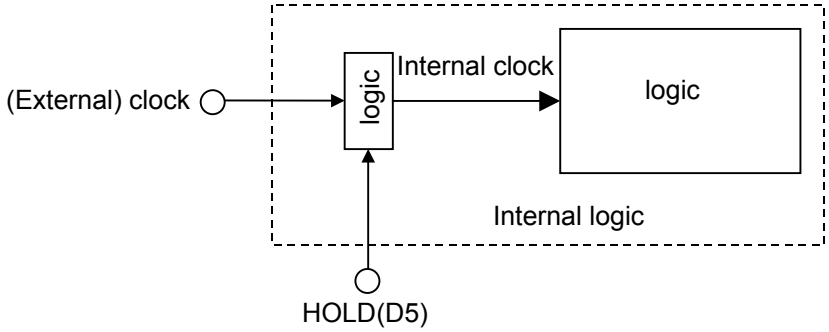
The IC internal D/A converter advances by one bit on the rising edge of each input clock pulse.
The clockwise/counterclockwise direction mode is switched by the D2 (F/R) data bit, and the direction in which the position number advances is changed by switching this mode.
In clockwise mode, the channel 2 current phase is delayed by 90° as seen from the channel 1 current.
In counterclockwise mode, the channel 2 current phase leads by 90° as seen from the channel 1 current.

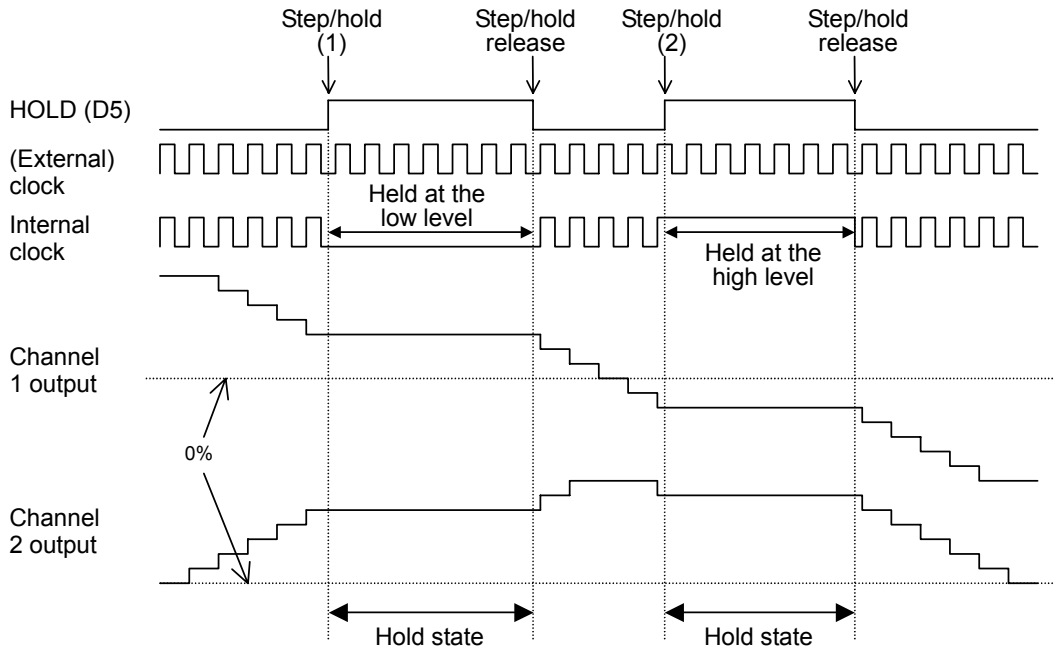
Output Enable (D7) and Reset (D6) Operational Description



When OE (D7) is set to 0, the outputs will be turned off on the next clock rising edge and set to the high-impedance state. However, since the internal logic circuits continue to operate, the position number will advance if the clock signal is input. Therefore, when OE (D7) is returned to 1, the IC will output levels according to the position number that has been advanced by the clock input.
When RST (D6) is set to 0, the outputs are set to the initial state at the next clock rising edge, and the MO output goes to the low level. When RST (D6) is set to one after that, the operation starts from the initial state on the next clock input, and the position number begins advancing.

Hold Bit (D5) Operational Description

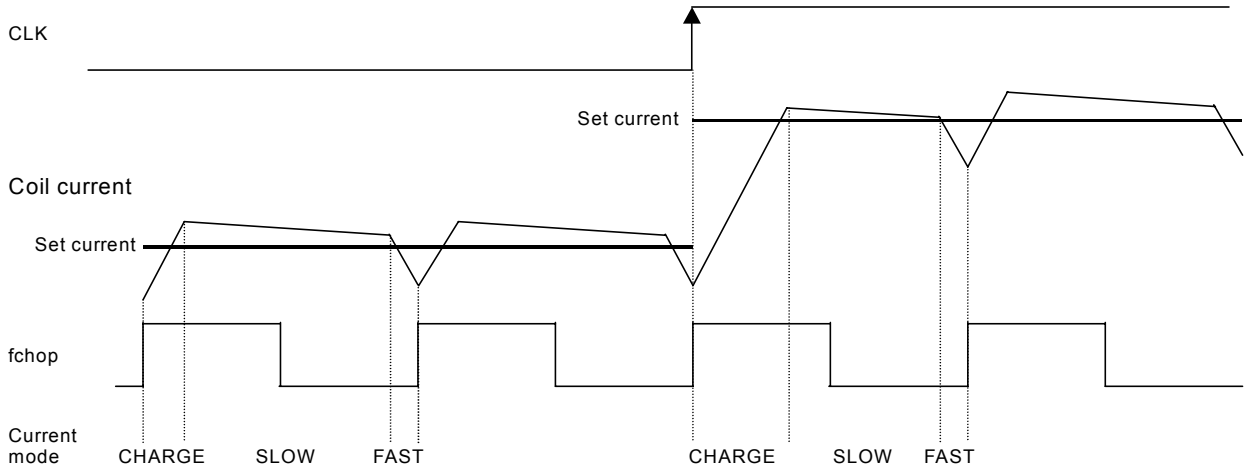




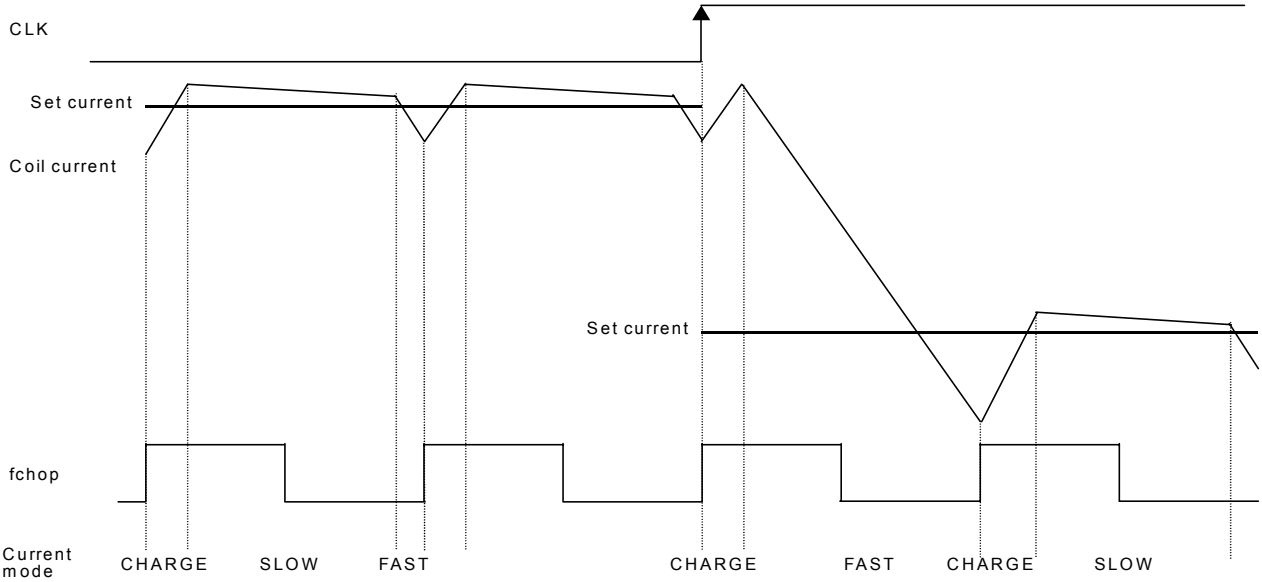
When the HOLD bit (D5) is set to 1, the internal clock signal is held at the state of the external clock at that point.
Since the external clock is low at the timing of the step/hold (1) operation in the figure, the internal clock is then held at the low level. Similarly, since the external clock is high at the timing of the step/hold (2) operation in the figure, the internal clock is then held at the high level.
When the HOLD bit (D5) is set to 0, the internal clock is synchronized with the normal (external) clock.
The outputs retain their states at the time the step/hold operation was input, and after the step/hold is released, they proceed with the timing of the next input clock rising edge.
As long as the IC is in the hold state, the position number will not be advanced even if the external clock signal is input.

Current Control Operation Specifications

- Sine Wave Increasing Direction



- Sine Wave Decreasing Direction
  Each current mode operates with the following sequence.



- The IC goes to charge mode during chopping oscillation startup. (A period in which the IC forcibly operates in charge mode exists as 1/8 of a single chopping period regardless of the relationship between the magnitudes of the coil current (ICOIL) and the set current (IREF).)
- During charge mode, the IC compares the coil current (ICOIL) and the set current (IREF).

  If the ICOIL < IREF state occurs during charge mode:
  – Charge mode continues until ICOIL ≥ IREF. After that, the IC switches to slow decay mode and then switches to fast decay mode for the last 1/8 of a single chopping period.

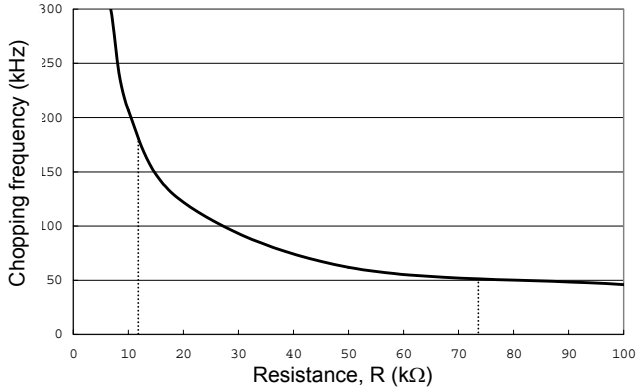
  If the ICOIL < IREF state does not occur during charge mode:
  – The IC switches to fast decay mode and the coil current is attenuated in fast decay mode until the end of the single chopping period.

The IC repeats the above operation. Normally, in the sine wave increasing direction, the IC operates in slow (+ fast) decay mode, and in the sine wave decreasing direction, the IC operates in fast decay mode until the current is attenuate to the set level, and then the IC operates in slow decay mode.

- Setting the Chopping Frequency (fchop)

  When this IC performs constant current control, it uses a chopping operation based on a frequency set by an external resistor.

  The chopping frequency set by the value of the resistor connected to the R pin (pin 24) is set as shown in the figure below.



We recommend that a frequency in the range 50 kHz to 200 kHz be used.

Serial Data Truth Table for Monitor Output Settings (Monitor/channel 5 and 6 drive mode settings register)

- MO12 Output Setting: 2 bits

D3(MO_SELECT2)	D2(MO_SELECT1)	MO12 output state
0	0	The STP1 monitor is output
0	1	The STP2 monitor is output
1	0	The STP3 monitor is output (If PWM/MICRO is 1.)
1	1	A fixed high level is output

The MO12 pin can be set up to output any of the stepping motor driver states shown in the table above with the monitor settings register settings shown in that table.

- Monitor Output Mode Setting: 3 bits

D6 (MO56_MD)	D5 (MO34_MD)	D4 (MO12_MD)	Monitor output mode state
*	*	0	A low level is output from MO12 in the STP1 initial state (Only when (D3, D2) = (0, 0))
*	*	1	A low level is output from MO12 each STP1 1/4 period (Only when (D3, D2) = (0, 0))
*	0	*	A low level is output from MO34 in the STP2 initial state (When (D3, D2) = (0, 1) this is also output from MO12)
*	1	*	A low level is output from MO34 each STP2 1/4 period (When (D3, D2) = (0, 1) this is also output from MO12)
0	*	*	A low level is output from MO56 in the STP3 initial state (When (D3, D2) = (1, 0) this is also output from MO12)
1	*	*	A low level is output from MO56 each STP3 1/4 period (When (D3, D2) = (1, 0) this is also output from MO12)

Note ∗: Don't Care

The stepping motor driver monitor outputs can be switched between a mode in which an output is only provided in the initial position and a mode in which an output is provided each 1/4 period by setting the monitor setting register as shown in the table above.

PWM Drive Forward/Reverse Motor Driver (Channels 5 and 6)

Drive Mode Setting Serial Data Truth Table: 1 bit (Monitor/channel 5 and 6 drive mode settings register)

D7(PWM/MICRO)	Operating mode	Pin functions	
		Pin 25	Pin 26
Low	PWM: 2 systems	PWM5	PWM6
High	One microstep drive STP system	CLK56	MO56

The circuit operating mode can be switched between direct PWM drive H bridge drive operation and 2W1-2 phase microstep drive stepping motor drive operation by setting the D7 bit (PWM/MAICRO) as shown in the table above.

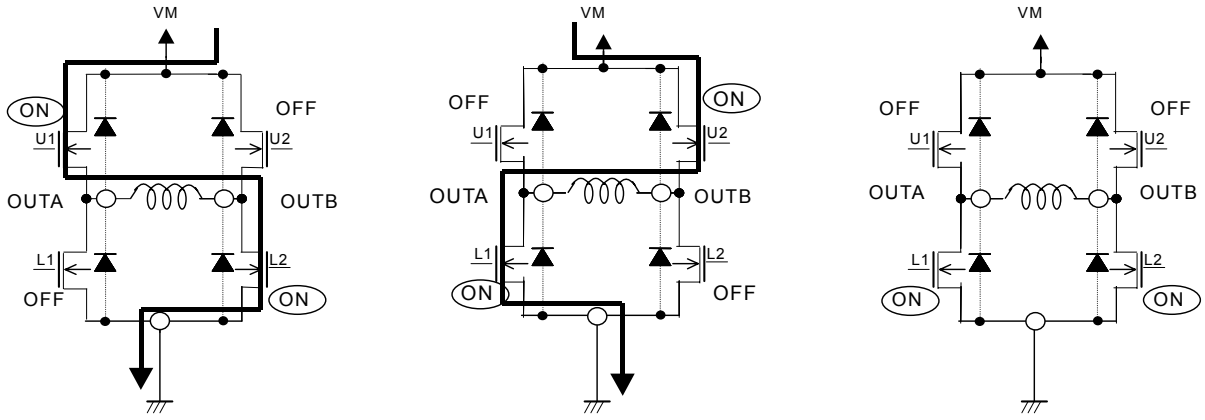
PWM Drive Mode (Channels 5 and 6 drive mode setting register bit D7 = 0)

- Truth Table (Channels 5 and 6 driver settings register)

Inputs				Outputs		Operating mode	Charge pump circuit
ST	PWM5 (PWM6)	D2 (D4)	D3 (D5)	OUTA	OUTB		
Low	*	*	*	OFF	OFF	Standby mode	Stopped
High	High	Low	*	High	Low	Clockwise (forward)	Operating
High	High	High	*	Low	High	Counterclockwise (reverse)	
High	Low	*	Low	OFF	OFF	Fast decay (output off)	
High	Low	*	High	Low	Low	Slow decay (short-circuit braking)	

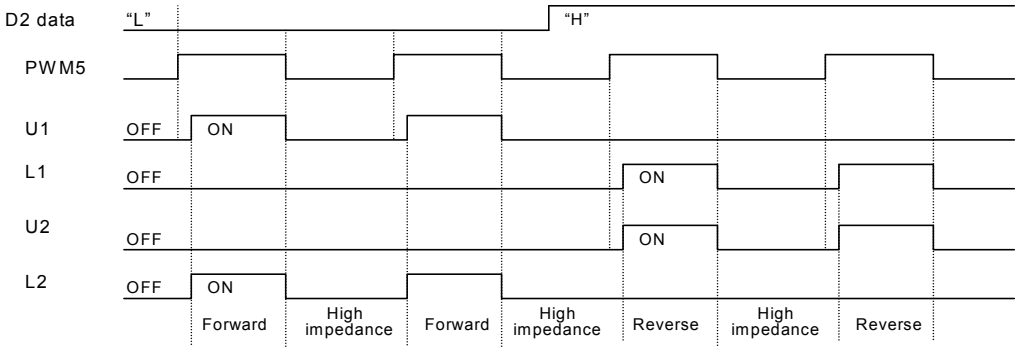
Note *: Don't care

- Output Stage Transistor Functions

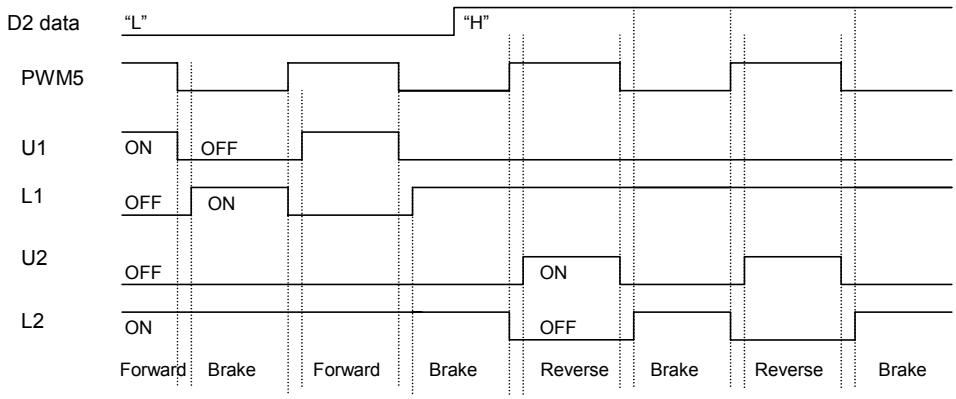


(Forward) (Reverse) (Brake)

- Forward/Reverse Output Operation Timing Chart (D3 = 0)



• Brake Mode Output Operation Timing Chart (D3 = 1)



Microstep Drive Mode (Channels 5 and 6 drive mode setting register bit D7 = 1)

Clock Function (STP3)

Input		Operating mode	Charge pump circuit
ST	CLK56		
Low	*	Standby mode	Stopped
High	↑	Drive step mode	Operating
High	↓	Drive step hold	

STP State Setting Serial Data Truth Table: 4 bits (Channels 5 and 6 driver settings register)

D5 (OE3)	D4 (RES3)	D3 (HOLD3)	D2 (F/R3)	Operating mode
*	*	*	0	Clockwise (forward)
*	*	*	1	Counterclockwise (reverse)
*	*	0	*	Step/hold clear
*	*	1	*	Step/hold
*	0	*	*	Counter reset (Drive goes to the initial position)
*	1	*	*	Counter reset release
0	*	*	*	Outputs: high impedance
1	*	*	*	Output operating state

Note *: Don't Care

Initial Drive Position

Drive mode	Initial mode	
	5ch	6ch
2W1-2 phase drive	100%	0%

Reference Voltage Setting Serial Data: 2 bits (Channels 5 and 6 driver settings register)

D7 (VSEN2)	D6 (VSEN1)	Current control reference voltage (when 100%)
0	0	0.2 V
0	1	0.134 V
1	0	0.1 V
1	1	0.066 V

Set Current Calculation

I_{OUT} = (reference voltage × set current ratio)/(sense resistor (SEN) value)

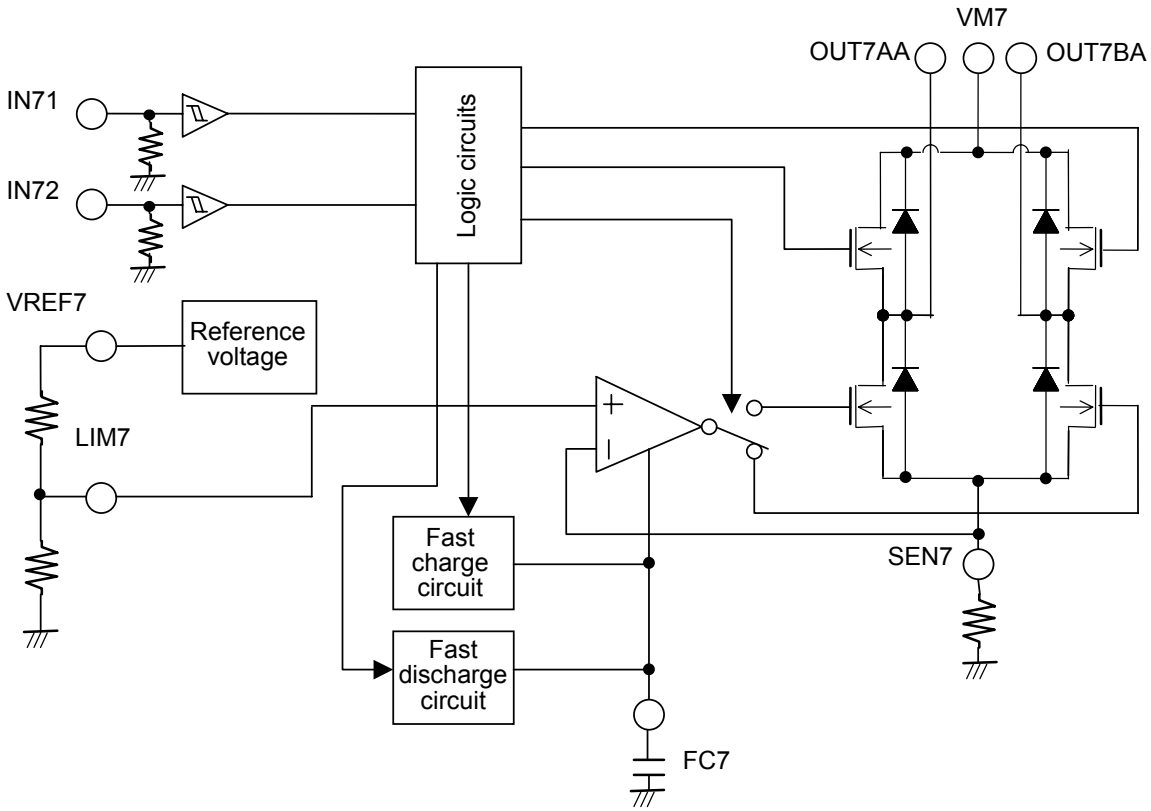
Since the reference voltage can be set to either 0.2, 0.134, 0.1, or 0.066 V with the serial data, the output current can be set with either the reference voltage or the value of the sense resistor SEN.

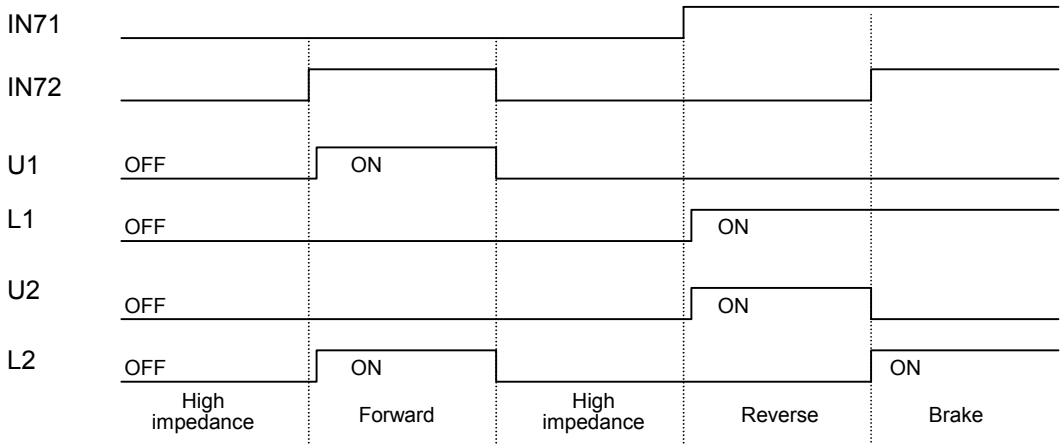
Constant Current Forward/Reverse Motor Driver (Channel 7)

Truth Table

Inputs			Outputs		Mode	Charge pump circuit
ST	IN71	IN72	OUT7A	OUT7B		
Low	*	*	OFF	OFF	Standby mode	Stopped
High	Low	Low	OFF	OFF	Outputs off	Operating
High	Low	High	High	Low	Forward	
High	High	Low	Low	High	Reverse	
High	High	High	Low	Low	Brake	

Note *: Don't care





Set Current Calculation

I_{OUT} = LIM7 voltage/SEN7 resistor

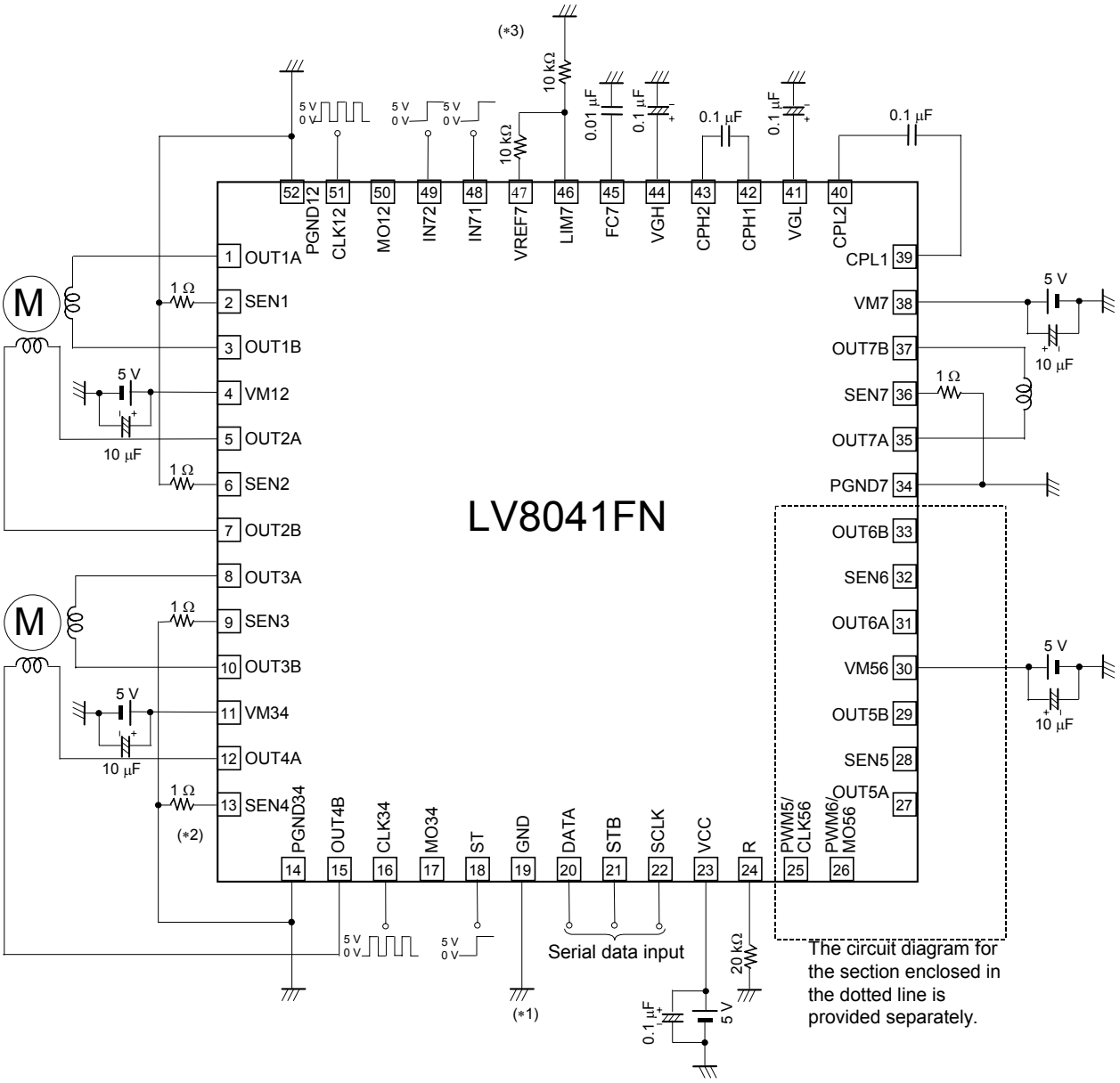
Since the LIM7 voltage is an external input, the reference voltage can be set arbitrarily.

The reference voltage can be set to 0.2 V by using the VREF7 pin and shorting it to the LIM7 pin. If a voltage created by resistor dividing the VREF7 voltage is input to LIM7, the reference voltage can be made variable (to voltages under 0.2 V).

Recommended Application Circuit

The values shown near the various pins are recommended values. See the Allowable Operating Ranges table earlier in this document for numerical values for the input conditions.

Channels 1 and 2: Microstep drive
Channels 3 and 4: Microstep drive
Channels 5 and 6: Described separately
Channel 7: Constant current drive



Note ∗1: Use a single point ground for the ground lines if at all possible.

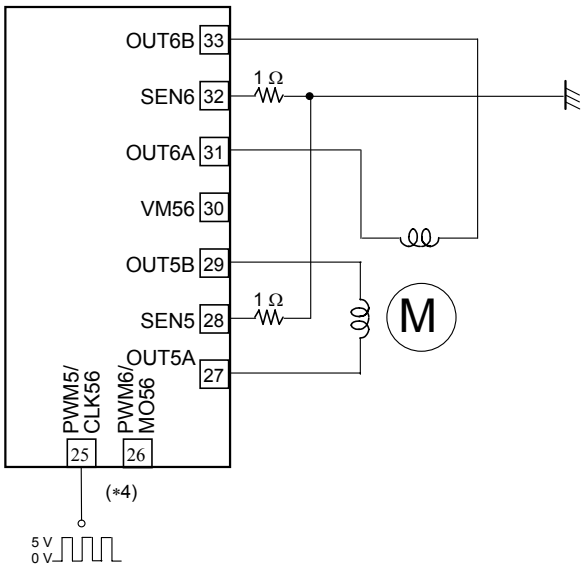
∗2: Here, a 1 Ω resistor is attached for each of the SEN pin resistors. This sets an output of 200 mA when the current ratio is 100%.

∗3: The LIM7 reference voltage can be provided either as an external voltage or by using VREF7: either voltage dividing VREF7 (0.2 V) or simply shorting LIM7 to VREF7.

Channels 5 and 6 Recommended Circuit

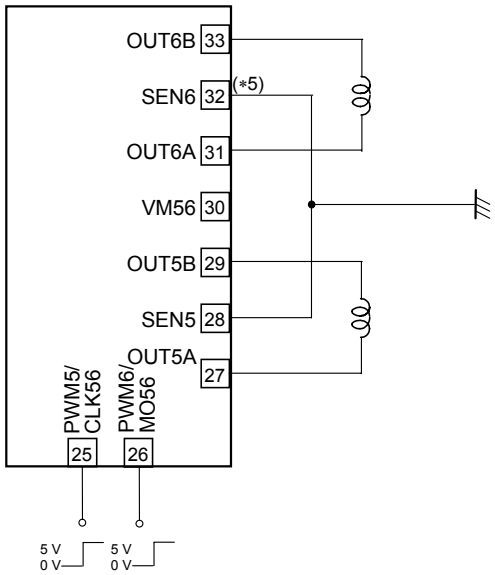
The channels 5 and 6 systems can be switched between microstep drive and PWM drive.
Set the mode using the serial data as described earlier in this document.

Application 1 ... Microstep Drive Mode (Fixed 2W1-2 phase drive)



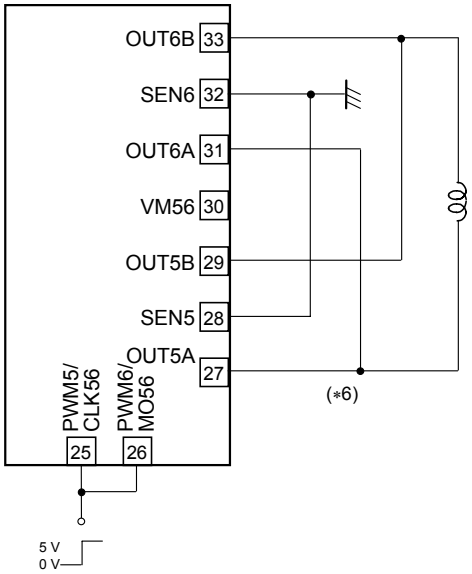
Note ∗4: In microstep drive mode, pin 26 functions as a position detection monitor pin.

Application 2 ... PWM Drive Mode (1)



Note ∗5: Since the current limiter does not operate in PWM drive mode, the sense resistor is not needed.

Application (3) PWM Drive Mode (2) (Doubled output capacity)



Note ∗6: Short the inputs together.
(Also short the outputs together. Do not short the outputs incorrectly: short OUT5A to OUT6A and short OUT5B to OUT6B.)