Preliminary **IBM 1394a 400Mb/s Physical Layer Transceiver (PHY)**

Features

- Complies with IEEE-1394-1995 [1] and the P1394a Supplement, version 2.0 [2].
- 400Mb/s max data rate; interoperable with 100 & 200Mb/s devices
- Available with one, two, or three ports
- Fully compliant with OpenHCI requirements
  - Programmable Port Disable
  - No phy_ID wrap past 63
- Selectable Link-PHY interface timings
- Advanced power management:
  - Programmable power save mode on unconnected ports
  - Sleep mode to minimize quiescent power
  - Sophisticated clock gating to reduce power consumption
- Single 3.3V power supply
- Tolerant of extra IDLE indications which circumvents Link-PHY "bus collision" conditions
- On-device PLL generates the 50MHz SCLK using an external crystal or crystal oscillator
- Supports optional 1394-1995 Isolation Barrier feature at Link-PHY Interface
- Supports optional IBM Dynamic Termination Isolation Barrier feature at Link-PHY Interface
- Interoperable with 5V Link Layer Controllers and 5V Transceivers
- Cable ports exceed 5kV of ESD protection (Human Body Model)
- Packet Separation Control for compatibility with some vendors' legacy hardware
- Fully integrated loop filter
- Easily configured as a repeater

Overview

The IBM21S860, IBM21S861, and IBM21S862 devices (PHYs) provide transceivers to implement a three, two, or one port node in a 1394 cable based network. The PHY complies with IEEE-1394-1995 [1] and the P1394a Supplement, version 2.0 [2]. These enhancements include Arbitrated Short Reset (for uninterrupted Isochronous data transport), multi-speed concatenation, accelerated arbitration techniques (to improve bandwidth utilization), Connection Debounce Hysteresis (to avoid "Reset Storms"), three independent TpBias regulators (providing the ability to disable individual ports), and numerous other features.

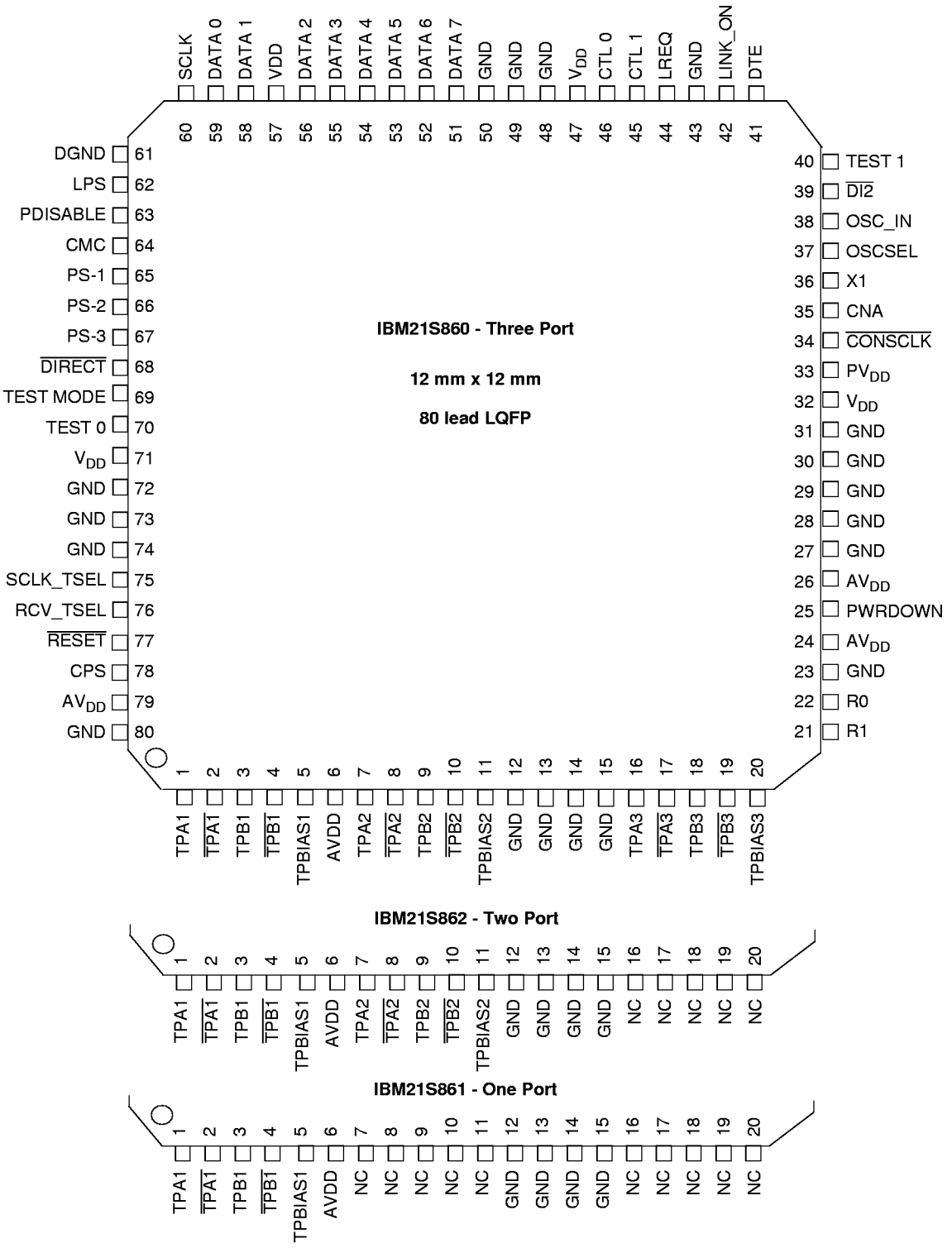
Each cable port is composed of two differential line transceivers (TPA and TPB) that transmit and receive serial data at 100, 200, or 400Mb/s (actually 98.304, 196.608, and 393.216Mb/s, respectively), depending on which data speed is routed through the bus. Each transceiver contains a differential current mode driver whose outputs provide signal swings around a common mode voltage called TpBias, which is generated on the PHY device. Two off-device 55 ohm resistors are connected in series across the differential outputs of each transceiver. TpBias voltage is connected to the midpoint connection of the resistors at TPA, while a 5Kohm resistor and a 250pF capacitor to ground are attached to the midpoint connection of the resistors at TPB. The TpBias voltage for the TPB line is supplied by the TPA of the PHY at the other end of the cable.

In addition to providing bus transceivers, the PHY serializes and deserializes data using Data and Strobe encoding. Data is sent from the Link Layer Controller to the PHY via a parallel interface. The parallel interface bus is up to 8 bits wide depending on the speed of the data (2 bits at 100Mb/s, 4 bits at 200Mb/s, and 8 bits at 400Mb/s). The two devices are synchronized by a 49.152MHz reference clock provided by the PHY. The data is then serialized and transmitted to the cable as Strobe on TPA and Data on TPB. Received data is resynchronized to the reference clock and decoded for parallel transmission to the Link Layer Controller.

PHY devices communicate their speed capabilities to one another through a process called Speed Signaling, in which common mode currents are withdrawn from the cable at TPB and $\overline{\text{TPB}}$. Three such common mode currents exist for this PHY: one for each of the supported transfer speeds. The nominal common mode currents are defined for 100Mb/s, 200Mb/s, and 400Mb/s as 0mA, -3.5mA, and -10mA respectively. The PHY is capable of 100, 200 or 400Mbits/sec operation, and will send or receive data at any of these speeds according to the capabilities of the adjacent PHYs.

Other functions of the PHY include system initialization and bus arbitration. The PHY also can determine whether or not a cable is attached to another PHY (con_status) as well as whether or not it is attached to an active PHY. Moreover, it functions as a repeater to pass data along the bus.

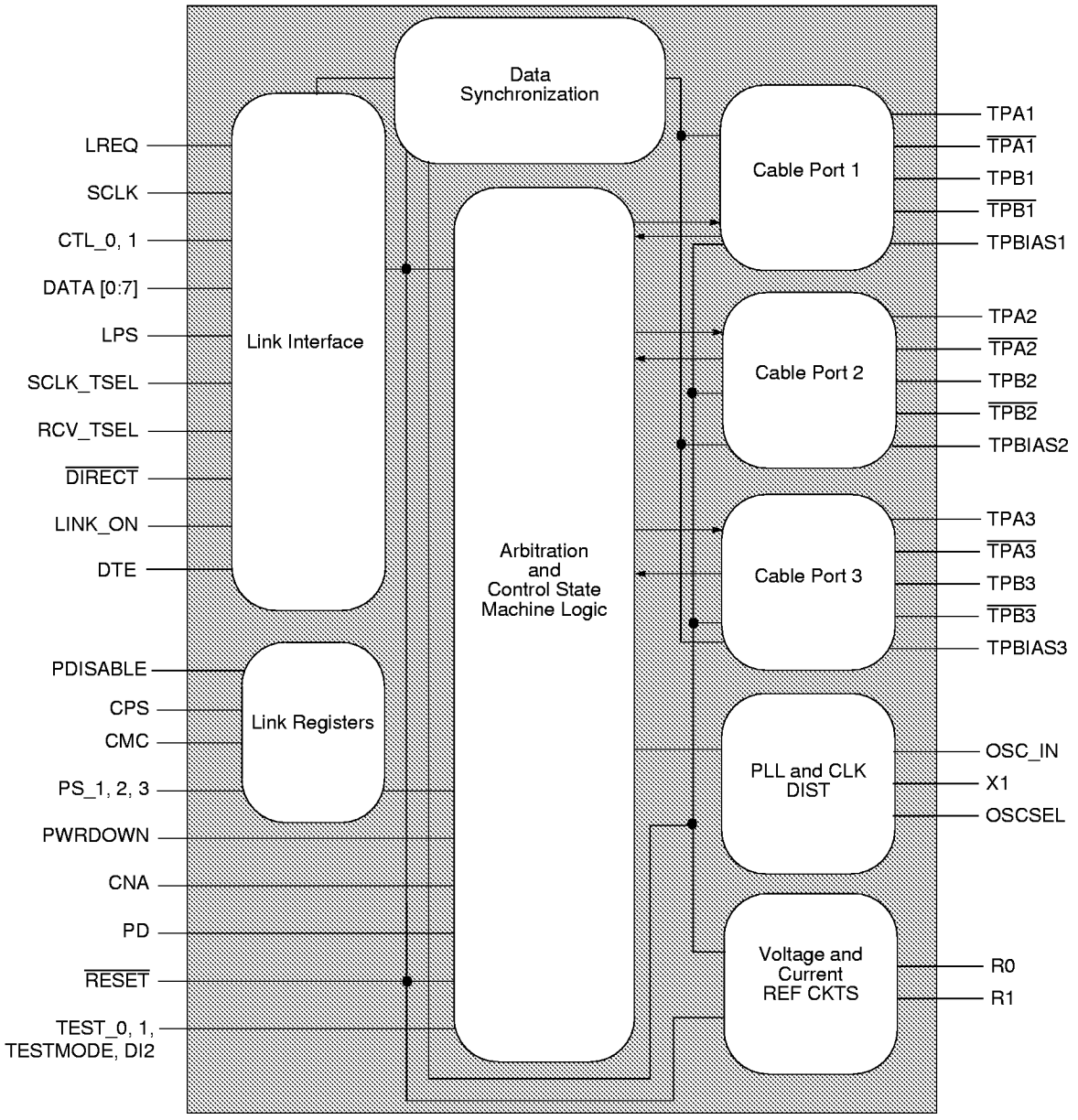
Pinout



Ordering Information

Product Number	Number of Ports	Maximum Data Rate	Power Supply
IBM21S860	3	400Mb/s	3.3V
IBM21S862	2	400Mb/s	3.3V
IBM21S861	1	400Mb/s	3.3V

Block Diagram: Three-Port PHY



Note: ¯ represents an active low input or inverted output

Circuit Description

Phase Locked Loop

The system reference clocks are generated by a frequency synthesizing Phase Locked Loop. The PLL generates a 49.152MHz system clock (SCLK) based on either an internal oscillator (with an external 24.576MHz crystal) or an external 24.576MHz crystal oscillator. The system clock is shipped to the Link Layer Controller to synchronize data transfer. The PLL also generates 98.304MHz, 196.608MHz, and 393.216MHz clocks for data encode/decode. All of the PLL loop filter components have been integrated onto the device, therefore no external components are needed for the loop filter.

Bandgap Reference Generator

The band gap reference generator provides a precision voltage supply from which several voltage and current sources required by the PHY are derived. One of the most important of these is the 4mA current source which is used in the current mode serial bus driver to maintain constant current.

TpBias Circuits

TpBias is a constant voltage source that maintains the common mode voltage of the TPA cable twisted pair at 1.84V nominal for each port. These PHYs contain one independent TpBias circuit per port. Each TpBias circuit can be disabled via software, thereby implementing the port disable feature required by OpenHCI. To meet the speed signaling requirements, each port must be used in conjunction with a 0.3μF minimum ceramic capacitor. The capacitor physical size is recommended to be the 0805 or 1206 form factor to reduce the parasitic inductance associated with the capacitor. The PHY registers enable software to disable any of the TpBias generators. In addition, the PDISABLE module pin allows the user to control the power-on-reset value for this port disable.

Analog Transceivers

There are two 4mA differential current mode serial bus drivers per port. They are designed to operate with external 110 ohm line matching resistor networks located at each end of the twisted pair cable. Each driver can be placed in a Hi-Z state in which the drive current is shut off. The receivers are connected to the drivers in a Bi-Di configuration, and capture differential data and strobe signals at each port.

The arbitration comparators are connected across the driver outputs, similar to the receivers. They detect logical DC levels used during bus arbitration. Two comparators are required per driver output, one to detect a logical “1” and one for a logical “0”. A logical “Z” state is also used in arbitration. It is considered to be the midpoint logical state in which both comparators are inactive.

The speed signaling comparator senses the common mode voltage at driver TPA and compares it with the TpBias reference, in order to detect whether any common mode controlled current signaling has been sent from the other end of the cable. The current pulses are used to signal the speed capability of the port at the other end.

The port status comparator senses the common mode voltage at driver TPB and compares it with a reference voltage, in order to detect whether TpBias voltage is being supplied by the port at the other end. It is used to determine whether or not the port is connected.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Supply voltage range	-0.3 to 5.1	V	1
V_{IN}	Logic input voltage range	-0.5 to 5.5	V	1
V_{OUT}	Logic output voltage range	-0.5 to 5.5	V	1
V_T	Test I/O voltage range	-0.5 to 3.6	V	1
V_C	Cable transceiver voltage range	-0.5 to 3.6	V	1
T_{OPR}	Operating Temperature	0 to 70	°C	1
T_{STG}	Storage Temperature	-65 to +150	°C	1

1. The device is not guaranteed to function at these limits, and exceeding the limits may damage the device.

Operating Conditions and Electrical Characteristics

The current polarity convention used in these tables is that current *into* a transceiver input is considered positive, while a current *out of* a transceiver output is considered positive.

Symbol	Parameter	Pin	Min	Typ	Max	Units
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
V_{OH}	High Level Output Voltage	CMOS outputs	2.6			V
V_{OL}	Low Level Output Voltage	CMOS outputs			0.4	V
V_{IH}	High Level Input Voltage	CMOS inputs	0.8 V_{DD}			V
V_{IL}	Low Level Input Voltage	CMOS inputs			0.2 V_{DD}	V
V_{ID}	Differential Input Voltage	Cable inputs	>90		265	mV
V_{IC}	Common Mode input Voltage	TPB, $\overline{TPB}$	1.165		2.515	V
		TPA, $\overline{TPA}$	1.665		2.015	V
V_{IT+}	Positive input threshold Voltage, V_{IT} + (Hysteresis)	LREQ, CTL, DATA	$V_{DD}/2 + 0.3$		$V_{DD}/2 + 0.8$	V
		LPS	1.33		1.75	V
		$\overline{RESET}$	1.35		1.8	V
V_{IT-}	Negative input threshold Voltage, V_{IT} - (Hysteresis)	LREQ, CTL, DATA	$V_{DD}/2 - 0.8$		$V_{DD}/2 - 0.3$	V
		LPS	1.04		1.42	V
		$\overline{RESET}$	0.8		1.24	V
V_{LREF}	LPS Reference Voltage (Isolation)	LPS		0.8		V
I_{IL}	Dynamic Termination Latch input Current @ V_{IL} = 0.66V	LREQ, CTL, DATA	0.1		1.2	mA
I_{IH}	Dynamic Termination Latch input Current @ V_{IH} = 2.64V	LREQ, CTL, DATA	-1.2		-0.1	mA
V_{OD}	Differential output voltage	Cable output	172	220	265	mV
V_O	Common mode output voltage	TPBIAS	1.665	1.85	2.015	V
I_{SP100}	S100 common mode output current (signaling off)	TPB, $\overline{TPB}$	-0.81		0.44	mA
I_{SP200}	S200 common mode output current (signaling on)	TPB, $\overline{TPB}$	-4.84	-3.5	-2.53	mA
I_{SP400}	S400 common mode output current (signaling on)	TPB, $\overline{TPB}$	-12.40	-10.00	-8.10	mA
I_{OL}	Output current @ 0.4V	SCLK	-9			mA
I_{OH}	Output current @ 2.6V	SCLK			9	mA
I_{OL}	Output current @ 0.4V	CTL, DATA	-9			mA
I_{OH}	Output current @ 2.6V	CTL, DATA			9	mA
I_O	Output current IO	TPBIAS1, TPBIAS2, TPBIAS3	-2.0		10.0	mA
T_{OPR}	Free Air Temperature		0		70	°C
P_{D3}	Power dissipation (3 port PHY)			0.6		W
P_{D2}	Power dissipation (2 port PHY)			0.5		W
P_{D1}	Power dissipation (1 port PHY)			0.45		W
I_{DD-PD}	The parameter is supply current during Power-down, or suspended mode.			3.0		mA

Data Signal Characteristics

Symbol	Parameter		Min	Typ	Max	Units
T_R	Output rise time		0.5	0.8	1.2	ns
T_F	Output fall time		0.5	0.8	1.2	ns
	Input slope		175			mV/ns
	Transmitter skew				0.10	ns
	Transmitter jitter				0.15	ns
	Skew at receive pins	Receiving 100Mb/s			0.80	ns
		Receiving 200Mb/s			0.55	ns
		Receiving 400Mb/s			0.50	ns
	Jitter at receiving pins	Receiving 100Mb/s			8.50	ns
		Receiving 200Mb/s			3.50	ns
		Receiving 400Mb/s			0.315	ns

I/O Pin Function (Part 1 of 3)

Pin Name	Function	Pin Number	Pin Type	I/O Type	Notes
TPA1	Port 1, Twisted pair A, positive signal	1	Differential	I/O	
$\overline{\text{TPA1}}$	Port 1, Twisted pair A, negative signal	2	Differential	I/O	
TPB1	Port 1, Twisted pair B, positive signal	3	Differential	I/O	
$\overline{\text{TPB1}}$	Port 1, Twisted pair B, negative signal	4	Differential	I/O	
TPBIAS1	Bias voltage/current supply for port 1 as defined in the P1394a draft V2.0 [2]	5	Supply	Output	
AV_{DD}	Analog circuit power (3.3V nom). These pins are separated from other power pins internal to the device to provide noise isolation. Decoupling capacitor networks are recommended at each pin. All the power supply pins should be tied together at a low impedance point on the circuit board.	6, 24, 26, 79	Supply	-	
TPA2	Port 2, Twisted pair A, positive signal	7	Differential	I/O	1
$\overline{\text{TPA2}}$	Port 2, Twisted pair A, negative signal	8	Differential	I/O	1
TPB2	Port 2, Twisted pair B, positive signal	9	Differential	I/O	1
$\overline{\text{TPB2}}$	Port 2, Twisted pair B, negative signal	10	Differential	I/O	1
TPBIAS2	Bias voltage/current supply for port 2 as defined in [2]	11	Supply	Output	1
GND	Digital circuit ground. These pins are separated from other ground pins internal to the device to provide noise isolation. All ground pins should be tied together at a low impedance point on the circuit board.	12, 13, 14, 15, 23, 27, 28, 29, 30, 31, 43, 48, 49, 50, 61, 72, 73, 74, 80	Supply	-	
TPA3	Port 3, Twisted pair A, positive signal	16	Differential	I/O	2
$\overline{\text{TPA3}}$	Port 3, Twisted pair A, negative signal	17	Differential	I/O	2
TPB3	Port 3, Twisted pair B, positive signal	18	Differential	I/O	2
$\overline{\text{TPB3}}$	Port 3, Twisted pair B, negative signal	19	Differential	I/O	2
TPBIAS3	Bias voltage/current supply for port 3 as defined in [2]	20	Supply	Output	2
R1, R0	3.01Kohm (±0.5%) external current setting resistor terminals	21, 22	Analog	Output	
PWRDOWN	Forces the PHY to immediately go to sleep	25	CMOS	Input	
V_{DD}	Digital circuit power (3.3V nom). These pins are separated from other power pins internal to the device to provide noise isolation. Decoupling capacitor networks are recommended at each pin. All the power supply pins should be tied together at a low impedance point on the circuit board.	32, 47, 57, 71	Supply	-	
PV_{DD}	PLL analog circuit power (3.3V nom). These pins are separated from other power pins internal to the device to provide noise isolation. Decoupling capacitor networks are recommended at each pin. All the power supply pins should be tied together at a low impedance point on the circuit board.	33	Supply	-	
$\overline{\text{CONSCLK}}$	Controls whether the PHY sends SCLK during POR. 1 = no SCLK during POR (P1394a behavior), 0 = SCLK outputted in POR. This pin contains an internal pull-up resistor to pull up a floating node to P1394a compliant behavior.	34	CMOS	Input	

1. These ports exist on the two and three-port PHYs only. These pins are NC on the one-port PHY.
2. These ports exist on the three-port PHY only. These pins are NC on the one and two-port PHY.
3. See Operating Conditions and Electrical Characteristics on page 6 for electrical characteristics.

I/O Pin Function (Part 2 of 3)

Pin Name	Function	Pin Number	Pin Type	I/O Type	Notes
CNA	Cable not active. 1 = the PHY is not detecting incoming bias on any of its ports. This pin is not debounced.	35	CMOS	Output	
X1	Second crystal input when operating with an external crystal.	36	Analog	Input	
OSCSEL	Selects whether the PHY is operating in crystal mode or oscillator mode. 0 = external crystal oscillator is attached to module pin 38 (OSC_IN). 1 = external crystal is attached between module pins 38 (OSC_IN) and 36 (X1). See External Component Connections on page 42.	37	CMOS	Input	
OSC_IN	Input for either a crystal or crystal oscillator @ 24.576MHz (±100 ppm), 3.3V. External oscillator provides stable reference frequency without sensitivity to board parasitics, and without the need for tank circuit components. This pin provides the X0 input when using only a crystal.	38	CMOS	Input	
$\overline{DI2}$	Driver Inhibit 2 test pin only. 1 = normal operation.	39	CMOS	Input	
TEST_1, 0	Reserved for test only. 0 = normal operation.	40, 70	CMOS	Input	
DTE	Dynamic termination enable pin. Used for Link-PHY interface isolation in instances where the Link uses bus holder circuitry. 1 = enable.	41	CMOS	Input	
LINK_ON	A 6MHz signal is transmitted from this pin when required by [2]. Link_on must be connected to a resistor (3.3K ohm recommended) to ground or floated if it is not utilized. See Link-On Packet Format on page 33.	42	CMOS	Output	
LREQ	Through the LREQ pin, the PHY receives serial commands from the Link. These commands include register reads, writes, arbitration commands, and access to the serial bus.	44	Hysteresis	I/O	3
CTL_1, 0	Link interface bidirectional control pins.	45, 46	Hysteresis	I/O	3
DATA [0:7]	Link interface bidirectional data pins.	59, 58, 56, 55, 54, 53, 52, 51	Hysteresis	I/O	3
SCLK	49.152MHz system clock to Link controller.	60	CMOS	Output	
PDISABLE	Controls whether the ports are disconnected or disabled after a power-on-reset. 0 = the port is in the disconnected state after a POR as defined in [2]. 1 = the port is in the disabled state after a POR.	63	CMOS	Input	
CMC	Bus Configuration Manager Contender. “1” causes the PHY to indicate in the self-ID packet that the node is capable of being the Bus Manager.	64	CMOS	Input	
LPS	Link power status as defined in [2].	62	Hysteresis	Input	3
PS_1, 2, 3	Power Status pins. These inputs are used to set the three POWER_CLASS bits in the self-ID packet. They describe the power consumption and source characteristics of the node, and are programmed by tying the pins high or low. PS_1, 2, & 3 are reflected in the self_id bits 21, 22, & 23, respectively.	65, 66, 67	CMOS	Input	
$\overline{DIRECT}$	Indicates presence of an Isolation Barrier using differentiated signals between the Link & PHY. 0 (GND) = direct coupling 1 (V_{DD}) = isolation with differentiated signals	68	CMOS	Input	
TEST_MODE	Reserved for test. For normal operation, connect to ‘0’ (GND).	69	CMOS	Input	

1. These ports exist on the two and three-port PHYs only. These pins are NC on the one-port PHY.
2. These ports exist on the three-port PHY only. These pins are NC on the one and two-port PHY.
3. See Operating Conditions and Electrical Characteristics on page 6 for electrical characteristics.

I/O Pin Function (Part 3 of 3)

Pin Name	Function	Pin Number	Pin Type	I/O Type	Notes
SCLK_TSEL	Select SCLK setting. 0 = default (P1394a) SCLK timing. 1 = alternate timings. See Link-PHY Interface Timing on page 15.	75	CMOS	Input	
RCV_TSEL	Select receive timing. This pin enables the selection of alternate timings between data received from the Link and the system clock. 0 = default (P1394a) timing. 1 = alternate timings. See Link-PHY Interface Timing on page 15.	76	CMOS	Input	
$\overline{\text{RESET}}$	Reset (active low). The reset pin requires a 220 ohm resistor to VDD and a 2.2uF capacitor to allow time for voltage buildup at power-on. 1 = normal operation of the PHY.	77	Custom	Input	3
CPS	Cable power status. This pin is connected to the cable power through a 400Kohm resistor. When cable power is considered lost when the cable voltage drops below 7.5V.	78	Analog	Input	3

1. These ports exist on the two and three-port PHYs only. These pins are NC on the one-port PHY.
2. These ports exist on the three-port PHY only. These pins are NC on the one and two-port PHY.
3. See Operating Conditions and Electrical Characteristics on page 6 for electrical characteristics.

Module Pin Differences between IBM21S850 Series and IBM21S860 Series PHYs

IBM21S850, 851	IBM21S860, 861, 862
Product recommends 1.0µF capacitors connected to TpBias1, TpBias2, and TpBias3.	Recommend 0.33µF capacitor connected to TpBias1, TpBias2, and TpBias3.
3.6Kohm ± 0.5% precision resistor between pins 21 & 22.	Value changed to 3.01Kohm ± 0.5% precision resistor between pins 21 & 22.
Pin 25 = AGND	Pin 25 = PWRDOWN. This pin may be left tied to ground or controlled by the application.
Pin 34 = PGND	Pin 34 = $\overline{\text{CONSCLK}}$. Pin tied to GND will cause SCLK pin 60 to function similarly to the IBM21S850 by supplying SCLK during power-on-reset.
0.1µF capacitor between pins 35 & 36.	Pin 35 = CNA output Pin 36 = X1 Oscillator mode: When repopulating an IBM21S850 with an IBM21S860 operating with a crystal oscillator, pin 35 may be floated or used by the application. Pin 36 may either be grounded or floated. Crystal Mode: When repopulating an IBM21S850 with an IBM21S860 operating with a crystal, X1 is tied to the crystal and its required load capacitor. CNA can be floated or used by the application.
Pin 37 = PGND	Pin 37 = OSCSEL. VDD = crystal mode, GND = oscillator mode.
Pin 38 = OSC_IN	Pin 38 = OSC_IN/X0. Connected to either the output of the crystal oscillator or the X0 of the crystal and its required load capacitor.
Pin 63 = SLEEP_EN	Pin 63 = PDISABLE.
CPS pin 78 recommends a diode to VDD along with a series 400Kohm resistor to sense cable power.	CPS pin 78 recommends a 390Kohm series resistor to sense when the cable power drops below 7.5V. The diode is not needed.

Establishing the Link-PHY Interface

Overview

The Link-PHY interface is a scalable, cost effective method for connecting one 1394 Link device to one 1394 PHY device. The characteristics of this interface are described in the diagram below and in the Link-PHY Interface Pin Description on page 12. The PHY device has control of the bidirectional pins. The Link only drives these pins when control is transferred to it by the PHY.

Data is transmitted between the two devices on the data bus. The data bus between the PHY and the Link device is clocked at the same rate for all supported speeds; however, the data rate is increased by widening the bus. The PHY uses two bits for 100Mb/s transfers, four bits for 200Mb/s, and eight bits for 400Mb/s. The control bus carries control information and is always two bits wide. The LREQ pin is used by the Link to request access to the serial bus and to read or write PHY registers. The $\overline{\text{DIRECT}}$ pin is used to disable the digital differentiator on the DATA and CTL pins, indicating that the two devices are connected directly, rather than through an isolation barrier requiring differentiating signals.

Specific guidelines for routing particular signals are given in Board Layout Recommendations on page 44.

Link-PHY Interface Pin Description

Pin	Driven By	Description
DATA(0:7)	Link & PHY (tri-state)	Data
CTL(0:1)	Link & PHY (tri-state)	Control
LREQ	Link	Link Request
SCLK	PHY	49.152MHz (sync to serial bus) clock
LINK_ON	PHY	Drives 6MHz signal to wake up Link when Link Power On packet is received and LPS = 0
LPS	Link	Link Power Status
$\overline{\text{DIRECT}}$	neither	Controls differentiator for interface pins

Link-PHY Electrical Isolation

The need to isolate the Link from the PHY electrically may arise when a difference in potential exists between their respective grounds (GND_L and GND_P). Each application should be assessed to determine whether the possibility exists that another device with a different ground potential could be attached to itself via a 1394 cable. If so, then isolation should be considered.

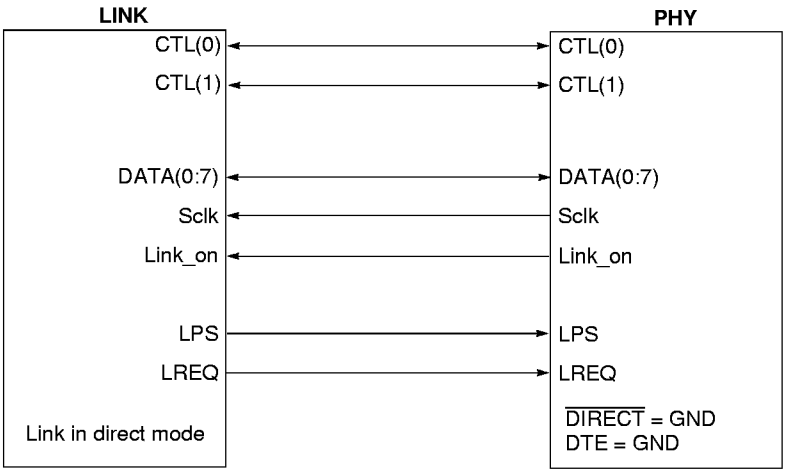
The PHY supports three types of connections between the Link and PHY: Direct, 1394-1995 Isolation, and IBM's Dynamic Termination for isolation between IBM's PHY and Links which support single capacitor isolation.

If isolation is required between the Link and PHY, the ground planes must be connected to each other by at least one trio of 0.001μF, 0.01μF, and 0.1μF coupling capacitors to provide an AC return path. The trio should be repeated as often as is feasible, equally distributed along the mutual borders of the ground planes, in close proximity to the PHY/Link interface signal traces.

Direct Connection Between Link and PHY

1. Link must be set in Direct mode.
2. $\overline{\text{DIRECT}}$ and DTE must be tied to ground.
3. LPS may be tied directly to the Link's V_{DD} if the Link does not support LPS.
4. If Link_on cannot be connected to the Link or Link support circuitry, it must be floated. This pin cannot be connected directly to ground.
5. The PHY supports communication with 3V or 5V Links.

Direct Connection Diagram



Capacitive Isolation with Differentiated Signals

The IBM PHY supports the Isolation barrier examples supplied in section 5.9.4 of [2]. This method requires that the $\overline{\text{DIRECT}}$ is tied to V_{DD} and DTE module pins are tied to GND.

Isolation Using IBM's Dynamic Termination

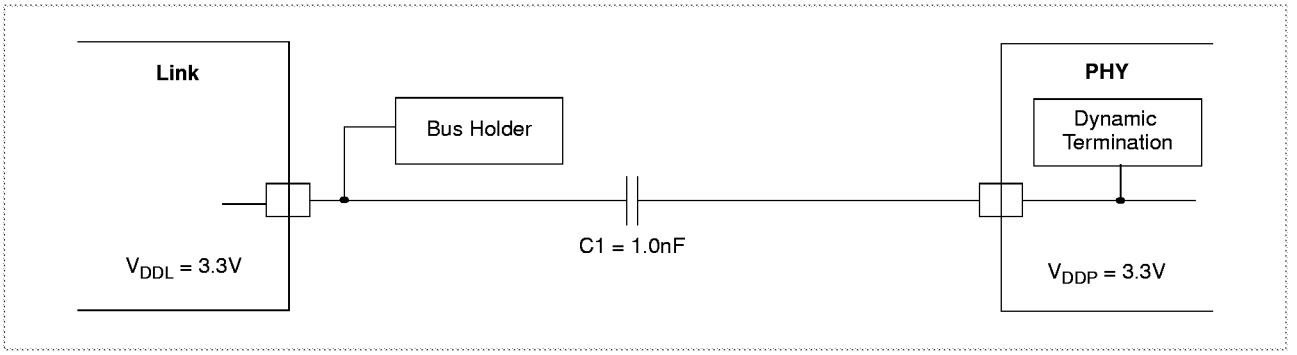
The Link and the PHY can be isolated using IBM's Dynamic Termination circuitry, provided that the power supply voltages of each are at the same nominal value. Isolation is achieved by using a 1.0nF capacitor, the PHY Dynamic Termination, and a Link bus latch, as shown below. For correct operation with isolation, please refer to the Dynamic Termination diagrams below.

The Link bus latch, which may be either built into the Link or external to it, holds received signals from the PHY at either an UP level or a DOWN level after they pass through the capacitor. Similarly, data pulses transmitted from the Link are held at their UP or DOWN levels by the Dynamic Termination of the PHY, which is enabled by tying the DTE pin high and the $\overline{\text{DIRECT}}$ pin low.

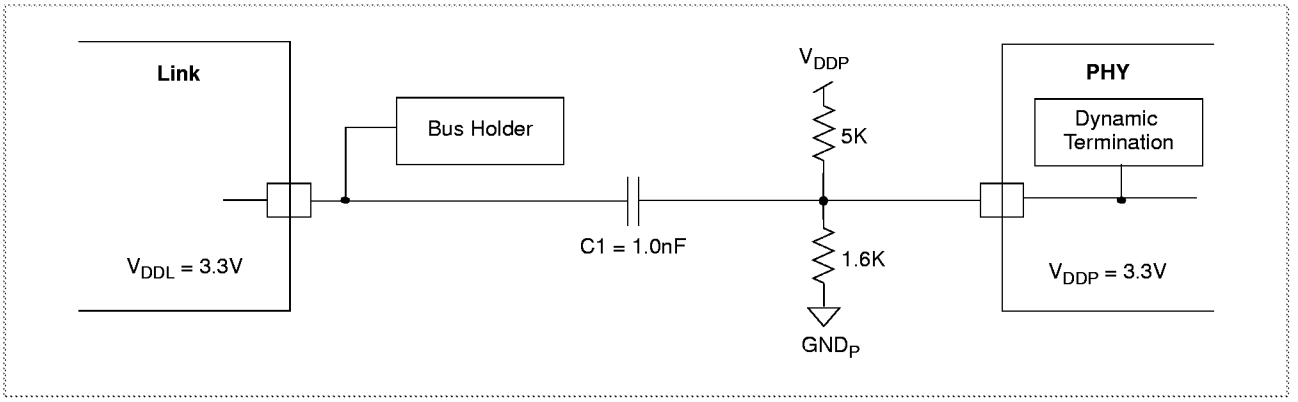
The PHY Dynamic Termination pins are automatically initialized at a DOWN level at power-on-reset. To assure proper data transmission, the Link must also be initialized at a DOWN level at power-on-reset.

Timing is not affected by the Dynamic Termination, so the timing values given in Link-PHY Interface Timing on page 15 are valid.

Dynamic Termination for DATA, CTL, SCLK, and LREQ Pins



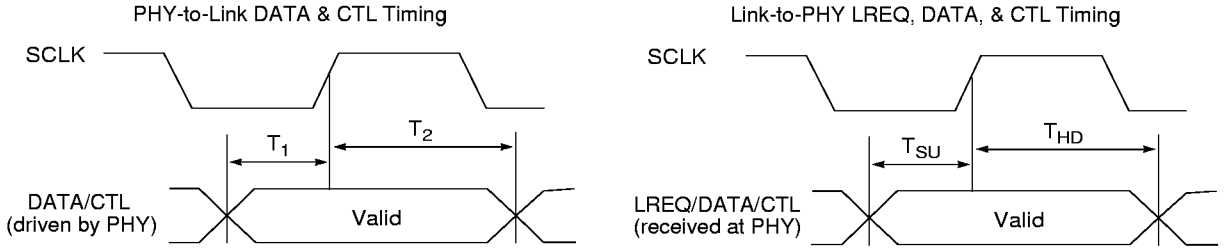
Dynamic Termination for LPS Pins



Link-PHY Interface Timing

The IBM PHY features selectable SCLK timing that can be tailored to the needs of the Link device. The SCLK timing is controlled by the SCLK_TSEL pin. When tied low, the SCLK has normal mode timing, and when tied high, the SCLK has early mode timing. In addition, the timing of data received from the Link can be adjusted using the RCV_TSEL pin.

Link-PHY Interface Timing Relationships



Normal Mode Timing (P1394a Compliant)

Symbol	Parameter	Min	Units
T_1	Time DATA/CTL valid before rising SCLK edge (PHY sending)	15.0	ns
T_2	Time DATA/CTL valid after rising SCLK edge (PHY sending)	0.5	ns
T_{SU}	Setup time LREQ, DATA, CTL before rising SCLK edge (PHY receiving)	5.5	ns
T_{HD}	Hold time LREQ, DATA, CTL after rising SCLK edge (PHY receiving)	-1.0	ns

Timing calculated with C_L = 10 pF
Module pin settings: SCLK_TSEL = 'GND', RCV_TSEL = 'GND'.

Early Mode SCLK Timing

Symbol	Parameter	Min	Units
T_1	Time DATA/CTL valid before rising SCLK edge (PHY sending)	6.5	ns
T_2	Time DATA/CTL valid after rising SCLK edge (PHY sending)	9.0	ns
T_{SU}	Setup time LREQ, DATA, CTL before rising SCLK edge (PHY receiving)	-1.0	ns
T_{HD}	Hold time LREQ, DATA, CTL after rising SCLK edge (PHY receiving)	8.0	ns

Timing calculated with C_L = 10 pF
Module pin settings: SCLK_TSEL = 'V_{DD}', RCV_TSEL = 'GND'.

RCV Delayed Timing

Symbol	Parameter	Min	Units
T_1	Time DATA/CTL valid before rising SCLK edge (PHY sending)	15.0	ns
T_2	Time DATA/CTL valid after rising SCLK edge (PHY sending)	0.5	ns
T_{SU}	Setup time LREQ, DATA, CTL before rising SCLK edge (PHY receiving)	9.5	ns
T_{HD}	Hold time LREQ, DATA, CTL after rising SCLK edge (PHY receiving)	-3.0	ns
Timing calculated with C_L = 10 pF Module pin settings: SCLK_TSEL = 'GND', RCV_TSEL = 'V_{DD}'.			

Early Mode RCV Delayed Timing

Symbol	Parameter	Min	Units
T_1	Time DATA/CTL valid before rising SCLK edge (PHY sending)	6.5	ns
T_2	Time DATA/CTL valid after rising SCLK edge (PHY sending)	9.0	ns
T_{SU}	Setup time LREQ, DATA, CTL before rising SCLK edge (PHY receiving)	3.5	ns
T_{HD}	Hold time LREQ, DATA, CTL after rising SCLK edge (PHY receiving)	6.5	ns
Timing calculated with C_L = 10 pF Module pin settings: SCLK_TSEL = 'V_{DD}', RCV_TSEL = 'V_{DD}'.			

Link-PHY Diagnostics

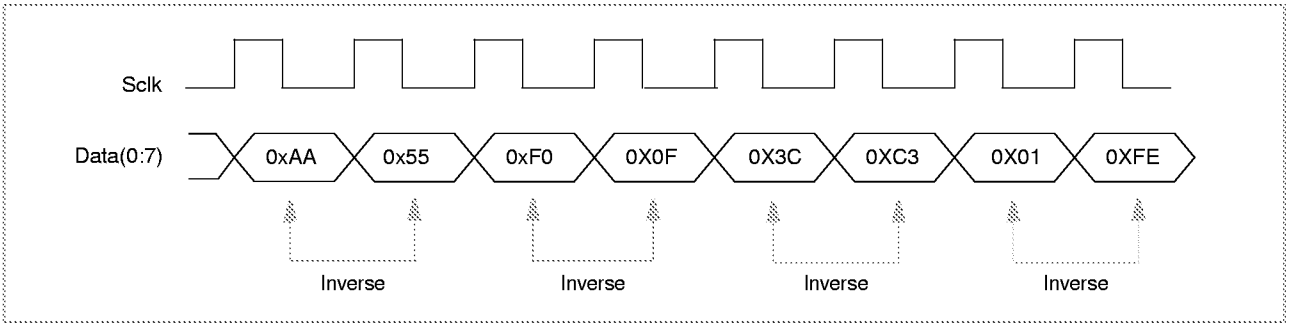
The IBM21S862, IBM21S861, and IBM21S860 offer the ability to test the Link-PHY interface using available Link-PHY protocol, a beneficial feature for hardware testing and field diagnostic software. When utilizing this feature outside a controlled environment, all ports should be disabled via PHY register page 0 for each port.

The Link-PHY interface can be tested in both directions: Link-to-PHY and PHY-to-Link. The following tests the interface from the Link to the PHY.

The Link-PHY interface self test is enabled by writing a logic '1' to bit 2 of address 0b1110 while pointing to PHY register page 7 (Vendor Specific Area).

At this point, the link issues either a fair, priority, or isochronous bus request via the LREQ to transmit a 400Mb/s packet. When the PHY grants the bus to the Link, the Link must respond by sending a packet of any length (IEEE-1394 packet length rules do not apply) to the PHY. The data must be in groups of two bytes in which the second byte is the logical inverse of the previous byte. For example, the 400Mb/s packet may be as follows:

400Mb/s Diagnostic Packet Example



The Link may use normal protocol (i.e. issue a "Hold" prior to Transmit). The data integrity is confirmed by the PHY inverse checking of the packet. The PHY indicates an inverse error by setting the Link-PHY Error Ever Happened bit (L/P Self-test EEH) contained within the vendor specific area of the PHY registers.

To confirm data transmission from the PHY to the Link, the Link needs to set the Send Phy/Link Diag Pkt bit in PHY register 0xF of Phy register page 7. The PHY responds by sending its self_ID packet to the Link as a 400Mb/s packet, at which time the Link and/or software may check that the last 32 bits are the inverse of the first 32 bits. The Phy/Link Diag Pkt bit is cleared after the transmission of the 400Mb/s self_ID packet.

Configuring Hardware Alternatives

Holding the PHY in Power-On-Reset

While in Power-On-Reset (POR), the PHY does not create TpBias and therefore will not be detected by PHYs designed to the IEEE 1394-1995 specification [1] (Legacy PHYs). In addition, the PHY will not disrupt a 1394a network. When it completes POR, the PHY creates TpBias on all its connected ports. The module pin PDISABLE enables the POR value of the ports such that the ports do not assert TpBias until enabled via the PHY registers. See the Disabled bit in PHY Register Page 0, Port Status Page Fields on page 23.

When the PHY is initially powered on, the PHY is held in reset via an RC circuit created with a 2.2µF capacitor as shown in External Component Connections on page 42.

Setting Module Pins to Configure PHY as a Repeater

Module Pin	Connection
Sclk, Ctl(0:1), Data(0:7)	Float
$\overline{\text{Direct}}$	GND
DTE	GND
CONSCLK	V_{DD}
LPS	GND
Link_on	Float (or 3.3 K ohm to GND to reduce EMI emissions).

PHY Hardware Simulation Mode

The IBM PHY offers the unique ability to operate in an environment that is at a very slow speed. This feature enables the IBM PHY to be connected directly to hardware emulators (i.e. emulating a Link), while supporting IEEE-1394 communication over the standard IEEE 1394 cable to other IBM PHYs running in the same mode. The PHY will initialize the bus and operate as it would normally, except much more slowly.

The procedure to slow down the PHY for simulation purposes is as follows.

1. The PHY must be wired to use a crystal oscillator as defined by this specification. The following changes must be made:
   - Module pin TEST_0 must be tied to V_{DD}.
   - The TpBias capacitor must be changed according to the following equation:

     $$C = \frac{0.0248\text{Amps} \times 48\text{cycles} \times \text{Toscin}}{0.05\text{V}}$$

     where Toscin = 1/(osc_in input frequency)
   - Osc_in is applied a frequency that should not exceed 50MHz.
2. All the PHYs on the “slow down” network must have their oscillators set within 100 PPM to function properly. You must comply with all 1394 rules (e.g. max. packet length at a given speed). For example, if you request the bus for a 400Mb/s, your packet length must not exceed 4K bytes even though you slowed down the frequency.

Frequency Translation for Hardware Simulation Mode

Signal Name	Signal Rate
Osc_in	400MHz
Osc_in/2	200MHz
Osc_in/4	100MHz
Osc_in/8	50MHz (sclk)

If you apply a 25MHz signal to osc_in, your sclk will be 3.13MHz (Osc_in/8) rather than the 50MHz if you were in normal mode. If you send the PHY a 400Mb/s link request, the PHY will transmit 400Mb/s speed signaling but the actual rate will be your osc_in (25Mb/s in this example).

Programming the PHY

Register Mapping

Registers 1000_2 to 1111_2 are an indexed register window whose contents change based upon the Page_Select and Port_Select fields in Register 7. Register Pages 0, 1, and 7 are defined and shown on pages 22, 24, and 25, respectively.

PHY Register Map

Address	0	1	2	3	4	5	6	7
0000_2	Physical_ID						R	CPS
0001_2	RHB	IBR	Gap_Count					
0010_2	Extended			Reserved	Total_ports			
0011_2	Max_speed			Reserved	Delay			
0100_2	Link Active	Contender	Jitter			Pwr_class		
0101_2	Resume_int	ISBR	Loop	Pwr_fail	Timeout	Port_Event	Enab_accel	Enab_multi
0110_2	Reserved							
0111_2	Page_select			Reserved	Port_Select			
1000_2	Register-0_{Page_Select}							
...	...							
1111_2	Register-7_{Page_Select}							

PHY Register Fields (Part 1 of 3)

Field	Size	Type	Description
Physical_ID	6	r	Node address determined during self-identification.
R	1	r	A one indicates that this node is the root.
CPS	1	r	Cable power status. A one indicates power in the cable.
RHB	1	rw	Root hold-off bit. A one instructs the PHY to attempt to become the root during the next tree identify process. Cleared on POR.
IBR	1	rw	Initiate bus reset. A one instructs the PHY to initiate a bus reset immediately (without arbitration). This bit causes assertion of the reset state for 166µs and is self-clearing. Cleared on POR.
Gap_count	6	rw	Arbitration timer setting. Used to optimize gap times of the Subaction Gap and Arbitration Reset Gap, and Arbitration Response Time threshold values, based on the size of the network. This field is initially reset to a value of 111111_2. See clauses 4.3.6 and 8.4.6.2 of the IEEE 1394-1995 Standard [1].
Extended	3	r	This field has a constant value of 111_2, which indicates the extended PHY register map.

PHY Register Fields (Part 2 of 3)

Field	Size	Type	Description
Total_ports	4	r	This returns the total number of ports on this PHY. This is a constant value but it changes depending on whether the PHY has 1, 2, or 3 ports. 0001_2 = IBM21S861, one port 0010_2 = IBM21S862, two ports 0011_2 = IBM21S860, three ports
Max_speed	3	r	Indicates the maximum speed of the PHY, a constant value of 010_2. 000_2 = 98.304 Mb/s 001_2 = 196.608 Mb/s 010_2 = 393.216 Mb/s 011_2 - 111_2 = reserved The IBM21S860, IBM21S861, and the IBM21S862 have this field set to 010 indicating the maximum speed of 393.216Mb/s.
Delay	4	r	Worst case repeater delay, expressed as 144 + ("delay" • 20) ns. This field has a constant value of 0000_2.
Link Active	1	rw	Cleared or set by software to control the value of the L bit transmitted in the node's self-ID packet. The transmitted L bit is the logical AND of this bit and LPS active. The Link_Active bit is one subsequent to a power reset.
Contender	1	rw	Contender. Cleared or set by software to control the value of the C bit transmitted in the self-ID packet. After a Power reset, this bit is initialized to the value currently at the CMC input. See section of 7.5.1 of [2].
Jitter	3	r	The difference between the fastest and slowest repeater data delay, expressed as (Jitter + 1) • 20 ns. This bit has a constant value of 000_2.
Pwr_class	3	rw	Power class. Controls the value of the Pwr field transmitted in the self-ID packet. After a Power reset, this field is initialized to the value present at the Power Status inputs (note that PS1 is highest order bit, and PS3 is the lowest order bit).
Resume_Int			Resume Interrupt enable. When set to one, the PHY sets the Port_event interrupt whenever resume operations commence for any port (regardless of the state of the individual port's Int_enable bit).
ISBR	1	rw	Initiate short (arbitrated) bus reset. A write of one to this bit requests the PHY to arbitrate and issue a short bus reset. This bit is self-clearing.
Loop	1	rw	Loop detect. The PHY sets this bit to one if it detects that the network has been configured in a loop. A write of one to this bit clears it to zero. The PHY also initiates a status transfer of PHY interrupt when the PHY sets this bit. Unless this bit is cleared, no future interrupts will be generated for this condition.
Pwr_fail	1	rw	Cable power failure detect. Set to one when the PS changes from one to zero. A write of one to this bit clears it to zero. The PHY also initiates a status transfer of PHY interrupt when the PHY sets this bit. Unless this bit is cleared, no future interrupts will be generated for this condition.
Timeout	1	rw	Arbitration state machine timeout. A write of one to this bit clears it to zero. The PHY sets this bit if it times out in any arbitration state other than Idle. The PHY also initiates a status transfer of PHY interrupt when the PHY sets this bit. Unless this bit is cleared, no future interrupts will be generated for this condition.
Port_Event	1	rw	Port Event detect. Set to one when Connect, Bias, Disabled, or Fault changes for a port whose Int_Enable is one. The PHY also sets this bit to one if resume operations commence for any port and Resume_int is one. A write of one to this bit clears it to zero.
Enab_accel	1	rw	Enable arbitration acceleration.
Enab_multi	1	rw	Enable multi-speed packet concatenation. When set to one, the Link signals the speed of all packets to the PHY.

PHY Register Fields (Part 3 of 3)

Field	Size	Type	Description
Page_select	3	rw	Selects which of eight possible PHY register pages are accessible through the window at PHY register addresses 1000_2 through 1111_2, inclusive.
Port_select	4	rw	If the page selected by Page_select presents per port information, this field selects which port's registers are accessible through the window at PHY register addresses 1000_2 through 1111_2, inclusive. 0000_2 = Port 1 0001_2 = Port 2 0010_2 = Port 3

PHY Register Page 0, Port Status Page

Address	0	1	2	3	4	5	6	7
1000_2	AStat		BStat		Child	Connected	Bias	Disabled
1001_2	Negotiated_speed			Int_enable	Fault	Reserved		
...	Reserved							
1111_2								

PHY Register Page 0, Port Status Page Fields

Field	Size	Type	Description
AStat	2	r	TPA (arbitration) line state for the port: 11 = Z 01 = 1 10 = 0 00 = invalid
BStat	2	r	TPB (arbitration) line state on the port: 11 = Z 01 = 1 10 = 0 00 = invalid
Child	1	r	If set to one, the port is a child port, otherwise it is the parent port. The meaning of this bit is undefined from the time a bus reset is detected until the PHY transitions to state T1: Child Handshake during the tree identify process.
Connected	1	r	If set to one, the port is connected, otherwise it is disconnected.
Bias	1	r	If equal to one, incoming TpBias bias voltage is being detected.
Disabled	1	rw	When set to one, the port is disabled. The value of this bit subsequent to a power reset is dependent on the “PDisable” input pin. The recommended method of disabling a port is via a remote command packet.
Negotiated_speed	3	r	Indicates the maximum speed negotiated between this PHY and its immediately connected port. 000 = 98.304 Mb/s 001 = 196.608 Mb/s 010 = 393.216 Mb/s 011 - 111 = reserved
Int_enable	1	rw	Enable port event interrupts. When set to one, the PHY shall set Port_event to one if any of Connected, Bias, Disabled, or Fault (for this port) change state.
Fault	1	rw	Set to one if an error is detected during a suspend or resume operation. A write of one to this bit clears it to zero.

PHY Register Page 1, Vendor Identification Page

Address	0	1	2	3	4	5	6	7
1000_2	Compliance_level							
1001_2								
1010_2	Vendor_ID							
1011_2								
1100_2								
1101_2	Product_ID							
1110_2								
1111_2								

PHY Register Page 1, Vendor Identification Page

Field	Size	Type	Description
Compliance_level	8	r	Standard to which this PHY is implemented. This field has a constant value of 0000001_2, meaning it is 1394a compliant.
Vendor_ID	24	r	This is the Organizationally Unique Identifier (OUI) of the PHY. This IBM PHY will have a constant value of $10005A_{16}$. Register 1010_2 contains the most significant byte, and register 1100_2 contains the least significant byte.
Product_ID	24	r	The Product ID Register 1101_2 contains the most significant byte, and register 1111_2 contains the least significant byte: 400Mb / 3-Port PHY: 21860_{16} 400Mb / 2-Port PHY: 21862_{16} 400Mb / 1-Port PHY: 21861_{16} The last 4 bits of the Product_ID are the revision code.

PHY Register Page 7, Vendor Specific Area

Address	0	1	2	3	4	5	6	7
1000_2	Reserved[1]							
...								
1100_2	Arb_Phase		Arb_State			L/P Self-test EEH	Initiated Last Bus Reset	0
1101_2	0	CMC pin	0	0	0	Pwr pins		
1110_2	Disable Timeouts	Ignore rx_suspend	Enable L/P Self-test	Reserved[1]	Disable short resets	Reserved[1]		Packet Separation Control
1111_2	Soft POR	Send P/L Diag packet	Reserved[1]					

1. Never set these bits by writing "1" to them.

PHY Register Page 7, Vendor Specific Area Fields (Part 1 of 2)

Field	Size	Type	Description
ARB Phase	2	r	Indicates the current Arbitration State Machine phase: 00 = Bus Reset 01 =Tree ID 11 = Self ID 10 = Normal Arbitration.
Arb State	3	r	Indicates the current Arbitration State Machine state (binary encoding of state).
LP_Selftst EEH	1	r	Link-PHY interface self test "Error Ever Happened" status indication. This bit is set to 1 when an error has occurred while testing the Link-PHY interface.
Initiated Last Bus Reset	1	r	Initiated reset indication. If set, this node initiated the last bus reset, meaning it started sending the bus_reset signal on the serial bus before it received one.
CMC pin	1	r	Reflects the current value of the CMC input.
Pwr pins	3	r	Reflects the current value of the Power class inputs.
Disable Timeouts	1	rw	Disables the Arb_State_Timeout, which normally occurs if the PHY remains in one state for longer than 333ms. This bit is for lab debug purposes only. Setting this bit will result in behavior that does not comply with P1394a.
Ignore Rx_Suspend	1	rw	When set to 1, the PHY will ignore incoming Rx_Suspend or Rx_Disable_Notify indications on the serial bus. This bit is for lab debug purposes only. Setting this bit will result in behavior that does not comply with P1394a.
Enable L-P Self Test	1	rw	Enables the Link/PHY Interface self test (EEH) function.
Disable Short Arb Reset	1	rw	Disables the arbitrated short reset function. When disabled, all bus resets revert back to the longer (167ms) bus reset.

PHY Register Page 7, Vendor Specific Area Fields (Part 2 of 2)

Field	Size	Type	Description
Packet Separation Control	1	rw	Some 100Mb/s legacy hardware is not compatible with the minimum packet separation allowed by the standard. To ensure compatibility with this legacy hardware, the IBM PHY generates 100Mb/s packets that comply with the standard and are compatible with this hardware. This bit is normally set to 0. If the Link already controls the packet separation, or if there are no legacy devices in the network that require longer packet separation, then writing a 1 to this bit disables this feature.
POR	1	w	Software control of Power On Reset function that is normally initiated through the $\overline{\text{RESET}}$ module pin.
Send PL Diag Pkt	1	w	Send a PHY-Link interface diagnostic packet (SID Pkt, without inverse bits) to the Link at 400Mb/s. This will enable the checking of PHY-Link data lines and timing. This feature is a diagnostic aid only and should not be used when the Link could receive information from the serial bus. One should disable the port when using this feature to prevent reception of unwanted packets. The packet consists of the first half of the Self-ID packet. The inverse bits are not sent.

Multi-Speed Concatenation

The IEEE1394-1995 standard [1] requires that all concatenated packets be transmitted at the same speed. If a node is required to transmit packets at various speeds, as in the case of isochronous data directed to different portions of the bus, the PHY must arbitrate for each change in speed. Multi-speed concatenation enables the node to concatenate packets at different speeds and therefore recover the lost bandwidth due to arbitration.

The PHY device concatenated packet reception follows the mechanism of Annex J of the 1394-1995 Standard [1], in which the packet speed code is expected at the beginning of each packet. Receive speed codes are shown in the Send and Receive Speed Codes table below. For transmission at multiple speeds, the Link needs a way to signal to the PHY what speed the next packet in the concatenated chain will be. This is accomplished in the P1394a specification [2] by letting the Link drive the speed code for the next packet onto the data bus at the same time that it drives the bus_hold code onto the control bus. See the following concatenation timing diagrams, as well as Block Diagram: Three-Port PHY on page 3, Direct Connection Diagram on page 13, and Capacitive Isolation with Differentiated Signals on page 14. The same speed codes that are used for receiving are to be used for sending. Note that in order to maintain compatibility with existing hardware, the speed is not allowed to be downgraded to S100 from a higher speed.

The IBM PHY has a control bit called Enab_Multi in the PHY register that enables it to interpret the speed codes as they are sent in each packet. When the control bit is set to 1, the PHY conforms to P1394a multi-speed concatenation rules. For compatibility with earlier vintage hardware, the control bit may be set to 0, causing the PHY to conform to 1394-1995 concatenation in which all packets are transmitted at the same speed as the first packet.

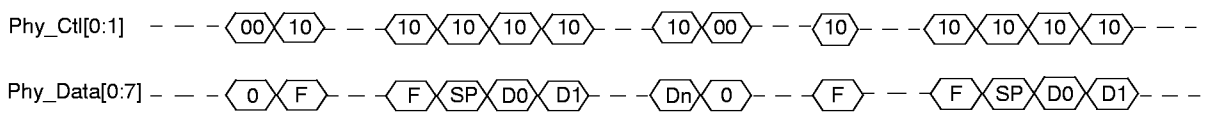
Even if this feature is disabled, the PHY always remains compatible with multi-speed concatenation on the serial bus. The concatenation is transparent to the Link. This enables the node to remain compatible with other nodes that will transmit multiple speed concatenated packets.

Send and Receive Speed Codes

D[0:7]	Data Rate
00xxxxxx[1]	S100
0100xxxx	S200
01010000	S400

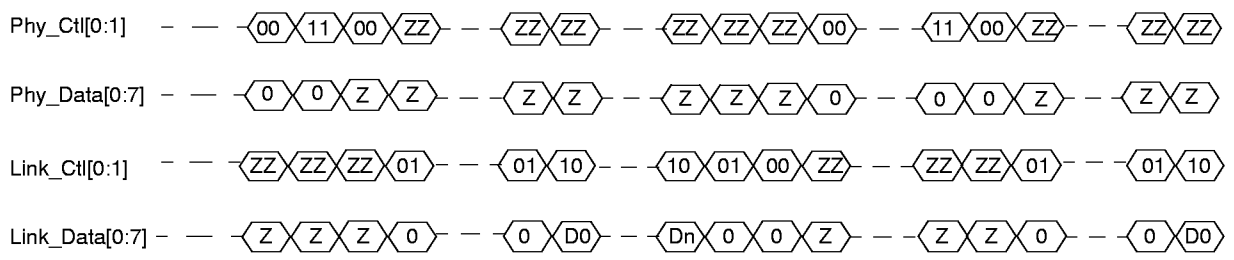
1. The “x” means transmitted as 0, ignored on receive.

Concatenated Packet Reception



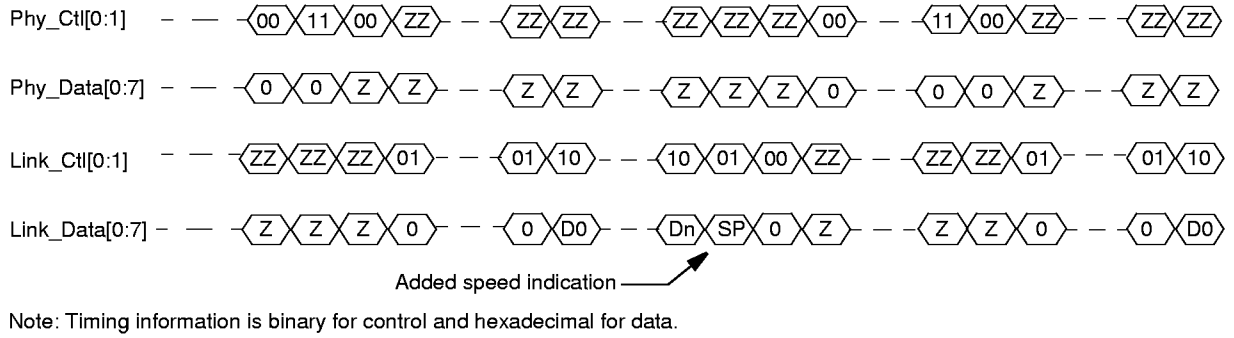
Note: Timing information is binary for control and hexadecimal for data.

1394-1995 Concatenated Packet Transmission



Note: Timing information is binary for control and hexadecimal for data.

P1394a Multi-Speed Packet Transmission



Note: Timing information is binary for control and hexadecimal for data.

Operating the Link-PHY Interface

Control Lines

The control lines between the Link and PHY are bidirectional and are encoded as described in the following two tables.

Ctl(0:1) When the PHY is Driving

Ctl(0:1)	Name	Description
00	Idle	No Activity.
01	Status	Status information is being sent to the Link.
10	Receive	Data is being transferred to the Link.
11	Grant	The PHY grants the Link the bus to transmit.

Ctl(0:1) When the Link is Driving

Ctl(0:1)	Name	Description
00	Idle	Transmit is complete, the Link releases the bus.
01	Hold	The Link is holding the bus or indicating that it wishes to concatenate a packet.
10	Transmit	Data is being transferred to the Link.
11	Unused	

Link Request

The link uses a serial data stream over the link request connection to request access to the serial bus, issue a register read or write, or control accelerations.

Bus Request

If the Link request transfer is a bus request, it is seven bits long and is of the format shown in the table below. The IBM PHY is also compatible with the Bus Request format as defined in the IEEE 1394-1995 standard [1]. This standard defined a bus request format to be only six bits in length by using a two-bit speed code.

Bus Request Format

Bit(s)	Name	Description
0	Start Bit	Always 1.
1-3	Request Type	Indicates the type of bus request: 000: Immediate request. 001: Isochronous request. 010: Priority request. 011: Fair request.
4-6	Request Speed	Requested speed for the transmission. 000: 100Mb/s. 010: 200Mb/s. 100: 400Mb/s.
7	Stop Bit	Stop Bit. Must be 0 for a valid request.

Read Request Format

Bit(s)	Name	Description
0	Start Bit	Always 1.
1-3	Request Type	100: Indicates that is a PHY register read request.
4-7	Address	The address of the request PHY register.
8	Stop Bit	Always 0 for a valid request.

Write Request Format

Bit(s)	Name	Description
0	Start Bit	Always 1.
1-3	Request Type	101: Indicates that is a PHY register write request.
4-7	Address	The address of the register to be written.
8-15	Data	Data to be written to the addressed register.
16	Stop Bit	Always 0 for a valid request.

Acceleration Control Request Format

Bit(s)	Name	Description
0	Start Bit	Always 1.
1-3	Request Type	Indicates that is a PHY register acceleration control request. 000: ImmReq Take control of the bus immediately upon detecting the file; do not arbitrate. Used for acknowledge packets. 001: IsoReq Arbitrate for the bus after an isochronous gap. Used for isochronous stream packet. 010: PriReq Ignore the PHY's fairness protocol and, unless accelerating, arbitrate after a subaction gap. Use for cycle master or other packets for which the link need not wait for a fairness interval. 011: Fair Req Arbitrate within the current fairness interval if permitted by the PHY's fairness interval. Otherwise, arbitrate after an arbitration gap. 100: RdReg Return specified register contents through status transfer. 101: WrReg Write to specified register. 110: AccCtrl Disable or enable PHY arbitration accelerations. 111: Reserved for future standardization.
4	Accelerate	When 0, instructs the PHY to disable arbitration accelerations. A value of 1 requests the PHY to enable arbitration accelerations.
5	Stop Bit	Always 0 for a valid request.

Status Transfer

The PHY places status on the control lines (ctl=01b) while it transfers the status information on data(0:1). The PHY may initiate a status transfer any time that the interface is idle and the PHY has status information to be transferred to the Link. A status transfer can vary between four and 15 bits and is of the format shown in the table below.

Status Format

Bit(s)	Name	Description
0	Arbitration Reset Gap	The PHY has detected an arbitration reset gap.
1	Subaction Gap	The PHY has detected a subaction gap.
2	Bus Reset	The PHY has entered the bus reset state.
3	PHY_interrupt	This indicates one or more of the following interrupt conditions: - Loop detect interrupt - Cable power fail interrupt - Arbitration state machine time-out - Port_event interrupt
4-7	Address	This contains the address of the register data when register data is being transferred.
8-15	Data	The register data from the address in bits 4-7.

Cable PHY Packets

Four categories of cable PHY packets are defined in the P1394a supplement to the IEEE standard [2].

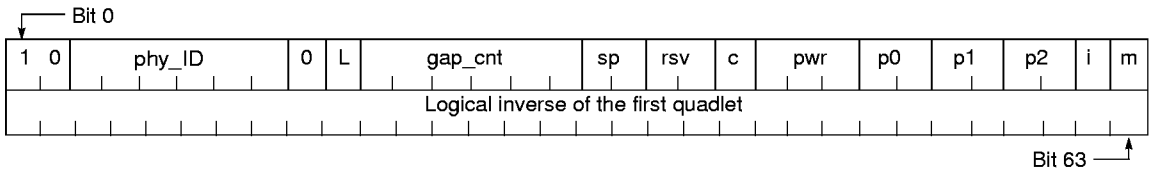
- Self_ID packet (defined in section 7.5.1 of [2])
- Link-on packet (defined in section 7.5.2 of [2])
- PHY configuration packet (defined in section 7.5.3 of [2])
- Extended PHY packets (defined in section 7.5.4 of [2])
    - Ping
    - Remote Access
    - Remote Reply
    - Remote Command
    - Remote Confirmation
    - Resume

All PHY packets are 64 bits long, in which the second 32 bits are the logical inverse of the first 32 bits.

Self Identification

Included below are tables which describe the format of the cable PHY packets.

Self_ID Packet Format



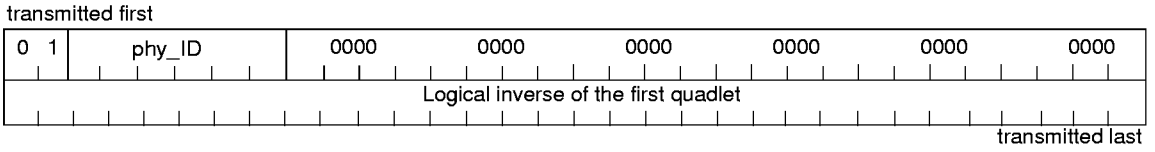
Self-ID Packet Information

Bit(s)	Name	Description
0-1	packet identifier	Always 01
2-7	phy_ID	Physical address of the packet originator
8		Always 0
9	L	Indicates an active link. 1 = active Link
10-15	gap_cnt	Value of the gap setting of the originator of this packet
16-17	sp	Maximum Speed capabilities for this PHY 00 = 98.304Mb/s 01 = 196.608Mb/s 10 = 393.216Mb/s The IBM21S860 or IBM21S861 transmits 10, indicating that it is capable of speeds up to 393.216Mb/s
18-19	rsv	Reserved. Set to “0”.
20	c	Indicates that the link is a contender to be the bus or isochronous resource manager.
21-23	pwr	Indicates the power class for the identified node. Module pin PS_1, 2, & 3 are reflected in the self_ID bits 21, 22, & 23, respectively. In the table below (from left to right) the first position = PS-1, the second position = PS-2 and the third position = PS-3. 000 = Node does not need power and does not repeat power. 001 = Node is self-powered and provides a minimum of 15W to the bus. 010 = Node is self-powered and provides a minimum of 30W to the bus. 011 = Node is self -powered and provides a minimum of 45W to the bus. 100 = Node may be powered from the bus and is using up to 1W. 101 = Reserved for future standardization. 110 = Node is powered from the bus and is using up to 1W. An additional 3 W is needed to enable he link and higher layers. 111 = Node is powered from the bus and is using up to 1W. An additional 7 W is needed to enable the link and higher layers. Note: This table is from the P1394a supplement of the IEEE 1394-1995 [2].
24-25 26-27 28-29	p0 p1 p2	Indicates the state of the ports on the PHY (p0 = port 0). 11 = Active and connected to child node 10 = Active and connected to parent node 01 = Not active (may be disabled, disconnected, or suspended) 00 = Not present on this PHY The IBM21S861 returns 00 for ports 2 & 3.
30	i	1 = this node initiated the current bus reset. More than one node may have this bit set at the same time.
31	m	0 = No additional self-id packets from this PHY will follow.
32-63	logical inverse	The logical inverse of the first 32 bits.

Link-On

The reception of a valid Link-On packet with a matching phy_ID, causes a PH_EVENT.indication of Link_On. The PH_EVENT.indication of Link_On causes the PHY to generate a 6MHz signal on the Link_On pin to the Link. This signal wil toggle until the LPS signal from the Link and the PHY register bit "Link_Active" are both active.

Link-On Packet Format



Link-On Packet Information

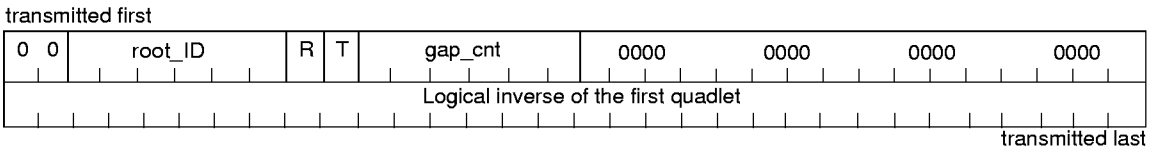
Bit(s)	Name	Description
0-1	Packet Identifier	Always 01.
2-7	phy_ID	Physical address of the packet recipient.
8-31		Always 0.
32-63	logical inverse	Logical inverse of the first 32 bits.

PHY Configuration

The PHY configuration packet configures the Serial Bus to

- Set the gap_count for all nodes to the smallest valid value, and
- Set a particular node to be the root after the next bus initialization.

PHY Configuration Packet Format



PHY Configuration Packet Information

Bit(s)	Name	Description
0-1	Packet Identifier	Always 01.
2-7	root_ID	Physical address of the node to have its force_root bit set if the force_root bit within this packet is set (bit 8).
8	force_root	1 sets the force_root bit of the node addressed in root_ID and clears all other nodes' force_root bits. 0 ignores the phy_ID field.
9	gap_count_reset_disable	1 sets the gap_count variable of all nodes to the gap count set in this packet.
10-15	gap_count	The new value for all nodes' gap_count variable. This value goes into effect immediately upon receipt and is valid through the next bus reset. A second bus reset without an intervening PHY configuration packet resets gap_count to 3F (hex).
16-31		Always 0.
32-63	logical inverse	Logical inverse of the first 32 bits.

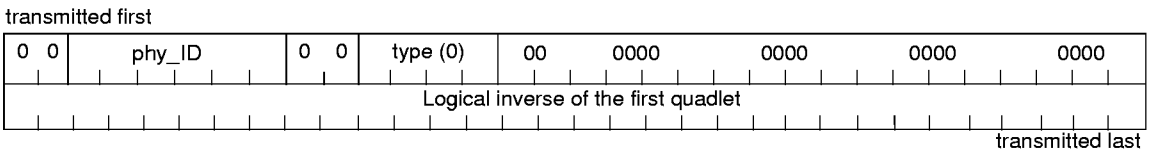
Extended PHY Packets

P1394a [2] defined Extended PHY Packets to enable features such as PHY Ping and Remote Access to PHY registers. The packet identifier (bits 0-1) for the extended packets as well as bits 8-9 are always zero. The Extended PHY packets are derived from a PHY configuration packet in which the bits R=0 and T=0 to identify them as extended PHY packets.

Extended PHY: Ping Packet

The PHY will transmit its self_ID packet to both its Link and over the 1394 serial bus if it receives a valid Ping packet with a matching phy_ID. The self_ID packet will reflect the current state of the PHY at the time of transmission. The self_ID packet is generated by the PHY in response to a Ping packet.

Ping Packet Format



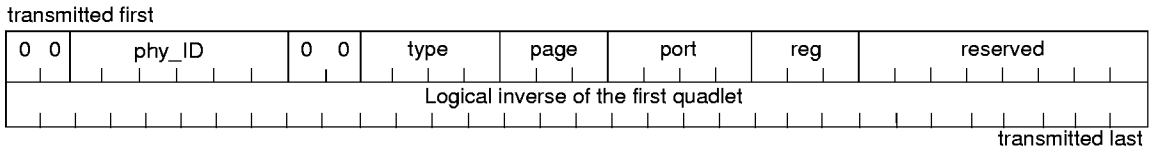
Ping Packet Information

Bit(s)	Name	Description
0-1	packet identifier	Always 00.
2-7	phy_ID	Physical address of the node to be pinged.
8-9		Always 00.
10-13	type	The type of this extended PHY packet (hex). 0 = ping packet
14-31		Always 0.
32-63	logical inverse	Logical inverse of the first 32 bits.

Extended PHY: Remote Access

A Remote Access packet is used to request a remote PHY to return the contents of a specified PHY register. The PHY returns the requested register information using a Remote Reply packet (see Extended PHY: Remote Reply on page 37).

Remote Access Format



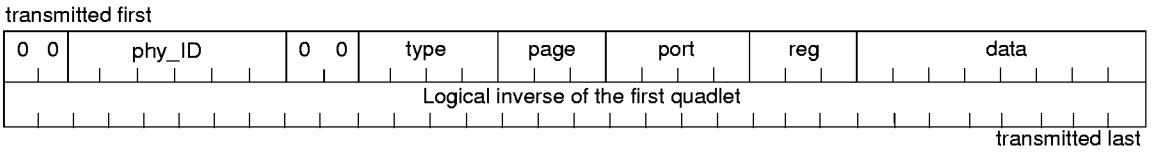
Remote Access Packet Information

Bit(s)	Name	Description
0-1	packet identifier	Always 00.
2-7	phy_ID	Physical address of the node to be read.
8-9		Always 00.
10-13	type	The type of this extended PHY packet (hex). 1 = read a base register 5 = read a paged register
14-16	page	Determines which page of the selected register will be read. Corresponds to that register's page_select field.
17-20	port	Determines which port of the selected register will be read. Corresponds to that register's port_select field.
21-23	reg	This field, in combination with page and port, specifies the PHY register to be read. If the type field indicates a read of the base PHY registers, the reg field directly addresses one of the first eight PHY registers. Otherwise the PHY register address is 100+reg.
24-31	res	Reserved.
32-63	logical inverse	Logical inverse of the first 32 bits.

Extended PHY: Remote Reply

A PHY uses a Remote Reply packet to return the information requested from a Remote Access packet (see Extended PHY: Remote Access on page 36). The PHY generates this packet and transmits the packet to its attached Link while transmitting to remote PHYs via the 1394 serial bus.

Remote Reply Packet Format



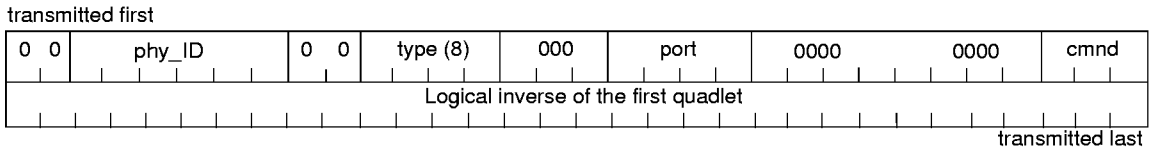
Remote Reply Packet Information

Bit(s)	Name	Description
0-1	packet identifier	Always 00.
2-7	phy_ID	Physical address of the node that is replying to the most recent remote access packet.
8-9		Always 00.
10-13	type	The type of this extended PHY packet (in hexadecimal). 3 = reply with the contents of a base register 7 = reply with the contents of a paged register
14-16	page	Indicates which page of the replying register is being returned. Corresponds to the replying register's page_select field.
17-20	port	Indicates which port of the replying register is being returned. Corresponds to the replying register's port_select field.
21-23	reg	This field, in combination with page and port, identifies the PHY register that is returning the status contained in the data field of this packet. If the type field indicates the base PHY registers, the reg field directly addresses one of the first eight PHY registers. Otherwise the PHY register address is 100+reg.
24-31	data	The status of the PHY register replying to the most recent remote access packet. 0 = reserved.
32-63	logical inverse	Logical inverse of the first 32 bits.

Extended PHY: Remote Command

A Remote Command packet is used to cause a remote PHY to take specific actions. The Remote Command packet is used primarily for power management. The PHY will respond with a Remote Confirmation packet (see Extended PHY: Remote Confirmation on page 39). The PHY does not generate a Remote Command packet.

Remote Command Packet Format



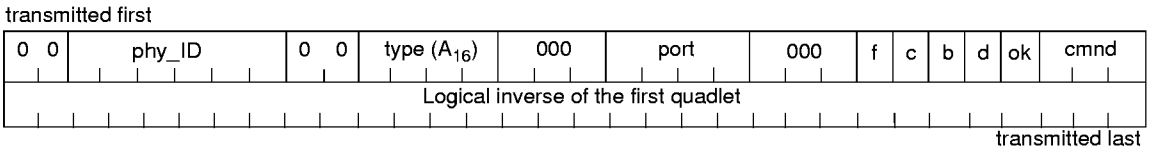
Remote Command Packet Information

Bit(s)	Name	Description
0-1	packet identifier	Always 00.
2-7	phy_ID	Physical address of the node that will receive this command.
8-9		Always 00.
10-13	type	The type of this extended PHY packet (hex). 8 = remote command packet
14-16		Always 00.
17-20	port	The PHY port that is the target of the command.
21-28		Always 0.
29-31	cmnd	The command to be carried out by the addressed node on the specified PHY port. 0 = NOP 1 = transmit TX_DISABLE_NOTIFY, then disable port 2 = initiate suspend 4 = clear the port's fault bit to 0. 5 = enable port 6 = resume port
32-63	logical inverse	Logical inverse of the first 32 bits.

Extended PHY: Remote Confirmation

The PHY will respond with a Remote Confirmation packet if it receives a valid Remote Command packet addressed to it. The Remote Confirmation packet enables the originator of the Remote Command packet to confirm the requested actions taken by the PHY. This packet is generated by the PHY and is sent to both its Link and remote PHYs over the 1394 serial bus.

Remote Confirmation Packet Format



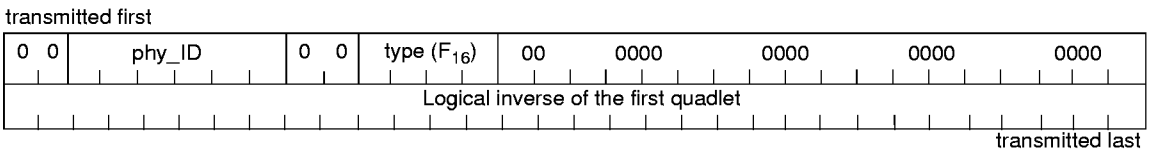
Remote Confirmation Packet Information

Bit(s)	Name	Description
0-1	packet identifier	Always 00.
2-7	phy_ID	Physical address of the node that is sending this packet in response to the most recent remote command packet.
8-9		Always 00.
10-13	type	The type of this extended PHY packet (hex). A = remote confirmation packet
14-16		Always 0.
17-20	port	The PHY port that will be targeted by the command.
21-23		Always 0.
24	fault	The current value of the Fault bit from PHY register 1001 for the addressed port.
25	connected	The current value of the Connected bit from PHY register 1000 for the addressed port.
26	bias	The current value of the Bias bit from PHY register 1000 for the addressed port.
27	disabled	The current value of the Disabled bit from PHY register 1000 for the addressed port.
28	ok	1 = the command was accepted by the PHY
29-31	cmnd	The command specified in the most recent remote command packet and carried out by this node. 0 = NOP 1 = transmit TX_DISABLE_NOTIFY, then disable port 2 = initiate suspend 4 = clear the port's fault bit to 0. 5 = enable port 6 = resume port
32-63	logical inverse	Logical inverse of the first 32 bits.

Extended PHY: Resume

The Resume packet will cause all PHYs to resume all connected and suspended ports. The packet is not generated by the PHY and there is no reply.

Resume Packet Format



Resume Packet Information

Bit(s)	Name	Description
0-1	packet identifier	Always 00.
2-7	phy_ID	Physical address of the node sending this packet.
8-9		Always 00.
10-13	type	The type of this extended PHY packet (hex). F = resume packet
14-31		Always 0.
32-63	logical inverse	Logical Inverse of the first 32 bits.

Cable Interface

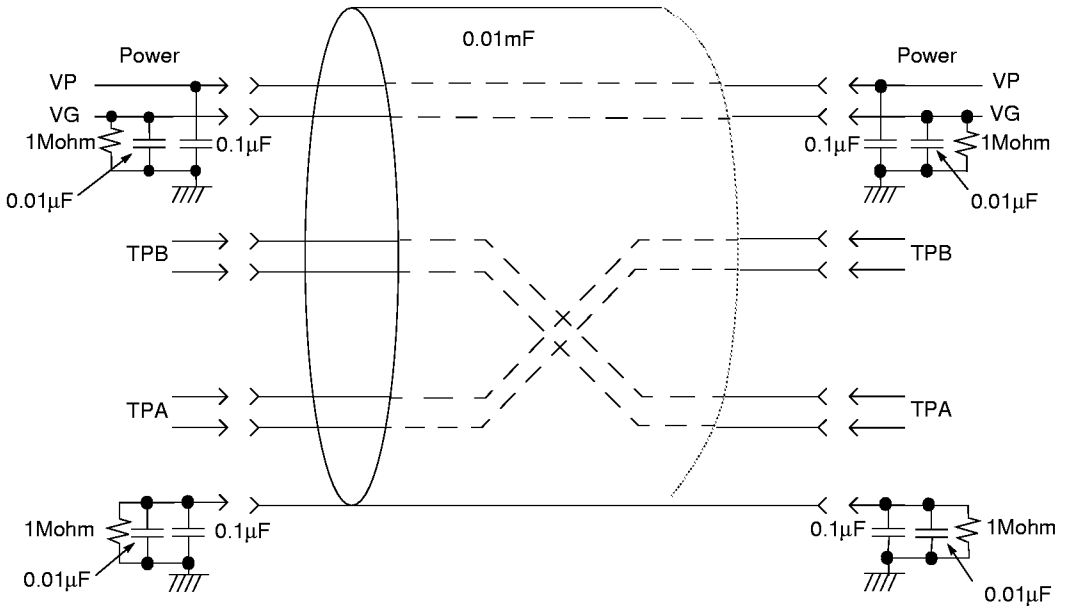
Twisted Pair

The twisted pair cable interface is the interface between the PHY and the serial cable. For the twisted pair A cables, TPA and $\overline{TPA}$, 55 ohm resistors are connected to Tp_Bias, with a .33µF capacitor from Tp_Bias to VG at each port. For the twisted pair B cables, TPB and $\overline{TPB}$, 55 ohm resistors are connected to a node having a 5 Kohm resistor and a 250pF capacitor connected in parallel to VG. It is also important to note that the diagram below represents only one of the PHY's three cable ports. The external component connections indicated must be repeated for each port. Please read Board Layout Recommendations on page 44 for additional guidelines.

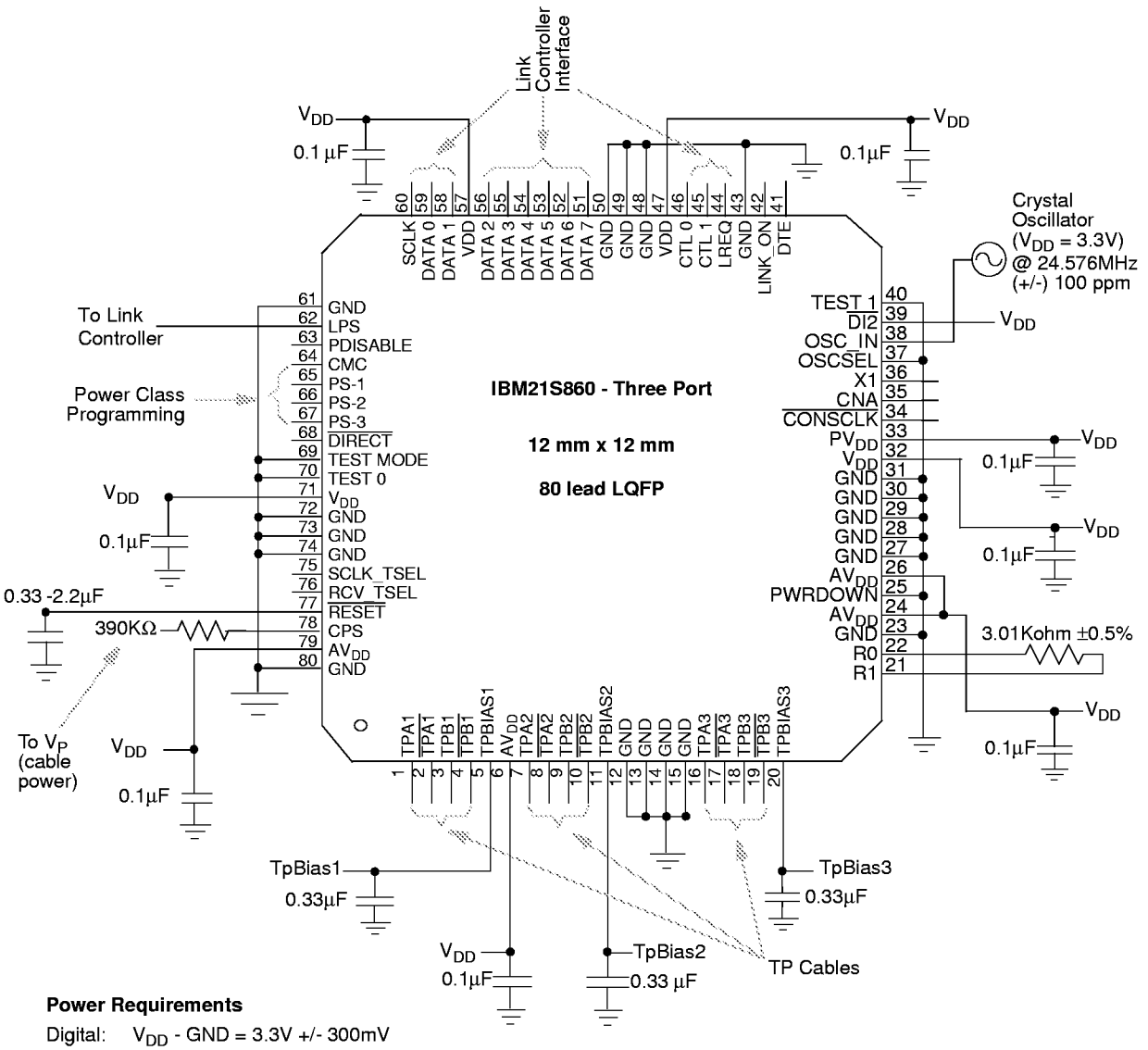
Cable Media

The cable media interface is the implementation of a physical connection. The cable media has two well shielded signal pairs with 110 ohm differential and one low impedance signal pair for the power. The diagram below shows all external component connections to the cable media. The cable shielding may be connected directly to ground in some applications.

Cable Media Interface



External Component Connections



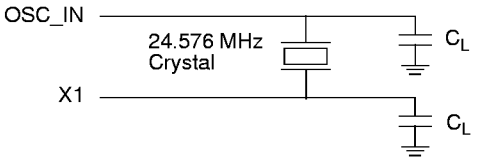
Power Requirements

Digital: V_{DD} - GND = 3.3V +/- 300mV

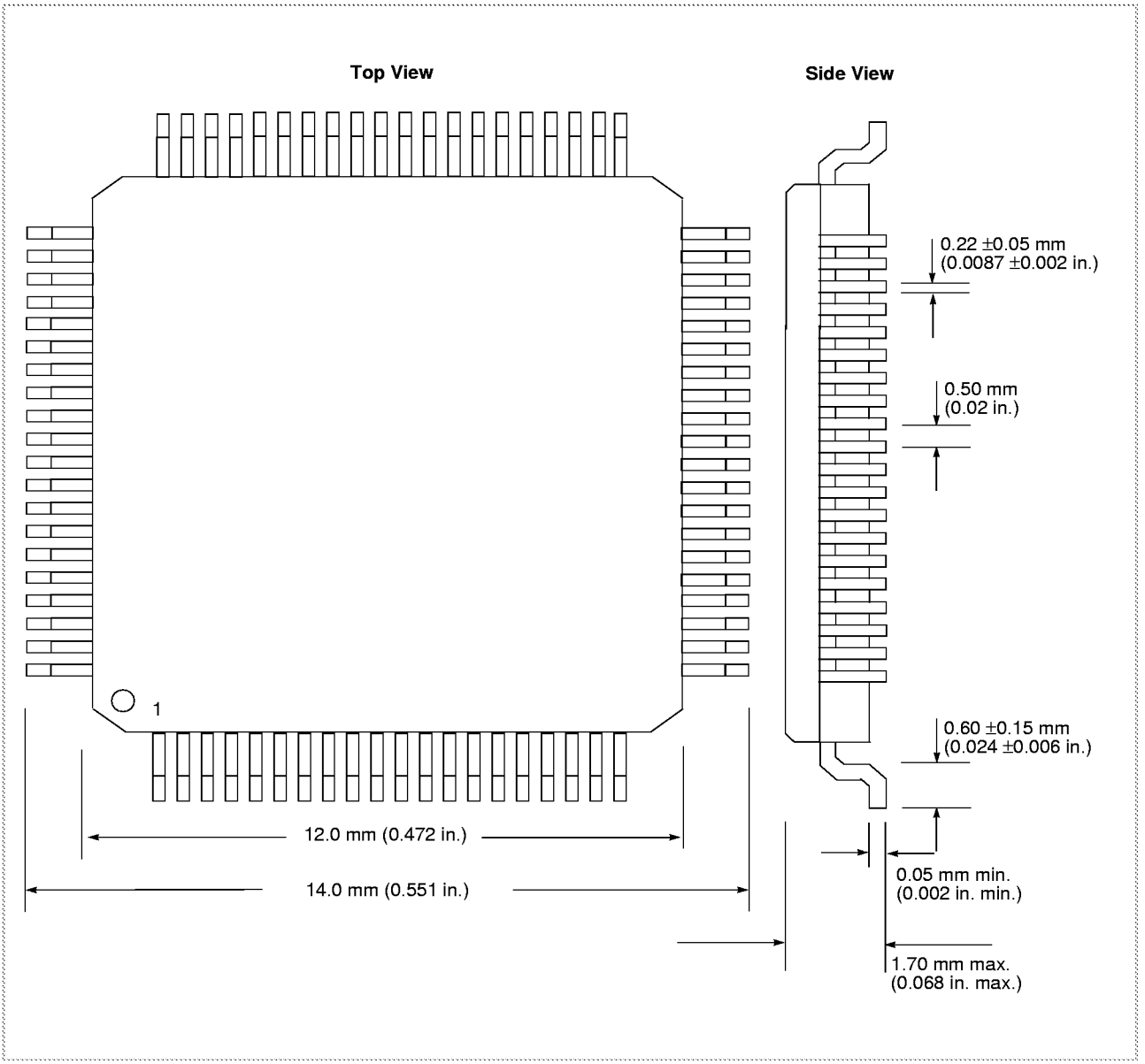
Analog: AV_{DD} - GND = 3.3V +/- 300mV
PV_{DD} - GND = 3.3V +/- 300mV (PLL supply may require filtering from the analog supply)

Option to use External Crystal:

Module pin 37 (OSCSEL) set to V_{DD}.



Package Diagram: 80-Lead LQFP



Board Layout Recommendations

- Route the traces for the differential pairs TPA/$\overline{\text{TPA}}$ and TPB/$\overline{\text{TPB}}$ very carefully. The signals within each pair should be routed quite closely, yet the two must maintain a differential impedance of 110 ohms. These guidelines help to achieve both of these goals.
  - Each trace should have a 55 ohm impedance.
  - Route the differential pair traces as closely as possible while maintaining a spacing between them of approximately four times the height of the traces from the ground plane. So, if the dielectric thickness between the signal traces and the ground plane is 10 mils, then maintain the spacing between the traces at approximately 40 mils.
  - The ground plane should be the layer directly under the signal layer on which the differential traces are run. Furthermore, in order to provide a good signal return path and avoid signal impedance discontinuities, the ground plane should be continuous in the area under the signal traces. In addition, route the majority of a given differential signal trace on the single signal layer above the ground plane to minimize the via count in the route. If the signal traces do change planes, ensure that there is no discontinuity in the ground return path by coupling the new power plane over which the signal trace is routed with the ground plane in close vicinity to the signal via. If the same ground plane is used, then place some vias connecting the two ground planes in close proximity (100 mils) to the signal via.
  - Differential pair traces must be the same length electrically so as not to introduce any skew between the differential signals. This is achieved by routing the two traces in each differential pair along the same path (adhering to the above spacings) and maintaining the same via count for each trace. The two traces within a pair should have matched lengths within approximately 50 mils of one anther. Furthermore, the lengths of the four traces within the two sets of differential pairs (TPA & TPB) in a given port should be kept within 100mils of one another. Each port, however, can be wired independently within these guidelines since there aren't any restrictions on trace variations from port to port.
- Transceiver signal routes should be routed from the 1394 connector to the PHY module pin and 55ohm terminator minimizing the stub length between the PHY module pins and terminator pins. Thus, the 55ohm terminators should be as close to the PHY as possible.
- Keep the TpBias traces from the PHY I/O to the filter capacitors short and wide to minimize delta I noise.
- Minimize interconnect signal trace length differences between the PHY and Link modules.
- In general, keep routes between the PHY and Link short and direct. Traces longer than 1.5 inches should be considered as transmissions lines and analyzed accordingly.

  Critical line length = $\frac{Vp \times tr}{2.5}$

  where tr = signal rise time in nsec
  and Vp = propagation velocity in unit length per nsec
- Place the 3.01Kohm external current setting resistor that is connected to PHY pins 21 & 22 as close to the pins as possible.
- As a general rule, each power pin on the PHY and Link modules should be capacitively decoupled with alternating 0.1 and 0.01µF ceramic capacitors to help reduce EMI emissions.
- As a general rule, each module power and ground pin should be connected directly to its appropriate power plane (i.e. do not float any of the power pins or run wires to connect to the power plane).
- The PHY should have its own ground plane which connects to Vg of the 1394 connector.
- When adding a via to TPA or TPB traces, ensure a 50 mil annular clearance (spacing from via barrel to solid GND/Power plane space).

References

1. IEEE Std 1394-1995, IEEE Standard for a High Performance Serial Bus.
2. IEEE P1394a, Draft Standard for High Performance Serial Bus (Supplement), Draft Revision 2.0.

Revision Log

Revision	Contents of Modification
8/7/98	Limited pre-publication release.
8/31/98	Second limited pre-publication release.
11/24/98	Initial release (00).

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