EMIF02-MIC02F1

2 LINES EMI FILTER AND ESD PROTECTION

IPAD.™

MAIN PRODUCT CHARACTERISTICS:

Where EMI filtering in ESD sensitive equipment is required :

- Mobile phones and communication systems
- Computers, printers and MCU Boards

DESCRIPTION

The EMIF02-MIC02 is a highly integrated devices designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF02 flip chip packaging means the package size is equal to the die size.

This filter includes an ESD protection circuitry which prevents the device from destruction when subjected to ESD surges up 15kV.
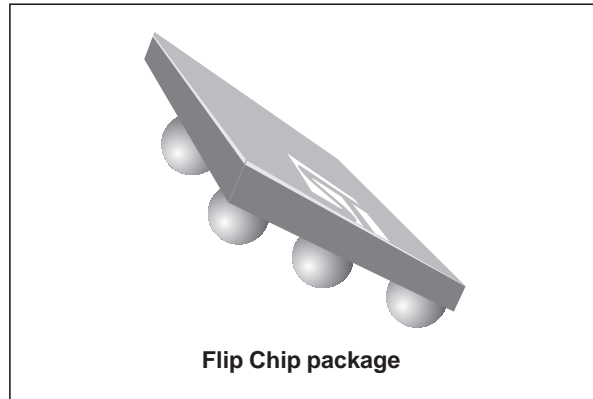
BENEFITS

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Very low PCB space consuming: 1.07mm x 1.57mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging.
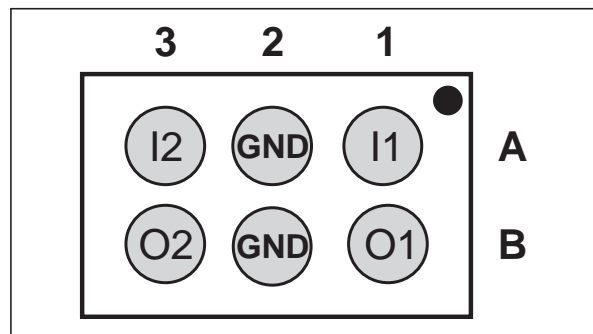
COMPLIES WITH THE FOLLOWING STANDARDS:
IEC61000-4-2

Level 4	on input pins	15kV	(air discharge)
		8 kV	(contact discharge)
Level 1	on output pins	2kV	(air discharge)
		2kV	(contact discharge)

MIL STD 883E - Method 3015-6 Class 3

Flip Chip package

PIN CONFIGURATION

BASIC CELL CONFIGURATION

Ri/o = 470Ω
Cline = 16pF
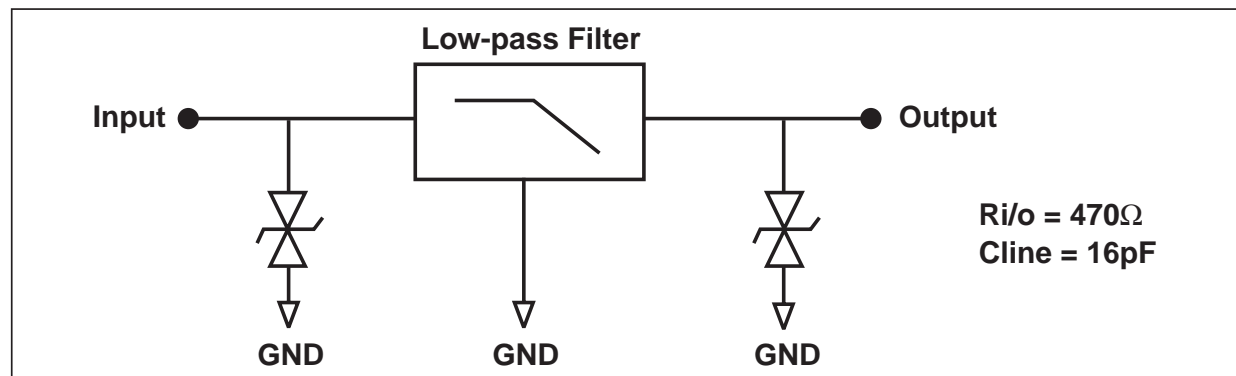
TM : IPAD is a trademark of STMicroelectronics.

ABSOLUTE RATINGS (limiting values)

Symbol	Parameter and test conditions	Value	Unit
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	-40 to + 85	°C
T_{stg}	Storage temperature range	125	°C

ELECTRICAL CHARACTERISTICS $(T_{amb} = 25\ °C)$

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
Rd	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
Cline	Input capacitance per line
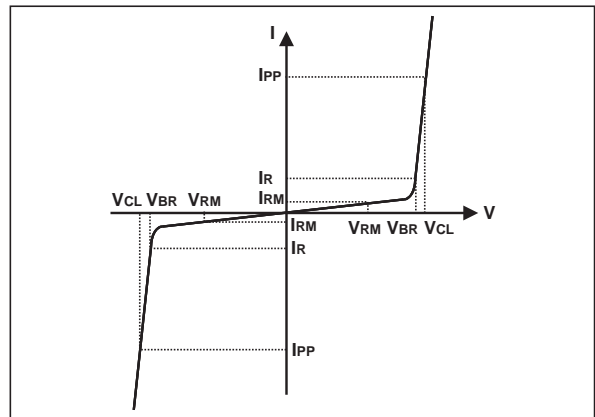
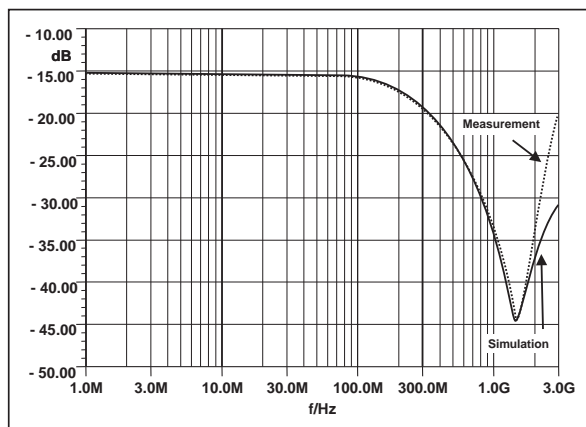| Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1\ mA$	14	16		V
I_{RM}	$V_{RM} = 12V$ per line			500	µA
$R_{I/O}$		423	470	517	Ω
C_{line}	@ 0V		16		pF

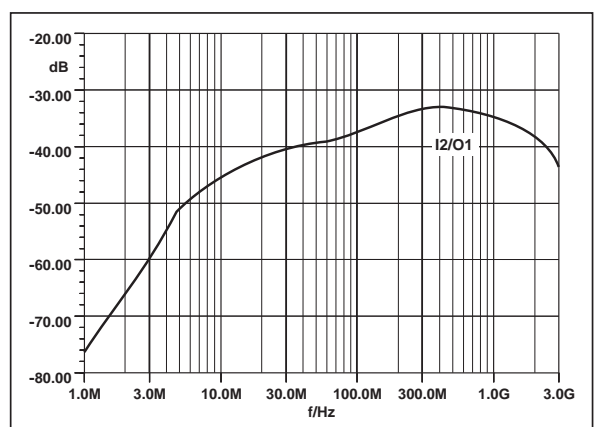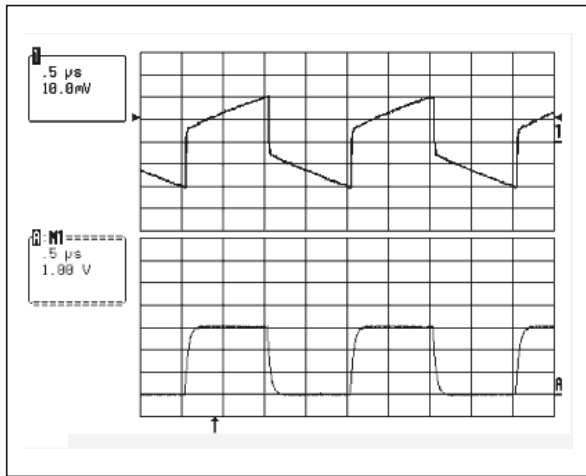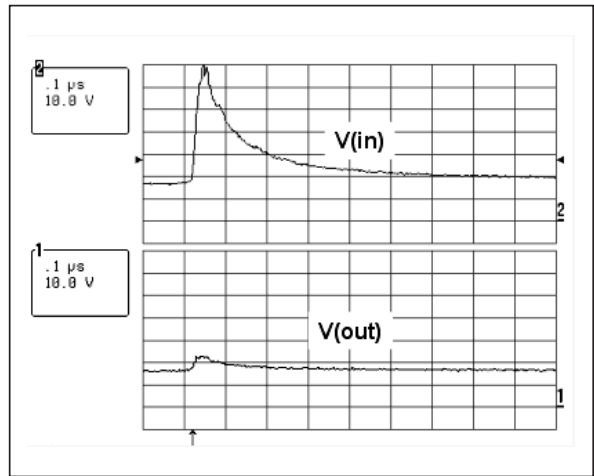**Fig. 1:** S21(dB) attenuation measurement and Aplac simulation.
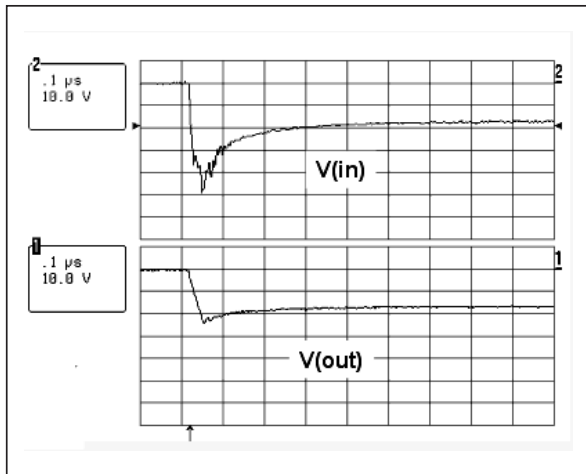

Fig. 2: Analog crosstalk measurements.

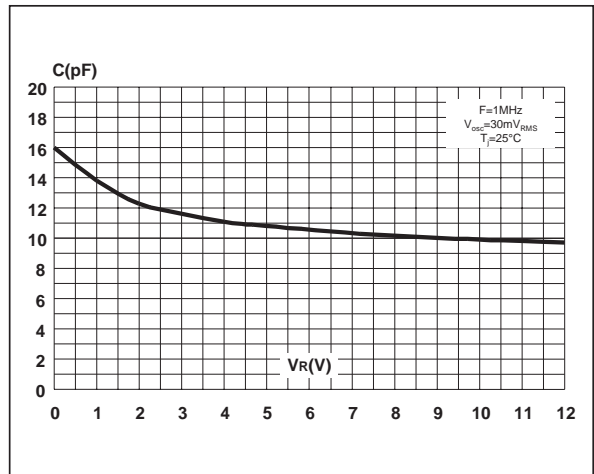**Fig. 3:** Digital crosstalk measurement

Fig. 4: ESD response to IEC61000-4-2 (+15kV air discharge) on one input V(in) and on one output (Vout).

Fig. 5: ESD response to IEC61000-4-2 (+15kV air discharge) on one input V(in) and on one output (Vout).
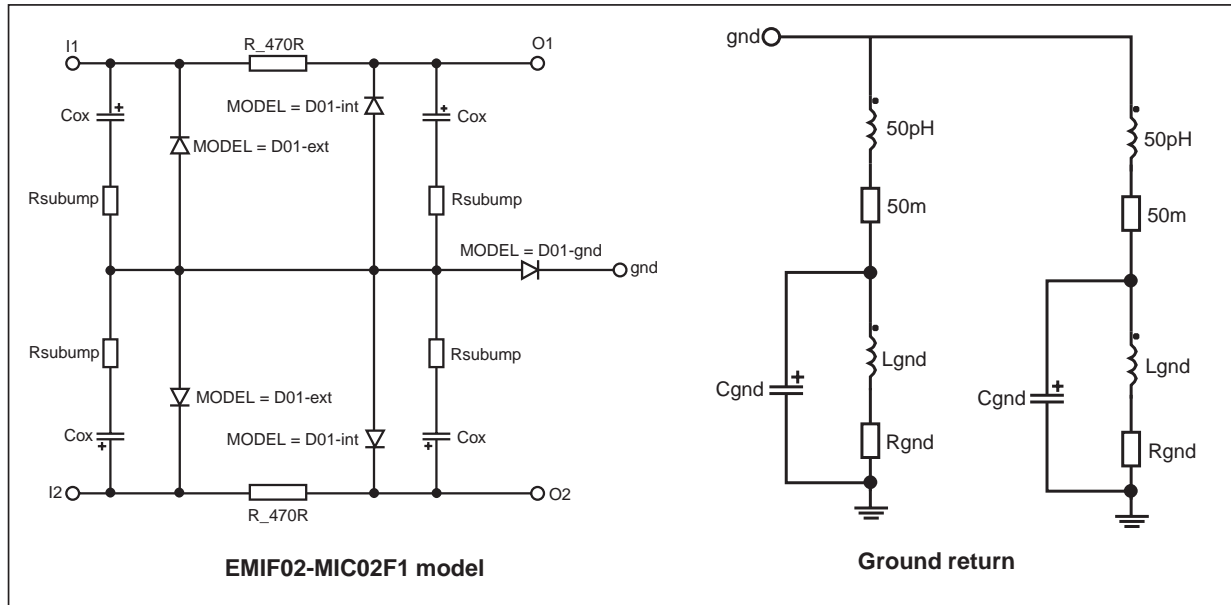

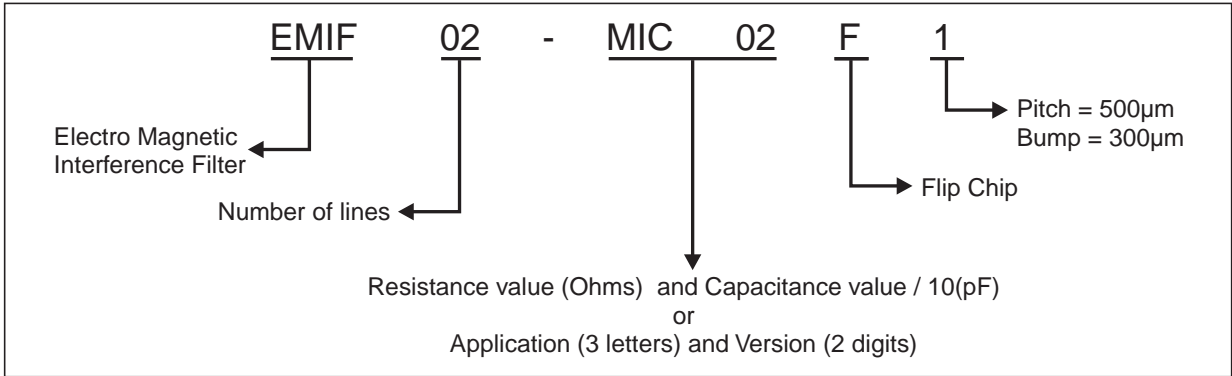
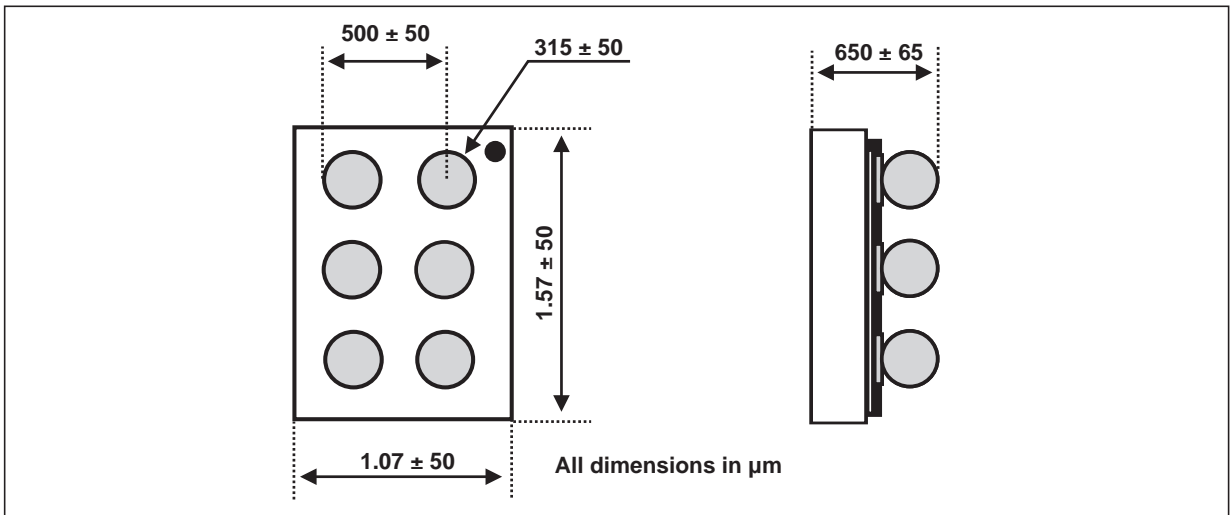**Fig. 6:** Line capacitance versus applied voltage.

Fig. 7: Aplac model

EMIF02-MIC02F1 model   **Ground return**

Fig. 8: Aplac parameters

Model D01-ext	Model D01-int	Model D01-gnd	
BV = 7	BV = 7	BV = 7	aplacvar Ls 400pH
CJO = Cz_ext	CJO = Cz_int	CJO = Cz_gnd	aplacvar Rs 100m
IBV = 1u	IBV = 1u	IBV = 1u	aplacvar R_470R 482.6
IKF = 1000	IKF = 1000	IKF = 1000	aplacvar Cz_ext 8.73pF
IS = 10f	IS = 10f	IS = 10f	aplacvar Rs_ext 850m
ISR = 100p	ISR = 100p	ISR = 100p	aplacvar Cz_int 2.9pF
N = 1	N = 1	N = 1	aplacvar Rs_int 850m
M = 0.3333	M = 0.3333	M = 0.3333	aplacvar Cz_gnd 215.61pF
RS = Rs_ext	RS = Rs_int	RS = Rs_gnd	aplacvar Rs_gnd 470m
VJ = 0.6	VJ = 0.6	VJ = 0.6	
TT = 50n	TT = 50n	TT = 50n	aplacvar Rgnd 10m
			aplacvar Lgnd 48pH
			aplacvar Cgnd 0.15pF
			aplacvar Cox 3.05pF
			aplacvar Rsubump 200m

ORDER CODE

EMIF   02   -   MIC   02   F   1

Electro Magnetic
Interference Filter

Number of lines

Pitch = 500µm
Bump = 300µm

Flip Chip

Resistance value (Ohms) and Capacitance value / 10(pF)
or
Application (3 letters) and Version (2 digits)

PACKAGE MECHANICAL DATA
FLIP CHIP

500 ± 50
315 ± 50
650 ± 65
1.57 ± 50
1.07 ± 50

All dimensions in µm

MARKING

365
240
365
XXX
yww
220
40

All dimensions in µm
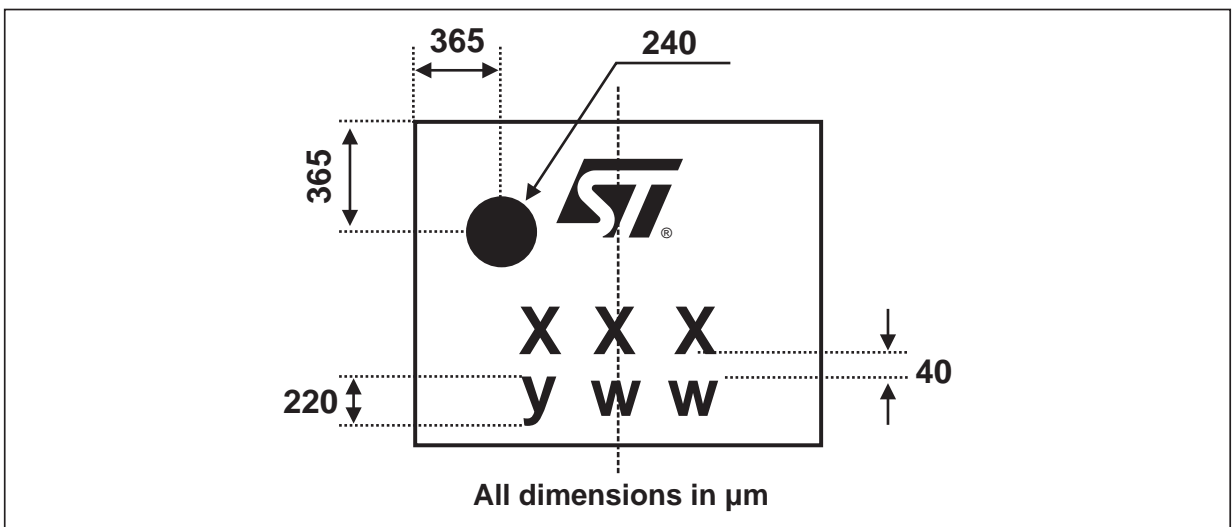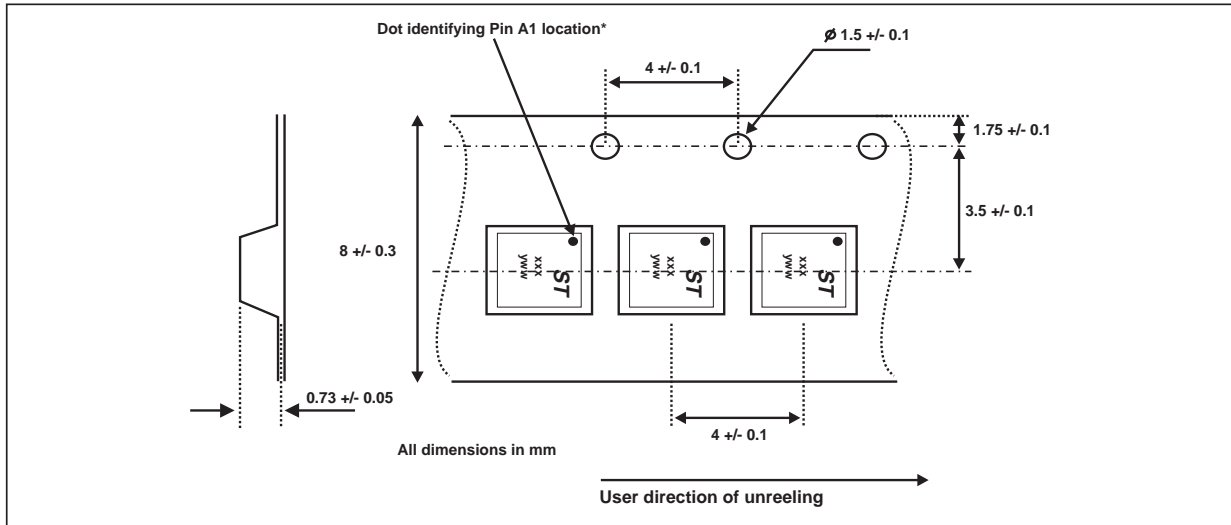
PACKING

OTHER INFORMATION

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-MIC02F1	FJT	Flip Chip	2.3 mg	5000	Tape & reel (7")

Note: More packing informations are available in the application note AN1235: "Flip-Chip: Package description and recommandations for use"