



#### **DUAL N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR**

### **Features**

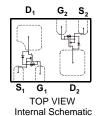
- Low On-Resistance
- Very Low Gate Threshold Voltage, 0.9V Max.
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- Lead Free By Design/RoHS Compliant (Note 2)
- "Green" Device (Note 4)
- ESD Protected Gate
- Ultra Low Profile Package

### **Mechanical Data**

- Case: DFN1310H4-6
- Case Material: Molded Plastic, "Green" Molding Compound.
  UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish NiPdAu annealed over Copper leadframe.
   Solderable per MIL-STD-202, Method 208
- Marking Information: See Page 3
- Ordering Information: See Page 3

DFN1310H4-6





## **Maximum Ratings** @T<sub>A</sub> = 25°C unless otherwise specified

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		$V_{DSS}$	20	V
Gate-Source Voltage		$V_{GSS}$	±10	V
Drain Current per element (Note 1)	Continuous Pulsed (Note 3)	I <sub>D</sub>	200 250	mA

### Thermal Characteristics @TA = 25°C unless otherwise specified

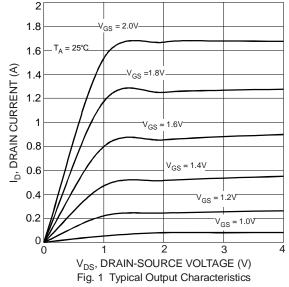
Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 1)	P <sub>D</sub>	350	mW
Thermal Resistance, Junction to Ambient	$R_{ hetaJA}$	357	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-65 to +150	°C

## **Electrical Characteristics** @T<sub>A</sub> = 25°C unless otherwise specified

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (per element) (Note 5)						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	20	_	_	V	$V_{GS} = 0V$ , $I_D = 100 \mu A$
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	_	_	10	μΑ	$V_{DS} = 17V, V_{GS} = 0V$
Gate-Source Leakage	I <sub>GSS</sub>	_	_	±5	μА	$V_{GS} = \pm 8V$ , $V_{DS} = 0V$
ON CHARACTERISTICS (per element) (Note 5)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	0.53	_	0.9	V	$V_{DS} = V_{GS}, I_D = 100 \mu A$
Static Drain-Source On-Resistance	R <sub>DS</sub> (ON)	   	0.9 0.85 1.2 2.4 2.5	1.5 1.7 1.7 3.5 3.5	Ω	$V_{GS} = 4V$ , $I_D = 10mA$ $V_{GS} = 2.7V$ , $I_D = 200mA$ $V_{GS} = 2.5V$ , $I_D = 10mA$ $V_{GS} = 1.8V$ , $I_D = 200mA$ $V_{GS} = 1.5V$ , $I_D = 1mA$
Forward Transfer Admittance	Y <sub>fs</sub>	40	_	_	mS	$V_{DS} = 3V$ , $I_D = 10mA$

- Notes:
- 1. Device mounted on FR-4 PCB.
- 2. No purposefully added lead.
- 3. Pulse width  $\leq 10\mu S$ , Duty Cycle  $\leq 1\%$ .
- 4. Diodes Inc.'s "Green" policy can be found on our website at http://www.diodes.com/products/lead\_free/index.php.
- Short duration pulse test used to minimize self-heating effect.





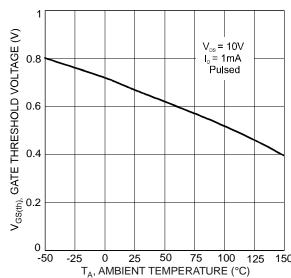
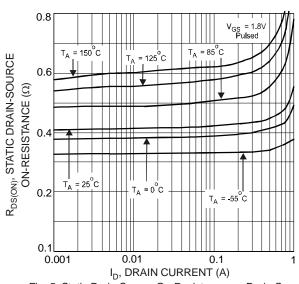


Fig. 3 Gate Threshold Voltage vs. Ambient Temperature





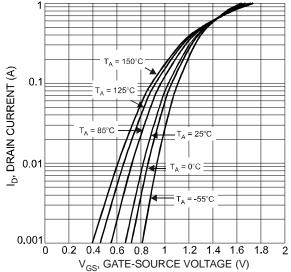


Fig. 2 Reverse Drain Current vs. Source-Drain Voltage

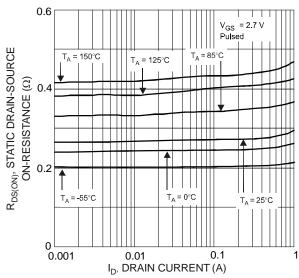


Fig. 4 Static Drain-Source On-State Resistance vs. Drain Current

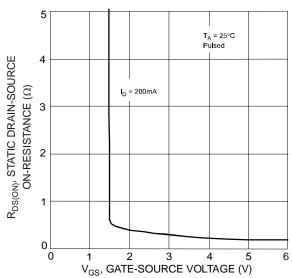


Fig. 6 Static Drain-Source, On-Resistance vs. Gate-Source Voltage



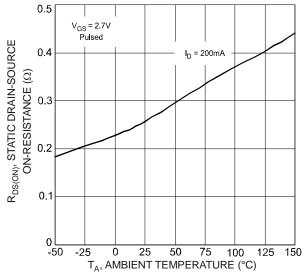


Fig. 7 Static Drain-Source, On-Resistance vs. Ambient Temperature

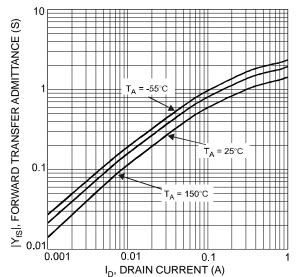


Fig. 9 Forward Transfer Admittance vs. Drain Current

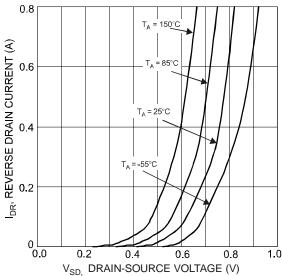
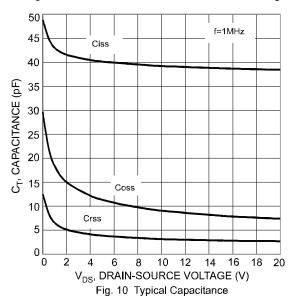


Fig. 8 Reverse Drain Current vs. Source-Drain Voltage



## Ordering Information (Note 6)

Part Number	Case	Packaging
DMN2005DLP4K-7	DFN1310H4-6	3000/Tape & Reel

Notes: 6. For packaging details, go to our website at http://www.diodes.com/datasheets/ap02007.pdf.

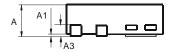
## **Marking Information**

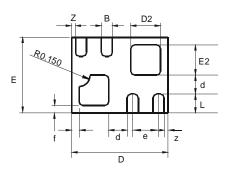
DL

DL = Product Type Marking Code



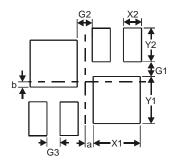
# **Package Outline Dimensions**





DFN1310H4-6				
Dim	Min	Max	Тур	
Α		0.40		
A1	0	0.05	0.02	
А3	_		0.13	
b	0.10	0.20	0.15	
D	1.25	1.38	1.30	
d			0.25	
D2	0.30	0.50	0.40	
Е	0.95	1.075	1.00	
е			0.35	
E2	0.30	0.50	0.40	
f	_	_	0.10	
L	0.20	0.30	0.25	
Z	_		0.05	
All Dimensions in mm				

# **Suggested Pad Layout**



Dimensions	Value (in mm)
G1	0.16
G2	0.17
G3	0.15
X1	0.52
X2	0.20
Y1	0.52
Y2	0.375
а	0.09
b	0.06



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