Features

- 20 ns, 25 ns, and 45 ns access times

- Internally organized as 512 K × 8 (CY14B104LA) or 256 K × 16 (CY14B104NA)

- Hands off automatic STORE on power-down with only a small capacitor

- STORE to QuantumTrap nonvolatile elements initiated by software, device pin, or AutoStore on power-down

- RECALL to SRAM initiated by software or power-up

- Infinite read, write, and recall cycles

- 1 million STORE cycles to QuantumTrap

- 20 year data retention

- Single 3 V +20%, -10% operation

- Industrial temperature

- Packages
  - 44-/54-pin thin small outline package (TSOP II)
  - 48-ball fine-pitch ball grid array (FBGA)

- Pb-free and restriction of hazardous substances (RoHS) compliant

Functional Description

The Cypress CY14B104LA/CY14B104NA is a fast static RAM (SRAM), with a nonvolatile element in each memory cell. The memory is organized as 512 K bytes of 8 bits each or 256 K words of 16 bits each. The embedded nonvolatile elements incorporate QuantumTrap technology, producing the world's most reliable nonvolatile memory. The SRAM provides infinite read and write cycles, while independent nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power-down. On power-up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control.

Logic Block Diagram[1, 2, 3]
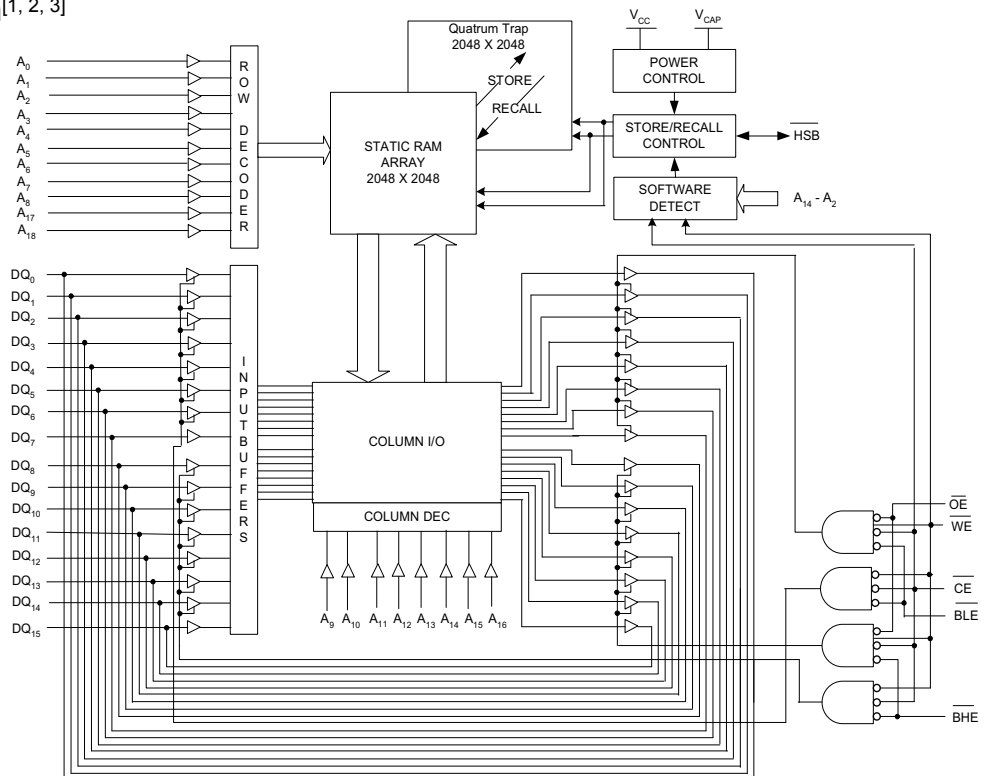
Notes
1. Address A_0 - A_{18} for ×8 configuration and Address A_0 - A_{17} for ×16 configuration.
2. Data DQ_0 - DQ_7 for ×8 configuration and Data DQ_0 - DQ_{15} for ×16 configuration.
3. BHE and BLE are applicable for ×16 configuration only.

[+] Feedback

Contents

Pinouts

Figure 1. Pin Diagram - 48-Ball FBGA

48 - FBGA
(×8)
Top View
(not to scale)

	1	2	3	4	5	6	
A	NC	$\overline{OE}$	A_0	A_1	A_2	NC	A
B	NC	NC	A_3	A_4	$\overline{CE}$	NC	B
C	DQ_0	NC	A_5	A_6	NC	DQ_4	C
D	V_{SS}	DQ_1	A_{17}	A_7	DQ_5	V_{CC}	D
E	V_{CC}	DQ_2	V_{CAP}	A_{16}	DQ_6	V_{SS}	E
F	DQ_3	NC	A_{14}	A_{15}	NC	DQ_7	F
G	NC	$\overline{HSB}$	A_{12}	A_{13}	$\overline{WE}$	NC	G
H	A_{18}	A_8	A_9	A_{10}	A_{11}	NC[4]	H

48 - FBGA
(×16)
Top View
(not to scale)

	1	2	3	4	5	6	
A	$\overline{BLE}$	$\overline{OE}$	A_0	A_1	A_2	NC	A
B	DQ_8	$\overline{BHE}$	A_3	A_4	$\overline{CE}$	DQ_0	B
C	DQ_9	DQ_{10}	A_5	A_6	DQ_1	DQ_2	C
D	V_{SS}	DQ_{11}	A_{17}	A_7	DQ_3	V_{CC}	D
E	V_{CC}	DQ_{12}	V_{CAP}	A_{16}	DQ_4	V_{SS}	E
F	DQ_{14}	DQ_{13}	A_{14}	A_{15}	DQ_5	DQ_6	F
G	DQ_{15}	$\overline{HSB}$	A_{12}	A_{13}	$\overline{WE}$	DQ_7	G
H	NC[4]	A_8	A_9	A_{10}	A_{11}	NC	H

Figure 2. Pin Diagram - 44-Pin TSOP II

(×8)

44 - TSOP II
(×8)
Top View
(not to scale)

Pin	Left		Right	Pin
1	NC		$\overline{HSB}$	44
2	NC[5]		NC	43
3	A_0		NC[4]	42
4	A_1		A_{18}	41
5	A_2		A_{17}	40
6	A_3		A_{16}	39
7	A_4		A_{15}	38
8	$\overline{CE}$		$\overline{OE}$	37
9	DQ_0		DQ_7	36
10	DQ_1		DQ_6	35
11	V_{CC}		V_{SS}	34
12	V_{SS}		V_{CC}	33
13	DQ_2		DQ_5	32
14	DQ_3		DQ_4	31
15	$\overline{WE}$		V_{CAP}	30
16	A_5		A_{14}	29
17	A_6		A_{13}	28
18	A_7		A_{12}	27
19	A_8		A_{11}	26
20	A_9		A_{10}	25
21	NC		NC	24
22	NC		NC	23

(×16)[6]

44 - TSOP II
(×16)
Top View
(not to scale)

Pin	Left		Right	Pin
1	A_0		A_{17}	44
2	A_1		A_{16}	43
3	A_2		A_{15}	42
4	A_3		$\overline{OE}$	41
5	A_4		$\overline{BHE}$	40
6	$\overline{CE}$		$\overline{BLE}$	39
7	DQ_0		DQ_{15}	38
8	DQ_1		DQ_{14}	37
9	DQ_2		DQ_{13}	36
10	DQ_3		DQ_{12}	35
11	V_{CC}		V_{SS}	34
12	V_{SS}		V_{CC}	33
13	DQ_4		DQ_{11}	32
14	DQ_5		DQ_{10}	31
15	DQ_6		DQ_9	30
16	DQ_7		DQ_8	29
17	$\overline{WE}$		V_{CAP}	28
18	A_5		A_{14}	27
19	A_6		A_{13}	26
20	A_7		A_{12}	25
21	A_8		A_{11}	24
22	A_9		A_{10}	23

Notes
4. Address expansion for 8 Mbit. NC pin not connected to die.
5. Address expansion for 16 Mbit. NC pin not connected to die.
6. HSB pin is not available in 44-TSOP II (×16) package.

Pinouts (continued)

Figure 3. Pin Diagram - 54-Pin TSOP II (×16)
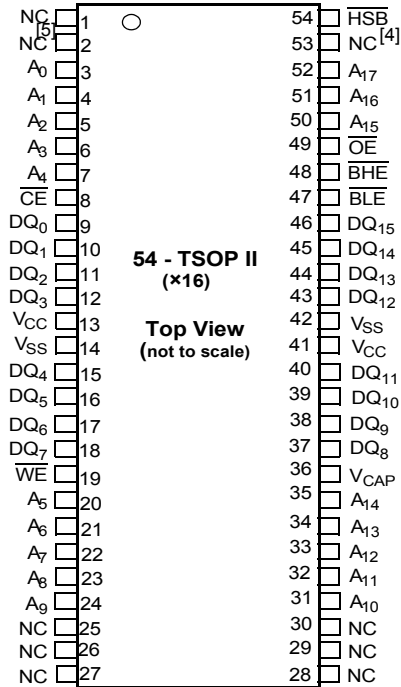

Pin			Pin	
NC[5]	1		54	$\overline{HSB}$
NC	2		53	NC[4]
A_0	3		52	A_{17}
A_1	4		51	A_{16}
A_2	5		50	A_{15}
A_3	6		49	$\overline{OE}$
A_4	7		48	$\overline{BHE}$
$\overline{CE}$	8		47	$\overline{BLE}$
DQ_0	9		46	DQ_{15}
DQ_1	10		45	DQ_{14}
DQ_2	11		44	DQ_{13}
DQ_3	12		43	DQ_{12}
V_{CC}	13		42	V_{SS}
V_{SS}	14		41	V_{CC}
DQ_4	15		40	DQ_{11}
DQ_5	16		39	DQ_{10}
DQ_6	17		38	DQ_9
DQ_7	18		37	DQ_8
$\overline{WE}$	19		36	V_{CAP}
A_5	20		35	A_{14}
A_6	21		34	A_{13}
A_7	22		33	A_{12}
A_8	23		32	A_{11}
A_9	24		31	A_{10}
NC	25		30	NC
NC	26		29	NC
NC	27		28	NC

54 - TSOP II (×16)

Top View (not to scale)

Table 1. Pin Definitions

Pin Name	I/O Type	Description
$A_0 – A_{18}$	Input	**Address inputs.** Used to select one of the 524,288 bytes of the nvSRAM for x8 Configuration.
$A_0 – A_{17}$		**Address inputs.** Used to Select one of the 262,144 words of the nvSRAM for x16 Configuration.
$DQ_0 – DQ_7$	Input/Output	**Bidirectional data I/O lines for ×8 configuration**. Used as input or output lines depending on operation.
$DQ_0 – DQ_{15}$		**Bidirectional data I/O lines for ×16 configuration**. Used as input or output lines depending on operation.
WE	Input	**Write Enable input, Active LOW**. When selected LOW, data on the I/O pins is written to the specific address location.
$\overline{CE}$	Input	**Chip Enable input, Active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	Input	**Output Enable, Active LOW**. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. I/O pins are tristated on deasserting $\overline{OE}$ HIGH.
$\overline{BHE}$	Input	**Byte High Enable, Active LOW**. Controls DQ_{15} - DQ_8.
$\overline{BLE}$	Input	**Byte Low Enable, Active LOW**. Controls DQ_7 - DQ_0.
V_{SS}	Ground	**Ground for the device**. Must be connected to the ground of the system.
V_{CC}	Power supply	**Power supply inputs to the device**.
$\overline{HSB}$[7]	Input/Output	**Hardware STORE Busy (HSB)**. When LOW this output indicates that a Hardware STORE is in progress. When pulled LOW external to the chip it initiates a nonvolatile STORE operation. After each Hardware and Software STORE operation, HSB is driven HIGH for a short time (t_{HHHD}) with standard output high current, and then a weak internal pull-up resistor keeps this pin HIGH (external pull-up resistor connection optional).
V_{CAP}	Power supply	**AutoStore Capacitor**. Supplies power to the nvSRAM during power loss to store data from SRAM to nonvolatile elements.
NC	No connect	**No Connect**. This pin is not connected to the die.

Note
7. $\overline{HSB}$ pin is not available in 44-TSOP II (×16) package.

Device Operation

The CY14B104LA/CY14B104NA nvSRAM is made up of two functional components paired in the same physical cell. They are a SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to the SRAM (the RECALL operation). Using this unique architecture, all cells are stored and recalled in parallel. During the STORE and RECALL operations, SRAM read and write operations are inhibited. The CY14B104LA/CY14B104NA supports infinite reads and writes similar to a typical SRAM. In addition, it provides infinite RECALL operations from the nonvolatile cells and up to 1 million STORE operations. Refer to the Truth Table For SRAM Operations on page 17 for a complete description of read and write modes.

SRAM Read

The CY14B104LA/CY14B104NA performs a read cycle when $\overline{CE}$ and $\overline{OE}$ are LOW and $\overline{WE}$ and $\overline{HSB}$ are HIGH. The address specified on pins A_{0-18} or A_{0-17} determines which of the 524,288 data bytes or 262,144 words of 16 bits each are accessed. Byte enables ($\overline{BHE}$, $\overline{BLE}$) determine which bytes are enabled to the output, in the case of 16-bit words. When the read is initiated by an address transition, the outputs are valid after a delay of t_{AA} (read cycle 1). If the read is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at t_{ACE} or at t_{DOE}, whichever is later (read cycle 2). The data output repeatedly responds to address changes within the t_{AA} access time without the need for transitions on any control input pins. This remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ or $\overline{HSB}$ is brought LOW.

SRAM Write

A write cycle is performed when $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{HSB}$ is HIGH. The address inputs must be stable before entering the write cycle and must remain stable until $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common I/O pins DQ_{0-15} are written into the memory if the data is valid (t_{SD} time) before the end of a $\overline{WE}$ controlled write or before the end of an $\overline{CE}$ controlled write. The Byte Enable inputs ($\overline{BHE}$, $\overline{BLE}$) determine which bytes are written, in the case of 16-bit words. It is recommended that $\overline{OE}$ be kept HIGH during the entire write cycle to avoid data bus contention on common I/O lines. If $\overline{OE}$ is left LOW, internal circuitry turns off the output buffers t_{HZWE} after $\overline{WE}$ goes LOW.

AutoStore Operation

The CY14B104LA/CY14B104NA stores data to the nvSRAM using one of the following three storage operations: Hardware STORE activated by the HSB; Software STORE activated by an address sequence; AutoStore on device power-down. The AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14B104LA/CY14B104NA.

During a normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC}. A STORE operation is initiated with power provided by the V_{CAP} capacitor.

Note
8. HSB pin is not available in 44-TSOP II (x16) package.

Note If the capacitor is not connected to V_{CAP} pin, AutoStore must be disabled using the soft sequence specified in Preventing AutoStore on page 7. In case AutoStore is enabled without a capacitor on V_{CAP} pin, the device attempts an AutoStore operation without sufficient charge to complete the Store. This corrupts the data stored in nvSRAM.

Figure 4 shows the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. Refer to DC Electrical Characteristics on page 9 for the size of V_{CAP}. The voltage on the V_{CAP} pin is driven to V_{CC} by a regulator on the chip. A pull-up should be placed on $\overline{WE}$ to hold it inactive during power-up. This pull-up is effective only if the $\overline{WE}$ signal is tristate during power-up. Many MPUs tristate their controls on power-up. This should be verified when using the pull-up. When the nvSRAM comes out of power-on-RECALL, the MPU must be active or the $\overline{WE}$ held inactive until the MPU comes out of reset.

To reduce unnecessary nonvolatile stores, AutoStore and hardware STORE operations are ignored unless at least one write operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a write operation has taken place. The HSB signal is monitored by the system to detect if an AutoStore cycle is in progress.

Figure 4. AutoStore Mode
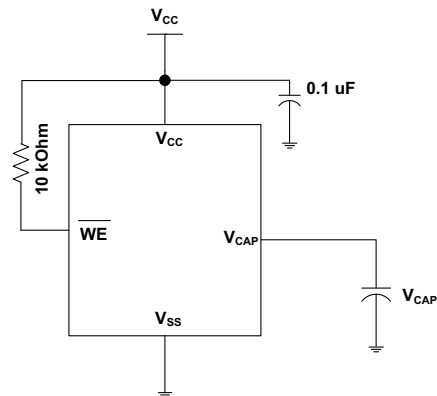
Hardware STORE Operation

The CY14B104LA/CY14B104NA provides the $\overline{HSB}$[8] pin to control and acknowledge the STORE operations. The $\overline{HSB}$ pin is used to request a hardware STORE cycle. When the HSB pin is driven LOW, the CY14B104LA/CY14B104NA conditionally initiates a STORE operation after t_{DELAY}. An actual STORE cycle only begins if a write to the SRAM has taken place since the last STORE or RECALL cycle. The HSB pin also acts as an open drain driver (internal 100 kΩ weak pull-up resistor) that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

Note After each Hardware and Software STORE operation $\overline{HSB}$ is driven HIGH for a short time (t_{HHHD}) with standard output high current and then remains HIGH by internal 100 kΩ pull-up resistor.

SRAM write operations that are in progress when $\overline{\text{HSB}}$ is driven LOW by any means are given time (t_{DELAY}) to complete before the STORE operation is initiated. However, any SRAM write cycles requested after HSB goes LOW are inhibited until HSB returns HIGH. In case the write latch is not set, HSB is not driven LOW by the CY14B104LA/CY14B104NA. But any SRAM read and write cycles are inhibited until $\overline{\text{HSB}}$ is returned HIGH by MPU or other external source.

During any STORE operation, regardless of how it is initiated, the CY14B104LA/CY14B104NA continues to drive the HSB pin LOW, releasing it only when the STORE is complete. Upon completion of the STORE operation, the nvSRAM memory access is inhibited for t_{LZHSB} time after HSB pin returns HIGH. Leave the HSB unconnected if it is not used.

Hardware RECALL (Power-Up)

During power-up or after any low power condition ($V_{CC} < V_{SWITCH}$), an internal RECALL request is latched. When V_{CC} again exceeds the V_{SWITCH} on powerup, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete. During this time, the HSB pin is driven LOW by the HSB driver and all reads and writes to nvSRAM are inhibited.

Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. The CY14B104LA/CY14B104NA software STORE cycle is initiated by executing sequential $\overline{\text{CE}}$ or $\overline{\text{OE}}$ controlled read cycles from six specific address locations in exact order. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. After a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence, or the sequence is aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following read sequence must be performed.

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x8FC0 Initiate STORE cycle

The software sequence may be clocked with $\overline{\text{CE}}$ controlled reads or $\overline{\text{OE}}$ controlled reads, with $\overline{\text{WE}}$ kept HIGH for all the six READ sequences. After the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. HSB is driven LOW. After the t_{STORE} cycle time is fulfilled, the SRAM is activated again for the read and write operation.

Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of read operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, perform the following sequence of $\overline{\text{CE}}$ or $\overline{\text{OE}}$ controlled read operations must be performed.

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x4C63 Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared; then, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is again ready for read and write operations. The RECALL operation does not alter the data in the nonvolatile elements.

Table 2. Mode Selection

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$, $\overline{\text{BLE}}$[9]	$A_{15} - A_0$[10]	Mode	I/O	Power
H	X	X	X	X	Not selected	Output high-Z	Standby
L	H	L	L	X	Read SRAM	Output data	Active
L	L	X	L	X	Write SRAM	Input data	Active
L	H	L	X	0x4E38	Read SRAM	Output data	Active[11]
				0xB1C7	Read SRAM	Output data	
				0x83E0	Read SRAM	Output data	
				0x7C1F	Read SRAM	Output data	
				0x703F	Read SRAM	Output data	
				0x8B45	AutoStore Disable	Output data	

Notes
9. $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ are applicable for x16 configuration only.
10. While there are 19 address lines on the CY14B104LA (18 address lines on the CY14B104NA), only 13 address lines ($A_{14} - A_2$) are used to control software modes. The remaining address lines are don't care.
11. The six consecutive address locations must be in the order listed. $\overline{\text{WE}}$ must be HIGH during all six cycles to enable a nonvolatile cycle.

Table 2. Mode Selection (continued)

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}, \overline{BLE}$[9]	A$_{15}$ - A$_0$[10]	Mode	I/O	Power
L	H	L	X	0x4E38	Read SRAM	Output data	Active[11]
				0xB1C7	Read SRAM	Output data	
				0x83E0	Read SRAM	Output data	
				0x7C1F	Read SRAM	Output data	
				0x703F	Read SRAM	Output data	
				0x4B46	AutoStore Enable	Output data	
L	H	L	X	0x4E38	Read SRAM	Output data	Active I$_{CC2}$[11]
				0xB1C7	Read SRAM	Output data	
				0x83E0	Read SRAM	Output data	
				0x7C1F	Read SRAM	Output data	
				0x703F	Read SRAM	Output data	
				0x8FC0	Nonvolatile STORE	Output high-Z	
L	H	L	X	0x4E38	Read SRAM	Output data	Active[11]
				0xB1C7	Read SRAM	Output data	
				0x83E0	Read SRAM	Output data	
				0x7C1F	Read SRAM	Output data	
				0x703F	Read SRAM	Output data	
				0x4C63	Nonvolatile RECALL	Output high-Z	

Preventing AutoStore

The AutoStore function is disabled by initiating an AutoStore disable sequence. A sequence of read operations is performed in a manner similar to the software STORE initiation. To initiate the AutoStore disable sequence, the following sequence of $\overline{CE}$ or $\overline{OE}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x8B45 AutoStore Disable

The AutoStore is re-enabled by initiating an AutoStore enable sequence. A sequence of read operations is performed in a manner similar to the software RECALL initiation. To initiate the AutoStore enable sequence, the following sequence of $\overline{CE}$ or $\overline{OE}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or re-enabled, a manual STORE operation (hardware or software) must be issued to save the AutoStore state through subsequent power-down cycles. The part comes from the factory with AutoStore enabled.

Data Protection

The CY14B104LA/CY14B104NA protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and write operations. The low voltage condition is detected when $V_{CC} < V_{SWITCH}$. If the CY14B104LA/CY14B104NA is in a write mode (both $\overline{CE}$ and $\overline{WE}$ are LOW) at power-up, after a RECALL or STORE, the write is inhibited until the SRAM is enabled after t_{LZHSB} (HSB to output active). This protects against inadvertent writes during power-up or brown out conditions.

Noise Considerations

Refer to CY application note AN1064.

Best Practices

nvSRAM products have been used effectively for over 27 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

■ The nonvolatile cells in this nvSRAM product are delivered from Cypress with 0x00 written in all cells. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, and so on should always program a unique NV pattern (that is, complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.

■ power-up boot firmware routines should rewrite the nvSRAM into the desired state (for example, AutoStore enabled). While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently such as program bugs and incoming inspection routines.

■ The V_{CAP} value specified in this datasheet includes a minimum and a maximum value size. Best practice is to meet this requirement and not exceed the maximum V_{CAP} value because the nvSRAM internal algorithm calculates V_{CAP} charge and discharge time based on this maximum V_{CAP} value. Customers that want to use a larger V_{CAP} value to make sure there is extra store charge and store time should discuss their V_{CAP} size selection with Cypress to understand any impact on the V_{CAP} voltage level at the end of a t_{RECALL} period.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Maximum accumulated storage time

    At 150 °C ambient temperature.........................1000 h

    At 85 °C ambient temperature.................... .. 20 Years

Ambient temperature with
power applied .... –55 °C to +150 °C

Supply voltage on V_{CC} relative to V_{SS}............–0.5 V to 4.1 V

Voltage applied to outputs
in high-Z state ....–0.5 V to V_{CC} + 0.5 V

Input voltage ....–0.5 V to Vcc + 0.5 V

Transient voltage (<20 ns) on
any pin to ground potential ....–2.0 V to V_{CC} + 2.0 V

Package power dissipation
capability (T_A = 25 °C) .... .1.0 W

Surface mount Pb soldering
temperature (3 Seconds)... +260 °C

DC output current (1 output at a time, 1s duration) ..... 15 mA

Static discharge voltage... > 2001 V
(per MIL-STD-883, Method 3015)

Latch up current... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	2.7 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range (V_{CC} = 2.7 V to 3.6 V)

Parameter	Description	Test Conditions	Min	Typ[12]	Max	Unit
V_{CC}	Power supply		2.7	3.0	3.6	V
I_{CC1}	Average V_{CC} current	t_{RC} = 20 ns t_{RC} = 25 ns t_{RC} = 45 ns Values obtained without output loads (I_{OUT} = 0 mA)	– 	– 	70 70 52	mA mA mA
I_{CC2}	Average V_{CC} current during STORE	All inputs don't care, V_{CC} = Max Average current for duration t_{STORE}	–	–	10	mA
I_{CC3}	Average V_{CC} current at t_{RC}= 200 ns, V_{CC} (Typ), 25 °C	All inputs cycling at CMOS levels. Values obtained without output loads (I_{OUT} = 0 mA).	–	35	–	mA
I_{CC4}	Average V_{CAP} current during AutoStore cycle	All inputs don't care. Average current for duration t_{STORE}	–	–	5	mA
I_{SB}	V_{CC} standby current	$\overline{CE} \geq (V_{CC} – 0.2$ V). $V_{IN} \leq 0.2$ V or $\geq (V_{CC} – 0.2$ V). Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.	–	–	5	mA
I_{IX}[13]	Input leakage current (except HSB)	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$	–1	–	+1	µA
	Input leakage current (for HSB)	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$	–100	–	+1	µA
I_{OZ}	Off-state output leakage current	V_{CC} = Max, $V_{SS} \leq V_{OUT} \leq V_{CC}$, $\overline{CE}$ or $\overline{OE} \geq V_{IH}$ or BHE/BLE $\geq V_{IH}$ or $\overline{WE} \leq V_{IL}$	–1	–	+1	µA
V_{IH}	Input HIGH voltage		2.0	–	V_{CC} + 0.5	V
V_{IL}	Input LOW voltage		V_{SS} – 0.5	–	0.8	V
V_{OH}	Output HIGH voltage	I_{OUT} = –2 mA	2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OUT} = 4 mA	–	–	0.4	V
V_{CAP}	Storage capacitor	Between V_{CAP} pin and V_{SS}, 5 V rated	61	68	180	µF

Notes
12. Typical values are at 25°C, V_{CC}= V_{CC} (Typ). Not 100% tested.
13. The HSB pin has I_{OUT} = -2 uA for V_{OH} of 2.4 V when both active HIGH and LOW drivers are disabled. When they are enabled standard V_{OH} and V_{OL} are valid. This parameter is characterized but not tested.

[+] Feedback

Data Retention and Endurance

Parameter	Description	Min	Unit
$DATA_R$	Data retention	20	Years
NV_C	Nonvolatile STORE operations	1,000	K

Capacitance

In the following table, the capacitance parameters are listed.[14]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance (except BHE, BLE and HSB)	T_A = 25 °C, f = 1 MHz, V_{CC} = V_{CC} (Typ)	7	pF
	Input capacitance (for BHE, BLE and HSB)		8	pF
C_{OUT}	Output capacitance (except HSB)		7	pF
	Output capacitance (for HSB)		8	pF

Thermal Resistance

In the following table, the thermal resistance parameters are listed. [14]

Parameter	Description	Test Conditions	48-FBGA	44-TSOP II	54-TSOP II	Unit
Θ_{JA}	Thermal resistance (Junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	28.82	31.11	30.73	°C/W
Θ_{JC}	Thermal resistance (Junction to case)		7.84	5.56	6.08	°C/W

Figure 5. AC Test Loads
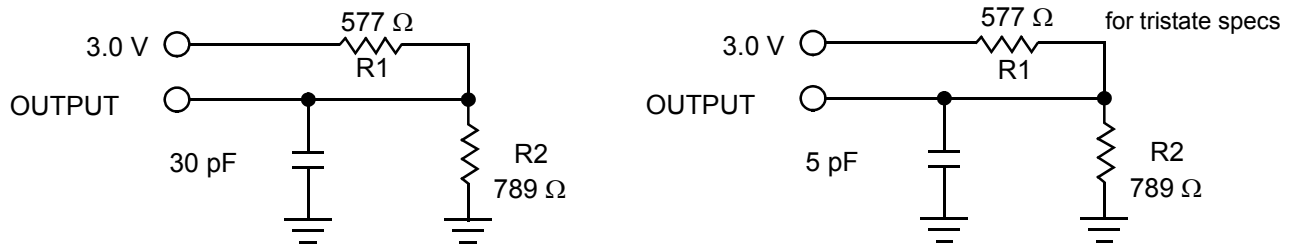
AC Test Conditions

Input pulse levels...0 V to 3 V

Input rise and fall times (10% - 90%) .... ≤3 ns

Input and output timing reference levels .... 1.5 V

Note
14. These parameters are guaranteed by design but not tested.

AC Switching Characteristics

Parameters		Description	20 ns		25 ns		45 ns		Unit
Cypress Parameter	Alt Parameter		Min	Max	Min	Max	Min	Max	
SRAM Read Cycle									
t_{ACE}	t_{ACS}	Chip enable access time	–	20	–	25	–	45	ns
t_{RC}[15]	t_{RC}	Read cycle time	20	–	25	–	45	–	ns
t_{AA}[16]	t_{AA}	Address access time	–	20	–	25	–	45	ns
t_{DOE}	t_{OE}	Output enable to data valid	–	10	–	12	–	20	ns
t_{OHA}[16]	t_{OH}	Output hold after address change	3	–	3	–	3	–	ns
t_{LZCE}[17, 18]	t_{LZ}	Chip enable to output active	3	–	3	–	3	–	ns
t_{HZCE}[17, 18]	t_{HZ}	Chip disable to output inactive	–	8	–	10	–	15	ns
t_{LZOE}[17, 18]	t_{OLZ}	Output enable to output active	0	–	0	–	0	–	ns
t_{HZOE}[17, 18]	t_{OHZ}	Output disable to output inactive	–	8	–	10	–	15	ns
t_{PU}[17]	t_{PA}	Chip enable to power active	0	–	0	–	0	–	ns
t_{PD}[17]	t_{PS}	Chip disable to power standby	–	20	–	25	–	45	ns
t_{DBE}	-	Byte enable to data valid	–	10	–	12	–	20	ns
t_{LZBE}[17]	-	Byte enable to output active	0	–	0	–	0	–	ns
t_{HZBE}[17]	-	Byte disable to output inactive	–	8	–	10	–	15	ns
SRAM Write Cycle									
t_{WC}	t_{WC}	Write cycle time	20	–	25	–	45	–	ns
t_{PWE}	t_{WP}	Write pulse width	15	–	20	–	30	–	ns
t_{SCE}	t_{CW}	Chip enable to end of write	15	–	20	–	30	–	ns
t_{SD}	t_{DW}	Data setup to end of write	8	–	10	–	15	–	ns
t_{HD}	t_{DH}	Data hold after end of write	0	–	0	–	0	–	ns
t_{AW}	t_{AW}	Address setup to end of write	15	–	20	–	30	–	ns
t_{SA}	t_{AS}	Address setup to start of write	0	–	0	–	0	–	ns
t_{HA}	t_{WR}	Address hold after end of write	0	–	0	–	0	–	ns
t_{HZWE}[17, 18,19]	t_{WZ}	Write enable to output disable	–	8	–	10	–	15	ns
t_{LZWE}[17, 18]	t_{OW}	Output active after end of write	3	–	3	–	3	–	ns
t_{BW}	-	Byte enable to end of write	15	–	20	–	30	–	ns

Switching Waveforms

Figure 6. SRAM Read Cycle #1: Address Controlled[15, 16, 20]
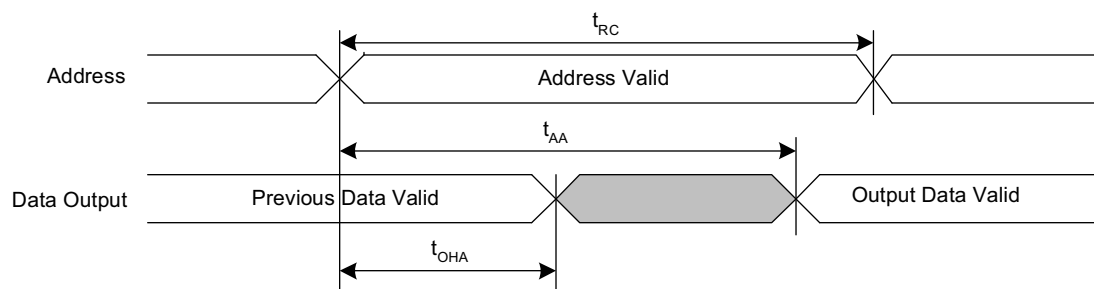
Notes
15. WE must be HIGH during SRAM read cycles.
16. Device is continuously selected with CE, OE and BHE / BLE LOW.
17. These parameters are guaranteed by design but not tested.
18. Measured ±200 mV from steady state output voltage.
19. If WE is LOW when CE goes LOW, the outputs remain in the high impedance state.
20. HSB must remain HIGH during read and write cycles.

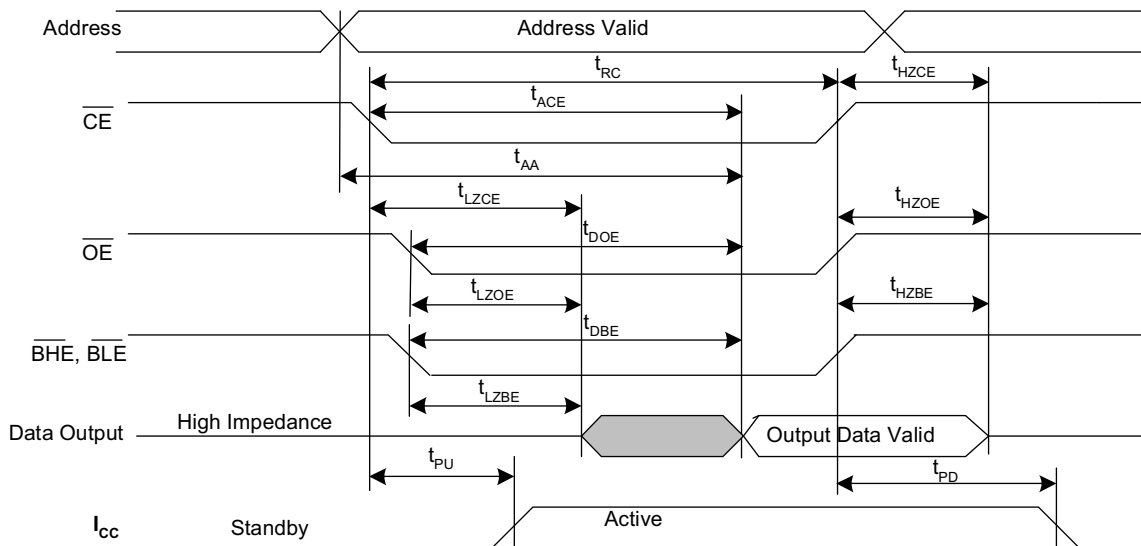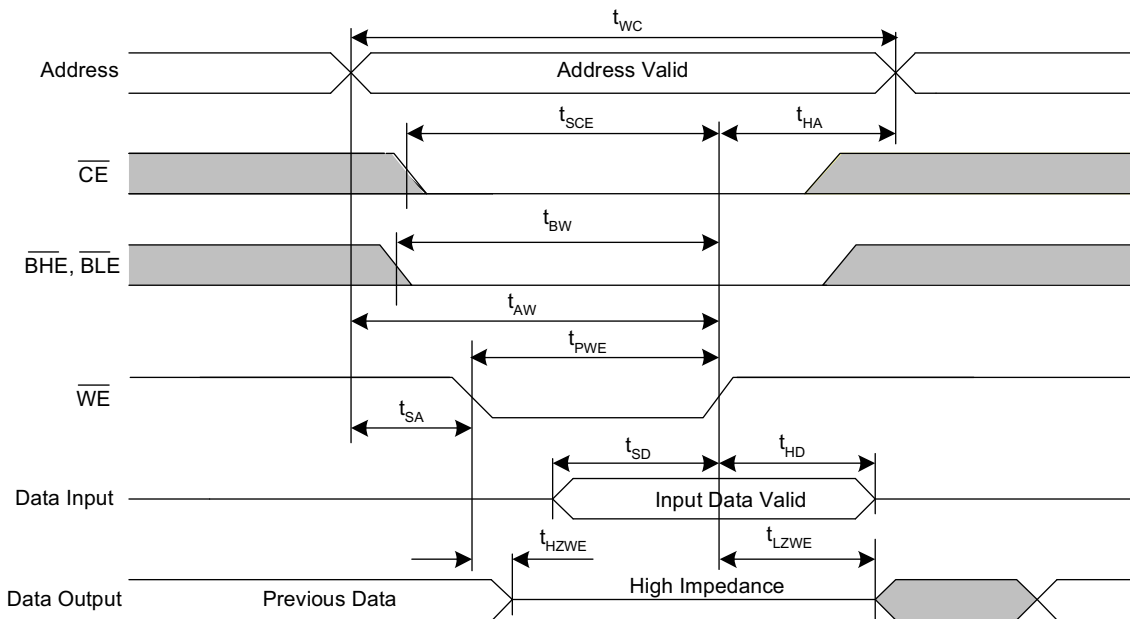**Figure 7. SRAM Read Cycle #2: $\overline{CE}$ and $\overline{OE}$ Controlled[21, 22, 23]**

Figure 8. SRAM Write Cycle #1: $\overline{WE}$ Controlled[21, 23, 24, 25]

Notes
21. $\overline{BHE}$ and $\overline{BLE}$ are applicable for ×16 configuration only.
22. $\overline{WE}$ must be HIGH during SRAM read cycles.
23. $\overline{HSB}$ must remain HIGH during read and write cycles.
24. If $\overline{WE}$ is LOW when $\overline{CE}$ goes LOW, the outputs remain in the high impedance state.
25. $\overline{CE}$ or $\overline{WE}$ must be $\geq V_{IH}$ during address transitions.

Figure 9. SRAM Write Cycle #2: $\overline{\text{CE}}$ Controlled[26, 27, 28, 29]
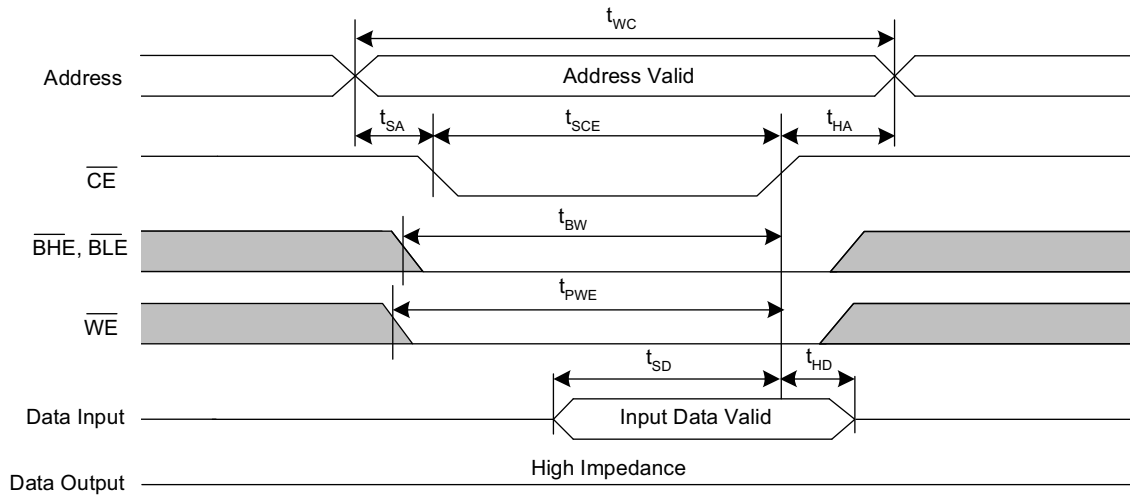
Figure 10. SRAM Write Cycle #3: $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ Controlled[26, 27, 28, 29]
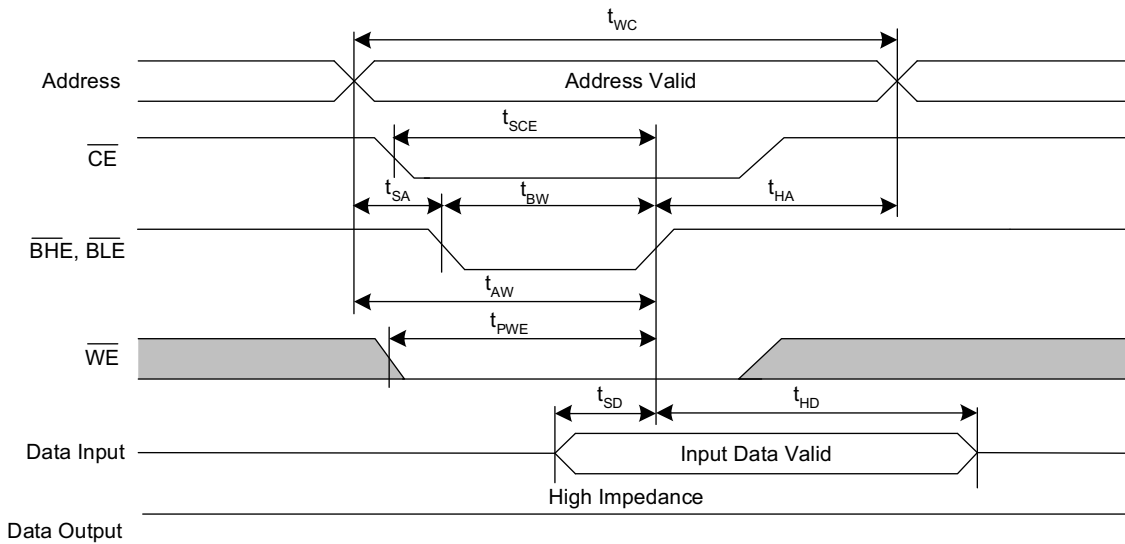
Notes
26. $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ are applicable for ×16 configuration only.
27. If $\overline{\text{WE}}$ is LOW when $\overline{\text{CE}}$ goes LOW, the outputs remain in the high impedance state.
28. $\overline{\text{HSB}}$ must remain HIGH during read and write cycles.
29. $\overline{\text{CE}}$ or $\overline{\text{WE}}$ must be $\geq V_{IH}$ during address transitions.

AutoStore/Power-Up RECALL

Parameter	Description	20 ns		25 ns		45 ns		Unit
		Min	Max	Min	Max	Min	Max	
$t_{HRECALL}$[30]	Power-Up RECALL duration	–	20	–	20	–	20	ms
t_{STORE}[31]	STORE cycle duration	–	8	–	8	–	8	ms
t_{DELAY}[32]	Time allowed to complete SRAM write cycle	–	20	–	25	–	25	ns
V_{SWITCH}	Low voltage trigger level	–	2.65	–	2.65	–	2.65	V
$t_{VCCRISE}$[14]	V_{CC} rise time	150	–	150	–	150	–	μs
V_{HDIS}[14]	HSB output disable voltage	–	1.9	–	1.9	–	1.9	V
t_{LZHSB}[14]	HSB to output active time	–	5	–	5	–	5	μs
t_{HHHD}[14]	HSB high active time	–	500	–	500	–	500	ns

Switching Waveforms

Figure 11. AutoStore or Power-Up RECALL[33]
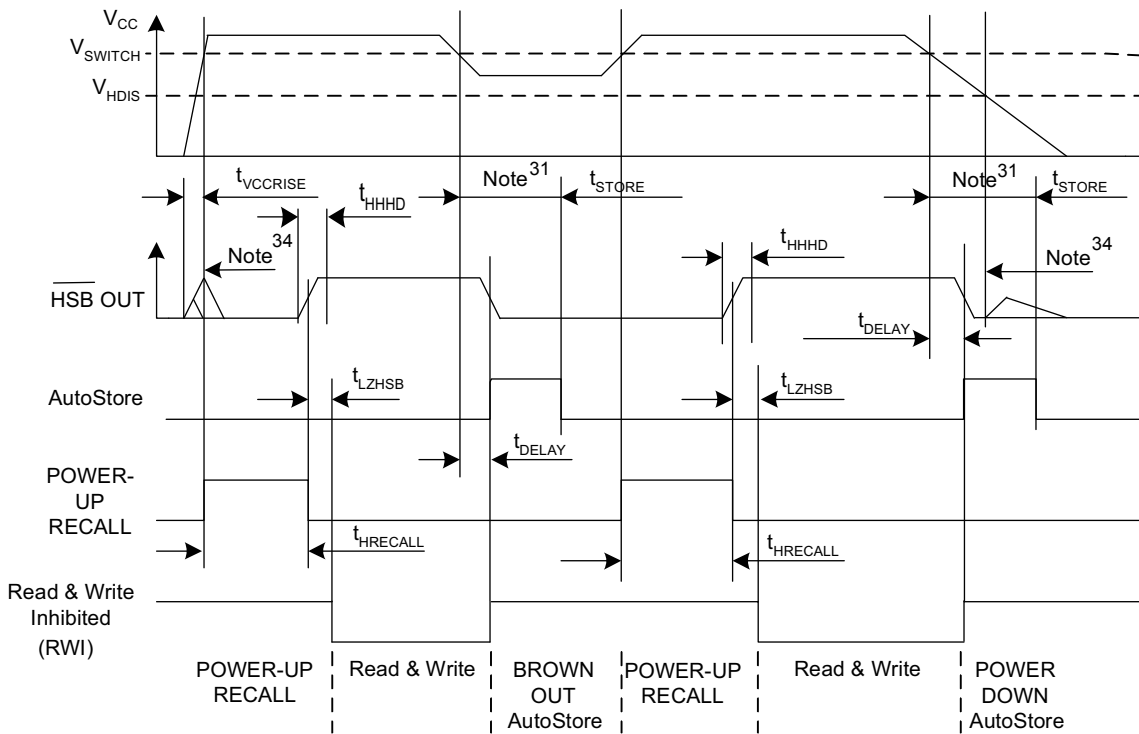
Notes
30. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.
31. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
32. On a Hardware STORE and AutoStore initiation, SRAM write operation continues to be enabled for time t_{DELAY}.
33. Read and write cycles are ignored during STORE, RECALL, and while V_{CC} is below V_{SWITCH}.
34. During power-up and power-down, HSB glitches when HSB pin is pulled up through an external resistor.

Software Controlled STORE/RECALL Cycle

In the following table, the software controlled STORE and RECALL cycle parameters are listed.[35, 36]

Parameter	Description	20 ns		25 ns		45 ns		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	STORE/RECALL initiation cycle time	20	–	25	–	45	–	ns
t_{SA}	Address setup time	0	–	0	–	0	–	ns
t_{CW}	Clock pulse width	15	–	20	–	30	–	ns
t_{HA}	Address hold time	0	–	0	–	0	–	ns
t_{RECALL}	RECALL duration	–	200	–	200	–	200	µs

Switching Waveforms

Figure 12. $\overline{CE}$ and $\overline{OE}$ Controlled Software STORE/RECALL Cycle[36]
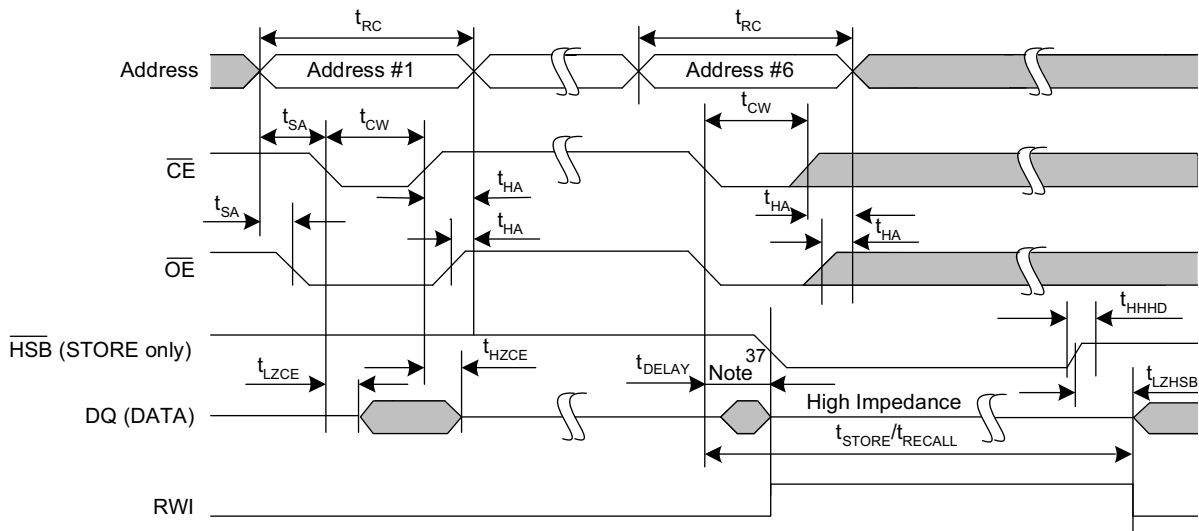
Figure 13. AutoStore Enable/Disable Cycle
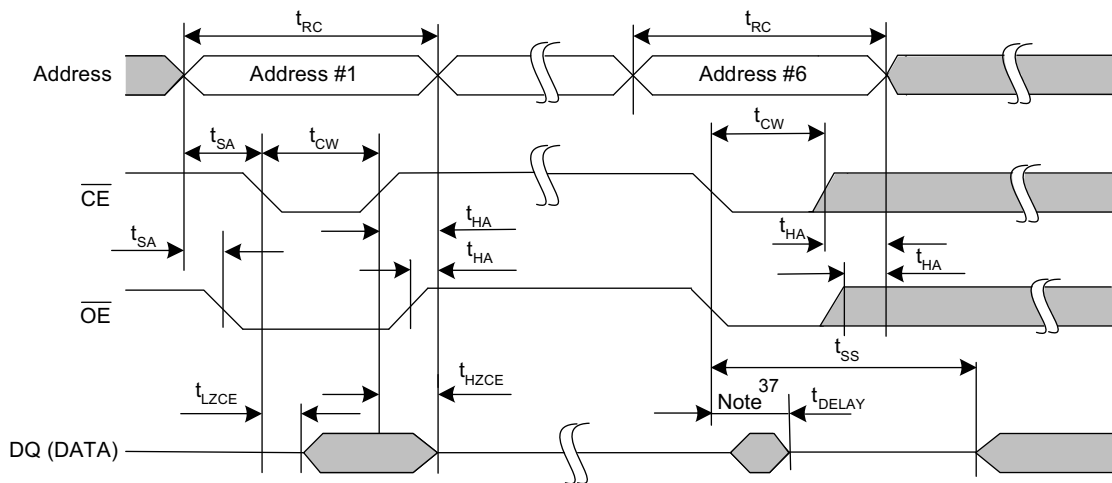
Notes
35. The software sequence is clocked with $\overline{CE}$ controlled or $\overline{OE}$ controlled reads.
36. The six consecutive addresses must be read in the order listed in Table 2 on page 6. $\overline{WE}$ must be HIGH during all six consecutive cycles.
37. DQ output data at the sixth read may be invalid since the output is disabled at t_{DELAY} time.

Hardware STORE Cycle

Parameter	Description	20 ns		25 ns		45 ns		Unit
		Min	Max	Min	Max	Min	Max	
t_{DHSB}	HSB to output active time when write latch not set	–	20	–	25	–	25	ns
t_{PHSB}	Hardware STORE pulse width	15	–	15	–	15	–	ns
t_{SS} [38, 39]	Soft sequence processing time	–	100	–	100	–	100	µs

Switching Waveforms

Figure 14. Hardware STORE Cycle[40]

Write latch set

Write latch not set

$\overline{HSB}$ pin is driven high to V_{CC} only by Internal 100 kOhm resistor,

$\overline{HSB}$ driver is disabled

SRAM is disabled as long as $\overline{HSB}$ (IN) is driven low.
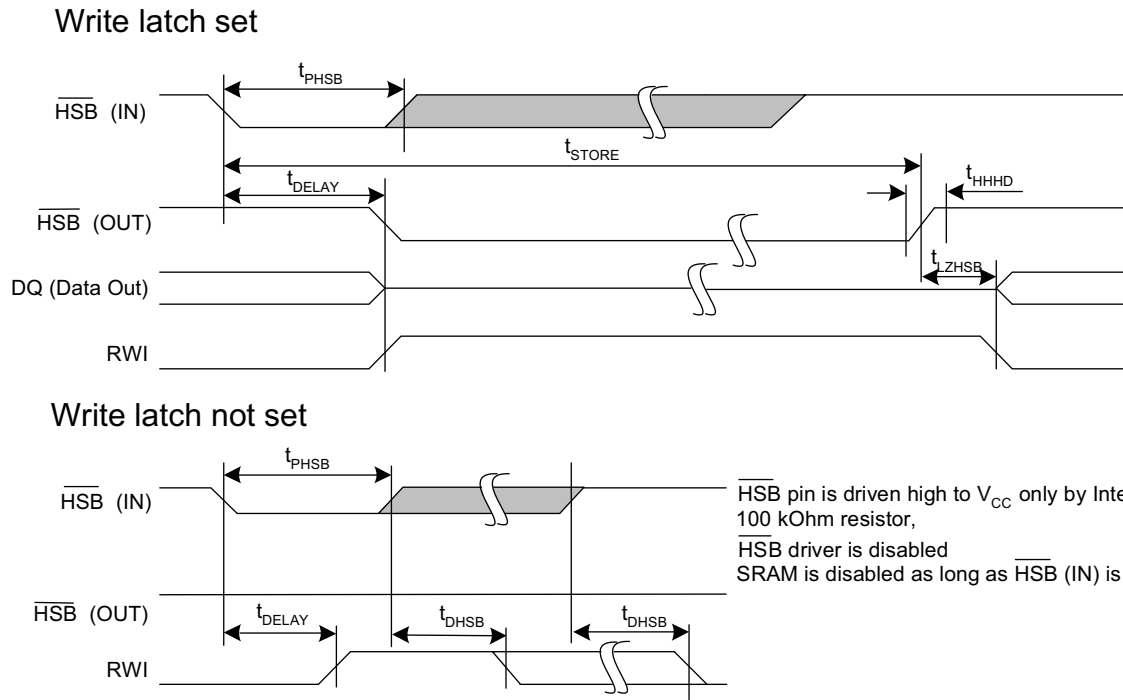
Figure 15. Soft Sequence Processing[38, 39]
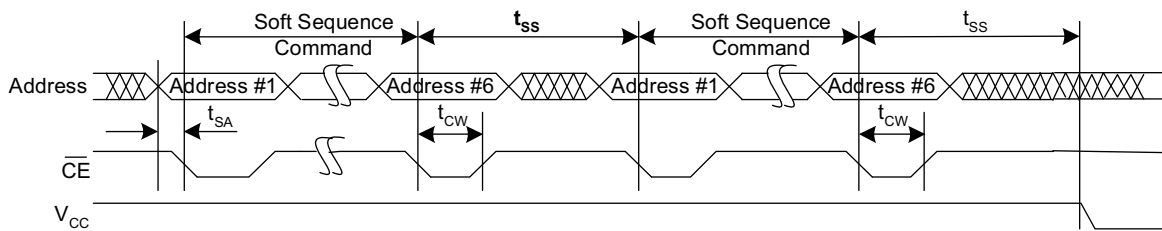
Notes
38. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain HIGH to effectively register command.
39. Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See the specific command.
40. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.

[+] Feedback

Truth Table For SRAM Operations

$\overline{HSB}$ should remain HIGH for SRAM Operations.

For x8 Configuration

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs[41]	Mode	Power
H	X	X	High-Z	Deselect/Power-down	Standby
L	H	L	Data out (DQ_0–DQ_7);	Read	Active
L	H	H	High-Z	Output disabled	Active
L	L	X	Data in (DQ_0–DQ_7);	Write	Active

For x16 Configuration

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$[42]	$\overline{BLE}$[42]	Inputs/Outputs[41]	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power-down	Standby
L	X	X	H	H	High-Z	Output disabled	Active
L	H	L	L	L	Data out (DQ_0–DQ_{15})	Read	Active
L	H	L	H	L	Data out (DQ_0–DQ_7); DQ_8–DQ_{15} in High Z	Read	Active
L	H	L	L	H	Data out (DQ_8–DQ_{15}); DQ_0–DQ_7 in High Z	Read	Active
L	H	H	L	L	High-Z	Output disabled	Active
L	H	H	H	L	High-Z	Output disabled	Active
L	H	H	L	H	High-Z	Output disabled	Active
L	L	X	L	L	Data in (DQ_0–DQ_{15})	Write	Active
L	L	X	H	L	Data in (DQ_0–DQ_7); DQ_8–DQ_{15} in High Z	Write	Active
L	L	X	L	H	Data in (DQ_8–DQ_{15}); DQ_0–DQ_7 in High Z	Write	Active

Notes
41. Data DQ_0 - DQ_7 for ×8 configuration and Data DQ_0 - DQ_{15} for ×16 configuration.
42. $\overline{BHE}$ and $\overline{BLE}$ are applicable for ×16 configuration only.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
20	CY14B104LA-ZS20XIT	51-85087	44-pin TSOP II	Industrial
	CY14B104LA-ZS20XI	51-85087	44-pin TSOP II	
	CY14B104NA-ZS20XIT	51-85087	44-pin TSOP II	
	CY14B104NA-ZS20XI	51-85087	44-pin TSOP II	
	CY14B104NA-BA20XIT	51-85128	48-ball FBGA	
	CY14B104NA-BA20XI	51-85128	48-ball FBGA	
25	CY14B104LA-ZS25XIT	51-85087	44-pin TSOP II	
	CY14B104LA-ZS25XI	51-85087	44-pin TSOP II	
	CY14B104LA-BA25XIT	51-85128	48-ball FBGA	
	CY14B104LA-BA25XI	51-85128	48-ball FBGA	
	CY14B104NA-ZS25XIT	51-85087	44-pin TSOP II	
	CY14B104NA-ZS25XI	51-85087	44-pin TSOP II	
	CY14B104NA-BA25XIT	51-85128	48-ball FBGA	
	CY14B104NA-BA25XI	51-85128	48-ball FBGA	
	CY14B104NA-BA25I	51-85128	48-ball FBGA	
	CY14B104NA-ZSP25XIT	51-85160	54-pin TSOP II	
	CY14B104NA-ZSP25XI	51-85160	54-pin TSOP II	
45	CY14B104LA-ZS45XIT	51-85087	44-pin TSOP II	
	CY14B104LA-ZS45XI	51-85087	44-pin TSOP II	
	CY14B104LA-BA45XIT	51-85128	48-ball FBGA	
	CY14B104LA-BA45XI	51-85128	48-ball FBGA	
	CY14B104NA-ZS45XIT	51-85087	44-pin TSOP II	
	CY14B104NA-ZS45XI	51-85087	44-pin TSOP II	
	CY14B104NA-BA45XIT	51-85128	48-ball FBGA	
	CY14B104NA-BA45XI	51-85128	48-ball FBGA	
	CY14B104NA-ZSP45XIT	51-85160	54-pin TSOP II	
	CY14B104NA-ZSP45XI	51-85160	54-pin TSOP II	

Ordering Code Definition

CY 14 B 104 L A -ZS 20 X I T

Option:
T - Tape & Reel
Blank - Std.

Temperature:
I - Industrial (–40 to 85 °C)

X - Pb-free
Blank - Sn Pb

Speed:
20 - 20 ns
25 - 25 ns
45 - 45 ns

Package:
BA - 48 FBGA
ZS - 44 TSOP II
ZSP - 54 TSOP II

Die Revision:
Blank - No Rev
A - 1st Rev

Data Bus:
L - x8
N - x16

Density:
104 - 4 Mb

Voltage:
B - 3.0 V

14 - nvSRAM

Cypress
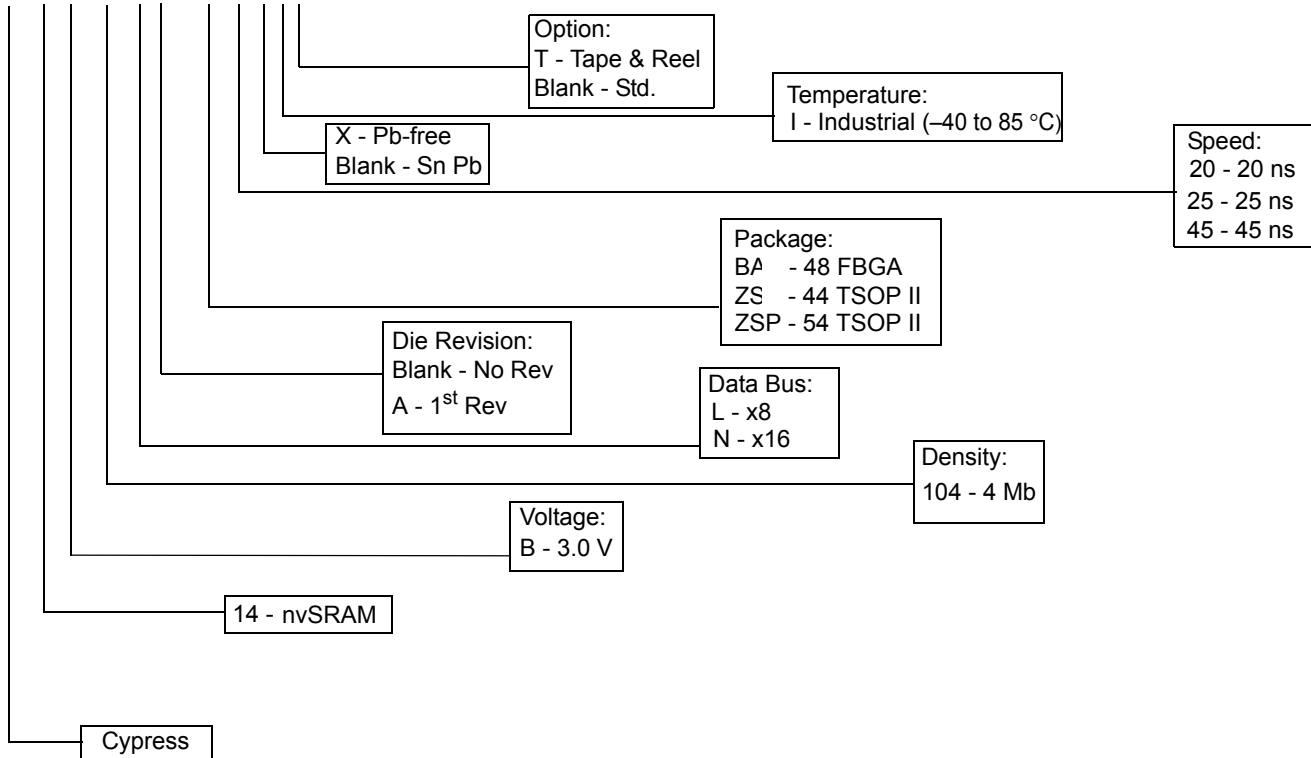
Package Diagrams

Figure 16. 44-Pin TSOP II (51-85087)

TOP VIEW

BOTTOM VIEW

EJECTOR MARK
(OPTIONAL)
CAN BE LOCATED
ANYWHERE IN THE
BOTTOM PKG

DIMENSION IN MM (INCH)
MAX
MIN.

51-85087 *C
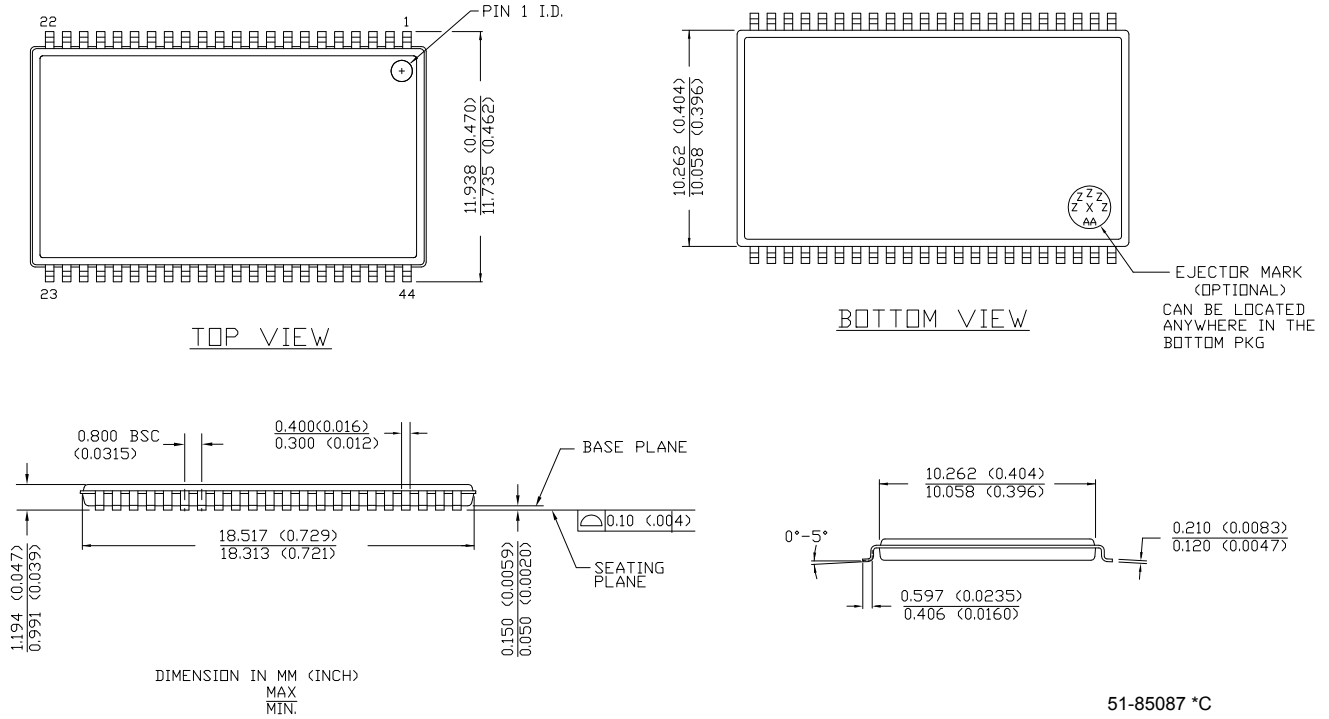
Package Diagrams (continued)

Figure 17. 48-Ball FBGA - 6 mm x 10 mm x 1.2 mm
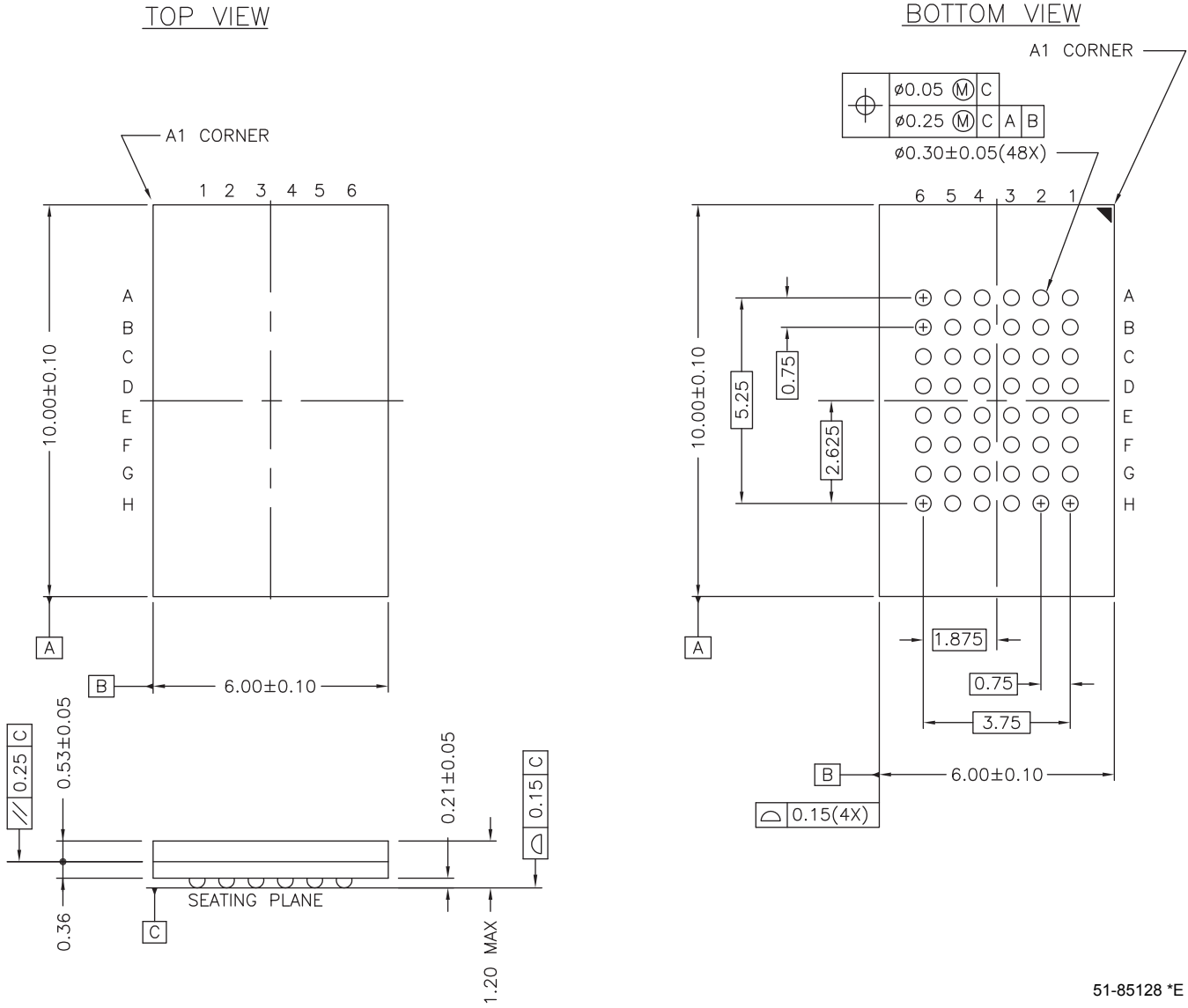
51-85128 *E

Package Diagrams (continued)

Figure 18. 54-Pin TSOP II (51-85160)
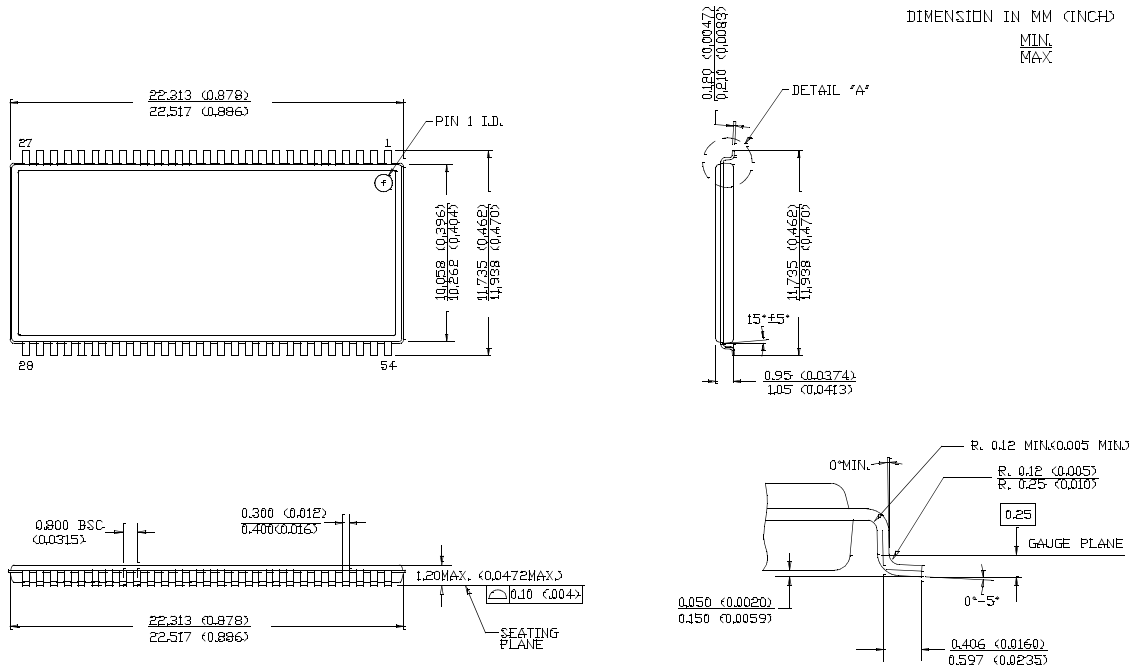
51-85160 *A

Acronyms

Acronym	Description
nvSRAM	nonvolatile static random access memory
TSOP II	thin small outline package
FBGA	fine-pitch ball grid array
RoHS	restriction of hazardous substances
I/O	input/output
CMOS	complementary metal oxide semiconductor
EIA	electronic industries alliance
RWI	read and write inhibited

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees celsius
Hz	hertz
kbit	1024 bits
kHz	kilohertz
KΩ	kilo ohms
μA	microamperes
mA	milliampere
μF	microfarads
MHz	megahertz
μs	microseconds
ms	millisecond
ns	nanoseconds
pF	picofarads
V	volts
Ω	ohms
W	watts

Document History Page

Document Title: CY14B104LA, CY14B104NA 4-Mbit (512 K × 8/256 K × 16) nvSRAM **Document Number: 001-49918**				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2606696	GVCH/PYRS	11/13/08	New Datasheet
*A	2672700	GVCH/PYRS	03/12/09	Added best practices Added CY14B104NA-BA25I part number Added footnote12 for HZ/LZ parameters
*B	2710274	GVCH/AESA	05/22/09	Moved datasheet status from Preliminary to Final Updated AutoStore operation Updated I_{SB} test condition Updated footnote 9 Referenced footnote 12 to V_{CCRISE}, t_{HHHD} and t_{LZHSB} parameters Updated V_{HDIS} parameter description Updated figure 12
*C	2738586	GVCH	07/15/09	Page 4: Updated Hardware STORE Operation description Page 5: Updated Software STORE description Updated t_{DELAY} parameter description Updated footnote 20 Added footnote 25 referenced footnote 25 to figure 12 and figure 13
*D	2758397	GVCH/AESA	09/01/09	Removed commercial temperature related specifications
*E	2773362	GVCH	10/06/09	Ordering Information: Added 20 ns part in a 48-FBGA package
*F	2826364	GVCH/PYRS	12/11/09	Changed STORE cycles to QuantumTrap from 200K to 1 Million
*G	2923475	GVCH/AESA	04/27/2010	Table 1: Added more clarity on HSB pin operation Hardware STORE Operation: Added more clarity on HSB pin operation Table 2: Added more clarity on BHE/BLE pin opeartion Updated HSB pin operation in Figure 11 Updated footnote 22 Updated Package Diagrams and Sales, Solutions, and Legal Information.
*H	3132368	GVCH	01/10/2011	48-ball FBGA package: 16 Mb address expansion is not supported Updated input capacitance for BHE and BLE pin Updated input and output capacitance for HSB pin Fixed typo in Figure 11 Added Acronyms table and Document Conventions table.

[+] Feedback

Sales, Solutions, and Legal Information

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[+] Feedback