TDA9884

I²C-bus controlled multistandard alignment-free IF-PLL for mobile reception

Rev. 02 — 12 May 2006 Product data sheet

1. General description

The TDA9884 is an alignment-free multistandard (PAL, SECAM and NTSC) vision and sound IF signal PLL demodulator for positive and negative modulation, including sound AM and FM processing.

The device is specially prepared for mobile TV applications.

2. Features

- 5 V supply voltage
- Gain controlled wide-band VIF amplifier, AC-coupled
- Multistandard true synchronous demodulation with active carrier regeneration: very linear demodulation, good intermodulation figures, reduced harmonics, and excellent pulse response
- Gated phase detector for L and L-accent standard
- Fully integrated VIF VCO, alignment-free, frequencies switchable for all negative and positive modulated standards via I²C-bus
- Digital acquisition help, VIF frequencies of 33.4 MHz, 33.9 MHz, 38.0 MHz, 38.9 MHz, 45.75 MHz and 58.75 MHz
- 4 MHz reference frequency input: signal from PLL tuning system or operating as crystal oscillator
- VIF AGC detector for gain control, operating as peak sync detector for negative modulated signals and as a peak white detector for positive modulated signals
- Mobile mode for negative modulation AGC (VIF and SIF) provides very fast reaction time
- External AGC setting via pin AGCSW; VIF-AGC and SIF-AGC monitor outputs
- Precise fully digital AFC detector with 4-bit digital-to-analog converter; AFC bits readable via I²C-bus
- TOP adjustable via I²C-bus or alternatively with potentiometer
- Fully integrated sound carrier trap for 4.5 MHz, 5.5 MHz, 6.0 MHz and 6.5 MHz; controlled by FM-PLL oscillator
- SIF input for single reference QSS mode; PLL controlled
- True split sound mode for sound demodulation at low RF level
- SIF-AGC for gain controlled SIF amplifier, single reference QSS mixer able to operate in high performance single reference QSS mode and in intercarrier mode, switchable via I²C-bus
- AM demodulator without extra reference circuit
- Alignment-free selective FM-PLL demodulator with high linearity and low noise

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- Four selectable I²C-bus addresses
- I²C-bus control for all functions
- I²C-bus transceiver with pin programmable MAD

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_P	supply voltage		[1][2]	4.5	5.0	5.5	V
I_P	supply current			52	63	70	mA
Video part							
$V_{i(VIF)(rms)}$	VIF input voltage sensitivity (RMS value)	–1 dB video at output		-	60	100	µV
$G_{VIF(cr)}$	VIF gain control range	see Figure 10		60	66	-	dB
f_{VIF}	vision carrier operating frequencies	see Table 19		-	33.4	-	MHz
				-	33.9	-	MHz
				-	38.0	-	MHz
				-	38.9	-	MHz
				-	45.75	-	MHz
				-	58.75	-	MHz
Δf_{VIF}	VIF frequency window of digital acquisition help	related to f_{VIF}; see Figure 7		-	±2.3	-	MHz
$V_{o(v)(p-p)}$	video output voltage (peak-to-peak value)	see Figure 9					
		normal mode (sound carrier trap active) and sound carrier on		1.7	2.0	2.3	V
		trap bypass mode and sound carrier off		0.95	1.10	1.25	V
G_{dif}	differential gain	*"ITU-T J.63 line 330"*	[3]				
		B/G standard		-	-	5	%
		L standard		-	-	7	%
φ_{dif}	differential phase	*"ITU-T J.63 line 330"*		-	2	4	deg
$B_{v(-1dB)}$	–1 dB video bandwidth	trap bypass mode and sound carrier off; AC load; C_L < 20 pF; R_L > 1 kΩ		5	6	-	MHz
$B_{v(-3dB)(trap)}$	–3 dB video bandwidth including sound carrier trap	f_{trap} = 4.5 MHz	[4]	3.95	4.05	-	MHz
		f_{trap} = 5.5 MHz	[4]	4.90	5.00	-	MHz
		f_{trap} = 6.0 MHz	[4]	5.40	5.50	-	MHz
		f_{trap} = 6.5 MHz	[4]	5.50	5.95	-	MHz
α_{SC1}	attenuation at first sound carrier	M/N standard; f = 4.5 MHz		30	36	-	dB
		B/G standard; f = 5.5 MHz		30	36	-	dB
S/N_W	weighted signal-to-noise ratio	see Figure 5	[5]	56	59	-	dB
$PSRR_{CVBS}$	power supply ripple rejection at pin CVBS	f_{ripple} = 70 Hz; video signal; grey level; positive and negative modulation; see Figure 8		20	25	-	dB

Table 1. Quick reference data *…continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
AFC_{stps}	AFC control steepness	definition: $\Delta I_{AFC}/\Delta f_{VIF}$		0.85	1.05	1.25	µA/kHz
Audio part							
$V_{o(AF)(rms)}$	AF output voltage (RMS value)	27 kHz FM deviation; 50 µs de-emphasis		430	540	650	mV
THD	total harmonic distortion	FM: 27 kHz FM deviation; 50 µs de-emphasis		-	0.15	0.50	%
		AM: m = 54 %		-	0.5	1.0	%
$B_{AF(-3dB)}$	–3 dB AF bandwidth	without de-emphasis; measured with FM-PLL filter in Figure 23		80	100	-	kHz
$S/N_{W(AF)}$	weighted signal-to-noise ratio of audio signal	FM-PLL only: 27 kHz FM deviation; 50 µs de-emphasis		52	56	-	dB
		AM: in accordance with *"ITU-R BS.468-4"*		45	50	-	dB
$\alpha_{AM(sup)}$	AM suppression of FM demodulator	referenced to 27 kHz FM deviation; 50 µs de-emphasis; AM: f = 1 kHz; m = 54 %		40	46	-	dB
PSRR	power supply ripple rejection	f_{ripple} = 70 Hz; see Figure 8					
		for FM		14	20	-	dB
		for AM		20	26	-	dB
$V_{o(intc)(rms)}$	IF intercarrier output level (RMS value)	QSS mode; SC_1; SC_2 off		90	140	180	mV
		L standard; without modulation		90	140	180	mV
		intercarrier mode; PC/SC_1 = 20 dB; SC_2 off	[6]	-	75	-	mV
Reference frequency input (pin REF)							
f_{ref}	reference signal frequency		[7]	-	4	-	MHz
$V_{ref(rms)}$	reference signal voltage (RMS value)	operation as input terminal		80	-	400	mV

[1] Values of video and sound parameters can be decreased at V_P = 4.5 V.

[2] For applications without I²C-bus, the time constant (R × C) at the supply must be > 1.2 µs (e.g. 1 Ω and 2.2 µF).

[3] Condition: luminance range (5 steps) from 0 % to 100 %.

[4] AC load: C_L < 20 pF and R_L > 1 kΩ. The sound carrier frequencies (depending on the TV standard) are attenuated by the integrated sound carrier traps (see Figure 16 to Figure 21; $|H(s)|$ is the absolute value of transfer function).

[5] Measurement using unified weighting filter ("*ITU-T J.61*"), 200 kHz high-pass filter, 5 MHz low-pass filter and subcarrier notch filter ("*ITU-T J.64*").

[6] The intercarrier output signal at pin SIOMAD can be calculated by the following formulae taking into account the internal video signal with 1.1 V (p-p) as a reference: $V_{o(intc)(rms)} = 1.1 \times \frac{1}{2\sqrt{2}} \times 10^{r}\ V$ and $r = \frac{1}{20} \times \left(\frac{V_{i(SC)}}{V_{i(PC)}}(dB) + 6\ dB \pm 3\ dB\right)$, where: $\frac{1}{2\sqrt{2}}$ is the correction term for RMS value, $\frac{V_{i(SC)}}{V_{i(PC)}}(dB)$ is the sound-to-picture carrier ratio at pins VIF1 and VIF2 in dB, 6 dB is the correction term of internal circuitry and ±3 dB is the tolerance of video output and intercarrier output $V_{o(intc)(rms)}$.

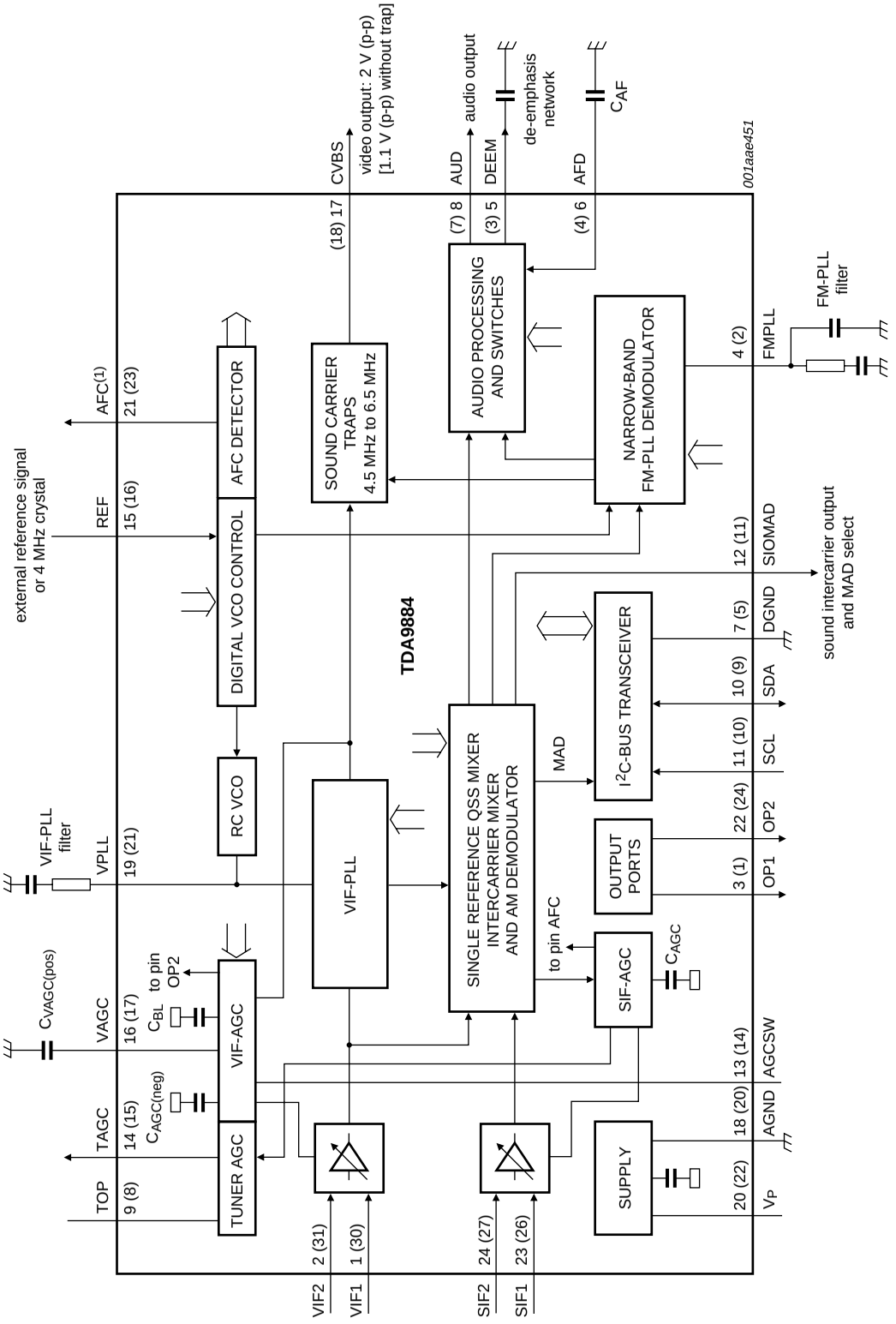
[7] Pin REF is able to operate as a 1-pin crystal oscillator input as well as an external reference signal input, e.g. from the tuning system.

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA9884TS	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
TDA9884HN	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-3

5. Block diagram



Pin numbers for TDA9884HN in parentheses.

(1) SIF-AGC monitor output at pin AFC.

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

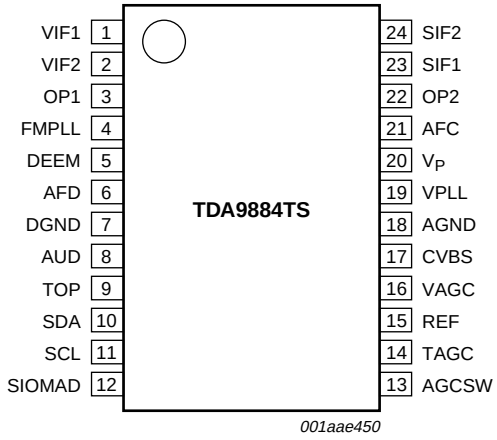


Fig 2. Pin configuration for SOT340-1 (SSOP24)

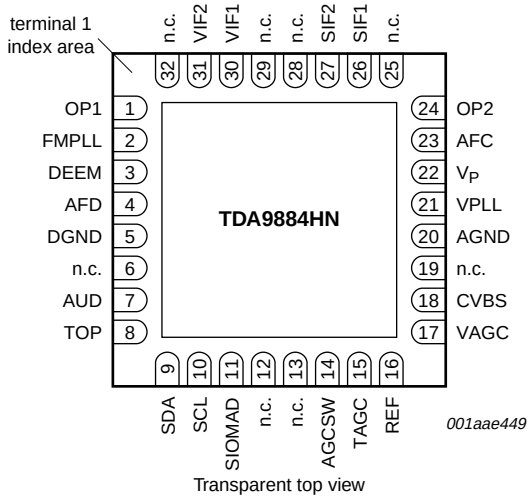


Fig 3. Pin configuration for SOT617-3 (HVQFN32)

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TDA9884TS	TDA9884HN	
VIF1	1	30	VIF differential input 1
VIF2	2	31	VIF differential input 2
n.c.	-	32	not connected
OP1	3	1	output port 1; open-collector

Table 3. Pin description *…continued*

Symbol	Pin		Description
	TDA9884TS	TDA9884HN	
FMPLL	4	2	FM-PLL for loop filter
DEEM	5	3	de-emphasis output for capacitor
AFD	6	4	AF decoupling input for capacitor
DGND	7	5	digital ground
n.c.	-	6	not connected
AUD	8	7	audio output
TOP	9	8	tuner AGC TakeOver Point (TOP) for resistor adjustment
SDA	10	9	I²C-bus data input and output
SCL	11	10	I²C-bus clock input
SIOMAD	12	11	sound intercarrier output and MAD select with resistor
n.c.	-	12	not connected
n.c.	-	13	not connected
AGCSW	13	14	fast external AGC enable switch
TAGC	14	15	tuner AGC output
REF	15	16	4 MHz crystal or reference signal input
VAGC	16	17	VIF-AGC capacitor for L standard
CVBS	17	18	composite video output
n.c.	-	19	not connected
AGND	18	20	analog ground
VPLL	19	21	VIF-PLL for loop filter
V_P	20	22	supply voltage
AFC	21	23	AFC output
OP2	22	24	output port 2; open-collector
n.c.	-	25	not connected
SIF1	23	26	SIF differential input 1 and MAD select with resistor
SIF2	24	27	SIF differential input 2 and MAD select with resistor
n.c.	-	28	not connected
n.c.	-	29	not connected

7. Functional description

Figure 1 shows the simplified block diagram of the device which comprises the following functional blocks:

- VIF amplifier
- Tuner AGC and VIF-AGC
- VIF-AGC detector

- FPLL detector
- VCO and divider
- AFC and digital acquisition help
- Video demodulator and amplifier
- Sound carrier trap
- SIF amplifier
- SIF-AGC detector
- Single reference QSS mixer
- AM demodulator
- FM demodulator and acquisition help
- Audio amplifier and mute time constant
- Internal voltage stabilizer
- I²C-bus transceiver and MAD

7.1 VIF amplifier

The VIF amplifier consists of three AC-coupled differential stages. Gain control is performed by emitter degeneration. The total gain control range is typically 66 dB. The differential input impedance is typically 2 kΩ in parallel with 3 pF.

7.2 Tuner AGC and VIF-AGC

This block adapts the voltages, generated at the VIF-AGC and SIF-AGC detectors, to the internal signal processing at the VIF and SIF amplifiers and performs the tuner AGC control current generation. Normally it is derived from the VIF-AGC, for the true split sound mode it is derived from the SIF-AGC. The onset of the tuner AGC control current generation can be set either via the I²C-bus (see Table 16) or optionally by a potentiometer at pin TOP (in case that the I²C-bus information cannot be stored). The presence of a potentiometer is automatically detected and the I²C-bus setting is disabled.

Furthermore, derived from the AGC detector voltage, a comparator is used to test if the corresponding VIF input voltage is higher than 200 μV. This information can be read out via the I²C-bus (bit VIFLEV = 1).

7.3 VIF-AGC detector

Gain control is performed by sync level detection (negative modulation) or peak white detection (positive modulation).

For negative modulation, the sync level voltage is compared with a reference voltage (nominal sync level) by a comparator which charges or discharges the integrated AGC capacitor directly for the generation of the required VIF gain. With mobile mode the currents are increased by a factor of approximately 8 for very fast reaction. By use of an AGC event detector, the gain increase time constant (discharge current) additionally reduces in with a too-low VIF signal.

For positive modulation, the white peak level voltage is compared with a reference voltage (nominal white level) by a comparator which charges (fast) or discharges (slow) the external AGC capacitor directly for the generation of the required VIF gain. The need of a

very long time constant for VIF gain increase is because the peak white level may appear only once in a field. In order to reduce this time constant, an additional level detector increases the discharging current of the AGC capacitor (fast mode) in the event of a decreasing VIF amplitude step controlled by the detected actual black level voltage. The threshold level for fast mode AGC is typically −6 dB video amplitude. The fast mode state is also transferred to the SIF-AGC detector for speed-up. In case of missing peak white pulses, the VIF gain increase is limited to typically +3 dB by comparing the detected actual black level voltage with a corresponding reference voltage.

7.4 FPLL detector

The VIF amplifier output signal is fed into a frequency detector and into a phase detector via a limiting amplifier for removing the video AM.

During acquisition the frequency detector produces a current proportional to the frequency difference between the VIF and the VCO signals. After frequency lock-in the phase detector produces a current proportional to the phase difference between the VIF and the VCO signals. The currents from the frequency and phase detectors are charged into the loop filter which controls the VIF VCO and locks it to the frequency and phase of the VIF carrier.

For a positive modulated VIF signal, the charging currents are gated by the composite sync in order to avoid signal distortion in case of overmodulation. The gating depth is switchable via the I²C-bus.

7.5 VCO and divider

The VCO of the VIF-FPLL operates as an integrated low radiation relaxation oscillator at double the picture carrier frequency. The control voltage, required to tune the VCO to double the picture carrier frequency, is generated at the loop filter by the frequency phase detector. The possible frequency range is 50 MHz to 140 MHz (typical value).

The oscillator frequency is divided-by-two to provide two differential square wave signals with exactly 90 degrees phase difference, independent of the frequency, for use in the FPLL detectors, the video demodulator and the intercarrier mixer.

7.6 AFC and digital acquisition help

Each relaxation oscillator of the VIF-PLL and FM-PLL demodulator has a wide frequency range. To prevent false locking of the PLLs and with respect to the catching range, the digital acquisition help provides an individual control, until the frequency of the VCO is within the preselected standard dependent lock-in window of the PLL.

The in-window and out-window control at the FM-PLL is additionally used to mute the audio stage (if auto mute is selected via the I²C-bus).

The working principle of the digital acquisition help is as follows. The PLL VCO output is connected to a down counter which has a predefined start value (standard dependent). The VCO frequency clocks the down counter for a fixed gate time. Thereafter, the down counter stop value is analyzed. In case the stop value is higher (lower) than the expected value range, the VCO frequency is lower (higher) than the wanted lock-in window frequency range. A positive (negative) control current is injected into the PLL loop filter and consequently the VCO frequency is increased (decreased) and a new counting cycle starts.

The gate time as well as the control logic of the acquisition help circuit is dependent on the precision of the reference signal at pin REF. Operation as a crystal oscillator is possible as well as connecting this input via a serial capacitor to an external reference frequency, e.g. the tuning system oscillator.

The AFC signal is derived from the corresponding down counter stop value after a counting cycle. The last four bits are latched and can be read out via the I²C-bus (see Table 10). Also the digital-to-analog converted value is given as current at pin AFC.

7.7 Video demodulator and amplifier

The video demodulator is realized by a multiplier which is designed for low distortion and large bandwidth. The VIF signal is multiplied with the 'in phase' signal of the VIF-PLL VCO.

The demodulator output signal is fed into the video preamplifier via a level shift stage with integrated low-pass filter to achieve carrier harmonics attenuation.

The output signal of the preamplifier is fed to the VIF-AGC detector (see Section 7.3) and in the sound trap mode also fed internally to the integrated sound carrier trap (see Section 7.8). The differential trap output signal is converted and amplified by the following post-amplifier. The video output level at pin CVBS is 2 V (p-p).

In the bypass mode the output signal of the preamplifier is fed directly through the post-amplifier to pin CVBS. The output video level is 1.1 V (p-p) for using an external sound trap with 10 % overall loss.

Noise clipping is provided in both cases.

7.8 Sound carrier trap

The sound carrier trap consists of a reference filter, a phase detector and the sound trap itself.

A sound carrier reference signal is fed into the reference low-pass filter and is shifted by nominal 90 degrees. The phase detector compares the original reference signal with the signal shifted by the reference filter and produces a DC voltage by charging or discharging an integrated capacitor with a current proportional to the phase difference between both signals, respectively to the frequency error of the integrated filters. The DC voltage controls the frequency position of the reference filter and the sound trap. So the accurate frequency position for the different standards is set by the sound carrier reference signal.

The sound trap itself is constructed of three separate traps to realize sufficient suppression of the first and second sound carriers.

7.9 SIF amplifier

The SIF amplifier consists of three AC-coupled differential stages. Gain control is performed by emitter degeneration. The total gain control range is typically 66 dB. The differential input impedance is typically 2 kΩ in parallel with 3 pF.

7.10 SIF-AGC detector

SIF gain control is performed by the detection of the DC component of the AM demodulator output signal. This DC signal corresponds directly to the SIF voltage at the output of the SIF amplifier so that a constant SIF signal is supplied to the AM demodulator and to the single reference QSS mixer.

By switching the gain of the input amplifier of the SIF-AGC detector via the I²C-bus, the internal SIF level for FM sound is 5.5 dB lower than for AM sound. This is to adapt the SIF-AGC characteristic to the VIF-AGC characteristic. The adaption is ideal for a picture-to-sound FM carrier ratio of 13 dB.

Via a comparator, the integrated AGC capacitor is charged or discharged for the generation of the required SIF gain. Due to AM sound, the AGC reaction time is slow (f_c < 20 Hz for the closed AGC loop). For reducing this AM sound time constant in the event of a decreasing IF amplitude step, the charging and discharging currents of the AGC capacitor are increased by a factor of 12 (fast mode) when the VIF-AGC detector (at positive modulation mode) operates in the fast mode too. An additional circuit (threshold approximately 7 dB) ensures a very fast gain reduction for a large increasing IF amplitude step.

For negative modulation and QSS mode the AGC also is set to fast mode. For negative modulation and mobile mode the currents are increased additionally by a factor of 36.

7.11 Single reference QSS mixer

With the present system a high performance Hi-Fi stereo sound processing can be achieved. For a simplified application without a SIF SAW filter, the single reference QSS mixer can be switched to the intercarrier mode via the I²C-bus.

The single reference QSS mixer generates the 2nd FM TV sound intercarrier signal. It is realized by a linear multiplier which multiplies the SIF amplifier output signal and the VIF-PLL VCO signal (90 degrees output) which is locked to the picture carrier. In this way the QSS mixer operates as a quadrature mixer in the intercarrier mode and provides suppression of the low frequency video signals.

In the true split sound mode the VIF-PLL VCO is locked by a synthesizer. By this the 2nd FM TV sound intercarrier signal is generated independently from the vision carrier so that in the case of a low RF level, the sound demodulation is possible where the VIF-PLL would unlock. In the true split sound mode the VIF demodulation is not available.

The QSS mixer output signal is fed internally via a high-pass and low-pass combination to the FM demodulator as well as via an operational amplifier to the intercarrier output pin SIOMAD.

7.12 AM demodulator

The amplitude modulated SIF amplifier output signal is fed both to a two-stage limiting amplifier that removes the AM and to a linear multiplier. The result of the multiplication of the SIF signal with the limiter output signal is AM demodulation (passive synchronous demodulator). The demodulator output signal is fed via a low-pass filter that attenuates the carrier harmonics and via the input amplifier of the SIF-AGC detector to the audio amplifier.

7.13 FM demodulator and acquisition help

The narrow-band FM-PLL detector consists of:

- Gain controlled FM amplifier and AGC detector
- Narrow-band PLL

The intercarrier signal from the intercarrier mixer is fed to the input of an AC-coupled gain controlled amplifier with two stages. The gain controlled output signal is fed to the phase detector of the narrow-band FM-PLL (FM demodulator). For good selectivity and robustness against disturbance caused by the video signal, a high linearity of the gain controlled FM amplifier and of the phase detector as well as a constant signal level are required. The gain control is done by means of an 'in phase' demodulator for the FM carrier (from the output of the FM amplifier). The demodulation output is fed into a comparator for charging or discharging the integrated AGC capacitor. This leads to a mean value AGC loop to control the gain of the FM amplifier.

The FM demodulator is realized as a narrow-band PLL with an external loop filter, which provides the necessary selectivity (bandwidth approximately 100 kHz). To achieve good selectivity, a linear phase detector and a constant input level are required. The gain controlled intercarrier signal from the FM amplifier is fed to the phase detector. The phase detector controls via the loop filter the integrated low radiation relaxation oscillator. The designed frequency range is from 4 MHz to 7 MHz.

The VCO within the FM-PLL is phase-locked to the incoming 2nd SIF signal, which is frequency modulated. As well as this, the VCO control voltage is superimposed by the AF voltage. Therefore, the VCO tracks with the FM of the 2nd SIF signal. So, the AF voltage is present at the loop filter and is typically 5 mV (RMS) for 27 kHz FM deviation. This AF signal is fed via a buffer to the audio amplifier.

The correct locking of the PLL is supported by the digital acquisition help circuit (see Section 7.6).

7.14 Audio amplifier and mute time constant

The audio amplifier consists of two parts:

- AF preamplifier
- AF output amplifier

The AF preamplifier used for FM sound is an operational amplifier with internal feedback, high gain and high common mode rejection. The AF voltage from the PLL demodulator is 5 mV (RMS) for a frequency deviation of 27 kHz and is amplified by 30 dB. By the use of a DC operating point control circuit (with external capacitor C_{AF}), the AF preamplifier is decoupled from the PLL DC voltage. The low-pass characteristic of the amplifier reduces the harmonics of the sound intercarrier signal at the AF output terminal.

For FM sound a switchable de-emphasis network (with external capacitor) is implemented between the preamplifier and the output amplifier.

The AF output amplifier provides the required AF output level by a rail-to-rail output stage. A preceding stage makes use of an input selector for switching between FM sound, AM sound and mute state. The gain can be switched between 10 dB (normal) and 4 dB (reduced).

Switching to the mute state is controlled automatically, dependent on the digital acquisition help in case the VCO of the FM-PLL is not in the required frequency window. This is done by a time constant: fast for switching to the mute state and slow (typically 40 ms) for switching to the no-mute state.

All switching functions are controlled via the I²C-bus:

- AM sound, FM sound and forced mute
- Auto mute enable or disable
- De-emphasis off or on with 50 µs or 75 µs
- Audio gain normal or reduced

7.15 Internal voltage stabilizer

The band gap circuit internally generates a voltage of approximately 2.4 V, independent of supply voltage and temperature. A voltage regulator circuit, connected to this voltage, produces a constant voltage of 3.55 V which is used as an internal reference voltage.

7.16 I²C-bus transceiver and module address

The device can be controlled via the 2-wire I²C-bus by a microcontroller. Two wires carry serial data (SDA) and serial clock (SCL) information between the devices connected to the I²C-bus.

The device has an I²C-bus slave transceiver with auto-increment. The circuit operates up to clock frequencies of 400 kHz.

A slave address is sent from the master to the slave receiver. To avoid conflicts in a real application with other devices providing similar or complementing functions, there are four possible slave addresses available. These Module Addresses (MADs) can be selected by connecting resistors on pin SIOMAD and/or pins SIF1 and SIF2 (see Figure 23). Pin SIOMAD relates to bit A0 and pins SIF1 and SIF2 relate to bit A3. The slave addresses of this device are given in Table 4.

The power-on preset value is dependent on the use of pin SIOMAD and can be chosen for 45.75 MHz NTSC as default (pin SIOMAD left open-circuit) or 58.75 MHz NTSC (resistor on pin SIOMAD). In this way the device can be used without the I²C-bus as an NTSC only device.

Remark: In case of using the device without the I²C-bus, then the rise time of the supply voltage after switching on power must be longer than 1.2 µs.

Table 4. Slave address detection

Slave address	Selectable address bit		Resistor on pin	
	A3	A0	SIF1 and SIF2	SIOMAD
MAD1	0	1	no	no
MAD2	0	0	no	yes
MAD3	1	1	yes	no
MAD4	1	0	yes	yes

8. I²C-bus control

8.1 Read format

Table 5. I²C-bus read format (slave transmits data)

S	Byte 1								A	Byte 2								AN	P
	A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$		D7	D6	D5	D4	D3	D2	D1	D0		
	slave address							1		data									

Table 6. Explanation of Table 5

Symbol	Function
S	START condition, generated by the master
Slave address	see Table 7
R/$\overline{W}$ = 1	read command, generated by the master
A	acknowledge bit, generated by the slave
Data	8-bit data word, transmitted by the slave, see Table 8
AN	acknowledge-not bit, generated by the master
P	STOP condition, generated by the master

The master generates an acknowledge when it has received the dataword READ. The master next generates an acknowledge, then slave begins transmitting the dataword READ, and so on until the master generates an acknowledge-not bit and transmits a STOP condition.

8.1.1 Slave address

The first module address MAD1 is the standard address, see Table 4.

Table 7. Slave addresses[1][2]

Symbol	Value (hex)	Bit						
		A6	A5	A4	A3	A2	A1	A0
MAD1	43	1	0	0	0	0	1	1
MAD2	42	1	0	0	0	0	1	0
MAD3	4B	1	0	0	1	0	1	1
MAD4	4A	1	0	0	1	0	1	0

[1] For MAD activation via external resistor: see Table 4 and Figure 23.

[2] For applications without I²C-bus: see Table 21 and Table 22.

8.1.2 Data byte

Table 8. Data read register (status register)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
AFCWIN	VIFLEV	CARRDET	AFC4	AFC3	AFC2	AFC1	PONR

Table 9. Description of status register bits

Symbol	Value	Description
AFCWIN		**AFC window**
	1	VCO in ±1.6 MHz AFC window[1]
	0	VCO out of ±1.6 MHz AFC window
VIFLEV		**VIF input level**
	1	high level; VIF input voltage ≥ 200 μV (typically)
	0	low level
CARRDET		**FM carrier detection**
	1	detection
	0	no detection
AFC[4:1]		**automatic frequency control**
		see Table 10
PONR		**power-on reset**
	1	after power-on reset or after supply breakdown
	0	after a successful reading of the status register

[1] If no IF input is applied, then bit AFCWIN = 1 due to the fact that the VCO is forced to the AFC window border for fast lock-in behavior.

Table 10. Automatic frequency control bits[1]

Bit				f_{VIF}
AFC4	**AFC3**	**AFC2**	**AFC1**	
0	1	1	1	≤ (f_0 – 187.5 kHz)
0	1	1	0	f_0 – 162.5 kHz
0	1	0	1	f_0 – 137.5 kHz
0	1	0	0	f_0 – 112.5 kHz
0	0	1	1	f_0 – 87.5 kHz
0	0	1	0	f_0 – 62.5 kHz
0	0	0	1	f_0 – 37.5 kHz
0	0	0	0	f_0 – 12.5 kHz
1	1	1	1	f_0 + 12.5 kHz
1	1	1	0	f_0 + 37.5 kHz
1	1	0	1	f_0 + 62.5 kHz
1	1	0	0	f_0 + 87.5 kHz
1	0	1	1	f_0 + 112.5 kHz
1	0	1	0	f_0 + 137.5 kHz
1	0	0	1	f_0 + 162.5 kHz
1	0	0	0	≥ (f_0 + 187.5 kHz)

[1] f_0 is the nominal frequency of f_{VIF}.

8.2 Write format

Table 11. I²C-bus write format (slave receive data)[1]

S	Byte 1		A	Byte 2	A	Byte 3	A	Byte n	A	P
	A6 to A0	R/$\overline{W}$		A7 to A0		bits 7 to 0		bits 7 to 0		
	slave address	0		subaddress		data 1		data 1		

[1] The auto-increment of the subaddress stops if the subaddress is 3.

Table 12. Explanation of Table 11

Symbol	Function
S	START condition, generated by the master
Slave address	see Table 7
R/$\overline{W}$ = 0	write command, generated by the master
A	acknowledge bit, generated by the slave
Subaddress (SAD)	see Table 13
Data 1, data n	8-bit data words, transmitted by the master (see Table 14, Table 15 and Table 17)
P	STOP condition

8.2.1 Subaddress

If more than one data byte is transmitted, then auto-increment is performed: starting from the transmitted subaddress and auto-increment of subaddress in accordance with the order of Table 13.

Table 13. Definition of the subaddress (second byte after slave address)[1]

Register	MSB							LSB
	A7[2]	A6[3]	A5[3]	A4[3]	A3[3]	A2[3]	A1	A0
SAD for switching mode	0	X	X	X	X	X	0	0
SAD for adjust mode	0	X	X	X	X	X	0	1
SAD for data mode	0	X	X	X	X	X	1	0

[1] X = don't care.

[2] Bit A7 = 1 is not allowed.

[3] Bits A6 to A2 will be ignored by the internal hardware.

8.2.2 Data byte for switching mode

Table 14. Bit description of SAD register for switching mode (SAD = 00)

Bit	Value	Description
B7		**output port 2 e.g. for SAW switching or AGC monitoring**
	1	high-impedance, disabled or HIGH
	0	low-impedance, active or LOW
B6		**output port 1 e.g. for SAW switching or external AGC input**
	1	high-impedance, disabled or HIGH
	0	low-impedance, active or LOW

Table 14. Bit description of SAD register for switching mode (SAD = 00) *…continued*

Bit	Value	Description
B5		**forced audio mute**
	0	on
	1	off
B4 and B3		**TV standard modulation and mobile mode**
	00	positive AM TV[1]
	01	positive AM TV[1][2]
	10	negative FM TV
	11	negative TV mobile mode[2][3]
B2		**carrier mode**
	1	QSS mode
	0	intercarrier mode
B1		**auto mute of FM AF output**
	1	active
	0	inactive
B0		**video mode (sound trap)**
	1	sound trap bypass
	0	sound trap active

[1] For positive AM TV choose 6.5 MHz for the second SIF.

[2] SIF-AGC monitor output at pin AFC.

[3] AGC (VIF/SIF) provides very fast reaction time.

8.2.3 Data byte for adjust mode

Table 15. Bit description of SAD register for adjust mode (SAD = 01)

Bit	Value	Description
C7		**audio gain**
	1	–6 dB
	0	0 dB
C6		**de-emphasis time constant**
	1	50 µs
	0	75 µs
C5		**de-emphasis**
	1	on
	0	off
C4 to C0		**tuner takeover point adjustment**
		see Table 16

Table 16. Tuner takeover point adjustment bits

Bit					Top adjustment (dB)
C4	C3	C2	C1	C0	
1	1	1	1	1	+15
1	1	1	1	0	+14
1	1	1	0	1	+13
1	1	1	0	0	+12
1	1	0	1	1	+11
1	1	0	1	0	+10
1	1	0	0	1	+9
1	1	0	0	0	+8
1	0	1	1	1	+7
1	0	1	1	0	+6
1	0	1	0	1	+5
1	0	1	0	0	+4
1	0	0	1	1	+3
1	0	0	1	0	+2
1	0	0	0	1	+1
1	0	0	0	0	0[1]
0	1	1	1	1	−1
0	1	1	1	0	−2
0	1	1	0	1	−3
0	1	1	0	0	−4
0	1	0	1	1	−5
0	1	0	1	0	−6
0	1	0	0	1	−7
0	1	0	0	0	−8
0	0	1	1	1	−9
0	0	1	1	0	−10
0	0	1	0	1	−11
0	0	1	0	0	−12
0	0	0	1	1	−13
0	0	0	1	0	−14
0	0	0	0	1	−15
0	0	0	0	0	−16

[1] 0 dB is equal to 17 mV (RMS).

8.2.4 Data byte for data mode

Table 17. Bit description of SAD register for data mode (SAD = 10)

Bit	Value	Description
E7		**VIF-AGC features**
		dependent on bit E5; see Table 18
E6		**L standard PLL gating**
	1	gating in case of 36 % positive modulation (B4 = 0)
	0	gating in case of 0 % positive modulation (B4 = 0)
	1	optimum for multipath condition (B4 = 1)
	0	optimum for overmodulation condition (B4 = 1)
E5		**VIF, SIF and tuner minimum gain**
		dependent on bit E7; see Table 18
E4 to E2		**vision intermediate frequency selection**
		see Table 19 and Table 20
E1 and E0		**sound intercarrier frequency selection (sound 2nd IF);** only valid for setting of bit E4 to bit E2 according to Table 19
	00	f_{FM} = 4.5 MHz
	01	f_{FM} = 5.5 MHz
	10	f_{FM} = 6.0 MHz
	11	f_{FM} = 6.5 MHz (for positive modulation choose 6.5 MHz)

Table 18. Options

Function	Bit E7 = 0		Bit E7 = 1	
	Bit E5 = 0	Bit E5 = 1	Bit E5 = 0	Bit E5 = 1
Pin OP1	port function	port function	port function	VIF-AGC external input[1][2][3]
Pin OP2	port function	port function	VIF-AGC output[1][2][3]	VIF-AGC output[1][2][3]
Gain	normal gain	minimum gain	normal gain	external gain

[1] The corresponding port function has to be disabled (set to 'high-impedance'); see Table 14.

[2] If selected by the I²C-bus, the VIF-AGC voltage can be monitored at pin OP2. In this case, OP2 cannot be used for the normal port function.

[3] If selected by the I²C-bus, pin OP1 can alternatively be used for external AGC control, activated by pin AGCSW. In this case, OP1 cannot be used for the normal port function.

Table 19. TV standard selection for VIF

Video IF select bits			f_{VIF} (MHz)
E4	E3	E2	
0	0	0	58.75[1]
0	0	1	45.75[1]
0	1	0	38.9
0	1	1	38.0
1	0	0	33.9
1	0	1	33.4

[1] Pin SIOMAD can be used for the selection of the different NTSC standards without I²C-bus. With a resistor on pin SIOMAD, f_{VIF} = 58.75 MHz; without a resistor on pin SIOMAD, f_{VIF} = 45.75 MHz (NTSC-M).

Table 20. True split sound mode

TV standard	Bit					Function	
	E4	E3	E2	E1	E0	f_{synth} (MHz)	Sound 2nd IF f_{FM} (MHz)
M/N	1	1	1	0	1	40	5.6
B/G	1	1	1	1	1	40	6.6
I	1	1	0	0	0	36	3.1
D/K	1	1	0	1	0	36	3.6

Table 21. Data setting after power-on reset (default setting with a resistor on pin SIOMAD)

Register	MSB							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Switching mode	1	1	0	1	0	1	1	0
Adjust mode	0	0	1	1	0	0	0	0
Data mode	0	0	0	0	0	0	0	0

Table 22. Data setting after power-on reset (default setting without a resistor on pin SIOMAD)

Register	MSB							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Switching mode	1	1	0	1	0	1	1	0
Adjust mode	0	0	1	1	0	0	0	0
Data mode	0	0	0	0	0	1	0	0

For selection of the different NTSC standards without I²C-bus, an application on pin SIOMAD is used (see Figure 23). Without a resistor, NTSC-M is selected (f_{VIF} = 45.75 MHz); with a resistor, the VIF frequency is 58.75 MHz (see Table 19).

9. Limiting values

Table 23. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_P	supply voltage			-	5.5	V
V_n	voltage on					
	pins VIF1, VIF2, OP1, FMPLL, AGCSW, V_P, AFC, OP2, SIF1 and SIF2			0	V_P	V
	pin TAGC			0	8.8	V
t_{sc}	short-circuit time to ground or V_P			-	10	s
T_{stg}	storage temperature			–25	+150	°C
T_{amb}	ambient temperature			–20	+70	°C
V_{esd}	electrostatic discharge voltage	machine model	[1]	–400	+400	V
		human body model	[2]	–4000	+4000	V

[1] Class C according to EIA/JESD22-A115-A.

[2] Class 3A according to JESD22-A114-B.

10. Thermal characteristics

Table 24. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient			
	TDA9884TS (SSOP24)	in free air	118	K/W
	TDA9884HN (HVQFN32)	in free air	40	K/W

11. Characteristics

Table 25. Characteristics

V_P = 5 V; T_{amb} = 25 °C; see Table 27 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC/SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 23; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply (pin V_P)							
V_P	supply voltage		[1][2]	4.5	5.0	5.5	V
I_P	supply current			52	63	70	mA
P_{tot}	total power dissipation			-	305	385	mW
Power-On Reset (POR)							
$V_{P(start)}$	supply voltage for start of reset	decreasing supply voltage		2.5	3.0	3.5	V
$V_{P(stop)}$	supply voltage for end of reset	increasing supply voltage; I²C-bus transmission enable		-	-	4.4	V
τ_P	time constant (R × C) for network at pin V_P	for applications without I²C-bus		1.2	-	-	µs
VIF amplifier (pins VIF1 and VIF2)							
$V_{i(VIF)(rms)}$	VIF input voltage sensitivity (RMS value)	−1 dB video at output		-	60	100	µV
$V_{i(max)(rms)}$	maximum input voltage (RMS value)	+1 dB video at output		150	190	-	mV
$V_{i(ovl)(rms)}$	overload input voltage (RMS value)		[3]	-	-	440	mV
$\Delta V_{IF(int)}$	internal IF amplitude difference between picture and sound carrier	within AGC range; Δf = 5.5 MHz		-	0.7	-	dB
$G_{VIF(cr)}$	VIF gain control range	see Figure 10		60	66	-	dB
$B_{VIF(-3dB)(ll)}$	lower limit −3 dB VIF bandwidth			-	15	-	MHz
$B_{VIF(-3dB)(ul)}$	upper limit −3 dB VIF bandwidth			-	80	-	MHz

Table 25. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 27 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC/SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 23; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{i(dif)}$	differential input resistance		[4]	-	2	-	kΩ
$C_{i(dif)}$	differential input capacitance		[4]	-	3	-	pF
V_I	DC input voltage			-	1.93	-	V
FPLL and true synchronous video demodulator [5]							
$f_{VCO(max)}$	maximum oscillator frequency for carrier regeneration	$f = 2f_{PC}$		120	140	-	MHz
f_{VIF}	vision carrier operating frequencies	see Table 19		-	33.4	-	MHz
				-	33.9	-	MHz
				-	38.0	-	MHz
				-	38.9	-	MHz
				-	45.75	-	MHz
				-	58.75	-	MHz
Δf_{VIF}	VIF frequency window of digital acquisition help	related to f_{VIF}; see Figure 7		-	±2.3	-	MHz
t_{acq}	acquisition time	BL = 70 kHz	[6]	-	-	30	ms
$V_{i(lock)(rms)}$	input voltage sensitivity for PLL to be locked (RMS value)	measured on pins VIF1 and VIF2; maximum IF gain		-	30	70	µV
$T_{cy(DAH)}$	cycle time of digital acquisition help			-	64	-	µs
$K_{O(VIF)}$	VIF VCO steepness	definition: $\Delta f_{VIF}/\Delta V_{VPLL}$		-	20	-	MHz/V
$K_{D(VIF)}$	VIF phase detector steepness	definition: $\Delta I_{VPLL}/\Delta\varphi_{VIF}$		-	23	-	µA/rad
Video output 2 V (pin CVBS)							
Normal mode (sound carrier trap active) and sound carrier on							
$V_{o(v)(p-p)}$	video output voltage (peak-to-peak value)	see Figure 9		1.7	2.0	2.3	V
ΔV_o	video output voltage difference	difference between L and B/G standard		–12	-	+12	%
V/S	ratio between video (black-to-white) and sync level			1.90	2.33	3.00	
V_{sync}	sync voltage level			1.0	1.2	1.4	V
$V_{clip(u)}$	upper video clipping voltage level			V_P – 1.1	V_P – 1	-	V
$V_{clip(l)}$	lower video clipping voltage level			-	0.7	0.9	V

Table 25. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 27 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC/SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 23; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_o	output resistance		[4]	-	-	30	Ω
$I_{bias(int)}$	internal DC bias current for emitter-follower			1.5	2.0	-	mA
$I_{o(sink)(max)}$	maximum AC and DC output sink current			1	-	-	mA
$I_{o(source)(max)}$	maximum AC and DC output source current			3.9	-	-	mA
$\Delta V_{o(CVBS)}$	deviation of CVBS output voltage	50 dB gain control		-	-	0.5	dB
		30 dB gain control		-	-	0.1	dB
$\Delta V_{o(bl)}$	black level tilt	negative modulation		-	-	1	%
$\Delta V_{o(bl)(v)}$	vertical black level tilt for worst case in L standard	vision carrier modulated by test line (VITS) only		-	-	3	%
G_{dif}	differential gain	*"ITU-T J.63 line 330"*	[7]				
		B/G standard		-	-	5	%
		L standard		-	-	7	%
φ_{dif}	differential phase	*"ITU-T J.63 line 330"*		-	2	4	deg
S/N_W	weighted signal-to-noise ratio	see Figure 5	[8]	56	59	-	dB
S/N_{UW}	unweighted signal-to-noise ratio		[9]	47	51	-	dB
$\alpha_{IM(blue)}$	intermodulation attenuation at 'blue'	see Figure 6	[10]				
		f = 1.1 MHz		58	64	-	dB
		f = 3.3 MHz		58	64	-	dB
$\alpha_{IM(yellow)}$	intermodulation attenuation at 'yellow'	see Figure 6	[10]				
		f = 1.1 MHz		60	66	-	dB
		f = 3.3 MHz		59	65	-	dB
$\Delta V_{r(PC)(rms)}$	residual picture carrier (RMS value)	fundamental wave and harmonics		-	2	5	mV
$\Delta f_{unw(p-p)}$	robustness for unwanted frequency deviation of picture carrier (peak-to-peak value)	3 % residual carrier; 50 % serration pulses; L standard	[4]	-	-	12	kHz
$\Delta\varphi$	robustness for modulator imbalance	0 % residual carrier; 50 % serration pulses; L standard; L-gating = 0 %	[4]	-	-	3	%
α_H	suppression of video signal harmonics	AC load; C_L < 20 pF; R_L > 1 kΩ	[11]	35	40	-	dB

Table 25. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 27 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC/SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 23; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
α_{spur}	suppression of spurious elements		[12]	40	-	-	dB
$PSRR_{CVBS}$	power supply ripple rejection at pin CVBS	f_{ripple} = 70 Hz; video signal; grey level; positive and negative modulation; see Figure 8		20	25	-	dB
M/N standard including Korea; see Figure 16							
$B_{v(-3dB)(trap)}$	–3 dB video bandwidth including sound carrier trap	f_{trap} = 4.5 MHz	[13]	3.95	4.05	-	MHz
α_{SC1}	attenuation at first sound carrier	f = 4.5 MHz		30	36	-	dB
$\alpha_{SC1(60kHz)}$	attenuation at first sound carrier $f_{SC1} \pm 60$ kHz	f = 4.5 MHz		21	27	-	dB
α_{SC2}	attenuation at second sound carrier	f = 4.724 MHz		21	27	-	dB
$\alpha_{SC2(60kHz)}$	attenuation at second sound carrier $f_{SC2} \pm 60$ kHz	f = 4.724 MHz		15	21	-	dB
$t_{d(g)(cc)}$	group delay at color carrier frequency	f = 3.58 MHz; see Figure 17		110	180	250	ns
B/G standard; see Figure 18							
$B_{v(-3dB)(trap)}$	–3 dB video bandwidth including sound carrier trap	f_{trap} = 5.5 MHz	[13]	4.90	5.00	-	MHz
α_{SC1}	attenuation at first sound carrier	f = 5.5 MHz		30	36	-	dB
$\alpha_{SC1(60kHz)}$	attenuation at first sound carrier $f_{SC1} \pm 60$ kHz	f = 5.5 MHz		24	30	-	dB
α_{SC2}	attenuation at second sound carrier	f = 5.742 MHz		21	27	-	dB
$\alpha_{SC2(60kHz)}$	attenuation at second sound carrier $f_{SC2} \pm 60$ kHz	f = 5.742 MHz		15	21	-	dB
$t_{d(g)(cc)}$	group delay at color carrier frequency	f = 4.43 MHz; see Figure 19		110	180	250	ns
I standard; see Figure 20							
$B_{v(-3dB)(trap)}$	–3 dB video bandwidth including sound carrier trap	f_{trap} = 6.0 MHz	[13]	5.40	5.50	-	MHz
α_{SC1}	attenuation at first sound carrier	f = 6.0 MHz		26	32	-	dB

Table 25. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 27 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC/SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 23; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\alpha_{SC1(60kHz)}$	attenuation at first sound carrier $f_{SC1} \pm 60$ kHz	f = 6.0 MHz		20	26	-	dB
α_{SC2}	attenuation at second sound carrier	f = 6.55 MHz		12	18	-	dB
$\alpha_{SC2(60kHz)}$	attenuation at second sound carrier $f_{SC2} \pm 60$ kHz	f = 6.55 MHz		10	15	-	dB
$t_{d(g)(cc)}$	group delay at color carrier frequency	f = 4.43 MHz		-	90	160	ns
D/K standard; see Figure 21							
$B_{v(-3dB)(trap)}$	–3 dB video bandwidth including sound carrier trap	f_{trap} = 6.5 MHz	[13]	5.50	5.95	-	MHz
α_{SC1}	attenuation at first sound carrier	f = 6.5 MHz		26	32	-	dB
$\alpha_{SC1(60kHz)}$	attenuation at first sound carrier $f_{SC1} \pm 60$ kHz	f = 6.5 MHz		20	26	-	dB
α_{SC2}	attenuation at second sound carrier	f = 6.742 MHz		18	24	-	dB
$\alpha_{SC2(60kHz)}$	attenuation at second sound carrier $f_{SC2} \pm 60$ kHz	f = 6.742 MHz		13	18	-	dB
$t_{d(g)(cc)}$	group delay at color carrier frequency	f = 4.28 MHz		-	60	130	ns
Video output 1.1 V (pin CVBS)							
Trap bypass mode and sound carrier off[14]							
$V_{o(v)(p-p)}$	video output voltage (peak-to-peak value)	see Figure 9		0.95	1.10	1.25	V
V_{sync}	sync voltage level			1.35	1.5	1.6	V
$V_{clip(u)}$	upper video clipping voltage level			3.5	3.6	-	V
$V_{clip(l)}$	lower video clipping voltage level			-	0.9	1.0	V
$B_{v(-1dB)}$	–1 dB video bandwidth	AC load; C_L < 20 pF; R_L > 1 kΩ		5	6	-	MHz
$B_{v(-3dB)}$	–3 dB video bandwidth	AC load; C_L < 20 pF; R_L > 1 kΩ		7	8	-	MHz
S/N_W	weighted signal-to-noise ratio	Figure 5	[8]	56	59	-	dB
S/N_{UW}	unweighted signal-to-noise ratio		[9]	48	52	-	dB

Table 25. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 27 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC/SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 23; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VIF-AGC[15]							
$t_{resp(inc)}$	AGC response time to an increasing VIF step	negative modulation; normal mode	[16]	-	4.3	-	µs/dB
		negative modulation; mobile mode	[16]	-	1.5	-	µs/dB
		positive modulation; VIF step: 20 dB	[16]	-	2.6	-	ms
$t_{resp(dec)}$	AGC response time to a decreasing VIF step	negative modulation					
		normal mode	[16]	-	1.9	-	ms/dB
		fast normal mode	[16][17]	-	0.08	-	ms/dB
		mobile mode	[16]	-	0.25	-	ms/dB
		fast mobile mode	[16][17]	-	0.01	-	ms/dB
		positive modulation					
		normal mode; VIF step: 20 dB	[16]	-	890	-	ms
		normal mode	[16]	-	143	-	ms/dB
		fast mode	[16][18]	-	2.6	-	ms/dB
$\Delta V_{i(VIF)}$	VIF amplitude step for activating AGC fast mode	L standard		–2	–6	–10	dB
V_{VAGC}	gain control voltage range	see Figure 10		0.8	-	3.5	V
CR_{stps}	control steepness	definition: $\Delta G_{VIF}/\Delta V_{VAGC}$; V_{VAGC} = 2 V to 3 V		-	–80	-	dB/V
$V_{th(VIF)}$	threshold voltage for high level VIF input	see Table 8 and Table 9		120	200	320	µV
Pin VAGC							
$I_{ch(max)}$	maximum charge current	L standard		-	100	-	µA
$I_{ch(add)}$	additional charge current	L standard: in the event of missing VITS pulses and no white video content		-	100	-	nA
I_{dch}	discharge current	L standard; normal mode		-	35	-	nA
		L standard; fast mode		-	1.8	-	µA
AGC input switch (pin AGCSW)[19]; see Table 18							
$V_{ext(AGCOFF)}$	voltage level for external AGC = OFF	bit E5 = 1; bit E7 = 1		-	-	0.3	V
$V_{ext(AGCON)}$	voltage level for external AGC = ON	bit E5 = 1; bit E7 = 1		2.5	-	-	V
R_i	input resistance	bit E5 = 1; bit E7 = 1		8	-	-	kΩ

Table 25. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 27 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC/SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 23; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_i	input current	bit E5 = 1; bit E7 = 1; V_{AGCSW} = 0 V	-	5	-	µA
V_i	input voltage	bit E5 = 1; bit E7 = 1; pin AGCSW open-circuit	V_P – 1.7	-	-	V
t_{d1}	switching delay for external AGC = ON	bit E5 = 1; bit E7 = 1; V_{AGCSW} = 2.5 V	-	-	150	ns
t_{d2}	switching delay for external AGC = OFF	bit E5 = 1; bit E7 = 1; V_{AGCSW} = 0.3 V	-	-	150	ns
Tuner AGC (pin TAGC); see Figure 4, Figure 10 and Figure 11						
$V_{i(VIF)(start1)(rms)}$	VIF input signal voltage for minimum starting point of tuner takeover at pins VIF1 and VIF2 (RMS value)	I_{TAGC} = 120 µA; R_{TOP} = 22 kΩ or no R_{TOP} and –15 dB via I²C-bus (see Table 16)	-	2	5	mV
$V_{i(VIF)(start2)(rms)}$	VIF input signal voltage for maximum starting point of tuner takeover at pins VIF1 and VIF2 (RMS value)	I_{TAGC} = 120 µA; R_{TOP} = 0 Ω or no R_{TOP} and +15 dB via I²C-bus (see Table 16)	45	90	-	mV
$V_{i(SIF)(start1)(rms)}$	SIF input signal voltage for minimum starting point of tuner takeover at pins SIF1 and SIF2 (RMS value)	true split sound mode; I_{TAGC} = 120 µA; R_{TOP} = 22 kΩ or no R_{TOP} and –15 dB via I²C-bus (see Table 16)	-	1	2.5	mV
$V_{i(SIF)(start2)(rms)}$	SIF input signal voltage for maximum starting point of tuner takeover at pins SIF1 and SIF2 (RMS value)	true split sound mode; I_{TAGC} = 120 µA; R_{TOP} = 0 Ω or no R_{TOP} and +15 dB via I²C-bus (see Table 16)	22.5	45	-	mV
QV_{TOP}	tuner takeover point accuracy	I_{TAGC} = 120 µA; R_{TOP} = 10 kΩ; or no R_{TOP} and 0 dB via I²C-bus (see Table 16)				
		normal mode	7	17	43	mV
		true split sound mode	4	9	22	mV
$\Delta QV_{TOP}/\Delta T$	takeover point variation with temperature	I_{TAGC} = 120 µA	-	0.03	0.07	dB/K
V_o	permissible output voltage	from external source	-	-	8.8	V
V_{sat}	saturation voltage	I_{TAGC} = 450 µA	-	-	0.5	V

Table 25. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 27 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC/SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 23; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{sink}	sink current	no tuner gain reduction; V_{TAGC} = 8.8 V	-	-	0.75	µA
		maximum tuner gain reduction; V_{TAGC} = 1 V	450	600	750	µA
ΔG_{IF}	IF slip by automatic gain control	tuner gain current from 20 % to 80 %	3	5	8	dB
AFC circuit (pin AFC)[20][21]; see Figure 7						
$V_{sat(ul)}$	lower limit saturation voltage		V_P – 0.6	V_P – 0.3	-	V
$V_{sat(ll)}$	lower limit saturation voltage		-	0.3	0.6	V
$I_{o(source)}$	output source current		160	200	240	µA
$I_{o(sink)}$	output sink current		160	200	240	µA
AFC_{stps}	AFC control steepness	definition: $\Delta I_{AFC}/\Delta f_{VIF}$	0.85	1.05	1.25	µA/kHz
$Qf_{VIF(a)}$	analog accuracy of AFC circuit	I_{AFC} = 0 A; f_{REF} = 4 MHz	–20	-	+20	kHz
$Qf_{VIF(d)}$	digital accuracy of AFC circuit via I²C-bus	I_{AFC} = 0 A; f_{REF} = 4 MHz; 1 digit = 25 kHz	–20 – 1 digit	-	+20 + 1 digit	kHz
SIF-AGC monitor (pin AFC)[20]; see Table 14						
$I_{o(source)}$	SIF-AGC monitor source current		-	-	600	µA
$I_{o(sink)}$	SIF-AGC monitor sink current		-	-	270	µA
SIF amplifier (pins SIF1 and SIF2)						
$V_{i(SIF)(rms)}$	SIF input voltage sensitivity (RMS value)	FM mode; –3 dB at intercarrier output pin SIOMAD	-	30	70	µV
		AM mode; –3 dB at AF output pin AUD	-	70	100	µV
$V_{i(max)(rms)}$	maximum input voltage (RMS value)	FM mode; 1 dB at intercarrier output pin SIOMAD	50	70	-	mV
		AM mode; 1 dB at AF output pin AUD	80	140	-	mV
$V_{i(ovl)(rms)}$	overload input voltage (RMS value)	[3]	-	-	320	mV
$G_{SIF(cr)}$	SIF gain control range	FM and AM mode; see Figure 11	60	66	-	dB
$B_{SIF(-3dB)(ll)}$	lower limit –3 dB SIF bandwidth		-	15	-	MHz

Table 25. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 27 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC/SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 23; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$B_{SIF(-3dB)(ul)}$	upper limit −3 dB SIF bandwidth			-	80	-	MHz
$R_{i(diff)}$	differential input resistance		[4]	-	2	-	kΩ
$C_{i(diff)}$	differential input capacitance		[4]	-	3	-	pF
V_I	DC input voltage			-	1.93	-	V
SIF-AGC detector							
t_{resp}	AGC response time to an increasing or decreasing SIF step of 20 dB	FM or AM fast step; normal mode	[20]				
		increasing		-	8	-	ms
		decreasing		-	25	-	ms
		FM or AM fast step; mobile mode	[20]				
		increasing		-	0.25	-	ms
		decreasing		-	0.7	-	ms
		AM slow step					
		increasing		-	80	-	ms
		decreasing		-	250	-	ms
Single reference QSS intercarrier mixer (pin SIOMAD)							
$V_{o(intc)(rms)}$	IF intercarrier output level (RMS value)	QSS mode; SC_1; SC_2 off		90	140	180	mV
		L standard; without modulation		90	140	180	mV
		intercarrier mode; PC/SC_1 = 20 dB; SC_2 off	[22]	-	75	-	mV
$B_{intc(-3dB)(ul)}$	upper limit −3 dB intercarrier bandwidth			12	15	-	MHz
$\Delta V_{r(SC)(rms)}$	residual sound carrier (RMS value)	fundamental wave and harmonics					
		QSS mode		-	2	5	mV
		intercarrier mode		-	2	5	mV
$\Delta V_{r(PC)(rms)}$	residual picture carrier (RMS value)	fundamental wave and harmonics					
		QSS mode		-	2	5	mV
		intercarrier mode		-	5	20	mV
α_H	suppression of video signal harmonics	intercarrier mode; f_{video} = 5 MHz		35	40	-	dB
R_o	output resistance		[4]	-	-	30	Ω
V_O	DC output voltage			-	2	-	V

Table 25. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 27 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC/SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 23; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{bias(int)}$	internal DC bias current for emitter follower			0.90	1.15	-	mA
$I_{o(sink)(max)}$	maximum AC output sink current			0.6	0.8	-	mA
$I_{o(source)(max)}$	maximum AC output source current			0.6	0.8	-	mA
$I_{o(source)}$	DC output source current	MAD2 activated	[23]	0.75	0.93	1.20	mA
FM-PLL demodulator [21][24][25][26][27][28]							
Sound intercarrier output (pin SIOMAD)							
$V_{FM(rms)}$	IF intercarrier level for gain controlled operation of FM-PLL (RMS value)	corresponding PC/SC ratio at input pins VIF1 and VIF2 is 7 dB to 47 dB		3.2	-	320	mV
$V_{FM(lock)(rms)}$	IF intercarrier level for lock-in of PLL (RMS value)			-	-	2	mV
$V_{FM(det)(rms)}$	IF intercarrier level for FM carrier detect (RMS value)	see Table 9		-	-	2.3	mV
f_{FM}	sound intercarrier operating FM frequencies	see Table 17		-	4.5	-	MHz
				-	5.5	-	MHz
				-	6.0	-	MHz
				-	6.5	-	MHz
		true split sound mode; see Table 20		-	3.1	-	MHz
				-	3.6	-	MHz
				-	5.6	-	MHz
				-	6.6	-	MHz
Audio output (pin AUD)							
$V_{o(AF)(rms)}$	AF output voltage (RMS value)	25 kHz FM deviation; 75 µs de-emphasis		400	500	600	mV
		27 kHz FM deviation; 50 µs de-emphasis		430	540	650	mV
$V_{o(AF)(cl)(rms)}$	AF output clipping level (RMS value)	THD < 1.5 %		1.3	1.4	-	V
$\Delta V_{o(AF)}/\Delta T$	AF output voltage variation with temperature			-	3×10^{-3}	7×10^{-3}	dB/K
THD	total harmonic distortion	27 kHz FM deviation; 50 µs de-emphasis		-	0.15	0.50	%

Table 25. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 27 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC/SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 23; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Δf_{AF}	frequency deviation	THD < 1.5 %	[25]	-	-	±55	kHz
		–6 dB AF output via I²C-bus	[25]	-	-	±110	kHz
$B_{AF(-3dB)}$	–3 dB AF bandwidth	without de-emphasis; measured with FM-PLL filter in Figure 23		80	100	-	kHz
$S/N_{W(AF)}$	weighted signal-to-noise ratio of audio signal	FM-PLL only; 27 kHz FM deviation; 50 µs de-emphasis		52	56	-	dB
		black picture; see Figure 12		50	56	-	dB
$\Delta V_{r(SC)(rms)}$	residual sound carrier (RMS value)	fundamental wave and harmonics; without de-emphasis		-	-	2	mV
$\alpha_{AM(sup)}$	AM suppression of FM demodulator	referenced to 27 kHz FM deviation; 50 µs de-emphasis; AM: f = 1 kHz; m = 54 %		40	46	-	dB
PSRR	power supply ripple rejection	f_{ripple} = 70 Hz; see Figure 8		14	20	-	dB
FM-PLL filter (pin FMPLL)							
V_{loop}	DC loop voltage			1.5	-	3.3	V
$I_{o(source)(PD)(max)}$	maximum phase detector output source current			-	60	-	µA
$I_{o(sink)(PD)(max)}$	maximum phase detector output sink current			-	60	-	µA
$I_{o(source)(DAH)}$	output source current of digital acquisition help			-	55	-	µA
$I_{o(sink)(DAH)}$	output sink current of digital acquisition help			-	55	-	µA
$t_{W(DAH)}$	pulse width of digital acquisition help current			-	16	-	µs
$T_{cy(DAH)}$	cycle time of digital acquisition help			-	64	-	µs
$K_{O(FM)}$	VCO steepness	definition: $\Delta f_{FM}/\Delta V_{FMPLL}$		-	3.3	-	MHz/V
$K_{D(FM)}$	phase detector steepness	definition: $\Delta I_{FMPLL}/\Delta\varphi_{FM}$		-	4	-	µA/rad

Table 25. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 27 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC/SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 23; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Audio amplifier							
De-emphasis network (pin DEEM)							
R_o	output resistance	50 µs de-emphasis; see Table 15		4.4	5.0	5.6	kΩ
		75 µs de-emphasis; see Table 15		6.6	7.5	8.4	kΩ
$V_{AF(rms)}$	audio signal (RMS value)	f_{AF} = 400 Hz; V_{AUD} = 500 mV		-	170	-	mV
V_O	DC output voltage			-	2.37	-	V
AF decoupling (pin AFD)							
V_{dec}	DC decoupling voltage	dependent on f_{FM} intercarrier frequency		1.5	-	3.3	V
I_L	leakage current	$\Delta V_{O(AUD)}$ < ±50 mV		-	-	±25	nA
$I_{ch(max)}$	maximum charge current			1.15	1.50	1.85	µA
$I_{dch(max)}$	maximum discharge current			1.15	1.50	1.85	µA
Audio output (pin AUD)							
R_o	output resistance		[4]	-	-	300	Ω
$V_{O(AUD)}$	DC output voltage			-	2.37	-	V
R_L	load resistance	AC-coupled		10	-	-	kΩ
$R_{L(DC)}$	DC load resistance			100	-	-	kΩ
C_L	load capacitance			-	-	1.5	nF
$B_{AF(-3dB)(ul)}$	upper limit –3 dB AF bandwidth of audio amplifier			150	-	-	kHz
$B_{AF(-3dB)(ll)}$	lower limit –3 dB AF bandwidth of audio amplifier		[26]	-	-	20	Hz
α_{mute}	mute attenuation of AF signal	via I²C-bus		70	75	-	dB
ΔV_{jump}	DC jump voltage for switching AF output to mute state and vice versa	activated by digital acquisition help or via I²C-bus mute		-	±50	±150	mV

Table 25. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 27 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC/SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 23; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FM operation[27][29]						
Intercarrier AF performance[30]						
S/N_W	weighted signal-to-noise ratio	PC/SC ratio is 21 dB to 27 dB at pins VIF1 and VIF2				
		black picture	50	56	-	dB
		white picture	45	51	-	dB
		6 kHz sine wave (black-to-white modulation)	40	46	-	dB
		sound carrier subharmonics; f = 2.75 MHz ± 3 kHz	35	40	-	dB
Single reference QSS AF performance[31][32]						
$S/N_{W(SC1)}$	weighted signal-to-noise ratio for SC_1	PC/SC_1 ratio at pins VIF1 and VIF2; 27 kHz (54 % FM deviation); *"ITU-R BS.468-4"*	40	-	-	dB
		black picture	53	58	-	dB
		white picture	50	53	-	dB
		6 kHz sine wave (black-to-white modulation)	44	48	-	dB
		250 kHz square wave (black-to-white modulation)	40	45	-	dB
		sound carrier subharmonics; f = 2.75 MHz ± 3 kHz	45	51	-	dB
		sound carrier subharmonics; f = 2.87 MHz ± 3 kHz	46	52	-	dB

Table 25. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 27 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC/SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 23; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$S/N_{W(SC2)}$	weighted signal-to-noise ratio for SC_2	PC/SC_2 ratio at pins VIF1 and VIF2; 27 kHz (54 % FM deviation); *"ITU-R BS.468-4"*		40	-	-	dB
		black picture		48	55	-	dB
		white picture		46	51	-	dB
		6 kHz sine wave (black-to-white modulation)		42	46	-	dB
		250 kHz square wave (black-to-white modulation)		29	34	-	dB
		sound carrier subharmonics; f = 2.75 MHz ± 3 kHz		44	50	-	dB
		sound carrier subharmonics; f = 2.87 MHz ± 3 kHz		45	51	-	dB
AM operation							
L standard (pin AUD)[33]; see Figure 13 and Figure 14							
$V_{o(AF)(rms)}$	AF output voltage (RMS value)	54 % modulation		400	500	600	mV
THD	total harmonic distortion	54 % modulation		-	0.5	1.0	%
$B_{AF(-3dB)}$	–3 dB AF bandwidth			100	125	-	kHz
$S/N_{W(AF)}$	weighted signal-to-noise ratio of audio signal	in accordance with *"ITU-R BS.468-4"*		45	50	-	dB
$V_{O(AUD)}$	DC potential voltage			-	2.37	-	V
PSRR	power supply ripple rejection	f_{ripple} = 70 Hz; see Figure 8		20	26	-	dB
Reference frequency input (pin REF)							
V_I	DC input voltage			2.3	2.6	2.9	V
R_i	input resistance		[4]	-	5	-	kΩ
R_{xtal}	resonance resistance of crystal	operation as crystal oscillator		-	-	200	Ω
C_x	pull-up/down capacitance		[34]	-	-	-	pF
f_{ref}	reference signal frequency		[35]	-	4	-	MHz
Δf_{ref}	tolerance of reference signal frequency		[21]	-	-	±0.1	%

Table 25. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 27 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC/SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 23; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ref(rms)}$	reference signal voltage (RMS value)	operation as input terminal	80	-	400	mV
$R_{o(ref)}$	output resistance of reference signal source		-	-	4.7	kΩ
C_K	decoupling capacitance to external reference signal source	operation as input terminal	22	100	-	pF
I²C-bus transceiver (pins SDA and SCL)[36][37]						
f_{SCL}	SCL clock frequency		0	-	400	kHz
V_{IH}	HIGH-level input voltage		3	-	V_{CC}	V
V_{IL}	LOW-level input voltage		–0.3	-	+1.5	V
I_{IH}	HIGH-level input current		–10	-	+10	µA
I_{IL}	LOW-level input current		–10	-	+10	µA
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	-	-	0.4	V
$I_{o(sink)}$	output sink current	V_P = 0 V	-	-	10	µA
$I_{o(source)}$	output source current	V_P = 0 V	-	-	10	µA
Output ports (pins OP1 and OP2)[15][19][38]						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA (sink current)	-	-	0.4	V
V_{OH}	HIGH-level output voltage		-	-	6	V
$I_{o(sink)}$	output sink current		-	-	2	mA
$I_{o(sink/source)(max)}$	maximum output sink or source current	pin OP2 functions as VIF-AGC output	-	-	10	µA

[1] Values of video and sound parameters can be decreased at V_P = 4.5 V.

[2] For applications without I²C-bus, the time constant (R × C) at the supply must be > 1.2 µs (e.g. 1 Ω and 2.2 µF).

[3] Level headroom for input level jumps during gain control setting.

[4] This parameter is not tested during the production and is only given as application information for designing the receiver circuit.

[5] Loop bandwidth BL = 70 kHz (damping factor d = 1.9; calculated with sync level within gain control range). Calculation of the VIF-PLL filter can be done by use of the following formulae: $BL_{-3dB} = \frac{1}{2\pi} K_O K_D R$, valid for d ≥ 1.2; $d = \frac{1}{2} R \sqrt{K_O K_D C}$, where: K_O is the VCO steepness $\left(\frac{rad}{V}\right)$ or $\left(2\pi\frac{Hz}{V}\right)$; K_D is the phase detector steepness $\left(\frac{\mu A}{rad}\right)$; R is the loop resistor; C is the loop capacitor; BL_{-3dB} is the loop bandwidth for −3 dB; d is the damping factor.

[6] $V_{i(VIF)}$ = 10 mV (RMS); Δf = 1 MHz (VCO frequency offset related to picture carrier frequency); white picture video modulation.

[7] Condition: luminance range (5 steps) from 0 % to 100 %.

[8] Measurement using unified weighting filter ("*ITU-T J.61*"), 200 kHz high-pass filter, 5 MHz low-pass filter and subcarrier notch filter ("*ITU-T J.64*").

[9] Noise analyzer setting: 200 kHz high-pass and SC-trap switched on.

[10] The intermodulation figures are defined for:

a) f = 1.1 MHz (referenced to black and white signal) as $\alpha_{IM} = 20 \log\left(\frac{V_0 \text{ at } 4.4 \text{ MHz}}{V_0 \text{ at } 1.1 \text{ MHz}}\right) + 3.6$ dB.

b) f = 3.3 MHz (referenced to color carrier) as $\alpha_{IM} = 20 \log\left(\frac{V_0 \text{ at } 4.4 \text{ MHz}}{V_0 \text{ at } 3.3 \text{ MHz}}\right)$.

[11] Measurements taken with SAW filter M1963M (sound shelf: 20 dB); loop bandwidth BL = 70 kHz. Modulation VSB; sound carrier off; f_{video} > 0.5 MHz.

[12] Measurements taken with SAW filter M1963M (sound shelf: 20 dB); loop bandwidth BL = 70 kHz. Sound carrier on; f_{video} = 10 kHz to 10 MHz.

[13] AC load; C_L < 20 pF and R_L > 1 kΩ. The sound carrier frequencies (depending on TV standard) are attenuated by the integrated sound carrier traps (see Figure 16 to Figure 21; |H (s)| is the absolute value of transfer function).

[14] The sound carrier trap can be bypassed by switching the I²C-bus. In this way the full composite video spectrum appears at pin CVBS. The amplitude is 1.1 V (p-p).

[15] If selected by the I²C-bus, the VIF-AGC voltage can be monitored at pin OP2. In this case, OP2 cannot be used for the normal port function.

[16] The response time is valid for a VIF input level range from 200 µV to 70 mV.

[17] The fast mode will be activated automatically, if within a time of typically 150 µs for mobile mode and 1.2 ms for normal mode no AGC event occurs. An AGC event is a charge current pulse into the AGC capacitor due to reaching AGC reference voltage the sync level.

[18] The fast mode will be activated automatically, if the black level drops down by half of the sync amplitude.

[19] If selected by the I²C-bus, pin OP1 can alternatively be used for external AGC control, activated by pin AGCSW. In this case, OP1 cannot be used for the normal port function.

[20] Pin AFC is usable as AFC output or as SIF-AGC.

a) To match the AFC output signal to different tuning systems a current source output is provided. The test circuit is given in Figure 7. The AFC steepness can be changed by resistors R1 and R2.

b) In mobile mode the internal SIF-AGC is switched to pin AFC. In this case AFC out is disabled.

[21] The tolerance of the reference frequency determines the accuracy of the VIF-AFC, FM demodulator center frequency and maximum FM deviation.

[22] The intercarrier output signal at pin SIOMAD can be calculated by the following formulae taking into account the internal video signal with 1.1 V (p-p) as a reference: $V_{o(intc)(rms)} = 1.1 \times \frac{1}{2\sqrt{2}} \times 10^r \ V$ and $r = \frac{1}{20} \times \left(\frac{V_{i(SC)}}{V_{i(PC)}}\ (dB) + 6\ dB \pm 3\ dB\right)$, where: $\frac{1}{2\sqrt{2}}$ is the correction term for RMS value, $\frac{V_{i(SC)}}{V_{i(PC)}}\ (dB)$ is the sound-to-picture carrier ratio at pins VIF1 and VIF2 in dB, 6 dB is the correction term of internal circuitry and ±3 dB is the tolerance of video output and intercarrier output $V_{o(intc)(rms)}$.

[23] For normal operation (with the I²C-bus) no DC load at pin SIOMAD is allowed. The second module address (MAD2) will be activated by the application of a 2.2 kΩ resistor between pin SIOMAD and ground. If this MAD2 is activated, also the power-on setup state activates a VIF frequency of 58.75 MHz.

[24] SIF input level is 10 mV (RMS); VIF input level is 10 mV (RMS) unmodulated.

[25] Measured with an FM deviation of 25 kHz and the typical AF output voltage of 500 mV (RMS). The AF output signal can be attenuated by 6 dB to 250 mV (RMS) via the I²C-bus. For handling a frequency deviation of more than 55 kHz, the AF output signal has to be reduced in order to avoid clipping (THD < 1.5 %).

[26] The lower limit of the audio bandwidth depends on the value of the capacitor at pin AFD. A value of C_{AF} = 470 nF leads to $f_{AF(-3dB)} \approx 20$ Hz and C_{AF} = 220 nF leads to $f_{AF(-3dB)} \approx 40$ Hz.

[27] For all S/N measurements the VIF modulator in use has to meet the following specifications:

a) Incidental phase modulation for black-to-white jump less than 0.5 degrees.

b) QSS AF performance, measured with the television demodulator AMF2 (audio output, weighted S/N ratio) better than 60 dB (at deviation 27 kHz) for 6 kHz sine wave black-to-white video modulation.

c) Picture-to-sound carrier ratio PC/SC_1 = 13 dB (transmitter).

[28] Calculation of the loop filter parameters can be done approximately using the following formulae: $f_o = \frac{1}{2\pi}\sqrt{\frac{K_O K_D}{C_P}}$;

$\vartheta = \frac{1}{2R\sqrt{K_O K_D C_P}}$; $BL_{-3dB} = f_o(1.55 - \vartheta^2)$. The formulae are only valid under the following conditions: $\vartheta \leq 1$ and $C_S > 5C_P$, where:

K_O is the VCO steepness $\left(\frac{rad}{V}\right)$ or $\left(2\pi\frac{Hz}{V}\right)$; K_D is the phase detector steepness $\left(\frac{\mu A}{rad}\right)$; R is the loop resistor; C_S is the series capacitor; C_P is the parallel capacitor; f_o is the natural frequency of the PLL; BL_{-3dB} is the loop bandwidth for –3 dB; ϑ is the damping factor. For examples, see Table 26.

[29] The PC/SC ratio is calculated as the addition of TV transmitter PC/SC_1 ratio and SAW filter PC/SC_1 ratio. This PC/SC ratio is necessary to achieve the S/N_W values as noted. A different PC/SC ratio will change these values.

[30] Measurements taken with SAW filter G1984 (Siemens) for vision and sound IF (sound shelf: 14 dB). Picture-to-sound carrier ratio of transmitter PC/SC = 13 dB. Input level on pins VIF1 and VIF2 of $V_{i(SIF)}$ = 10 mV (RMS) sync level, 27 kHz FM deviation for sound carrier, f_{AF} = 400 Hz. Measurements in accordance with *"ITU-R BS.468-4"*. De-emphasis is 50 µs.

[31] The QSS signal output on pin SIOMAD is analyzed by a test demodulator TDA9820. The S/N ratio of this device is more than 60 dB, related to a deviation of ±27 kHz, in accordance with *"ITU-R BS.468-4"*.

[32] Measurements taken with SAW filter K3953 for vision IF (suppressed sound carrier) and K9453 for sound IF (suppressed picture carrier). Input level $V_{i(SIF)}$ = 10 mV (RMS), 27 kHz (54 % FM deviation).

[33] Measurements taken with SAW filter K9453 (Siemens) for AM sound IF (suppressed picture carrier).

[34] The value of C_x determines the accuracy of the resonance frequency of the crystal. It depends on the type of crystal used.

[35] Pin REF is able to operate as a 1-pin crystal oscillator input as well as an external reference signal input, e.g. from the tuning system.

[36] The SDA and SCL lines will not be pulled down if V_{CC} is switched off.

[37] The AC characteristics are in accordance with the I²C-bus specification for fast mode (maximum clock frequency is 400 kHz). Information about the I²C-bus can be found in the brochure *"The I²C-bus and how to use it" (order number 9398 393 40011).*

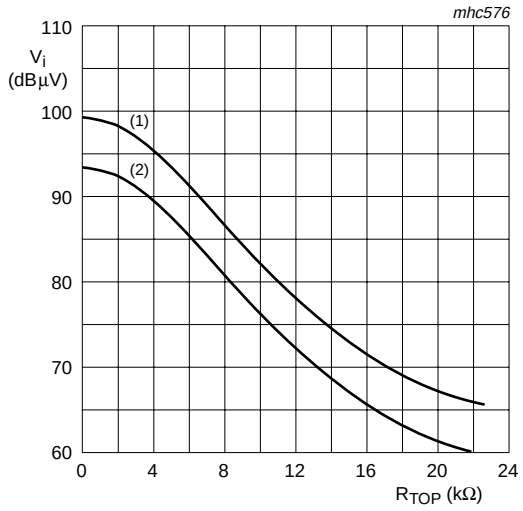
[38] Port P1 and port P2 are open-collector outputs.

Table 26. Examples for Table note 28 of Table 25 (FM-PLL filter)

BL_{-3dB} (kHz)	C_S (nF)	C_P (pF)	R (kΩ)	ϑ
100	10	390	5.6	0.5
160	10	150	9.1	0.5

Table 27. Input frequencies and carrier ratios

Description	Symbol	B/G standard	M/N standard	L standard	L accent standard	Unit
VIF carrier	f_{PC}	38.9	45.75 or 58.75	38.9	33.9	MHz
SIF carrier	f_{SC1}	33.4	41.25 or 54.25	32.4	40.4	MHz
	f_{SC2}	33.158	-	-	-	MHz
Picture-to-sound carrier ratio	SC_1	13	7	10	10	dB
	SC_2	20	-	-	-	dB



(1) $V_{i(VIF)}$.

(2) $V_{i(SIF)}$; true split sound mode.

Fig 4. Typical tuner takeover point as a function of resistor R_{TOP}

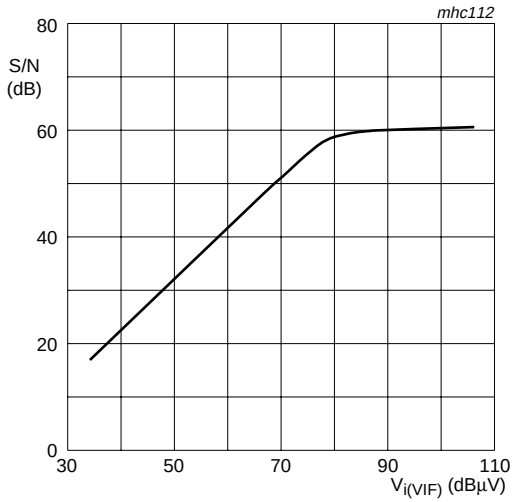
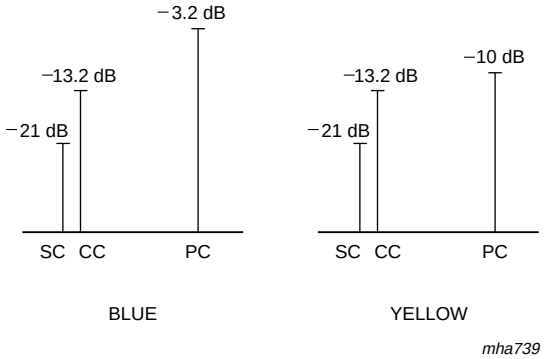


Fig 5. Typical signal-to-noise ratio as a function of VIF input voltage



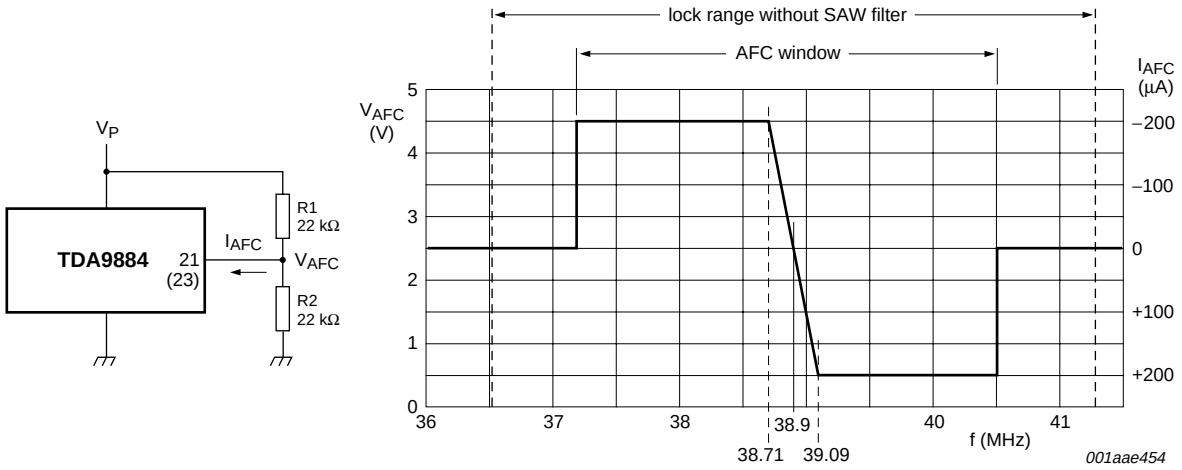
SC is sound carrier, with respect to sync level.

CC is chrominance carrier, with respect to sync level.

PC is picture carrier, with respect to sync level.

The sound carrier levels take into account a sound shelf attenuation of 14 dB (SAW filter G1984M).

Fig 6. Input signal conditions



Pin numbers for TDA9884HN in parentheses.

Fig 7. Typical analog AFC characteristic

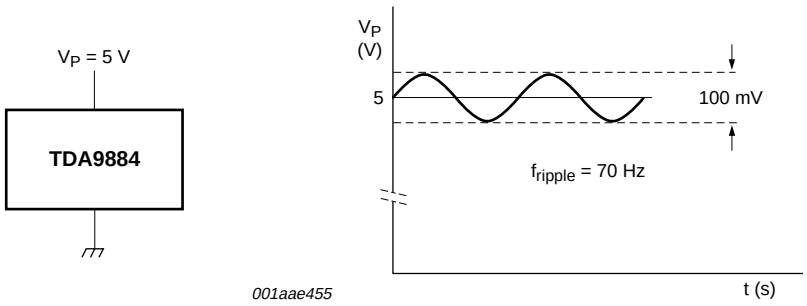


Fig 8. Ripple rejection condition

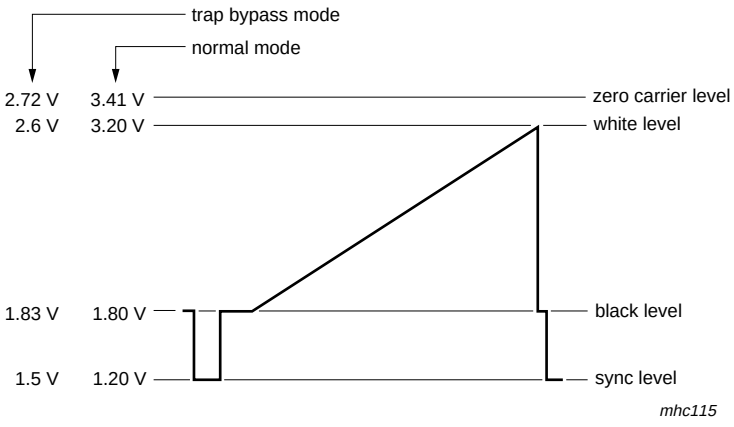
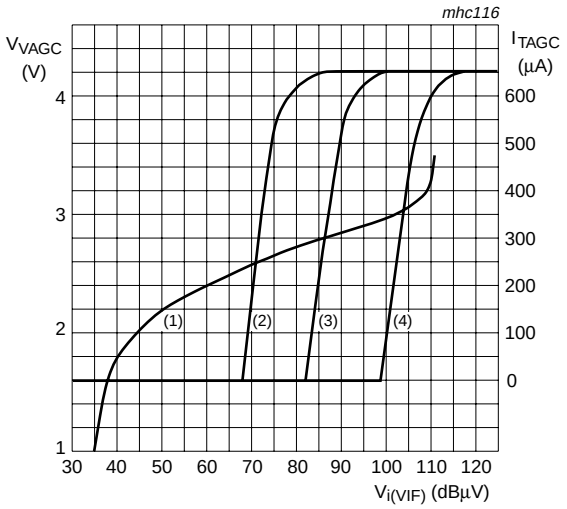


Fig 9. Typical video signal levels on output pin CVBS (sound carrier off)



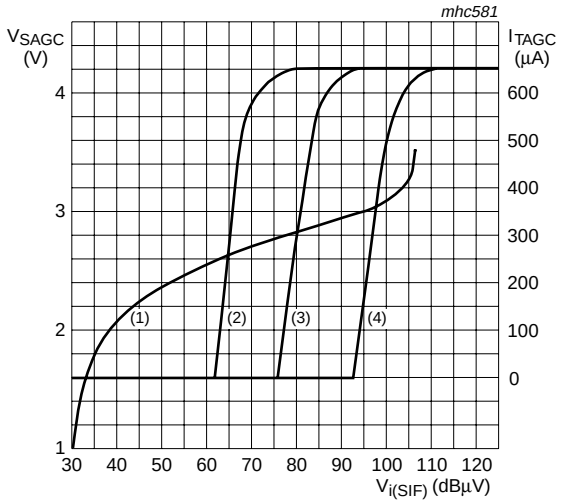
(1) V_{VAGC} is VIF-AGC voltage and can only be measured at pin OP2 controlled by the I²C-bus (see Table 18).

(2) I_{TAGC} is tuner current with R_{TOP} = 22 kΩ or setting via I²C-bus at –15 dB.

(3) I_{TAGC} is tuner current with R_{TOP} = 10 kΩ or setting via I²C-bus at 0 dB.

(4) I_{TAGC} is tuner current with R_{TOP} = 0 Ω or setting via I²C-bus at +15 dB.

Fig 10. Typical VIF and tuner AGC characteristic



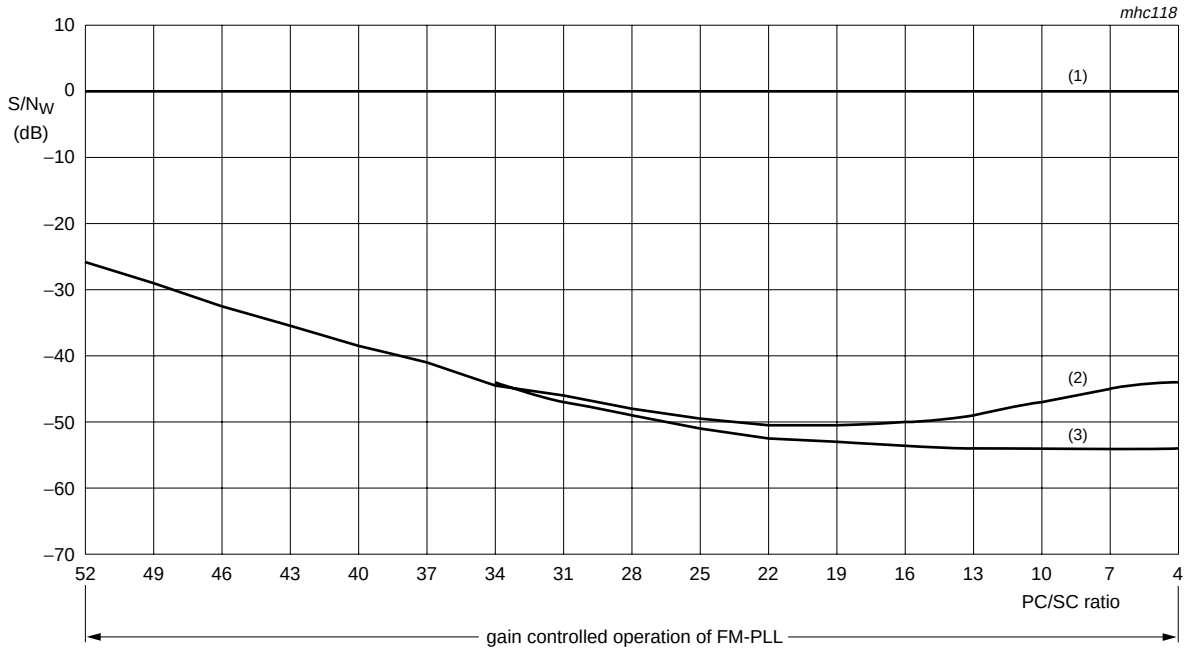
(1) V_{SAGC} is SIF-AGC voltage in FM mode and can only be measured at pin AFC controlled by the I²C-bus (see Table 14).

(2) I_{TAGC} is tuner current in true split sound mode with R_{TOP} = 22 kΩ or setting via I²C-bus at –15 dB.

(3) I_{TAGC} is tuner current in true split sound mode with R_{TOP} = 10 kΩ or setting via I²C-bus at 0 dB.

(4) I_{TAGC} is tuner current in true split sound mode with R_{TOP} = 0 Ω or setting via I²C-bus at +15 dB.

Fig 11. Typical SIF and tuner AGC characteristic



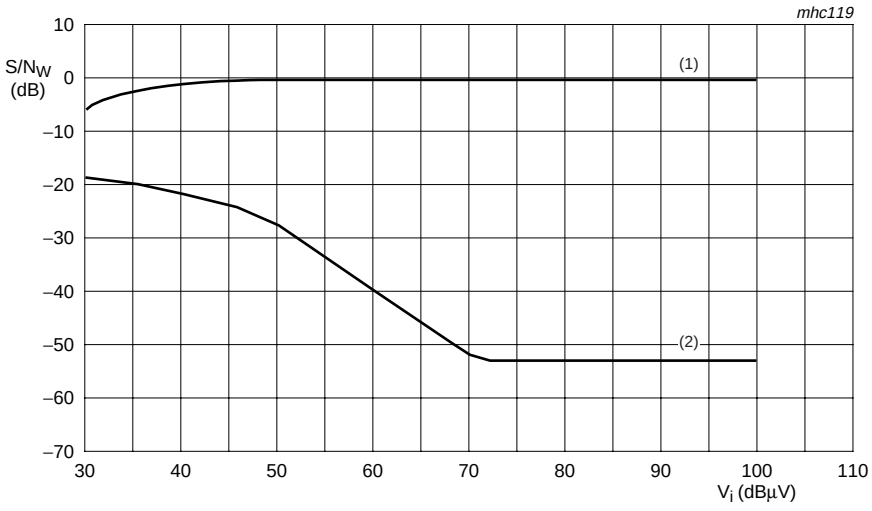
Conditions: PC/SC ratio measured at pins VIF1 and VIF2; via transformer; 27 kHz FM deviation; 50 µs de-emphasis.

(1) Signal.

(2) Noise at H-picture (weighted in accordance with *"ITU-R BS.468-4"* quasi peak).

(3) Noise at black picture (weighted in accordance with *"ITU-R BS.468-4"* quasi peak).

Fig 12. Audio signal-to-noise ratio as a function of picture-to-sound carrier ratio in intercarrier mode

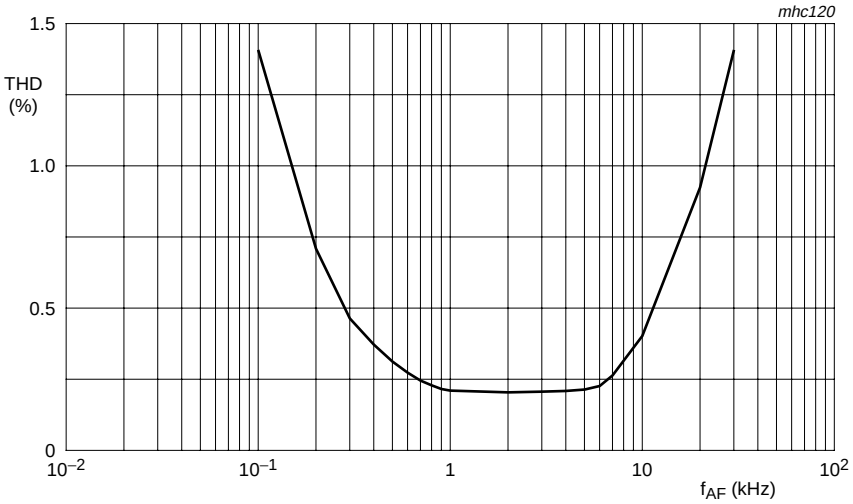


Condition: m = 54 %.

(1) Signal.

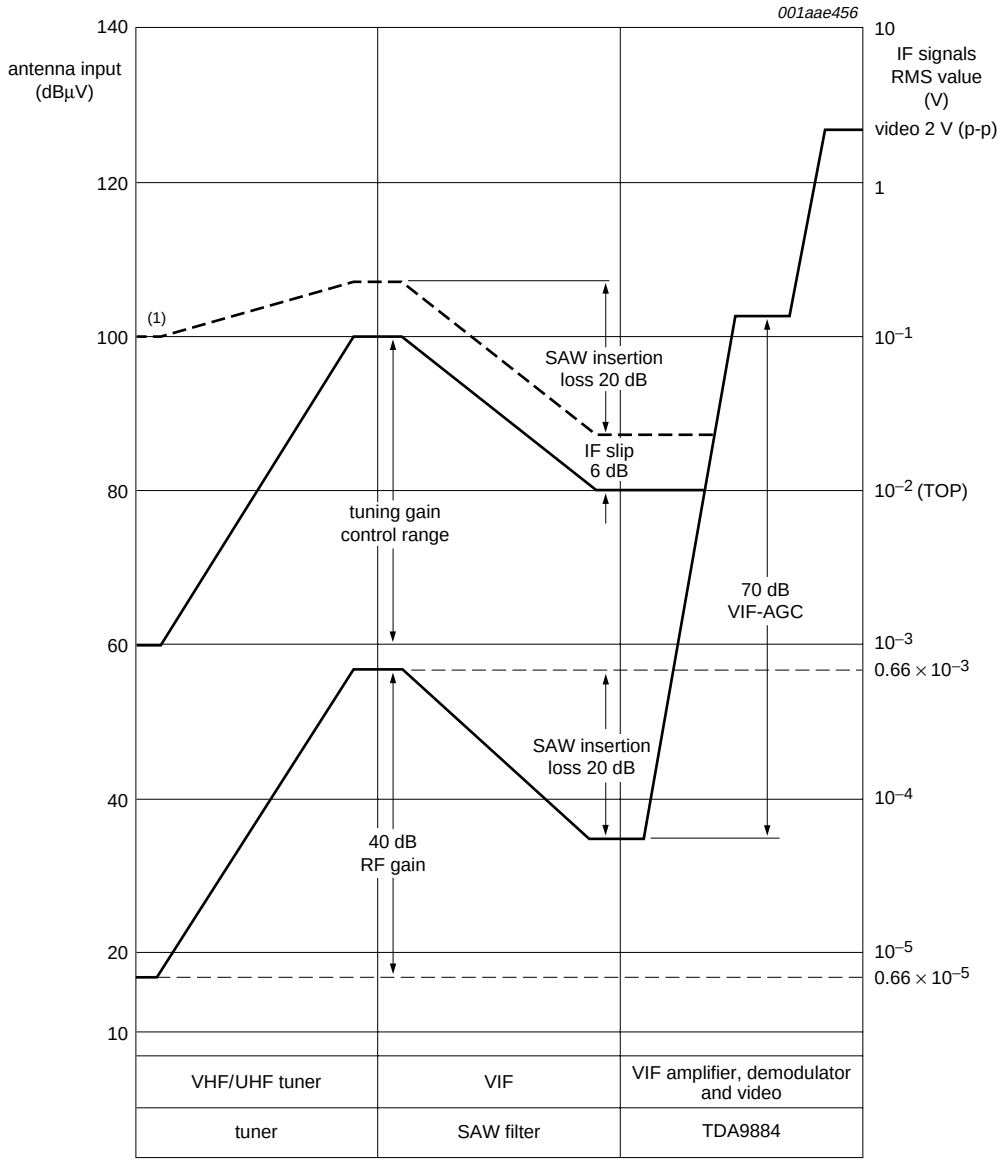
(2) Noise (weighted in accordance with *"ITU-R BS.468-4"* quasi peak).

Fig 13. Typical audio signal-to-noise ratio as a function of input signal at AM standard



C_{AGC} = 2.2 µF; m = 54 %.

Fig 14. Typical total harmonic distortion as a function of audio frequency at AM standard



(1) Depends on TOP.

Fig 15. Front-end level diagram

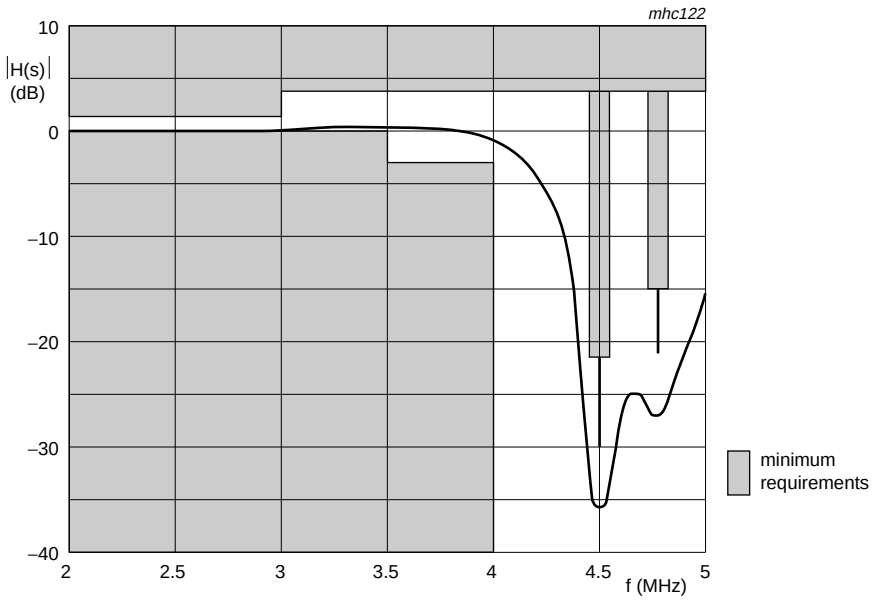
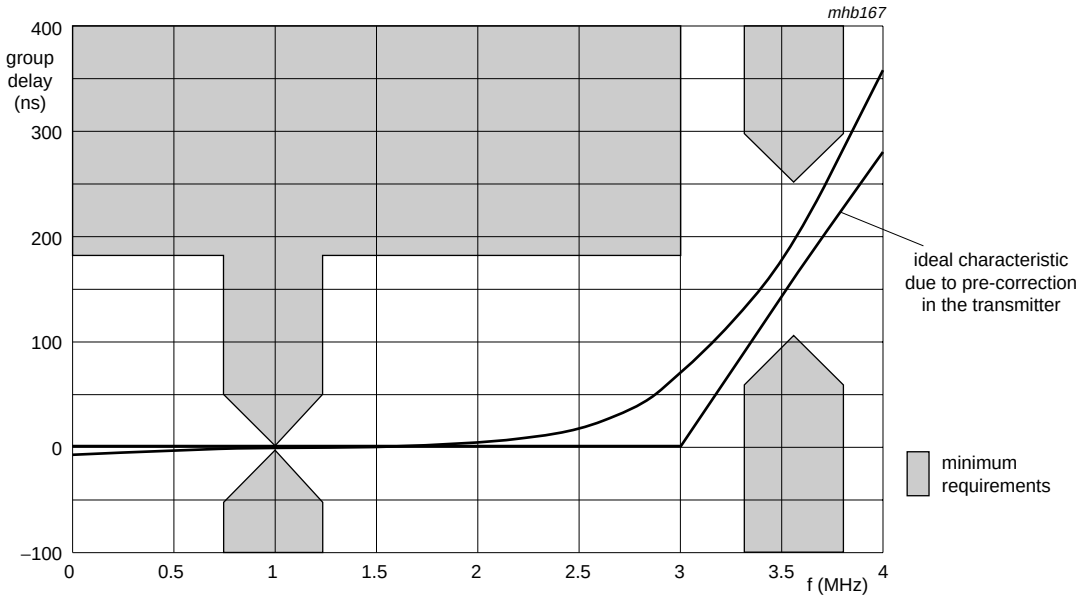


Fig 16. Typical amplitude response for sound trap at M/N standard (including Korea)



Overall delay is not shown, here the maximum ripple is specified.

Fig 17. Typical group delay for sound trap at M/N standard

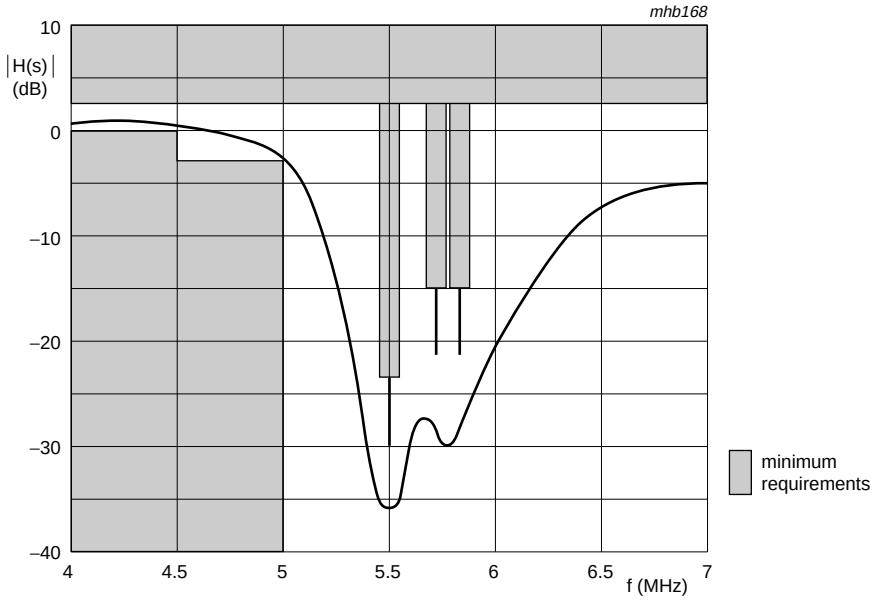
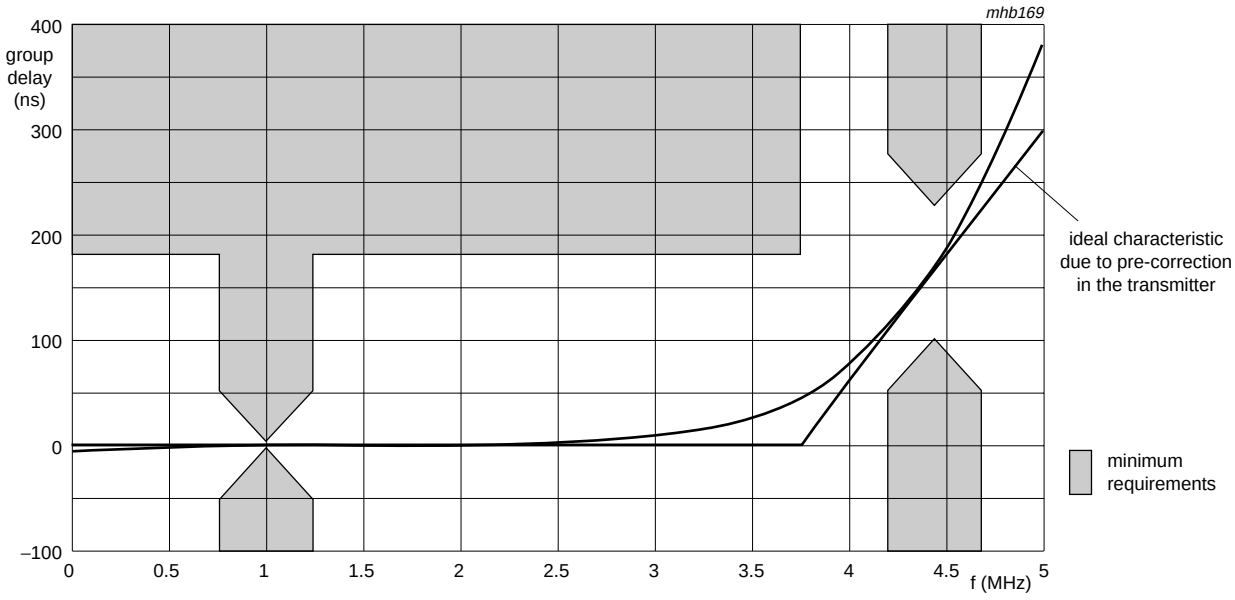


Fig 18. Typical amplitude response for sound trap at B/G standard



Overall delay is not shown, here the maximum ripple is specified.

Fig 19. Typical group delay for sound trap at B/G standard

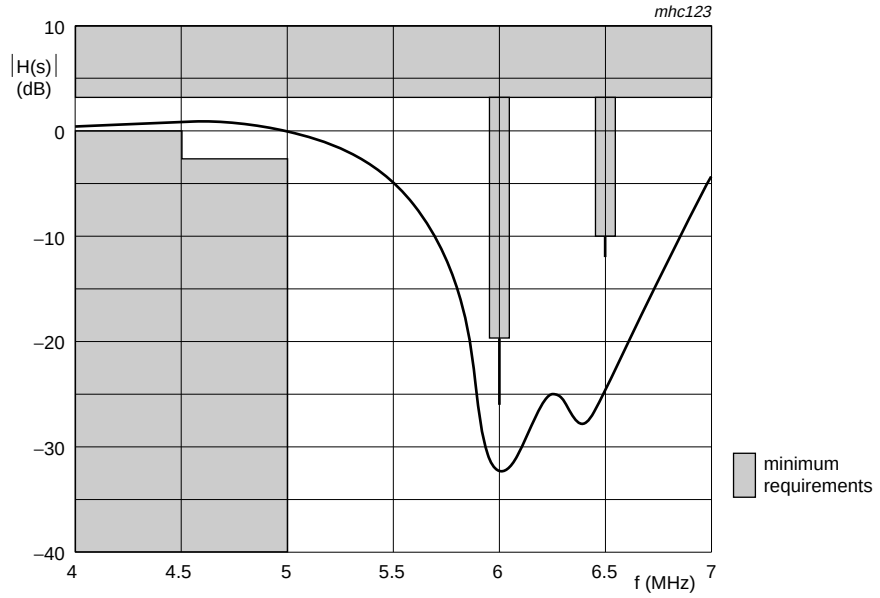


Fig 20. Typical amplitude response for sound trap at I standard

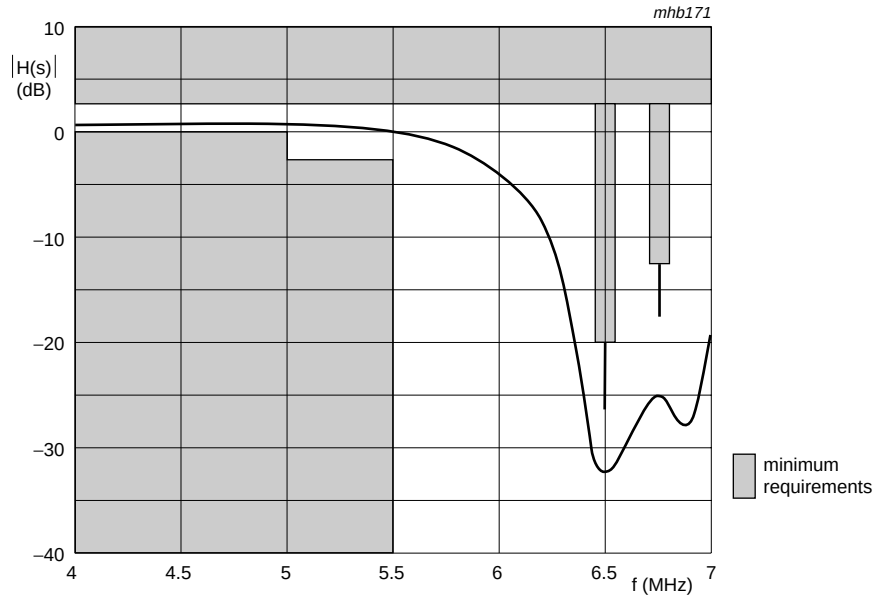
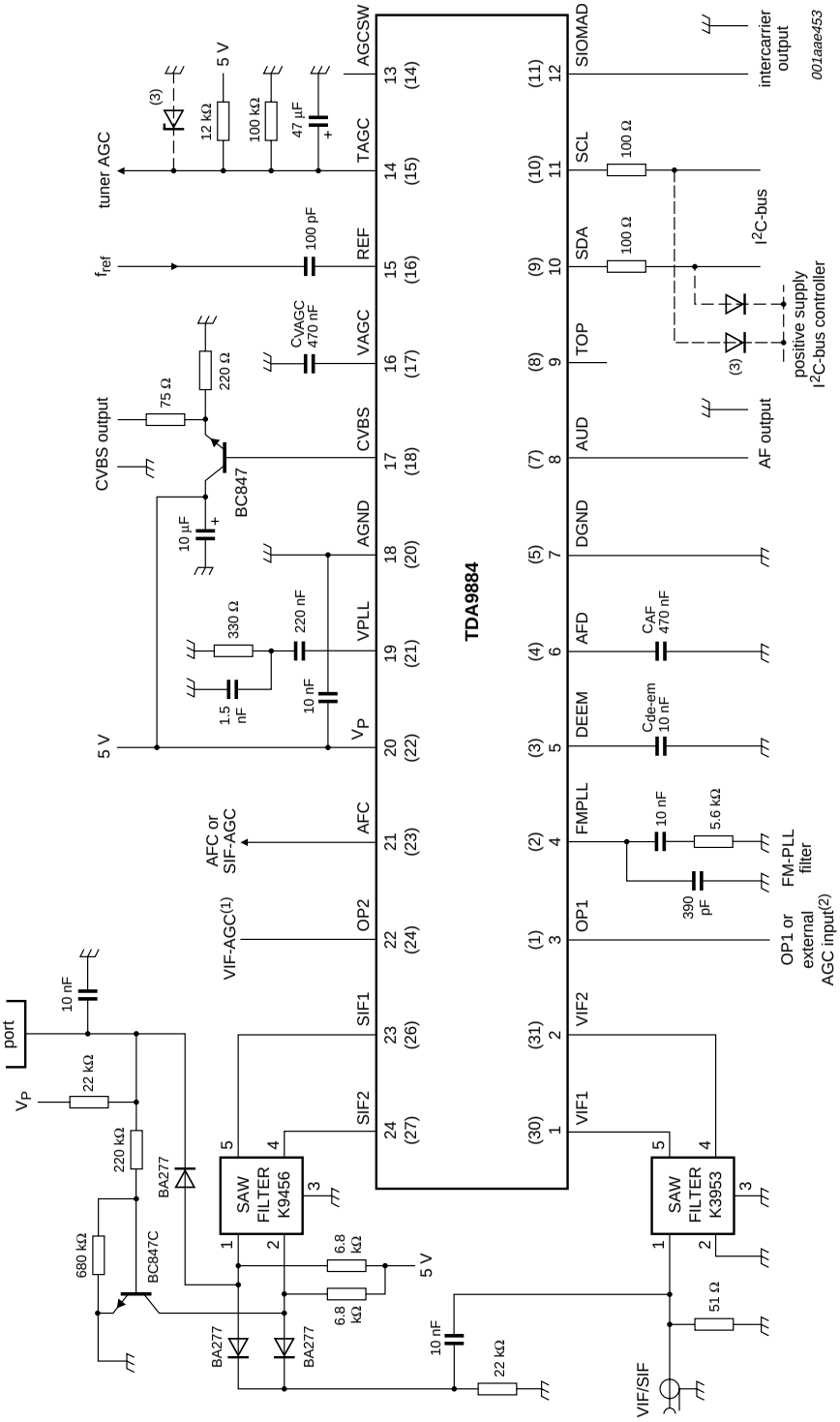


Fig 21. Typical amplitude response for sound trap at D/K standard

12. Application information



Pin numbers for TDA9884HN in parentheses.

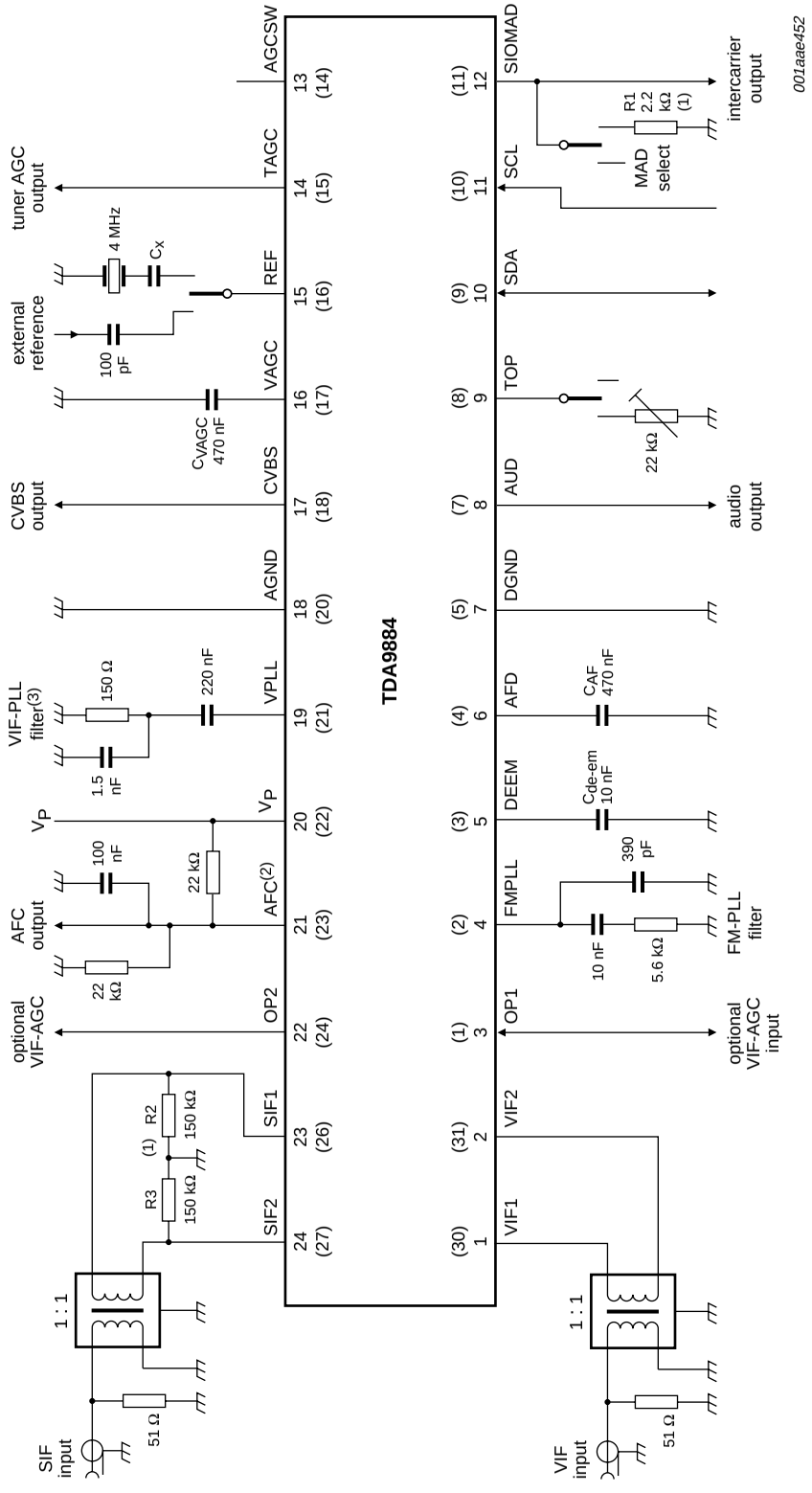
(1) See Table note 15 of Table 25.

(2) See Table note 19 of Table 25.

(3) Optional measures to improve ESD performance within a TV-set application.

Fig 22. Application circuit

13. Test information



Pin numbers for TDA9884HN in parentheses.

(1) Optional for I²C-bus address selection; see Table 28.

(2) SIF-AGC monitor output at pin AFC.

(3) Different VIF loop filter in comparison with the application circuit due to different input characteristics (SAW filter or transformer).

Fig 23. Test circuit

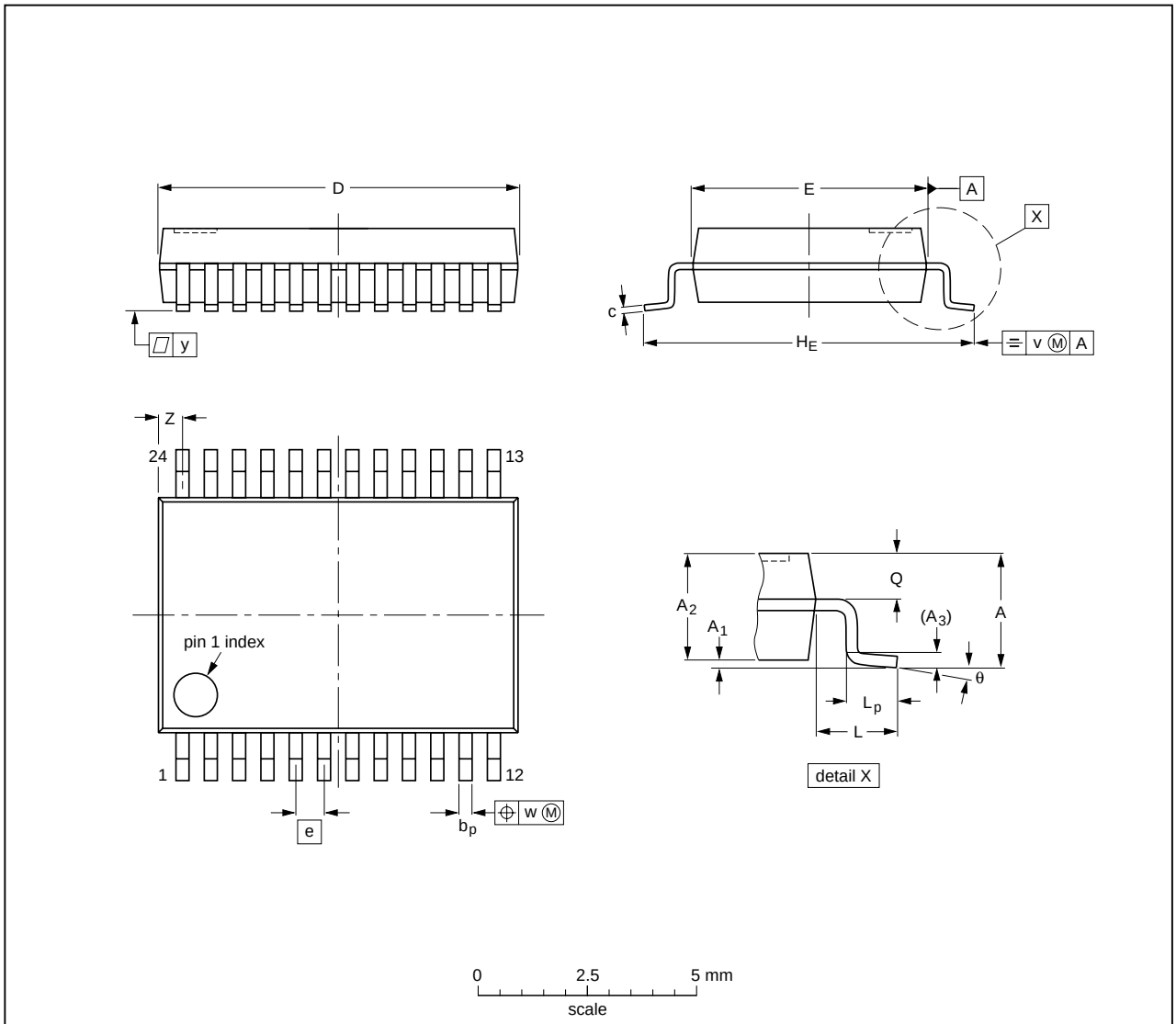
Table 28. I²C-bus address selection[1]

Option	R1 not used	R1 = 2.2 kΩ
R2 and R3 not used	1000 011S	1000 010S
R2 = R3 = 150 kΩ	1001 011S	1001 010S

[1] S = R/$\overline{W}$ selection bit.

14. Package outline

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

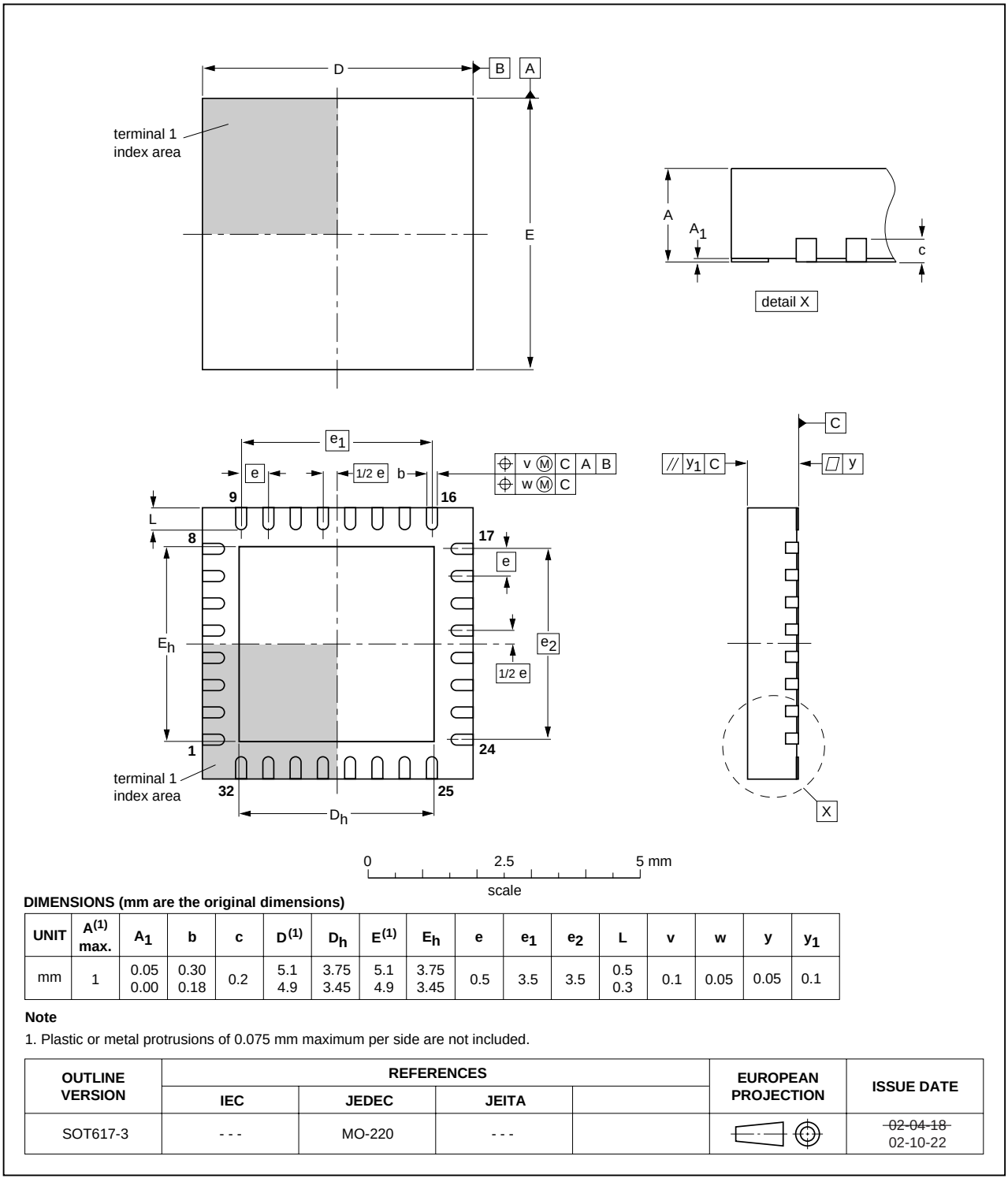
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

Fig 24. Package outline SOT340-1 (SSOP24)

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.75 3.45	5.1 4.9	3.75 3.45	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-3	- - -	MO-220	- - -			~~02-04-18~~ 02-10-22

Fig 25. Package outline SOT617-3 (HVQFN32)

15. Soldering

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 260 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

15.5 Package related soldering information

Table 29. Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

16. Abbreviations

Table 30. Abbreviations

Acronym	Description
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
FPLL	Frequency Phase-Locked Loop
MAD	Module Address
NTSC	National Television Standards Committee
PAL	Phase Alternating Line
PLL	Phase-Locked Loop
QSS	Quasi Split Sound
SECAM	Sequentiel Couleur avec Memoire
SIF	Sound Intermediate Frequency
TOP	TakeOver Point
VCO	Voltage-Controlled Oscillator
VIF	Vision Intermediate Frequency
VSB	Vestigial Side Band

17. Revision history

Table 31. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA9884_2	20060512	Product data sheet	-	TDA9884TS_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors • Added type number TDA9884HN • Table 25: inserted the value for t_{resp}, FM or AM fast step, mobile mode, increasing			
TDA9884TS_1	20031128	Product specification	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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