



CYPRESS

CY7C1380CV25  
CY7C1382CV25

# 18-Mbit (512K x 36/1M x 18) Pipelined SRAM

## Features

- Supports bus operation up to 250 MHz
- Available speed grades are 250, 225, 200, 166 and 133 MHz
- Registered inputs and outputs for pipelined operation
- 2.5V core power supply
- Fast clock-to-output times
  - 2.6 ns (for 250-MHz device)
  - 2.8 ns (for 225-MHz device)
  - 3.0 ns (for 200-MHz device)
  - 3.4 ns (for 166-MHz device)
  - 4.2 ns (for 133-MHz device)
- Provide high-performance 3-1-1-1 access rate
- User-selectable burst counter supporting Intel® Pentium interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed writes
- Asynchronous output enable
- Single Cycle Chip Deselect
- Offered in JEDEC-standard 100-pin TQFP, 119-ball BGA and 165-Ball fBGA packages
- IEEE 1149.1 JTAG-Compatible Boundary Scan
- “ZZ” Sleep Mode Option

## Functional Description<sup>[1]</sup>

The CY7C1380CV25/CY7C1382CV25 SRAM integrates 524,288 x 36 and 1,048,576 x 18 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ( $\overline{CE}_1$ ), depth-expansion Chip Enables ( $\overline{CE}_2$  and  $\overline{CE}_3$  [2]), Burst Control inputs ( $\overline{ADSC}$ ,  $\overline{ADSP}$ , and  $\overline{ADV}$ ), Write Enables ( $\overline{BW}_x$ , and  $\overline{BWE}$ ), and Global Write ( $\overline{GW}$ ). Asynchronous inputs include the Output Enable ( $\overline{OE}$ ) and the ZZ pin.

Addresses and chip enables are registered at rising edge of clock when either Address Strobe Processor ( $\overline{ADSP}$ ) or Address Strobe Controller ( $\overline{ADSC}$ ) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin ( $\overline{ADV}$ ).

Address, data inputs, and write controls are registered on-chip to initiate a self-timed Write cycle. This part supports Byte Write operations (see Pin Descriptions and Truth Table for further details). Write cycles can be one to two or four bytes wide as controlled by the byte write control inputs.  $\overline{GW}$  when active LOW causes all bytes to be written.

The CY7C1380CV25/CY7C1382CV25 operates from a +2.5V core power supply. All outputs also operate with a +2.5 supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

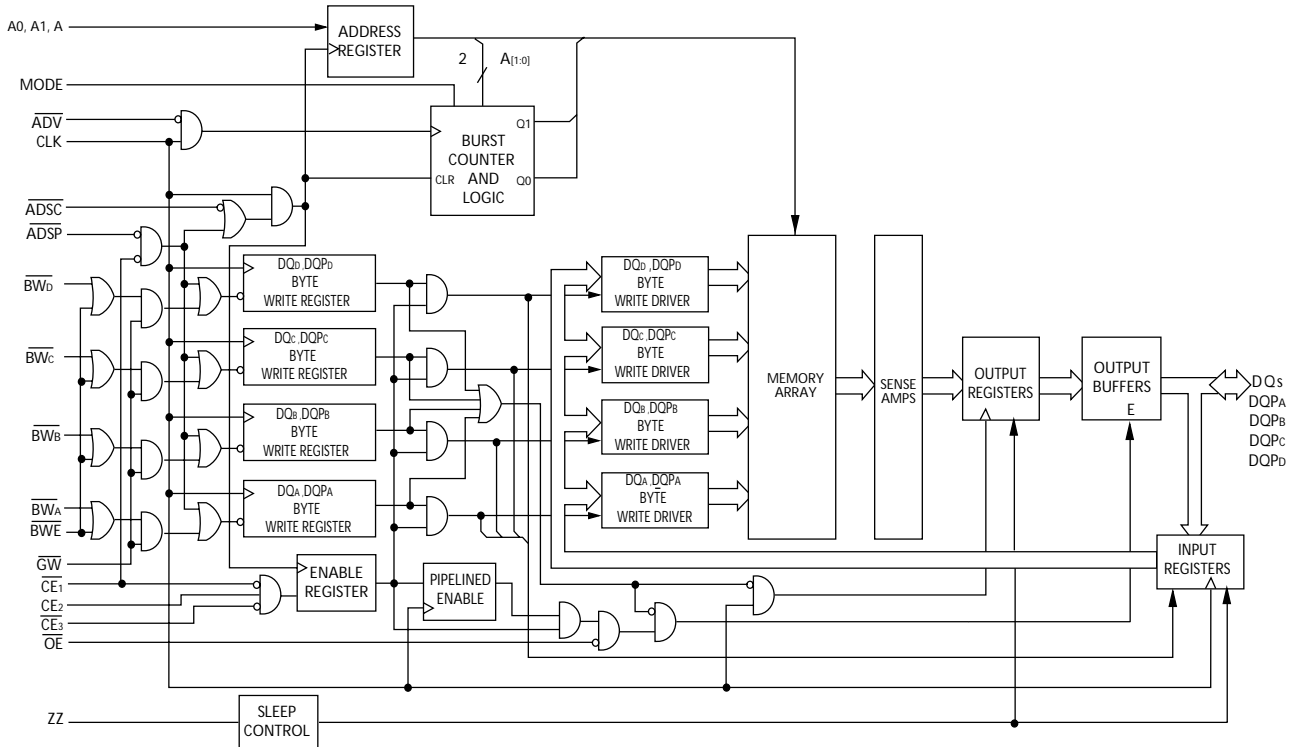
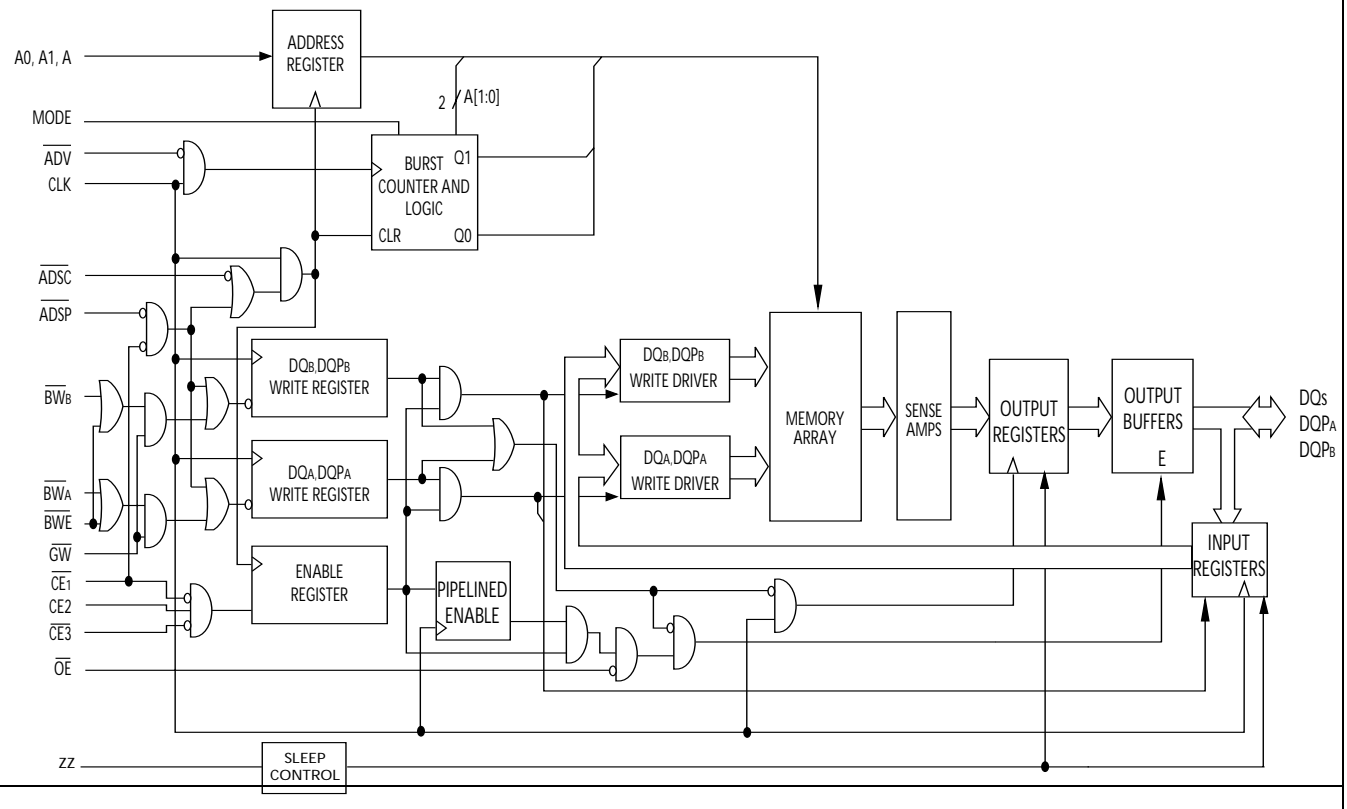
## Selection Guide

	250 MHz	225 MHz	200 MHz	167 MHz	133 MHz	Unit
Maximum Access Time	2.6	2.8	3.0	3.4	4.2	ns
Maximum Operating Current	350	325	300	275	245	mA
Maximum CMOS Standby Current	70	70	70	70	70	mA

Shaded areas contain advance information. Please contact your local Cypress sales representative for availability of these parts.

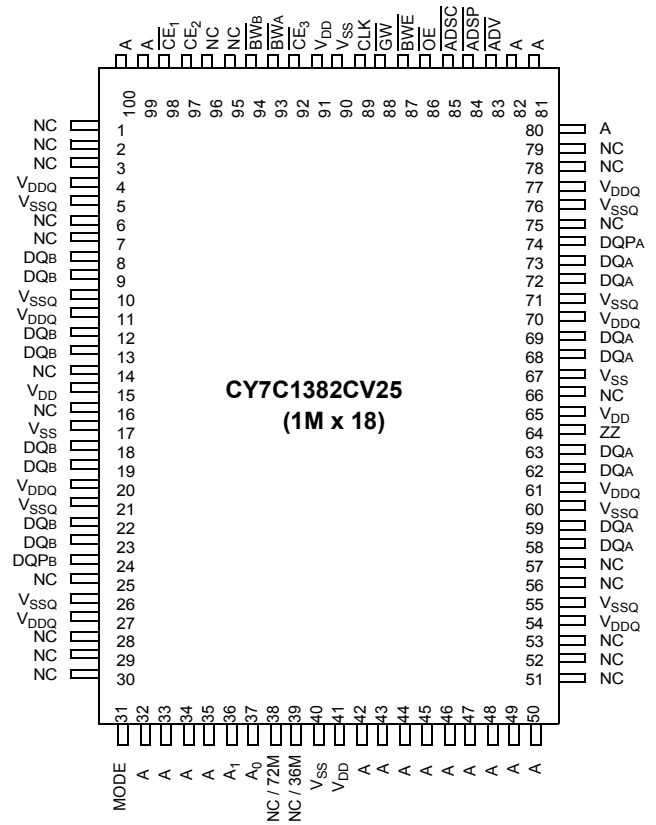
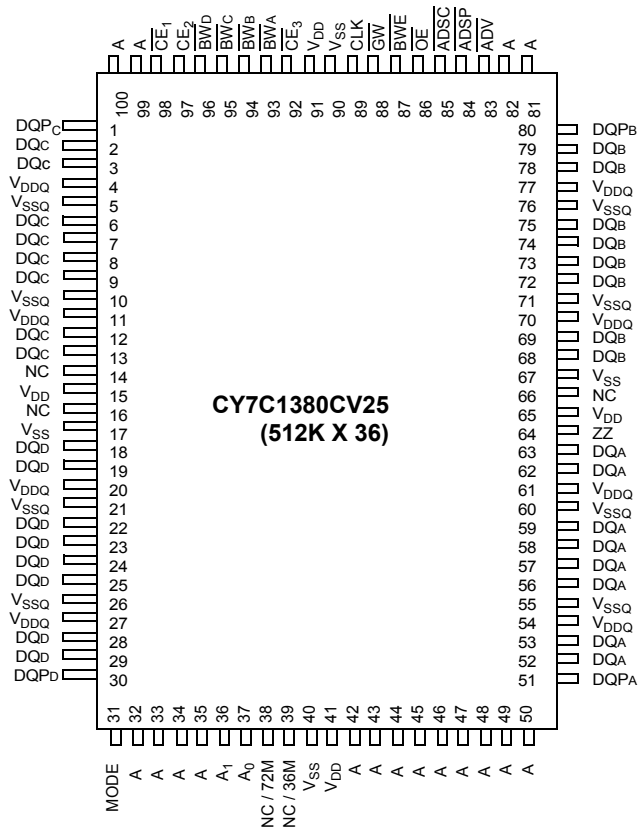
### Notes:

1. For best-practices recommendations, please refer to the Cypress application note *System Design Guidelines* on [www.cypress.com](http://www.cypress.com).
2.  $\overline{CE}_3$ ,  $\overline{CE}_2$  are for TQFP and 165 fBGA package only. 119 BGA is offered only in 1 Chip Enable.

**Logic Block Diagram – CY7C1380CV25 (512K x 36)**

**Logic Block Diagram – CY7C1382CV25 (1M x 18)**


Pin Configurations

100-pin TQFP Pinout



**Pin Configurations** (continued)

**119-ball BGA (1 Chip Enable with JTAG)**
**CY7C1380CV25 (512K x 36)**

	1	2	3	4	5	6	7
<b>A</b>	V <sub>DDQ</sub>	A	A	$\overline{\text{ADSP}}$	A	A	V <sub>DDQ</sub>
<b>B</b>	NC	A	A	$\overline{\text{ADSC}}$	A	A	NC
<b>C</b>	NC	A	A	V <sub>DD</sub>	A	A	NC
<b>D</b>	DQ <sub>C</sub>	DQP <sub>C</sub>	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQP <sub>B</sub>	DQ <sub>B</sub>
<b>E</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>SS</sub>	$\overline{\text{CE}}_1$	V <sub>SS</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>F</b>	V <sub>DDQ</sub>	DQ <sub>C</sub>	V <sub>SS</sub>	$\overline{\text{OE}}$	V <sub>SS</sub>	DQ <sub>B</sub>	V <sub>DDQ</sub>
<b>G</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	$\overline{\text{BW}}_C$	$\overline{\text{ADV}}$	$\overline{\text{BW}}_B$	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>H</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>SS</sub>	$\overline{\text{GW}}$	V <sub>SS</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>J</b>	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
<b>K</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>SS</sub>	CLK	V <sub>SS</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>L</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	$\overline{\text{BW}}_D$	NC	$\overline{\text{BW}}_A$	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>M</b>	V <sub>DDQ</sub>	DQ <sub>D</sub>	V <sub>SS</sub>	$\overline{\text{BWE}}$	V <sub>SS</sub>	DQ <sub>A</sub>	V <sub>DDQ</sub>
<b>N</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>SS</sub>	A1	V <sub>SS</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>P</b>	DQ <sub>D</sub>	DQP <sub>D</sub>	V <sub>SS</sub>	A0	V <sub>SS</sub>	DQP <sub>A</sub>	DQ <sub>A</sub>
<b>R</b>	NC	A	MODE	V <sub>DD</sub>	NC	A	NC
<b>T</b>	NC	NC / 72M	A	A	A	NC / 36M	ZZ
<b>U</b>	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	NC	V <sub>DDQ</sub>

**CY7C1382CV25 (1M x 18)**

	1	2	3	4	5	6	7
<b>A</b>	V <sub>DDQ</sub>	A	A	$\overline{\text{ADSP}}$	A	A	V <sub>DDQ</sub>
<b>B</b>	NC	A	A	$\overline{\text{ADSC}}$	A	A	NC
<b>C</b>	NC	A	A	V <sub>DD</sub>	A	A	NC
<b>D</b>	DQ <sub>B</sub>	NC	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQP <sub>A</sub>	NC
<b>E</b>	NC	DQ <sub>B</sub>	V <sub>SS</sub>	$\overline{\text{CE}}_1$	V <sub>SS</sub>	NC	DQ <sub>A</sub>
<b>F</b>	V <sub>DDQ</sub>	NC	V <sub>SS</sub>	$\overline{\text{OE}}$	V <sub>SS</sub>	DQ <sub>A</sub>	V <sub>DDQ</sub>
<b>G</b>	NC	DQ <sub>B</sub>	$\overline{\text{BW}}_B$	$\overline{\text{ADV}}$	V <sub>SS</sub>	NC	DQ <sub>A</sub>
<b>H</b>	DQ <sub>B</sub>	NC	V <sub>SS</sub>	$\overline{\text{GW}}$	V <sub>SS</sub>	DQ <sub>A</sub>	NC
<b>J</b>	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
<b>K</b>	NC	DQ <sub>B</sub>	V <sub>SS</sub>	CLK	V <sub>SS</sub>	NC	DQ <sub>A</sub>
<b>L</b>	DQ <sub>B</sub>	NC	V <sub>SS</sub>	NC	$\overline{\text{BW}}_A$	DQ <sub>A</sub>	NC
<b>M</b>	V <sub>DDQ</sub>	DQ <sub>B</sub>	V <sub>SS</sub>	$\overline{\text{BWE}}$	V <sub>SS</sub>	NC	V <sub>DDQ</sub>
<b>N</b>	DQ <sub>B</sub>	NC	V <sub>SS</sub>	A1	V <sub>SS</sub>	DQ <sub>A</sub>	NC
<b>P</b>	NC	DQP <sub>B</sub>	V <sub>SS</sub>	A0	V <sub>SS</sub>	NC	DQ <sub>A</sub>
<b>R</b>	NC	A	MODE	V <sub>DD</sub>	NC	A	NC
<b>T</b>	NC / 72M	A	A	NC / 36M	A	A	ZZ
<b>U</b>	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	NC	V <sub>DDQ</sub>



**Pin Configurations** (continued)

**165-ball fBGA**  
**CY7C1380CV25 (512K x 36)**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	NC / 288M	A	$\overline{CE}_1$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
<b>B</b>	NC	A	CE2	$\overline{BW}_D$	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC / 144M
<b>C</b>	DQP <sub>C</sub>	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	DQP <sub>B</sub>
<b>D</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>E</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>F</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>G</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>H</b>	NC	V <sub>SS</sub>	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC	NC	ZZ
<b>J</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>K</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>L</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>M</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>N</b>	DQP <sub>D</sub>	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	NC	A	NC	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	DQP <sub>A</sub>
<b>P</b>	NC	NC / 72M	A	A	TDI	A1	TDO	A	A	A	A
<b>R</b>	MODE	NC / 36M	A	A	TMS	A0	TCK	A	A	A	A

**CY7C1382CV25 (1M x 18)**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	NC / 288M	A	$\overline{CE}_1$	$\overline{BW}_B$	NC	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	A
<b>B</b>	NC	A	CE2	NC	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC / 144M
<b>C</b>	NC	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	DQP <sub>A</sub>
<b>D</b>	NC	DQ <sub>B</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>A</sub>
<b>E</b>	NC	DQ <sub>B</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>A</sub>
<b>F</b>	NC	DQ <sub>B</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>A</sub>
<b>G</b>	NC	DQ <sub>B</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>A</sub>
<b>H</b>	NC	V <sub>SS</sub>	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC	NC	ZZ
<b>J</b>	DQ <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	NC
<b>K</b>	DQ <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	NC
<b>L</b>	DQ <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	NC
<b>M</b>	DQ <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	NC
<b>N</b>	DQP <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	NC	A	NC	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	NC
<b>P</b>	NC	NC / 72M	A	A	TDI	A1	TDO	A	A	A	A
<b>R</b>	MODE	NC / 36M	A	A	TMS	A0	TCK	A	A	A	A

**CY7C1380CV25–Pin Definitions**

Name	TQFP	BGA	fBGA	I/O	Description
A <sub>0</sub> , A <sub>1</sub> , A	37,36,32, 33,34,35, 42,43,44,45, 46,47,48, 49,50,81, 82,99,100	P4,N4, A2,B2, C2,R2, A3,B3,C3, T3,T4,A5,B5, C5, T5,A6,B6,C6,R6	R6,P6,A2, A10,B2, B10,N6,P3,P4, P8,P9,P10, P11,R3,R4,R8, R9,R10,R11	Input- Synchronous	<b>Address Inputs used to select one of the address locations.</b> Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and CE <sub>1</sub> , CE <sub>2</sub> , and CE <sub>3</sub> <sup>[2]</sup> are sampled active. A1:A0 are fed to the two-bit counter.
$\overline{BW_A}$ , $\overline{BW_B}$ $\overline{BW_C}$ , $\overline{BW_D}$	93,94,95, 96	L5,G5, G3,L3	B5,A5,A4, B4	Input- Synchronous	<b>Byte Write Select Inputs, active LOW.</b> Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	88	H4	B7	Input- Synchronous	<b>Global Write Enable Input, active LOW.</b> When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{BW_X}$ and $\overline{BWE}$ ).
$\overline{BWE}$	87	M4	A7	Input- Synchronous	<b>Byte Write Enable Input, active LOW.</b> Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	89	K4	B6	Input- Clock	<b>Clock Input.</b> Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
$\overline{CE_1}$	98	E4	A3	Input- Synchronous	<b>Chip Enable 1 Input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with CE <sub>2</sub> and CE <sub>3</sub> to select/deselect the device. $\overline{ADSP}$ is ignored if CE <sub>1</sub> is HIGH.
CE <sub>2</sub> <sup>[2]</sup>	97	-	B3	Input- Synchronous	<b>Chip Enable 2 Input, active HIGH.</b> Sampled on the rising edge of CLK. Used in conjunction with CE <sub>1</sub> and CE <sub>3</sub> to select/deselect the device.
$\overline{CE_3}$ <sup>[2]</sup>	92	-	A6	Input- Synchronous	<b>Chip Enable 3 Input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with CE <sub>1</sub> and CE <sub>2</sub> to select/deselect the device. Not available for AJ package version. Not connected for BGA. Where referenced, CE <sub>3</sub> is assumed active throughout this document for BGA.
$\overline{OE}$	86	F4	B8	Input- Asynchronous	<b>Output Enable, asynchronous input, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	83	G4	A9	Input- Synchronous	<b>Advance Input signal, sampled on the rising edge of CLK, active LOW.</b> When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	84	A4	B9	Input- Synchronous	<b>Address Strobe from Processor, sampled on the rising edge of CLK, active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. A1:A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ADSP}$ is ignored when CE <sub>1</sub> is deasserted HIGH.

**CY7C1380CV25–Pin Definitions** (continued)

Name	TQFP	BGA	fBGA	I/O	Description
ADSC	85	B4	A8	Input-Synchronous	<b>Address Strobe from Controller, sampled on the rising edge of CLK, active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. A1:A0 are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized.
ZZ	64	T7	H11	Input-Asynchronous	<b>ZZ “sleep” Input, active HIGH.</b> When asserted HIGH places the device in a non-time-critical “sleep” condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQs, DQPs	52,53,56,57,58,59,62,63,68,69,72,73,74,75,78,79,2,3,6,7,8,9,12,13,18,19,22,23,24,25,28,29,51,80,1,30	K6,L6,M6,N6,K7,L7,N7,P7,E6,F6,G6,H6,D7,E7,G7,H7,D1,E1,G1,H1,E2,F2,G2,H2,K1,L1,N1,P1,K2,L2,M2,N2,P6,D6,D2,P2	M11,L11,K11,J11,J10,K10,L10,M10,D10,E10,F10,G10,D11,E11,F11,G11,D1,E1,F1,G1,D2,E2,F2,G2,J1,K1,L1,M1,J2,K2,L2,M2,N11,C11,C1,N1	I/O-Synchronous	<b>Bidirectional Data I/O lines.</b> As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQs and DQP <sub>X</sub> are placed in a three-state condition.
V <sub>DD</sub>	15,41,65,91	J2,C4,J4,R4,J6	D4,D8,E4,E8,F4,F8,G4,G8,H4,H8,J4,J8,K4,K8,L4,L8,M4,M8	Power Supply	<b>Power supply inputs to the core of the device.</b>
V <sub>SS</sub>	17,40,67,90	D3,E3,F3,H3,K3,M3,N3,P3,D5,E5,F5,H5,K5,M5,N5,P5	C4,C5,C6,C7,C8,D5,D6,D7,E5,E6,E7,F5,F6,F7,G5,G6,G7,H2,H5,H6,H7,J5,J6,J7,K5,K6,K7,L5,L6,L7,M5,M6,M7,N4,N8	Ground	<b>Ground for the core of the device.</b>
V <sub>SSQ</sub>	5,10,21,26,55,60,71,76	-	-	I/O Ground	<b>Ground for the I/O circuitry.</b>

**CY7C1380CV25–Pin Definitions** (continued)

Name	TQFP	BGA	fBGA	I/O	Description
V <sub>DDQ</sub>	4,11,20,27,54, 61,70, 77	A1,F1,J1,M1,U1, A7,F7,J7,M7,U7	C3,C9,D3,D9, E3,E9,F3,F9,G 3, G9,J3,J9, K3,K9,L3, L9,M3,M9,N3, N9	I/O Power Supply	<b>Power supply for the I/O circuitry.</b>
MODE	31	R3	R1	Input- Static	<b>Selects Burst Order.</b> When tied to GND selects linear burst sequence. When tied to V <sub>DD</sub> or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull-up.
TDO	-	U5	P7	JTAG serial output Synchronous	<b>Serial data-out to the JTAG circuit.</b> Delivers data on the negative edge of TCK. If the JTAG feature is not being utilized, this pin should be disconnected. This pin is not available on TQFP packages.
TDI	-	U3	P5	JTAG serial input Synchronous	<b>Serial data-In to the JTAG circuit.</b> Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be disconnected or connected to V <sub>DD</sub> . This pin is not available on TQFP packages.
TMS	-	U2	R5	JTAG serial input Synchronous	<b>Serial data-In to the JTAG circuit.</b> Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be disconnected or connected to V <sub>DD</sub> . This pin is not available on TQFP packages.
TCK	-	U4	R7	JTAG-Clock	<b>Clock input to the JTAG circuitry.</b> If the JTAG feature is not being utilized, this pin must be connected to V <sub>SS</sub> . This pin is not available on TQFP packages.
NC	14,16,66, 39,38	B1,C1, R1,T1,T2,J3, D4, L4,J5,R5,6T, 6U, B7,C7, R7	A11,B1,C2, C10,H1,H3,H9 ,H10, N2,N5,N7,N10 ,P1,A1,B11,P2 ,R2,N6	-	<b>No Connects.</b> Not internally connected to the die

**CY7C1382CV25–Pin Definitions**

Name	TQFP	BGA	fBGA	I/O	Description
A <sub>0</sub> , A <sub>1</sub> , A	37,36,32, 33,34,35, 42,43,44, 45,46,47, 48,49,50, 80,81,82, 99,100	P4,N4, A2,B2, C2,R2, T2,A3, B3,C3, T3,A5, B5,C5, T5,A6, B6,C6, R6,T6	R6,P6,A2, A10,A11, B2,B10,P3,P4,N6,P 8,P9, P10,P11, R3,R4,R8,R9,R10, R11	Input- Synchronous	<b>Address Inputs used to select one of the address locations.</b> Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and CE <sub>1</sub> , CE <sub>2</sub> , and CE <sub>3</sub> are sampled active. A1: A0 are fed to the two-bit counter..
$\overline{BW}_A$ , $\overline{BW}_B$	93,94	G3,L5	B5,A4	Input- Synchronous	<b>Byte Write Select Inputs, active LOW.</b> Qualified with BWE to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.



**CY7C1382CV25–Pin Definitions** (continued)

Name	TQFP	BGA	fBGA	I/O	Description
$\overline{GW}$	88	H4	B7	Input-Synchronous	<b>Global Write Enable Input, active LOW.</b> When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $BW_X$ and BWE).
$\overline{BWE}$	87	M4	A7	Input-Synchronous	<b>Byte Write Enable Input, active LOW.</b> Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	89	K4	B6	Input-Clock	<b>Clock Input.</b> Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
$\overline{CE}_1$	98	E4	A3	Input-Synchronous	<b>Chip Enable 1 Input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_2$ and $\overline{CE}_3$ to select/deselect the device. ADSP is ignored if $\overline{CE}_1$ is HIGH.
$\overline{CE}_2$ [2]	97	-	B3	Input-Synchronous	<b>Chip Enable 2 Input, active HIGH.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
$\overline{CE}_3$ [2]	92	-	A6	Input-Synchronous	<b>Chip Enable 3 Input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_2$ to select/deselect the device. Not available for AJ package version. Not connected for BGA. Where referenced, $\overline{CE}_3$ is assumed active throughout this document for BGA.
$\overline{OE}$	86	F4	B8	Input-Asynchronous	<b>Output Enable, asynchronous input, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	83	G4	A9	Input-Synchronous	<b>Advance Input signal, sampled on the rising edge of CLK, active LOW.</b> When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	84	A4	B9	Input-Synchronous	<b>Address Strobe from Processor, sampled on the rising edge of CLK, active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. A1: A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ADSP}$ is ignored when $\overline{CE}_1$ is deasserted HIGH.
$\overline{ADSC}$	85	P4	A8	Input-Synchronous	<b>Address Strobe from Controller, sampled on the rising edge of CLK, active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. A1: A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.

**CY7C1382CV25–Pin Definitions** (continued)

Name	TQFP	BGA	fBGA	I/O	Description
ZZ	64	T7	H11	Input-Asynchronous	<b>ZZ “sleep” Input, active HIGH.</b> When asserted HIGH places the device in a non-time-critical “sleep” condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQs, DQPs	58,59,62, 63,68,69, 72,73,8,9, 12,13,18, 19,22,23, 74,24	P7,K7, G7,E7, F6,H6,L6,N6, D1, H1,L1, N1,E2, G2,K2, M2,D6, P2	J10,K10, L10,M10, D11,E11, F11,G11,J1,K1,L1,M1,D2,E2,F2, G2,C11,N1	I/O-Synchronous	<b>Bidirectional Data I/O lines.</b> As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQs and DQP <sub>X</sub> are placed in a three-state condition.
V <sub>DD</sub>	15,41,65, 91	C4,J2,J4,J6, R4	D4,D8,E4,E8,F4,F8, G4,G8,H4, H8,J4,J8, K4,K8,L4, L8,M4,M8	Power Supply	<b>Power supply inputs to the core of the device.</b>
V <sub>SS</sub>	17,40,67, 90	D3,D5, E5,E3,F3,F5, G5, H3,H5, K3,K5,L3,M3, M5, N3,N5, P3,P5	H2,C4,C5,C6,C7,C8 ,D5,D6,D7,E5,E6,E7 , F5,F6,F7, G5,G6,G7, H5,H6,H7,J5,J6,J7, K5,K6,K7, L5,L6,L7, M5,M6,M7,N4,N8	Ground	<b>Ground for the core of the device.</b>
V <sub>SSQ</sub>	5,10,21,26,55, 60,71, 76	-	-	I/O Ground	<b>Ground for the I/O circuitry.</b>
V <sub>DDQ</sub>	4,11,20,27,54, 61,70, 77	A1,A7,F1,F7, J1,J7,M1,M7, U1,U7	C3,C9,D3,D9,E3,E9 , F3,F9,G3, G9,J3,J9, K3,K9,L3, L9,M3,M9,N3,N9	I/O Power Supply	<b>Power supply for the I/O circuitry.</b>
MODE	31	R3	R1	Input-Static	<b>Selects Burst Order.</b> When tied to GND selects linear burst sequence. When tied to V <sub>DD</sub> or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull-up.
TDO	-	U5	P7	JTAG serial output Synchronous	<b>Serial data-out to the JTAG circuit.</b> Delivers data on the negative edge of TCK. If the JTAG feature is not being utilized, this pin should be left unconnected. This pin is not available on TQFP packages.
TDI	-	U3	P5	JTAG serial input Synchronous	<b>Serial data-In to the JTAG circuit.</b> Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be left floating or connected to V <sub>DD</sub> through a pull up resistor. This pin is not available on TQFP packages.

**CY7C1382CV25–Pin Definitions** (continued)

Name	TQFP	BGA	fBGA	I/O	Description
TMS	-	U2	R5	JTAG serial input Synchronous	<b>Serial data-In to the JTAG circuit.</b> Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be disconnected or connected to V <sub>DD</sub> . This pin is not available on TQFP packages.
TCK	-	U4	R7	JTAG-Clock	<b>Clock input to the JTAG circuitry.</b> If the JTAG feature is not being utilized, this pin must be connected to V <sub>SS</sub> . This pin is not available on TQFP packages.
NC	1,2,3,6,7, 14,16,25, 28,29,30, 38,39, 51,52,53, 56,57,66, 75,78,79, 95,96	B1,B7, C1,C7, D2,D4, D7,E1, E6,H2, F2,G1, G6,H7, J3,J5,K1, K6,L4,L2,L7, M6, N2,L7,P1,P6, R1, R5,R7, T1,T4,U6	A5,B1,B4, C1,C2,C10,D1,D10, E1,E10,F1, F10,G1, G10,H1,H3,H9,H10, J2,J11, K2, K11,L2,L1,M2,M11, N2,N7,N10, N5, N11,P1,A1, B11, P2,R2	-	<b>No Connects.</b> Not internally connected to the die.

**Functional Overview**

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise ( $t_{CO}$ ) is 3.0ns (200-MHz device).

The CY7C1380CV25/CY7C1382CV25 supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe (ADSP) or the Controller Address Strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte Write operations are qualified with the Byte Write Enable (BWE) and Byte Write Select (BW<sub>X</sub>) inputs. A Global Write Enable (GW) overrides all Byte Write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed Write circuitry.

Three synchronous Chip Selects ( $\overline{CE}_1$ , CE<sub>2</sub>,  $\overline{CE}_3$ ) and an asynchronous Output Enable ( $\overline{OE}$ ) provide for easy bank selection and output three-state control. ADSP is ignored if CE<sub>1</sub> is HIGH.

**Single Read Accesses**

This access is initiated when the following conditions are satisfied at clock rise: (1) ADSP or ADSC is asserted LOW, (2)  $\overline{CE}_1$ , CE<sub>2</sub>,  $\overline{CE}_3$  are all asserted active, and (3) the Write signals (GW, BWE) are all deserted HIGH.  $\overline{ADSP}$  is ignored if

$\overline{CE}_1$  is HIGH. The address presented to the address inputs (A) is stored into the address advancement logic and the Address Register while being presented to the memory array. The corresponding data is allowed to propagate to the input of the Output Registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within 3.0 ns (200-MHz device) if  $\overline{OE}$  is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always three-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the  $\overline{OE}$  signal. Consecutive single Read cycles are supported. Once the SRAM is deselected at clock rise by the chip select and either  $\overline{ADSP}$  or ADSC signals, its output will three-state immediately.

**Single Write Accesses Initiated by ADSP**

This access is initiated when both of the following conditions are satisfied at clock rise: (1) ADSP is asserted LOW, and (2) CE<sub>1</sub>, CE<sub>2</sub>, CE<sub>3</sub> are all asserted active. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The Write signals (GW, BWE, and BW<sub>X</sub>) and ADV inputs are ignored during this first cycle.

$\overline{ADSP}$ -triggered Write accesses require two clock cycles to complete. If GW is asserted LOW on the second clock rise, the data presented to the DQs inputs is written into the corresponding address location in the memory array. If GW is HIGH, then the Write operation is controlled by BWE and BW<sub>X</sub> signals. The CY7C1380CV25/CY7C1382CV25 provides Byte Write capability that is described in the Write Cycle Descriptions table. Asserting the Byte Write Enable input (BWE) with the selected Byte Write (BW<sub>X</sub>) input, will selectively write to only the desired bytes. Bytes not selected during a Byte Write operation will remain unaltered. A synchronous self-timed

Write mechanism has been provided to simplify the Write operations.

Because the CY7C1380CV25/CY7C1382CV25 is a common I/O device, the Output Enable (OE) must be deserted HIGH before presenting data to the DQs inputs. Doing so will three-state the output drivers. As a safety precaution, DQs are automatically three-stated whenever a Write cycle is detected, regardless of the state of OE.

### Single Write Accesses Initiated by ADSC

ADSC Write accesses are initiated when the following conditions are satisfied: (1) ADSC is asserted LOW, (2) ADSP is deserted HIGH, (3)  $\overline{CE}_1$ ,  $CE_2$ ,  $\overline{CE}_3$  are all asserted active, and (4) the appropriate combination of the Write inputs (GW, BWE, and  $BW_x$ ) are asserted active to conduct a Write to the desired byte(s). ADSC-triggered Write accesses require a single clock cycle to complete. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The ADV input is ignored during this cycle. If a global Write is conducted, the data presented to the DQs is written into the corresponding address location in the memory core. If a Byte Write is conducted, only the selected bytes are written. Bytes not selected during a Byte Write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify the Write operations.

Because the CY7C1380CV25/CY7C1382CV25 is a common I/O device, the Output Enable (OE) must be deserted HIGH before presenting data to the DQs inputs. Doing so will three-state the output drivers. As a safety precaution, DQs are automatically three-stated whenever a Write cycle is detected, regardless of the state of OE.

### Burst Sequences

The CY7C1380CV25/CY7C1382CV25 provides a two-bit wraparound counter, fed by A1: A0, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support

### ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
$I_{DDZZ}$	Snooze mode standby current	$ZZ \geq V_{DD} - 0.2V$		60mA	mA
$t_{ZZS}$	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
$t_{ZZREC}$	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns
$t_{ZZI}$	ZZ Active to snooze current	This parameter is sampled		$2t_{CYC}$	ns
$t_{RZZI}$	ZZ Inactive to exit snooze current	This parameter is sampled	0		ns

processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input.

### Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode.  $\overline{CE}_1$ ,  $CE_2$ ,  $\overline{CE}_3$ , ADSP, and ADSC must remain inactive for the duration of  $t_{ZZREC}$  after the ZZ input returns LOW.

Asserting ADV LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both Read and Write burst operations are supported.

### Interleaved Burst Address Table (MODE = Floating or VDD)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

### Linear Burst Address Table (MODE = GND)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

**Truth Table** [ 3, 4, 5, 6, 7, 8]

Operation	Add. Used	$\overline{CE}_1$	$CE_2$	$\overline{CE}_3$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect Cycle, Power-down	None	H	X	X	L	X	L	X	X	X	L-H	three-state
Deselect Cycle, Power-down	None	L	L	X	L	L	X	X	X	X	L-H	three-state
Deselect Cycle, Power-down	None	L	X	H	L	L	X	X	X	X	L-H	three-state
Deselect Cycle, Power-down	None	L	L	X	L	H	L	X	X	X	L-H	three-state
Deselect Cycle, Power-down	None	L	X	H	L	H	L	X	X	X	L-H	three-state
Snooze Mode, Power-down	None	X	X	X	H	X	X	X	X	X	X	three-state
READ Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L-H	three-state
WRITE Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L-H	three-state
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	three-state
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	three-state
WRITE Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	three-state
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	three-state
WRITE Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

**Truth Table for Read/Write** [5]

Function (CY7C1380CV25)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_D$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{BW}_A$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte A – (DQ <sub>A</sub> and DQP <sub>A</sub> )	H	L	H	H	H	L
Write Byte B – (DQ <sub>B</sub> and DQP <sub>B</sub> )	H	L	H	H	L	H
Write Bytes B, A	H	L	H	H	L	L
Write Byte C – (DQ <sub>C</sub> and DQP <sub>C</sub> )	H	L	H	L	H	H
Write Bytes C, A	H	L	H	L	H	L
Write Bytes C, B	H	L	H	L	L	H

**Notes:**

- X = "Don't Care." H = Logic HIGH, L = Logic LOW.
- $\overline{WRITE} = L$  when any one or more Byte Write enable signals and  $\overline{BWE} = L$  or  $\overline{GW} = L$ .  $\overline{WRITE} = H$  when all Byte write enable signals,  $\overline{BWE}$ ,  $\overline{GW} = H$ .
- The DQ pins are controlled by the current cycle and the OE signal. OE is asynchronous and is not sampled with the clock.
- $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$  are available only in the TQFP package. BGA package has only 2 chip selects  $\overline{CE}_1$  and  $\overline{CE}_2$ .
- The SRAM always initiates a read cycle when  $\overline{ADSP}$  is asserted, regardless of the state of  $\overline{GW}$ ,  $\overline{BWE}$ , or  $\overline{BW}_x$ . Writes may occur only on subsequent clocks after the  $\overline{ADSP}$  or with the assertion of  $\overline{ADSC}$ . As a result, OE must be driven HIGH prior to the start of the write cycle to allow the outputs to three-state. OE is a don't care for the remainder of the write cycle.
- OE is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are three-state when OE is inactive or when the device is deselected, and all data bits behave as output when OE is active (LOW).

**Truth Table for Read/Write** (continued)<sup>[5]</sup>

Function (CY7C1380CV25)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_D$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{BW}_A$
Write Bytes C, B, A	H	L	H	L	L	L
Write Byte D – (DQ <sub>D</sub> and DQP <sub>D</sub> )	H	L	L	H	H	H
Write Bytes D, A	H	L	L	H	H	L
Write Bytes D, B	H	L	L	H	L	H
Write Bytes D, B, A	H	L	L	H	L	L
Write Bytes D, C	H	L	L	L	H	H
Write Bytes D, C, A	H	L	L	L	H	L
Write Bytes D, C, B	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

**Truth Table for Read/Write**<sup>[5]</sup>

Function (CY7C1382CV25)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_B$	$\overline{BW}_A$
Read	H	H	X	X
Read	H	L	H	H
Write Byte A – (DQ <sub>A</sub> and DQP <sub>A</sub> )	H	L	H	L
Write Byte B – (DQ <sub>B</sub> and DQP <sub>B</sub> )	H	L	L	H
Write Bytes B, A	H	L	L	L
Write All Bytes	H	L	L	L
Write All Bytes	L	X	X	X

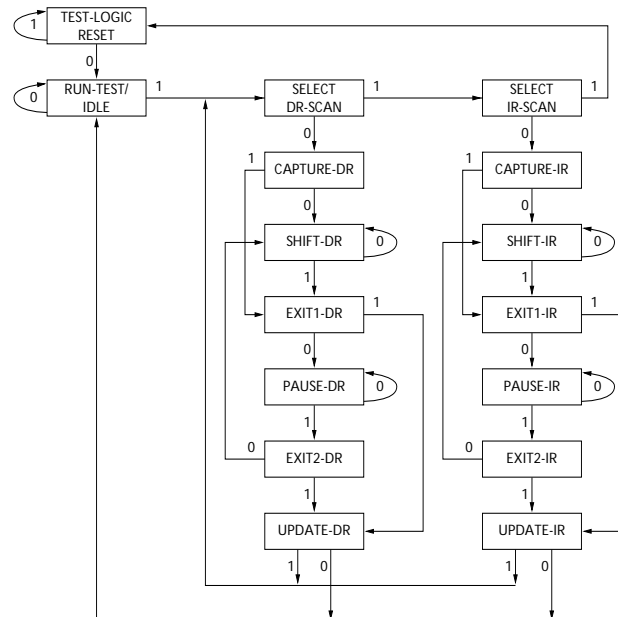
**IEEE 1149.1 Serial Boundary Scan (JTAG)**

The CY7C1380CV25/CY7C1382CV25 incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 2.5V I/O logic levels.

The CY7C1380CV25/CY7C1382CV25 contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

**Disabling the JTAG Feature**

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW(V<sub>ss</sub>) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V<sub>DD</sub> through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

**TAP Controller State Diagram**


The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

### Test Access Port (TAP)

#### Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

#### Test MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

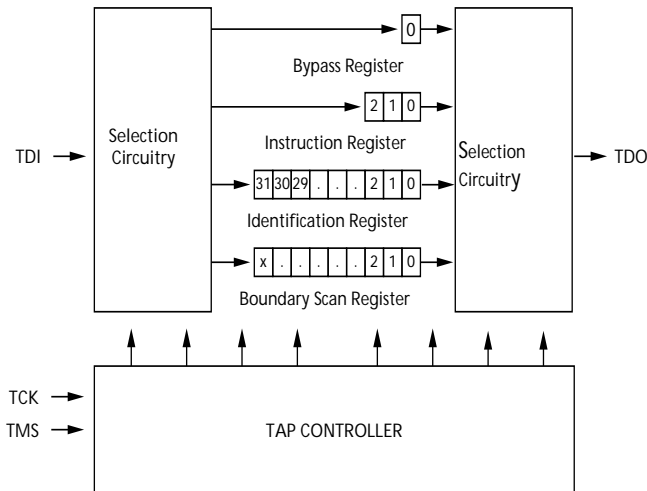
#### Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure . TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See Tap Controller Block Diagram.)

#### Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See Tap Controller State Diagram.)

### TAP Controller Block Diagram



#### Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (VDD) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

#### TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test

circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

#### Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the Tap Controller Block Diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

#### Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (Vss) when the BYPASS instruction is executed.

#### Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM. The SRAM has a 75-bit-long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

#### Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

#### TAP Instruction Set

##### Overview

Eight different instructions are possible with the three bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented.

The TAP controller cannot be used to load address data or control signals into the SRAM and cannot preload the I/O

buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

#### **EXTEST**

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1. The TAP controller does not recognize an all-0 instruction.

When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

#### **IDCODE**

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

#### **SAMPLE Z**

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

#### **SAMPLE/PRELOAD**

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1 compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time ( $t_{CS}$  plus  $t_{CH}$ ).

The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CLK captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO balls.

Note that since the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

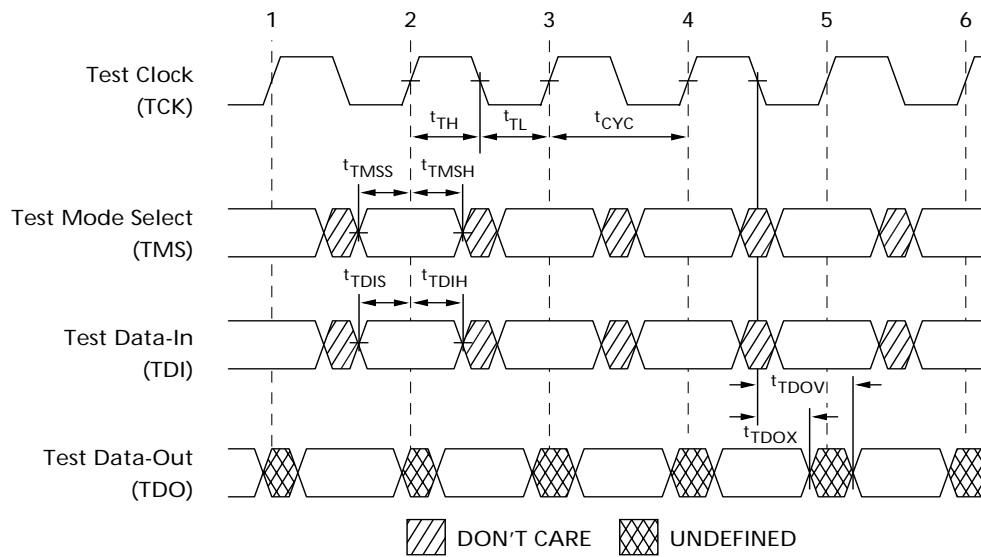
#### **BYPASS**

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.



**TAP Timing**

**TAP AC Switching Characteristics** Over the operating Range<sup>[9, 10]</sup>

Parameter	Description	Min.	Max.	Unit
<b>Clock</b>				
$t_{TCYC}$	TCK Clock Cycle Time	100		ns
$t_{TF}$	TCK Clock Frequency		10	MHz
$t_{TH}$	TCK Clock HIGH time	40		ns
$t_{TL}$	TCK Clock LOW time	40		ns
<b>Output Times</b>				
$t_{TDOV}$	TCK Clock LOW to TDO Valid		20	ns
$t_{TDOX}$	TCK Clock LOW to TDO Invalid	0		ns
<b>Set-up Times</b>				
$t_{TMSS}$	TMS Set-up to TCK Clock Rise	10		ns
$t_{TDIS}$	TDI Set-up to TCK Clock Rise	10		ns
$t_{CS}$	Capture Set-up to TCK Rise	10		
<b>Hold Times</b>				
$t_{TMSH}$	TMS hold after TCK Clock Rise	10		ns
$t_{TDIH}$	TDI Hold after Clock Rise	10		ns
$t_{CH}$	Capture Hold after Clock Rise	10		ns

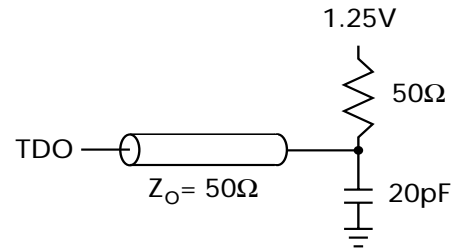
**Notes:**

9.  $t_{CS}$  and  $t_{CH}$  refer to the setup and hold time requirements of latching data from the boundary scan register.

10. Test conditions are specified using the load in TAP AC test Conditions.  $t_r/t_f = 1\text{ns}$ .

**2.5V TAP AC Test Conditions**

Input pulse levels .....  $V_{SS}$  to 2.5V  
 Input rise and fall time ..... 1 ns  
 Input timing reference levels ..... 1.25V  
 Output reference levels ..... 1.25V  
 Test load termination supply voltage ..... 1.25V

**2.5V TAP AC Output Load Equivalent**

**TAP DC Electrical Characteristics And Operating Conditions** ( $0^{\circ}\text{C} < T_A < +70^{\circ}\text{C}$ ;  $V_{DD} = 2.5\text{V} \pm 0.125\text{V}$  unless otherwise noted)<sup>[11]</sup>

Parameter	Description	Description	Conditions	Min.	Max.	Unit
$V_{OH1}$	Output HIGH Voltage	$I_{OH} = -1.0\text{ mA}$	$V_{DDQ} = 2.5\text{V}$	2.0		V
$V_{OH2}$	Output HIGH Voltage	$I_{OH} = -100\ \mu\text{A}$	$V_{DDQ} = 2.5\text{V}$	2.1		V
$V_{OL1}$	Output LOW Voltage	$I_{OL} = 8.0\text{ mA}$	$V_{DDQ} = 2.5\text{V}$		0.4	V
$V_{OL2}$	Output LOW Voltage	$I_{OL} = 100\ \mu\text{A}$	$V_{DDQ} = 2.5\text{V}$		0.2	V
$V_{IH}$	Input HIGH Voltage		$V_{DDQ} = 2.5\text{V}$	1.7	$V_{DD} + 0.3$	V
$V_{IL}$	Input LOW Voltage		$V_{DDQ} = 2.5\text{V}$	-0.3	0.7	V
$I_X$	Input Load Current	$GND \leq V_{IN} \leq V_{DDQ}$		-5	5	$\mu\text{A}$

**Identification Register Definitions**

Instruction Field	CY7C1380CV25 (512Kx36)	CY7C1382CV25 (1Mx18)	Description
Revision Number (31:29)	010	010	Describes the version number.
Device Depth (28:24)	01011	01011	Reserved for internal use.
Architecture/Memory type(23:18)	000000	000000	Defines memory type and architecture.
Bus Width/Density(17:12)	100101	010101	Defines width and density.
Cypress JEDEC ID Code (11:1)	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator (0)	1	1	Indicates the presence of an ID register.

**Scan Register Sizes**

Register Name	Bit Size (x36)	Bit Size (x18)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan Order	72	72

**Identification Codes**

Instruction	Code	Description
EXTTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1 compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.

**Note:**

11. All voltages referenced to  $V_{SS}$  (GND).

**Identification Codes** (continued)

Instruction	Code	Description
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1 compliant.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

**119-Ball BGA Boundary Scan Order**

CY7C1380CV25 (512K x 36)			
Bit#	Ball ID	Bit#	Ball ID
1	K4	37	B2
2	H4	38	P4
3	M4	39	N4
4	F4	40	R6
5	B4	41	T5
6	A4	42	T3
7	G4	43	R2
8	C6	44	R3
9	A6	45	P2
10	D6	46	P1
11	D7	47	N2
12	E6	48	L2
13	G6	49	K1
14	H7	50	N1
15	E7	51	M2
16	F6	52	L1
17	G7	53	K2
18	H6	54	Not Bonded (Preset to 1)
19	T7	55	H1
20	K7	56	G2
21	L6	57	E2
22	N6	58	D1
23	P7	59	H2
24	K6	60	G1
25	L7	61	F2
26	M6	62	E1
27	N7	63	D2
28	P6	64	A5
29	B5	65	A3
30	B3	66	E4
31	C5	67	Internal
32	C3	68	L3



**119-Ball BGA Boundary Scan Order** (continued)

33	C2	69	G3
34	A2	70	G5
35	T4	71	L5
36	B6	72	Internal

**CY7C1382CV25 (1M x 18)**

Bit#	Ball ID	Bit#	Ball ID
1	K4	37	B2
2	H4	38	P4
3	M4	39	N4
4	F4	40	R6
5	B4	41	T5
6	A4	42	T3
7	G4	43	R2
8	C6	44	R3
9	A6	45	Not Bonded (Preset to 0)
10	T6	46	Not Bonded (Preset to 0)
11	Not Bonded (Preset to 0)	47	Not Bonded (Preset to 0)
12	Not Bonded (Preset to 0)	48	Not Bonded (Preset to 0)
13	Not Bonded (Preset to 0)	49	P2
14	D6	50	N1
15	E7	51	M2
16	F6	52	L1
17	G7	53	K2
18	H6	54	Not Bonded (Preset to 1)
19	T7	55	H1
20	K7	56	G2
21	L6	57	E2
22	N6	58	D1
23	P7	59	Not Bonded (Preset to 0)
24	Not Bonded (Preset to 0)	60	Not Bonded (Preset to 0)
25	Not Bonded (Preset to 0)	61	Not Bonded (Preset to 0)
26	Not Bonded (Preset to 0)	62	Not Bonded (Preset to 0)
27	Not Bonded (Preset to 0)	63	Not Bonded (Preset to 0)
28	Not Bonded (Preset to 0)	64	A5
29	B5	65	A3
30	B3	66	E4
31	C5	67	Internal

**CY7C1382CV25 (1M x 18) (continued)**

Bit#	Ball ID	Bit#	Ball ID
32	C3	68	Not Bonded (Preset to 0)
33	C2	69	Internal
34	A2	70	G3
35	T2	71	L5
36	B6	72	Internal



**165-Ball fBGA Boundary Scan Order**

<b>CY7C1380CV25 (512K x 36)</b>			
<b>Bit#</b>	<b>Ball ID</b>	<b>Bit#</b>	<b>Ball ID</b>
1	B6	37	N6
2	B7	38	R6
3	A7	39	P6
4	B8	40	R4
5	A8	41	R3
6	B9	42	P4
7	A9	43	P3
8	B10	44	R1
9	A10	45	N1
10	C11	46	L2
11	E10	47	K2
12	F10	48	J2
13	G10	49	M2
14	D10	50	M1
15	D11	51	L1
16	E11	52	K1
17	F11	53	J1
18	G11	54	Not Bonded (Preset to 1)
19	H11	55	G2
20	J10	56	F2
21	K10	57	E2
22	L10	58	D2
23	M10	59	G1
24	J11	60	F1
25	K11	61	E1
26	L11	62	D1
27	M11	63	C1
28	N11	64	A2
29	R11	65	B2
30	R10	66	A3
31	R9	67	B3
<b>CY7C1380CV25 (512K x 36) (continued)</b>			
<b>Bit#</b>	<b>Ball ID</b>	<b>Bit#</b>	<b>Ball ID</b>
32	R8	68	B4
33	P10	69	A4
34	P9	70	A5
35	P8	71	B5
36	P11	72	A6
<b>CY7C1382CV25 (1M x 18)</b>			
<b>Bit#</b>	<b>Ball ID</b>	<b>Bit#</b>	<b>Ball ID</b>
1	B6	37	N6
2	B7	38	R6
3	A7	39	P6
4	B8	40	R4
5	A8	41	R3



**165-Ball fBGA Boundary Scan Order** (continued)

6	B9	42	P4
7	A9	43	P3
8	B10	44	R1
9	A10	45	Not Bonded (Preset to 0)
10	A11	46	Not Bonded (Preset to 0)
11	Not Bonded (Preset to 0)	47	Not Bonded (Preset to 0)
12	Not Bonded (Preset to 0)	48	Not Bonded (Preset to 0)
13	Not Bonded (Preset to 0)	49	N1
14	C11	50	M1
15	D11	51	L1
16	E11	52	K1
17	F11	53	J1
18	G11	54	Not Bonded (Preset to 1)
19	H11	55	G2
20	J10	56	F2
21	K10	57	E2
22	L10	58	D2
23	M10	59	Not Bonded (Preset to 0)
24	Not Bonded (Preset to 0)	60	Not Bonded (Preset to 0)
25	Not Bonded (Preset to 0)	61	Not Bonded (Preset to 0)
26	Not Bonded (Preset to 0)	62	Not Bonded (Preset to 0)
27	Not Bonded (Preset to 0)	63	Not Bonded (Preset to 0)
28	Not Bonded (Preset to 0)	64	A2
29	R11	65	B2
30	R10	66	A3
31	R9	67	B3
32	R8	68	Not Bonded (Preset to 0)
33	P10	69	Not Bonded (Preset to 0)
34	P9	70	A4
35	P8	71	B5
36	P11	72	A6



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature ..... -65°C to +150°C
- Ambient Temperature with Power Applied..... -55°C to +125°C
- Supply Voltage on V<sub>DD</sub> Relative to GND..... -0.3V to +4.6V
- DC Voltage Applied to Outputs in three-state ..... -0.5V to V<sub>DDQ</sub> + 0.5V

- DC Input Voltage ..... -0.5V to V<sub>DD</sub> + 0.5V
- Current into Outputs (LOW)..... 20 mA
- Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)
- Latch-up Current > 200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>DD</sub>	V <sub>DDQ</sub>
Commercial	0°C to +70°C	2.5V – 5%/+5%	2.5V – 5% to V <sub>DD</sub>
Industrial	-40°C to +85°C		

**Electrical Characteristics** Over the Operating Range [12, 13]

Parameter	Description	Test Conditions	Min.	Max.	Unit	
V <sub>DD</sub>	Power Supply Voltage		2.375	2.625	V	
V <sub>DDQ</sub>	I/O Supply Voltage	V <sub>DDQ</sub> = 2.5V	2.375	V <sub>DD</sub>	V	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>DDQ</sub> = 2.5V, V <sub>DD</sub> = Min., I <sub>OH</sub> = -1.0 mA	2.0		V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>DDQ</sub> = 2.5V, V <sub>DD</sub> = Min., I <sub>OL</sub> = 1.0 mA		0.4	V	
V <sub>IH</sub>	Input HIGH Voltage <sup>[12]</sup>	V <sub>DDQ</sub> = 2.5V	1.7	V <sub>DD</sub> + 0.3V	V	
V <sub>IL</sub>	Input LOW Voltage <sup>[12]</sup>	V <sub>DDQ</sub> = 2.5V	-0.3	0.7	V	
I <sub>X</sub>	Input Load Current except ZZ and MODE	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub>	-5	5	μA	
		Input = V <sub>SS</sub>	-30		μA	
		Input = V <sub>DD</sub>		5	μA	
		Input Current of ZZ	Input = V <sub>SS</sub>	-30		μA
		Input = V <sub>DD</sub>		5	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub> , Output Disabled	-5	5	μA	
I <sub>DD</sub>	V <sub>DD</sub> Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	4.0-ns cycle, 250 MHz		350	mA
			4.4-ns cycle, 225 MHz		325	mA
			5.0-ns cycle, 200 MHz		300	mA
			6.0-ns cycle, 167 MHz		275	mA
			7.5-ns cycle, 133 MHz		245	mA
I <sub>SB1</sub>	Automatic CE Power-down Current—TTL Inputs	V <sub>DD</sub> = Max, Device Deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	4.0-ns cycle, 250 MHz		120	mA
			4.4-ns cycle, 225 MHz		110	mA
			5.0-ns cycle, 200 MHz		100	mA
			6.0-ns cycle, 167 MHz		90	mA
			7.5-ns cycle, 133 MHz		85	mA
I <sub>SB2</sub>	Automatic CE Power-down Current—CMOS Inputs	V <sub>DD</sub> = Max, Device Deselected, V <sub>IN</sub> ≤ 0.3V or V <sub>IN</sub> ≥ V <sub>DDQ</sub> - 0.3V, f = 0	All speeds		70	mA
I <sub>SB3</sub>	Automatic CE Power-down Current—CMOS Inputs	V <sub>DD</sub> = Max, Device Deselected, or V <sub>IN</sub> ≤ 0.3V or V <sub>IN</sub> ≥ V <sub>DDQ</sub> - 0.3V, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	4.0-ns cycle, 250 MHz		105	mA
			4.4-ns cycle, 225 MHz		100	mA
			5.0-ns cycle, 200 MHz		95	mA
			6.0-ns cycle, 167 MHz		85	mA
			7.5-ns cycle, 133 MHz		80	mA
I <sub>SB4</sub>	Automatic CE Power-down Current—TTL Inputs	V <sub>DD</sub> = Max, Device Deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = 0	All speeds		80	mA

Shaded areas contain advance information.

**Notes:**

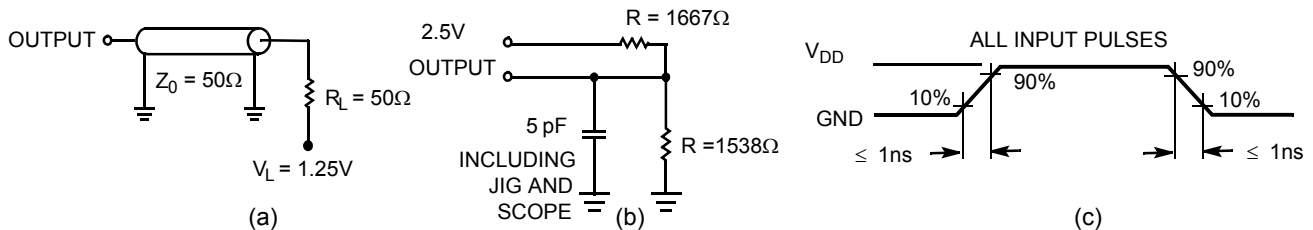
- 12. Overshoot: V<sub>IH</sub>(AC) < V<sub>DD</sub> + 1.5V (Pulse width less than t<sub>CYC</sub>/2), undershoot: V<sub>IL</sub>(AC) > -2V (Pulse width less than t<sub>CYC</sub>/2).
- 13. TPower-up: Assumes a linear ramp from 0v to V<sub>DD</sub>(min.) within 200ms. During this time V<sub>IH</sub> ≤ V<sub>DD</sub> and V<sub>DDQ</sub> ≤ V<sub>DD</sub>.

**Thermal Resistance<sup>[14]</sup>**

Parameter	Description	Test Conditions	TQFP Package	BGA Package	fBGA Package	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	31	45	46	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		6	7	3	°C/W

**Capacitance<sup>[14]</sup>**

Parameter	Description	Test Conditions	TQFP Package	BGA Package	fBGA Package	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{DD} = 2.5\text{V}$ , $V_{DDQ} = 2.5\text{V}$	5	8	9	pF
$C_{CLK}$	Clock Input Capacitance		5	8	9	pF
$C_{I/O}$	Input/Output Capacitance		5	8	9	pF

**AC Test Loads and Waveforms**
**2.5V I/O Test Load**

**Switching Characteristics Over the Operating Range<sup>[19, 20]</sup>**

Parameter	Description	250 MHz		225 MHz		200 MHz		167 MHz		133 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{POWER}$	$V_{DD}(\text{Typical})$ to the first Access <sup>[15]</sup>	1		1		1		1		1		ms
<b>Clock</b>												
$t_{CYC}$	Clock Cycle Time	4.0		4.4		5		6		7.5		ns
$t_{CH}$	Clock HIGH	1.7		2.0		2.0		2.2		2.5		ns
$t_{CL}$	Clock LOW	1.7		2.0		2.0		2.2		2.5		ns
<b>Output Times</b>												
$t_{CO}$	Data Output Valid After CLK Rise		2.6		2.8		3.0		3.4		4.2	ns
$t_{DOH}$	Data Output Hold After CLK Rise	1.0		1.0		1.3		1.3		1.3		ns
$t_{CLZ}$	Clock to Low-Z <sup>[16, 17, 18]</sup>	1.0		1.0		1.3		1.3		1.3		ns
$t_{CHZ}$	Clock to High-Z <sup>[16, 17, 18]</sup>		2.6		2.8		3.0		3.4		3.4	ns
$t_{OEV}$	$\overline{OE}$ LOW to Output Valid		2.6		2.8		3.0		3.4		4.2	ns
$t_{OELZ}$	$\overline{OE}$ LOW to Output Low-Z <sup>[16, 17, 18]</sup>	0		0		0		0		0		ns
$t_{OEZH}$	$\overline{OE}$ HIGH to Output High-Z <sup>[16, 17, 18]</sup>		2.6		2.8		3.0		3.4		4.0	ns

Shaded areas contain advance information.

**Notes:**

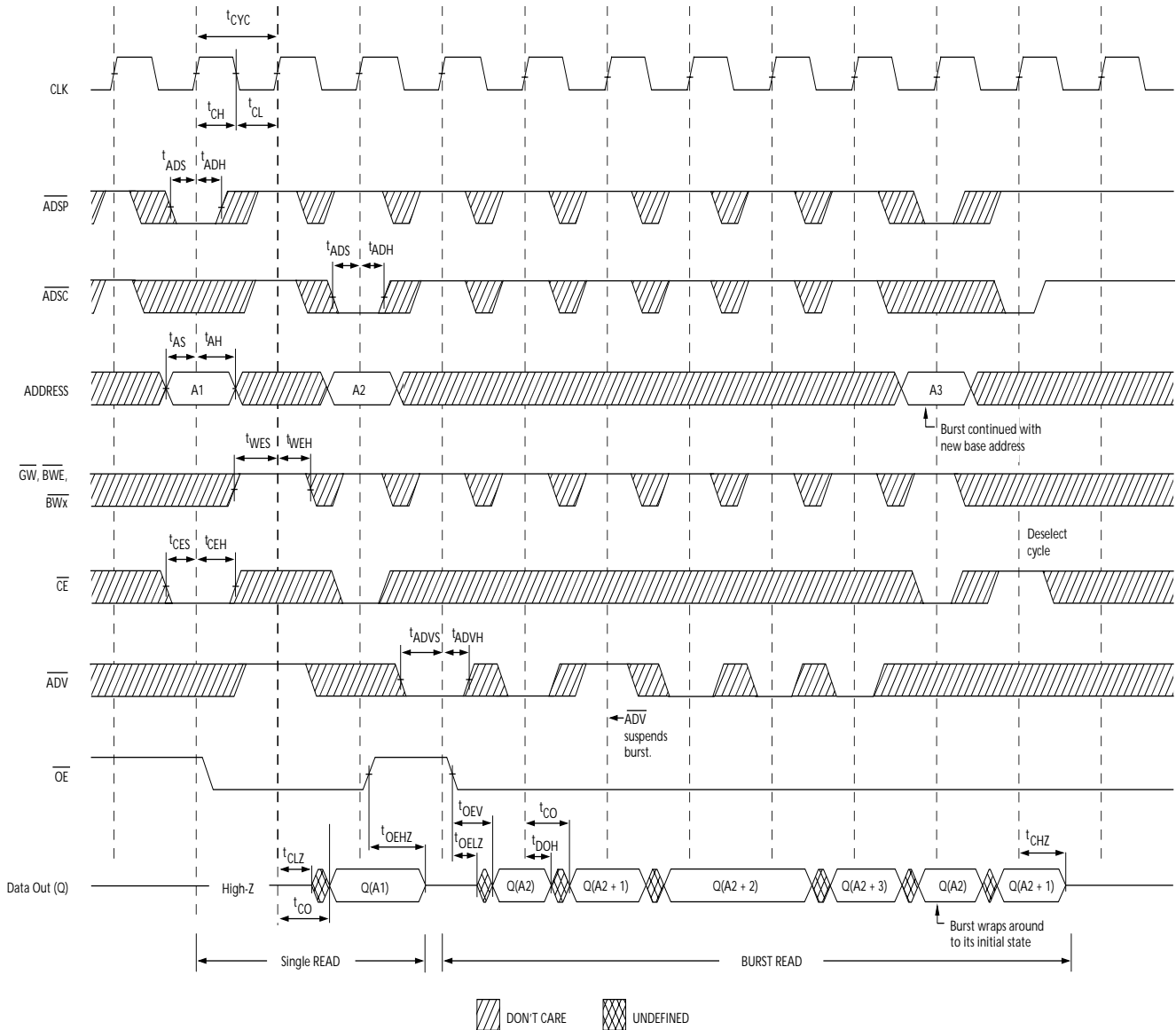
14. Tested initially and after any design or process change that may affect these parameters
15. This part has a voltage regulator internally;  $t_{POWER}$  is the time that the power needs to be supplied above  $V_{DD}(\text{minimum})$  initially before a read or write operation can be initiated.
16.  $t_{CHZ}$ ,  $t_{CLZ}$ ,  $t_{OELZ}$ , and  $t_{OEZH}$  are specified with AC test conditions shown in part (b) of AC Test Loads. Transition is measured  $\pm 200\text{ mV}$  from steady-state voltage.
17. At any given voltage and temperature,  $t_{OEZH}$  is less than  $t_{OELZ}$  and  $t_{CHZ}$  is less than  $t_{CLZ}$  to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions
18. This parameter is sampled and not 100% tested.
19. Timing reference level is 1.25V when  $V_{DDQ}=2.5\text{V}$ .
20. Test conditions shown in (a) of AC Test Loads unless otherwise noted.



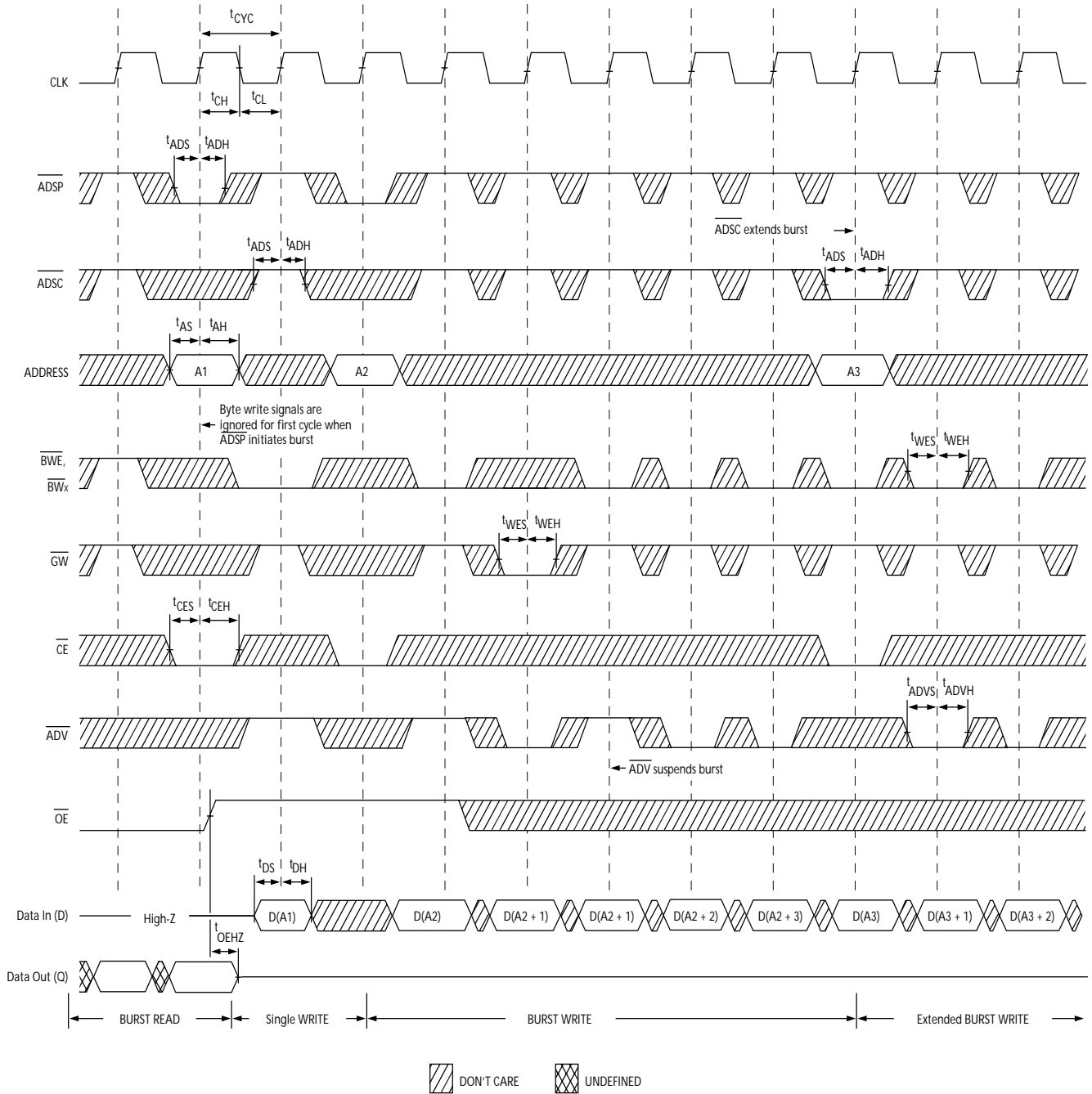


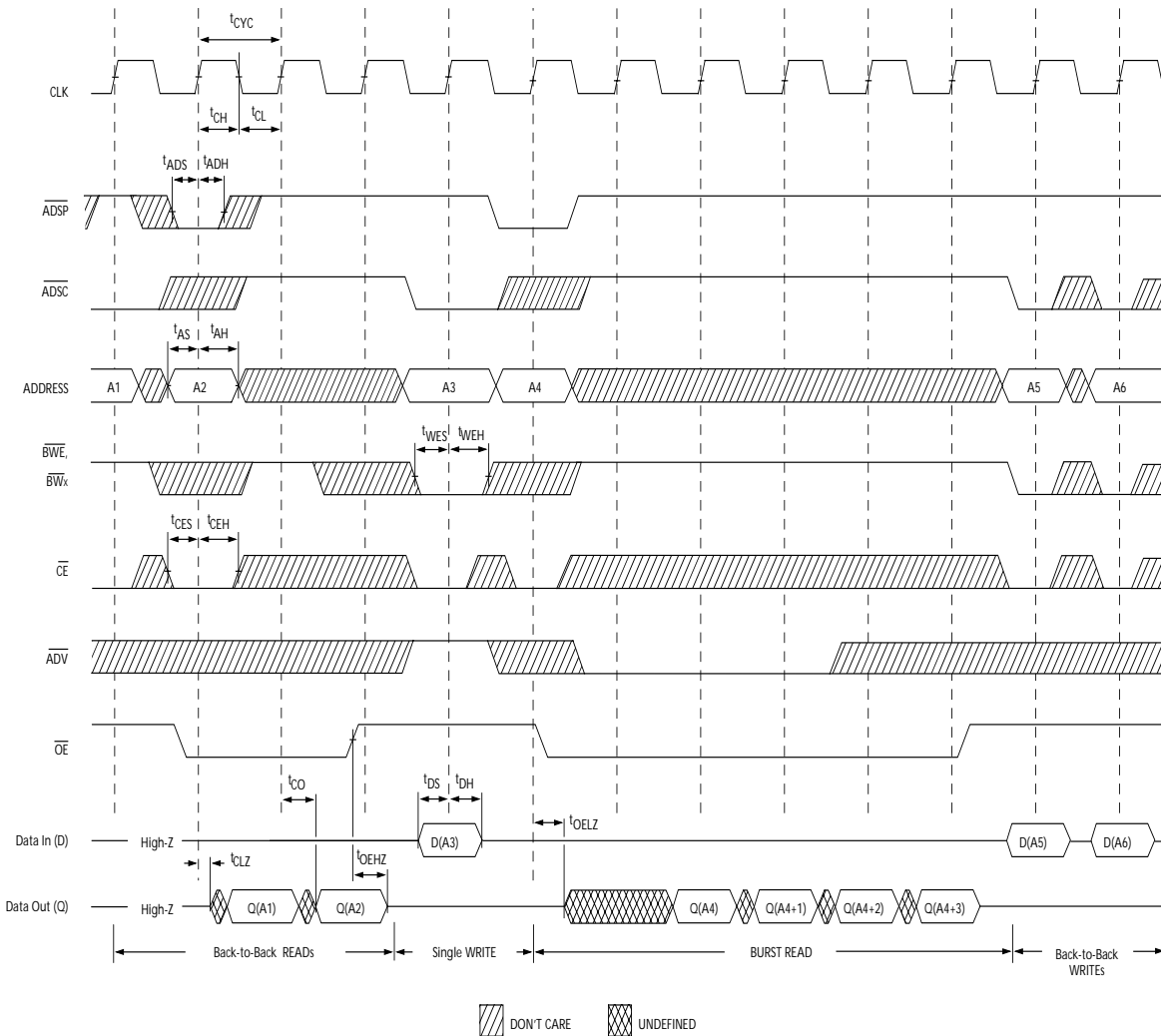
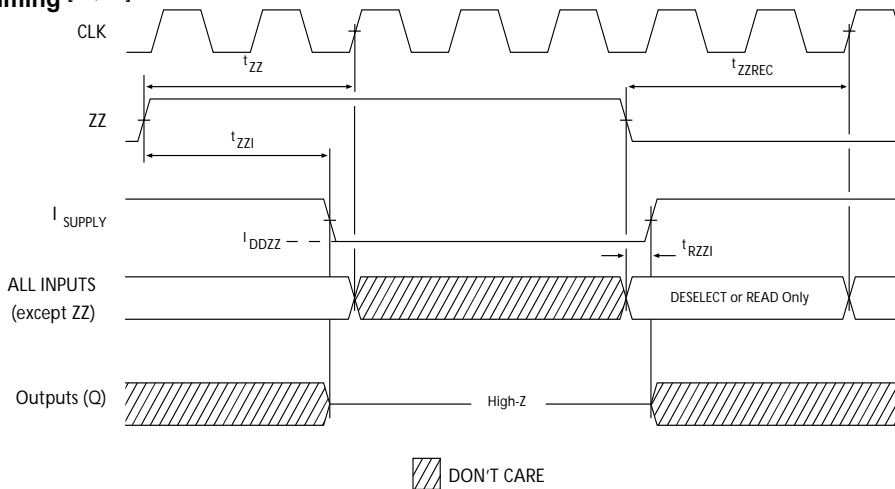
**Switching Characteristics** Over the Operating Range (continued)<sup>[19, 20]</sup>

Parameter	Description	250 MHz		225 MHz		200 MHz		167 MHz		133 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Set-up Times</b>												
t <sub>AS</sub>	Address Set-up Before CLK Rise	1.2		1.4		1.4		1.5		1.5		ns
t <sub>ADS</sub>	$\overline{ADSC}$ , $\overline{ADSP}$ Set-up Before CLK Rise	1.2		1.4		1.4		1.5		1.5		ns
t <sub>ADVS</sub>	$\overline{ADV}$ Set-up Before CLK Rise	1.2		1.4		1.4		1.5		1.5		ns
t <sub>WES</sub>	$\overline{GW}$ , $\overline{BWE}$ , $\overline{BW}_X$ Set-up Before CLK Rise	1.2		1.4		1.4		1.5		1.5		ns
t <sub>DS</sub>	Data Input Set-up Before CLK Rise	1.2		1.4		1.4		1.5		1.5		ns
t <sub>CES</sub>	Chip Enable Set-Up Before CLK Rise	1.2		1.4		1.4		1.5		1.5		ns
<b>Hold Times</b>												
t <sub>AH</sub>	Address Hold After CLK Rise	0.3		0.4		0.4		0.5		0.5		ns
t <sub>ADH</sub>	$\overline{ADSP}$ , $\overline{ADSC}$ Hold After CLK Rise	0.3		0.4		0.4		0.5		0.5		ns
t <sub>ADVH</sub>	$\overline{ADV}$ Hold After CLK Rise	0.3		0.4		0.4		0.5		0.5		ns
t <sub>WEH</sub>	$\overline{GW}$ , $\overline{BWE}$ , $\overline{BW}_X$ Hold After CLK Rise	0.3		0.4		0.4		0.5		0.5		ns
t <sub>DH</sub>	Data Input Hold After CLK Rise	0.3		0.4		0.4		0.5		0.5		ns
t <sub>CEH</sub>	Chip Enable Hold After CLK Rise	0.3		0.4		0.4		0.5		0.5		ns

**Switching Waveforms**
**Read Cycle Timing<sup>[21]</sup>**

**Notes:**

21. On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $CE_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW or  $\overline{CE}_3$  is HIGH.  
 22. Full width write can be initiated by either GW LOW; or by GW HIGH, BWE LOW and BW<sub>x</sub> LOW.

**Switching Waveforms (continued)**  
**Write Cycle Timing<sup>[21, 22]</sup>**


**Switching Waveforms (continued)**  
**Read/Write Cycle Timing<sup>[21, 23, 24]</sup>**

**ZZ Mode Timing<sup>[25, 26]</sup>**

**Notes:**

23. The data bus (Q) remains in high-Z following a WRITE cycle, unless a new read access is initiated by  $\overline{\text{ADSP}}$  or  $\overline{\text{ADSC}}$ .  
 24. GW is HIGH.

**Ordering Information**

Speed (MHz)	Ordering Code	Package Name	Part and Package Type	Operating Range
250	CY7C1380CV25-250AC CY7C1382CV25-250AC	A101	100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm)	Commercial
	CY7C1380CV25-250BGC CY7C1382CV25-250BGC	BG119	119 PBGA	
	CY7C1380CV25-250BZC CY7C1382CV25-250BZC	BB165A	165 fBGA	
225	CY7C1380CV25-225AC CY7C1382CV25-225AC	A101	100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm)	
	CY7C1380CV25-225BGC CY7C1382CV25-225BGC	BG119	119 PBGA	
	CY7C1380CV25-225BZC CY7C1382CV25-225BZC	BB165A	165 fBGA	
200	CY7C1380CV25-200AC CY7C1382CV25-200AC	A101	100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm)	
	CY7C1380CV25-200BGC CY7C1382CV25-200BGC	BG119	119 PBGA	
	CY7C1380CV25-200BZC CY7C1382CV25-200BZC	BB165A	165 fBGA	
167	CY7C1380CV25-167AC CY7C1382CV25-167AC	A101	100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm)	
	CY7C1380CV25-167BGC CY7C1382CV25-167BGC	BG119	119 PBGA	
	CY7C1380CV25-167BZC CY7C1382CV25-167BZC	BB165A	165 fBGA	
133	CY7C1380CV25-133AC	A101	100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm)	

**Notes:**

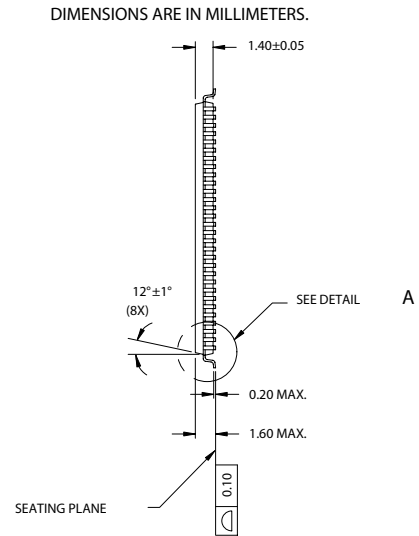
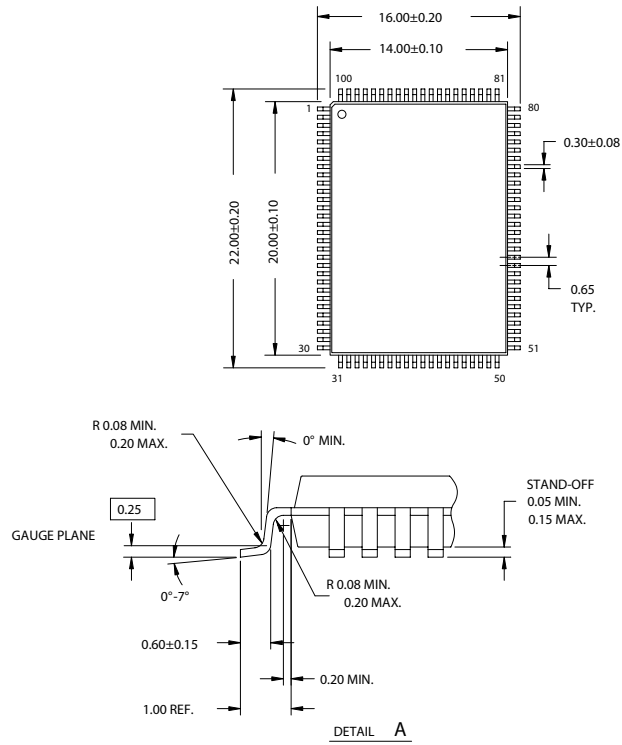
25. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.  
 26. DQs are in high-Z when exiting ZZ sleep mode.

167	CY7C1380CV25-167AI CY7C1382CV25-167AI	A101	100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm)	Industrial
	CY7C1380CV25-167BGI CY7C1382CV25-167BGI	BG119	119 PBGA	
	CY7C1380CV25-167BZI CY7C1382CV25-167BZI	BB165A	165 fBGA	

Shaded areas contain advance information. Please contact your local sales representative for availability of these parts.

Package Diagrams

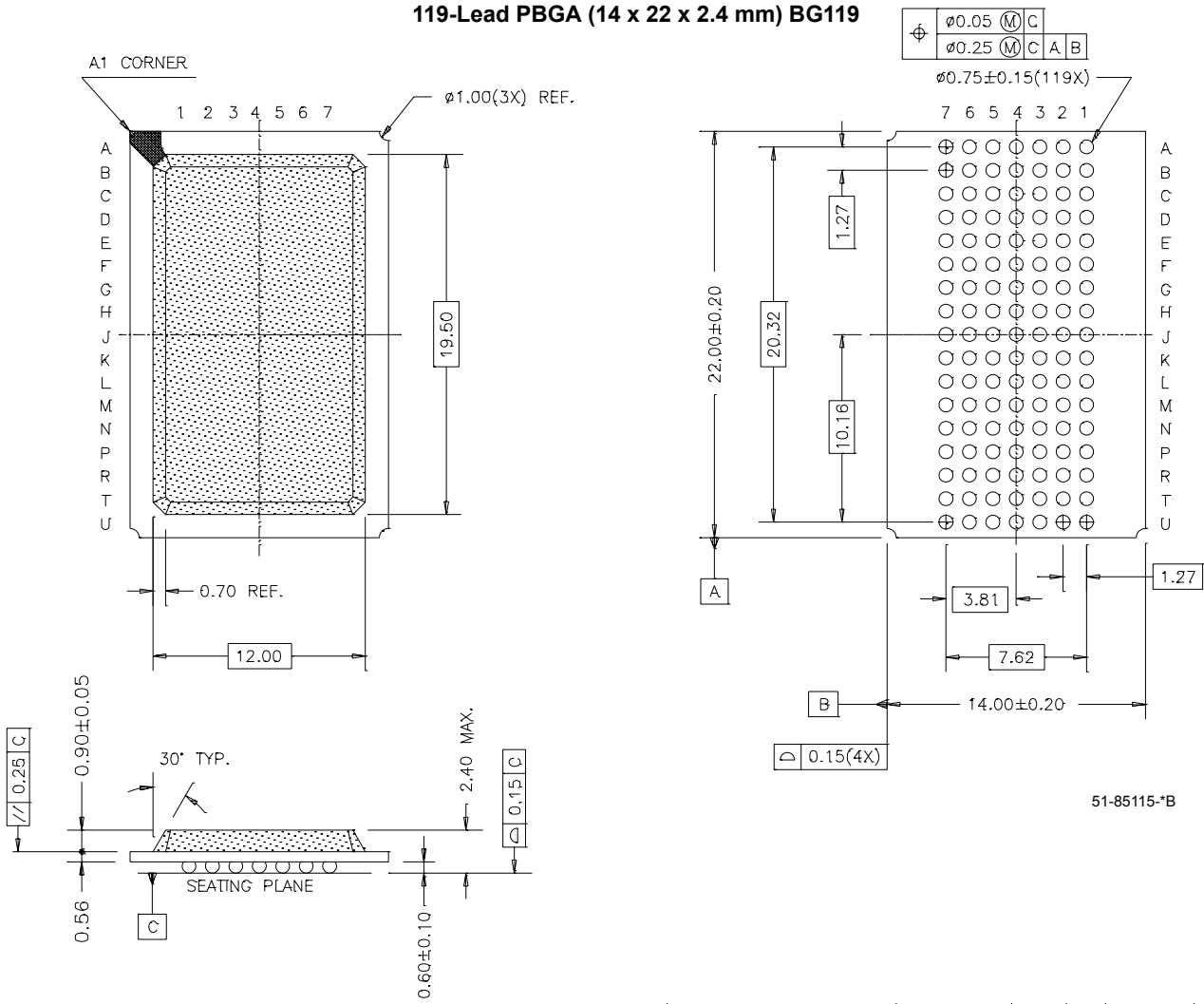
100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101



51-85050-\*A

**Package Diagrams** (continued)

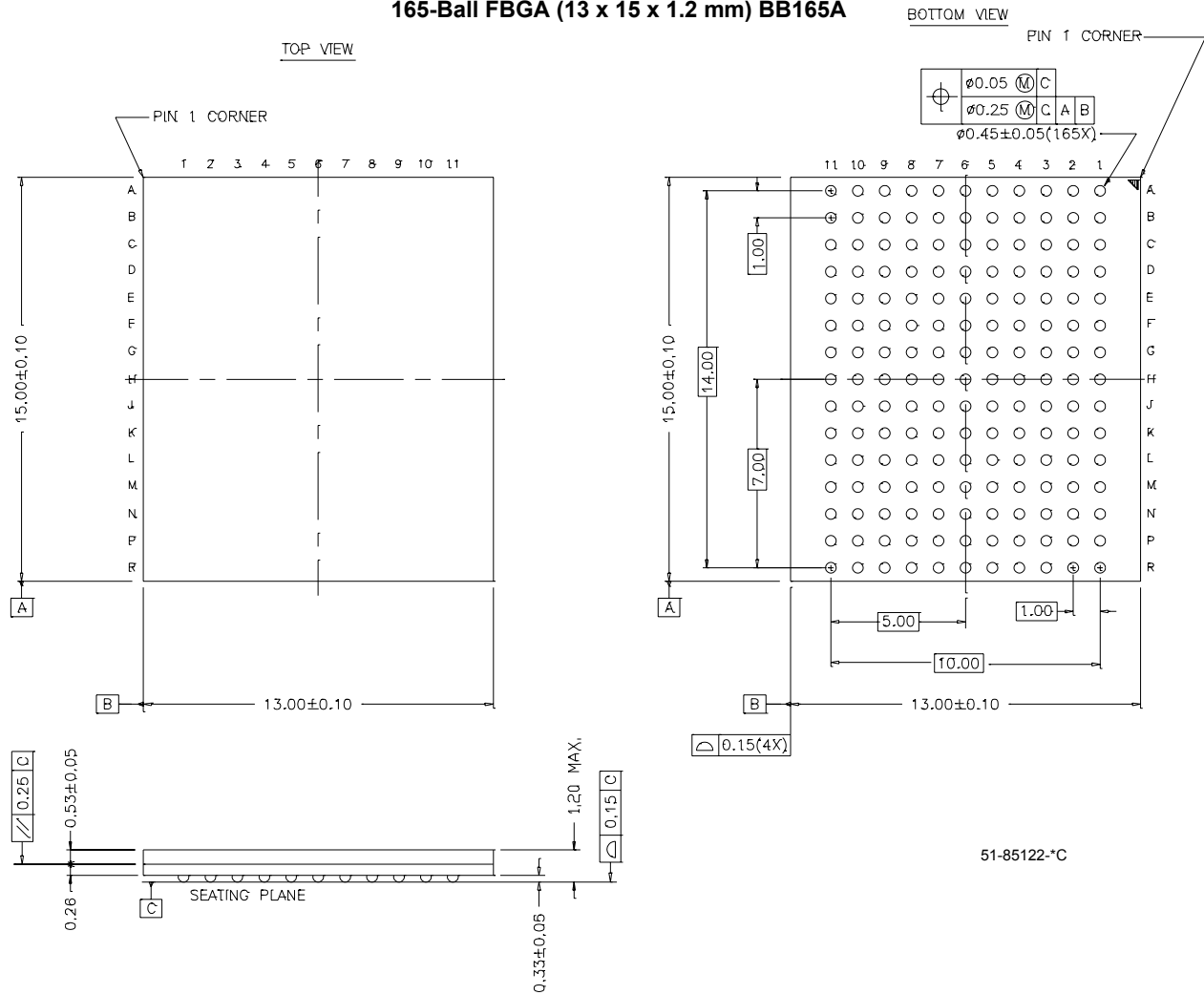
**119-Lead PBGA (14 x 22 x 2.4 mm) BG119**



51-85115-B

Package Diagrams (continued)

**165-Ball FBGA (13 x 15 x 1.2 mm) BB165A**



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**Document History Page**

Document Title: CY7C1380CV25/CY7C1382CV25 18-Mbit (512K x 36/1M x 18) Pipelined SRAM				
Document Number: 38-05240				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	116280	08/29/02	SKX	New Data Sheet
*A	121543	11/21/02	DSG	Updated package diagrams 51-85115 (BG119) to rev. *B and 51-85122 (BB165A) to rev. *C
*B	206081	See ECN	RKF	Final data sheet
*C	230388	See ECN	VBL	Update Ordering Info section: Shade Selection Guide and Characteristics table Changed the title for 119-BGA pin table for CY7C1382CV25 from "512K x 18" to "1M x 18" Modified Identification Register Definitions table: Changed Bit #24 from "0" to "1" and changed "Device Width" to "Architecture/Memory type"