SLA7070M(P)R through SLA7078M(P)R

February, 2006

Series SLA7070M Motor Driver ICs

INTRODUCTION

This document describes the function and features of SLA7070M series, which are unipolar 2-phase stepping motor driver ICs. This document contains preliminary information on the products under development. Should you have any questions, including information on options, contact your nearest sales or representative office.

Features

- Power supply voltages, V_{BB}: 46 V(max.), 10 to 44 V normal operating range
- Logic supply voltages, V_{DD}: 3.0 to 5.5 V
- Maximum output currents: 1 A, 1.5 A, 2 A, 3 A
- Built-in sequencer
- Simplified clock-in stepping control
- Both full/half-stepping, and microstepping versions;
  microstepping versions (SLA7075M, -76M, -77M, -78M) are capable of full-, half-, quarter-, eighth-, and sixteenth-stepping
- Built-in sense resistor, R_{SInt} (*NEW*)
- All variants are pin-compatible for enhanced design flexibility
- ZIP type 23-pin molded package (SLA package)
- Self-excitation PWM current control with fixed off-time
  For microstepping parts, off-time adjusted automatically by step reference current ratio (3 levels)
- Built-in synchronous rectifying circuit reduces losses at PWM off (*NEW*)
- Synchronous PWM chopping function prevents motor noise in Hold mode
- Sleep mode for reducing the IC input current in stand-by state
- Built-in protection circuitry against motor coil opens/shorts option available (*NEW*, patent pending)

All performance characteristics given are typical values for circuit or system baseline design only and are at the nominal operating voltage and an ambient temperature of +25°C, unless otherwise stated.

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PART NUMBERS AND OPTIONS

The following are the product variants and optional features available in the SLA707*0*M series.

Not all combinations of standard models and product options are available in high-volume production quantities. For information on product availability, and assistance with determining the IC features that are the best fit for your application, please contact our sales office or representative.

NOTE
The following abbreviations are used throughout this document to refer to product variants:
PR – Product with both Protection Circuitry and built-in R_{SInt} options
R – Product with the built-in R_{SInt} option

Part Number	Protection	Output Current, I_{OUT} (A)	Sequencer	Blanking Time (µs)	Clock Edge
SLA7070MR	R_{SInt}	1	Full/half Step	3.2	Positive
SLA7070MPR	Protection Circuitry and R_{SInt}				
SLA7071MR	R_{SInt}	1.5			
SLA7071MPR	Protection Circuitry and R_{SInt}				
SLA7072MR	R_{SInt}	2			
SLA7072MPR	Protection Circuitry and R_{SInt}				
SLA7073MR	R_{SInt}	3			
SLA7073MPR	Protection Circuitry and R_{SInt}				
SLA7075MR	R_{SInt}	1	Microstep	1.7	
SLA7075MPR	Protection Circuitry and R_{SInt}				
SLA7076MR	R_{SInt}	1.5			
SLA7076MPR	Protection Circuitry and R_{SInt}				
SLA7077MR	R_{SInt}	2			
SLA7077MPR	Protection Circuitry and R_{SInt}				
SLA7078MR	R_{SInt}	3			
SLA7078MPR	Protection Circuitry and R_{SInt}				

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS, valid at T_A = 25°C, applicable to both PR and R products, unless otherwise specified

Characteristics	Symbol	Remarks	Ratings	Units
Load (Motor) Supply Voltage	V_M		46	V
Main Power Supply Voltage	V_{BB}		46	V
Logic Supply Voltage	V_{DD}		7	V
Output Current	I_{OUT}	SLA7070M and SLA7075M	1.0	A
		SLA7071M and SLA7076M	1.5	A
		SLA7072M and SLA7077M	2.0	A
		SLA7073M and SLA7078M	3.0	A
Logic Input Voltage	V_{IN}		–0.3 to V_{DD}+0.3	V
REF Input Voltage	V_{REF}		–0.3 to V_{DD}+0.3	V
Sense Voltage	V_{Sint}	t_w < 1 µs is not considered	±2	V
Power Dissipation	P_D	Without heat sink	4.7	W
Junction Temperature	T_J		150	°C
Ambient Temperature	T_A		–20 to 85	°C
Storage Temperature	T_{stg}		–30 to 150	°C

RECOMMENDED OPERATING RANGES, applicable to both PR and R products, unless otherwise specified

Characteristics	Symbol	Remarks	Min	Max	Units
Load (Motor) Supply Voltage	V_M		–	44	V
Main Power Supply Voltage	V_{BB}		10	44	V
Logic Supply Voltage	V_{DD}	Surge voltage at VDD pin should be less than ±0.5 V to avoid malfunctioning in operation	3.0	5.5	V
Case Temperature	T_C	Measured at pin 12, without heat sink	–	90	°C

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ELECTRICAL CHARACTERISTICS, valid at T_A = 25°C, V_{BB} = 24 V, V_{DD} = 5 V, applicable to both PR and R products, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Main Power Supply Current	I_{BB}	Normal mode	–	–	15	mA
	I_{BBS}	Sleep1 and Sleep2 modes	–	–	100	µA
Logic Power Current	I_{DD}		–	–	5	mA
MOSFET Breakdown Voltage	V_{DSS}	V_{BB} = 44 V, I_{DS} = 1 mA	–	–	–	V
Maximum Response Frequency	f_{clk}	Clock Duty Cycle = 50%	250	–	–	kHz
Logic Supply Voltage	V_{IL}		–	–	0.25 × V_{DD}	V
	V_{IH}		0.75 × V_{DD}	–	–	V
Logic Supply Current	I_{IL}		–	±1	–	µA
	I_{IH}		–	±1	–	µA
REF Input Voltage	V_{REF}	See pages 6 and 7	–	–	–	V
	V_{REFS}	Output OFF, Sleep1 mode, I_{BBS} in specification, sequencer = enable	2.0	–	V_{DD}	V
REF Input Current	I_{REF}		–	±10	–	µA
SENSE Voltage	V_{SInt}	V_{REF} = 0.1 V to 0.5 V, Step reference current ratio: 100%	V_{REF} − 0.03	V_{REF}	V_{REF} + 0.03	V
Sleep-Enable Recovery Time	t_{SE}	V_{REF} = 2.0 V → 1.5 V	100	–	–	µs
Switching Time	t_{con}	Clock → Output ON	–	2.0	–	µs
	t_{coff}	Clock → Output OFF	–	1.5	–	µs

STEPPING CHARACTERISTICS, applicable to both PR and R products; representative values from SLA7070M series shown
Valid at T_A = 25°C, V_{BB} = 24 V, V_{DD} = 5 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Full/half step products, SLA7070M, SLA7071M, SLA7072M, and SLA7073M						
Step Reference Current Ratio	Mode F	$V_{REF} \approx V_{SInt}$ = 100 %, V_{REF} = 0.1 to 0.5 V	–	100	–	%
	Mode 8		–	70	–	%
PWM Minimum On-Time	$t_{on(min)}$		–	3.2	–	µs
PWM Off-Time	t_{off}		–	12	–	µs
Microstepping products, SLA7075M to SLA7078M						
Step Reference Current Ratio	Mode F	$V_{REF} \approx V_{SInt}$ = 100 %, V_{REF} = 0.1 to 0.5 V	–	100	–	%
	Mode E		–	98.1	–	%
	Mode D		–	95.7	–	%
	Mode C		–	92.4	–	%
	Mode B		–	88.2	–	%
	Mode A		–	83.1	–	%
	Mode 9		–	77.3	–	%
	Mode 8		–	70.7	–	%
	Mode 7		–	63.4	–	%
	Mode 6		–	55.5	–	%
	Mode 5		–	47.1	–	%
	Mode 4		–	38.2	–	%
	Mode 3		–	29	–	%
	Mode 2		–	19.5	–	%
	Mode 1		–	9.8	–	%
Mo (Load) Output Voltage	V_{MOL}	I_{MOL} = 1.25 mA	–	–	1.25	V
	V_{MOH}	I_{MOH} = –1.25 mA	V_{DD} – 1.25	–	–	V
Mo (Load) Output Current	I_{MOL}		–	–	1.25	mA
	I_{MOH}		–1.25	–	–	mA
PWM Minimum On-Time	$t_{on(min)}$		–	1.7	–	µs
PWM Off-Time	t_{off1}	Mode 8 to Mode F	–	12	–	µs
	t_{off2}	Mode 4 to Mode 7	–	9	–	µs
	t_{off3}	Mode 1 to Mode 3	–	7	–	µs

OUTPUT CHARACTERISTICS for both PR and R products
Valid at T_A = 25°C, V_{BB} = 24 V, V_{DD} = 5 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
I_{OUT} = 1.0 A (SLA7070M and SLA7075M)						
Output On Resistance	$R_{DS(ON)}$	I_{DS} = 1 A	–	0.7	0.85	Ω
Body Diode Forward Voltage	V_f	I_f = 1 A	–	0.85	1.1	V
I_{OUT} = 1.5 A (SLA7071M and SLA7076M)						
Output On Resistance	$R_{DS(ON)}$	I_{DS} = 1.5 A	–	0.45	0.6	Ω
Body Diode Forward Voltage	V_f	I_f = 1.5 A	–	1.0	1.25	V
I_{OUT} = 2.0 A (SLA7072M and SLA7077M)						
Output On Resistance	$R_{DS(ON)}$	I_{DS} = 2 A	–	0.25	0.4	Ω
Body Diode Forward Voltage	V_f	I_f = 2 A	–	0.95	1.2	V
I_{OUT} = 3.0 A (SLA7073M and SLA7078M)						
Output On Resistance	$R_{DS(ON)}$	I_{DS} = 3 A	–	0.18	0.24	Ω
Body Diode Forward Voltage	V_f	I_f = 3 A	–	0.95	2.1	V

BUILT-IN SENSE RESISTOR CHARACTERISTICS for PR and R products
Valid at T_A = 25°C, V_{BB} = 24 V, V_{DD} = 5 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
I_{OUT} = 1.0 A (SLA7070MPR, SLA7070MR, SLA7075MPR, and SLA7075MR)						
Sense Resistor Rating*	R_{SInt}	Tolerance: ±3 %	0.296	0.305	0.314	Ω
REF Input Voltage	V_{REF}	Within specified current limit	0.1	–	0.3	V
I_{OUT} = 1.5 A (SLA7071MPR, SLA7071MR, SLA7076MPR, and SLA7076MR)						
Sense Resistor Rating*	R_{SInt}	Tolerance: ±3 %	0.296	0.305	0.314	Ω
REF Input Voltage	V_{REF}	Within specified current limit	0.1	–	0.45	V
I_{OUT} = 2.0 A (SLA7072MPR, SLA7072MR, SLA7077MPR, and SLA7077MR)						
Sense Resistor Rating*	R_{SInt}	Tolerance: ±3 %	0.199	0.205	0.211	Ω
REF Input Voltage	V_{REF}	Within specified current limit	0.1	–	0.4	V
I_{OUT} = 3.0 A (SLA7073MPR, SLA7073MR, SLA7078MPR, and SLA7078MR)						
Sense Resistor Rating*	R_{SInt}	Tolerance: ±3 %	0.150	0.155	0.160	Ω
REF Input Voltage	V_{REF}	Within specified current limit	0.1	–	0.45	V

*R_{SInt} includes approximately 5 mΩ circuit resistance in addition to the resistance of the resistor itself.

PROTECTION CIRCUIT CHARACTERISTICS*

Valid at T_A = 25°C, V_{BB} = 24 V, V_{DD} = 5 V, unless otherwise specified

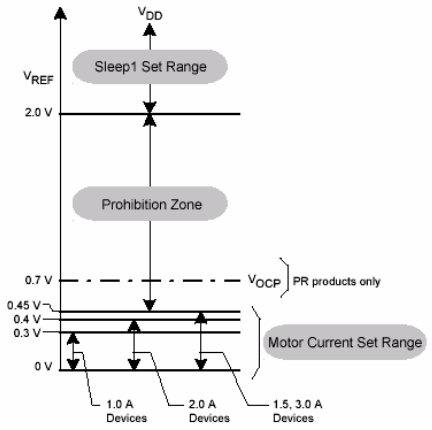
Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
PR products						
Overcurrent Sense Voltage	V_{OCP}	Motor coils shorted	0.65	0.7	0.75	V
FLAG Output Voltage	V_{FlagL}	I_{FLAGL} = 1.25 mA	–	–	1.25	V
	V_{FlagH}	I_{FLAGH} = –1.25 mA	V_{DD}–1.25	–	–	V
FLAG Output Current	I_{FlagL}		–	–	1.25	mA
	I_{FlagH}		–1.25	–	–	mA

*Protection circuits work on the condition of $V_{SInt} \geq V_{OCP}$.

REFERENCE VOLTAGE SETTING

V_{REF} (REF/SLEEP1 Pin)

PR and R Products



Motor Current Set Range is determined by the built-in resistor value, R_{SInt}. For PR products, pay extra attention to the change-over between the motor current specification range, I_{MO}, and the Sleep1 Set Range. V_{OCP} falls on the "prohibition zone" threshold. If the change-over time is too slow, OCP operation would start when $V_{SInt} > V_{OCP}$.

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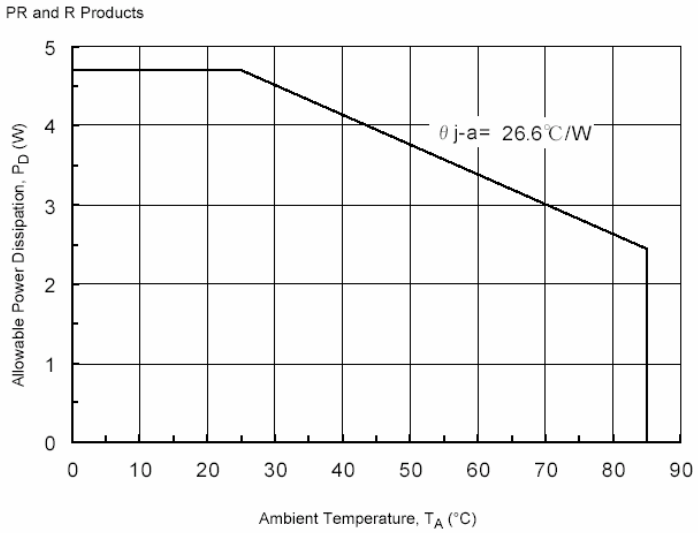
ALLOWABLE POWER DISSIPATION



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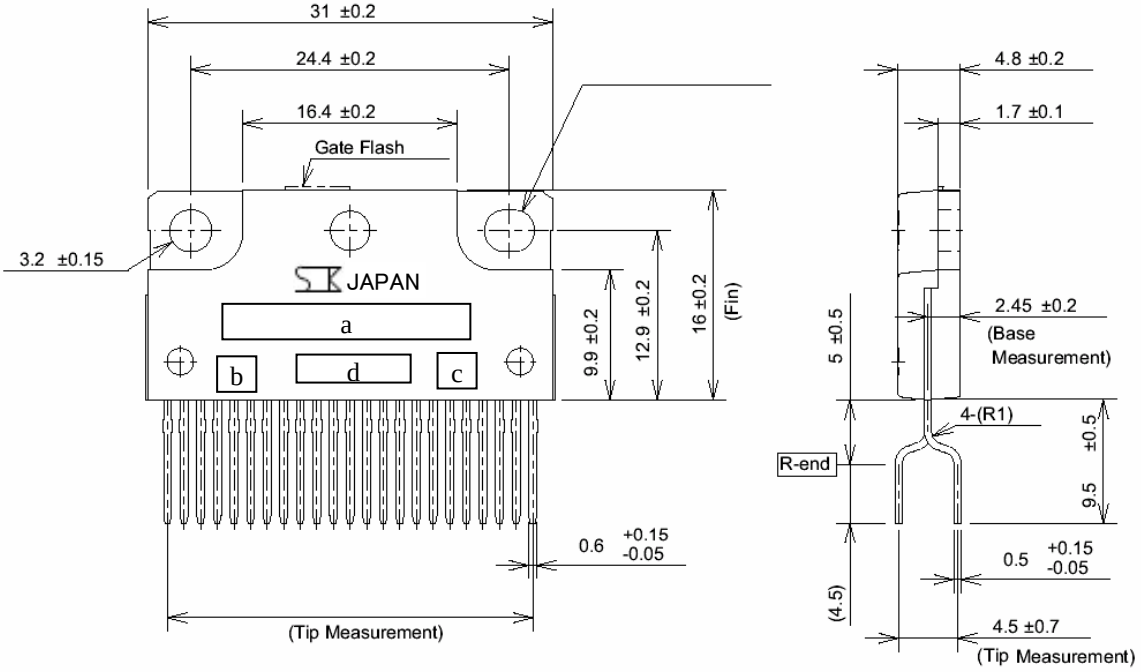
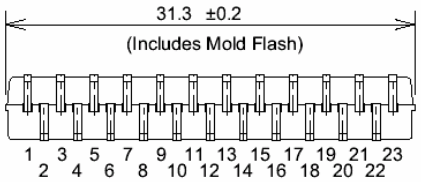
PACKAGE OUTLINE DRAWING, SLA-23 PIN





a. Part Number (1) SLA707xMR*

b. Part Number (2) W B
(Marked per functions.)*

c. Part Number (3) P
(Marked per functions.)*

d. Lot Number

1st letter: The last digit of year

2nd letter: Month

1 to 9 : Arabic Numerals for Jan. to Sep.
October : O
November : N
December : D

3rd &4th letter: Day

01 to 31 : Arabic Numerals

* The letter x in Part Number (1) represents one number from 0 to 3 and 5 to 8 according to the combination of the current rating and sequencer.
The letter P, R, W, B represent the functions built-in. (No marking for non built-in functions.)

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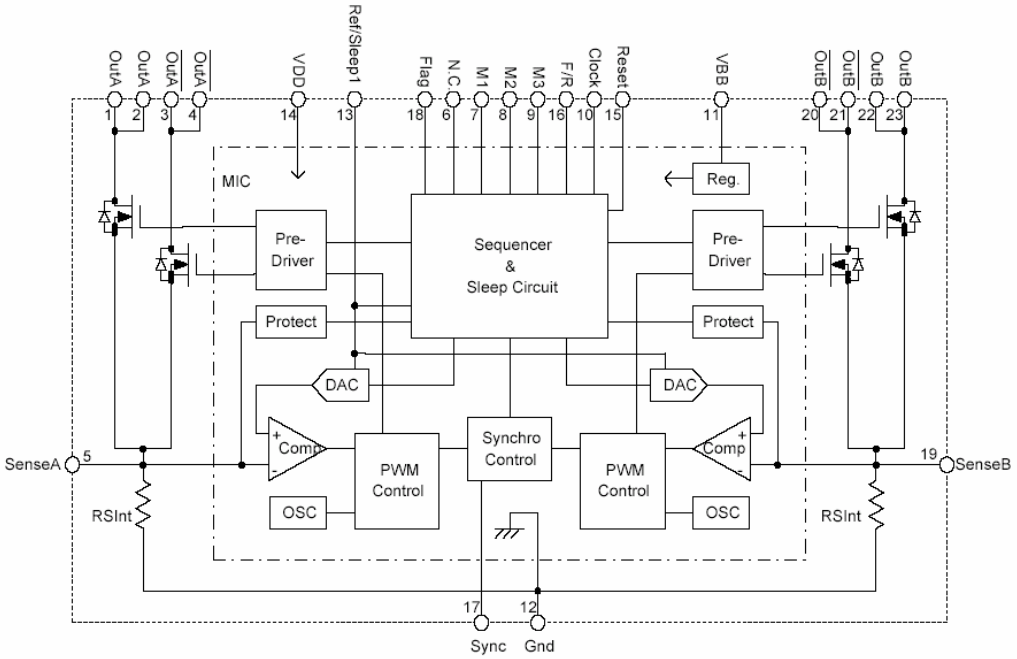
FUNCTIONAL BLOCK DIAGRAM AND PIN ASSIGNMENTS

Full/half step products: SLA7070MPR, SLA7071MPR, SLA7072MPR, and SLA7073MPR



For R products, protection circuits not built-in. FLAG pin is not connected internally.

Pin No.	Symbol	Functions
1	OutA	Output of phase A
2		
3	$\overline{\text{OutA}}$	Output of phase $\overline{\text{A}}$
4		
5	SenseA	Phase A current sensing
6	NC	No internal connection
7	M1	Commutation and Sleep2 setting
8	M2	
9	M3	
10	Clock	Step clock input
11	VBB	Main power supply (for motor)
12	GND	Ground

Pin No.	Symbol	Functions
13	Ref/Sleep1	Input for control current and Sleep 1 setting
14	VDD	Power supply to logic
15	Reset	Reset for internal logic
16	F/R	Forward/reverse switch input
17	Sync	Synchronous PWM control switch input
18	Flag*	Output from protection circuits monitor
19	SenseB	Phase B current sensing
20	$\overline{\text{OutB}}$	Output of phase $\overline{\text{B}}$
21		
22	OutB	Output of phase B
23		

*Flag pin active on PR products only; not internally connected for R products.

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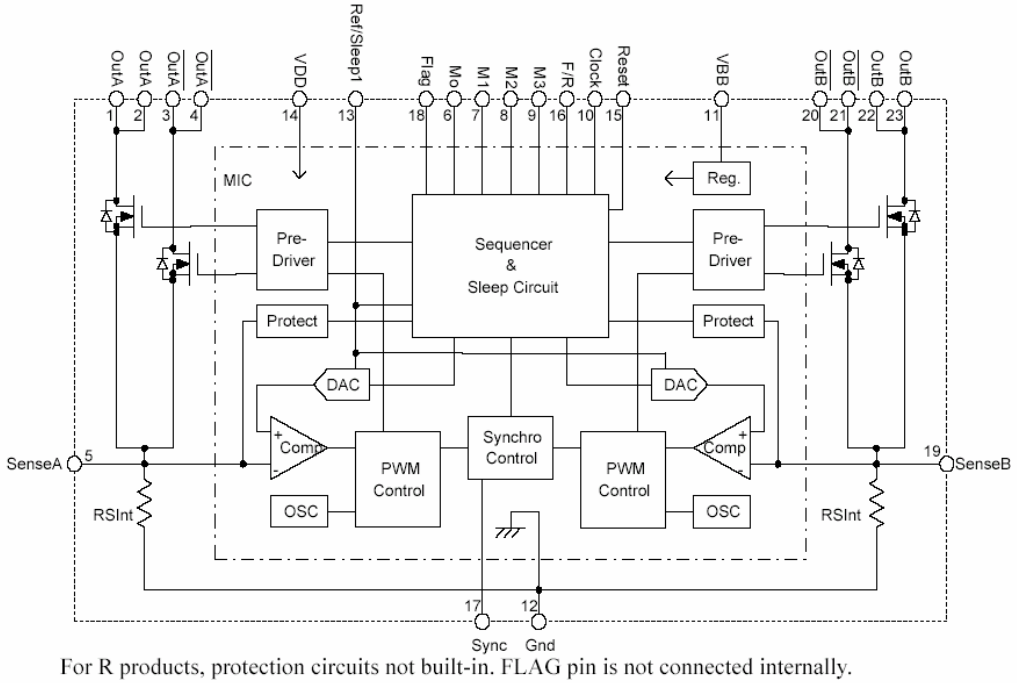
Microstepping products: SLA7075MPR, SLA7076MPR, SLA7077MPR, and SLA7078MPR



For R products, protection circuits not built-in. FLAG pin is not connected internally.

Pin No.	Symbol	Functions
1	OutA	Output of phase A
2		
3	$\overline{\text{OutA}}$	Output of phase $\overline{\text{A}}$
4		
5	SenseA	Phase A current sensing
6	Mo	Output from monitor of 2-phase excitation status
7	M1	Commutation and Sleep2 setting
8	M2	
9	M3	
10	Clock	Step clock input
11	VBB	Main power supply (for motor)
12	GND	Ground

Pin No.	Symbol	Functions
13	Ref/Sleep1	Input for control current and Sleep1 setting
14	VDD	Power supply to logic
15	Reset	Reset for internal logic
16	F/R	Forward/reverse switch input
17	Sync	Synchronous PWM control switch input
18	Flag*	Output from protection circuits monitor
19	SenseB	Phase B current sensing
20	$\overline{\text{OutB}}$	Output of phase $\overline{\text{B}}$
21		
22	OutB	Output of phase B
23		

*Flag pin active on PR products only; not internally connected for R products.

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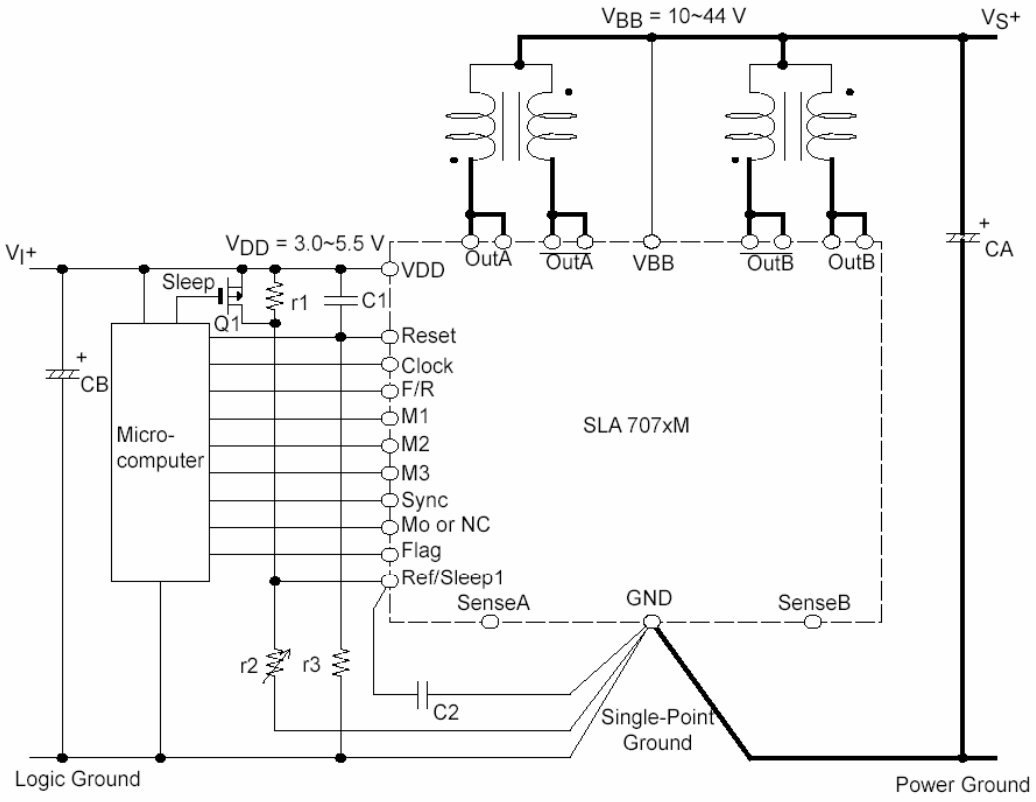
APPLICATION EXAMPLE FOR MICROSTEPPING PRODUCTS

Microstepping products: SLA7075MPR, SLA7076MPR, SLA7077MPR, and SLA7078MPR



- Take precautions to avoid noise on the V_{DD} line; noise levels greater than 0.5 V on the V_{DD} line may cause device malfunction. Noise can be reduced by separating the Logic Ground and the Power Ground on a PCB from the GND pin (pin 12).
- Constants, for reference use only:

r1 = 10 kΩ	CA = 100 µF / 50 V
r2 = 1 kΩ (VR)	CB = 10 µF / 10 V
r3 = 10 kΩ	C1 = 0.1 µF

- Unused logic input pins (F/R, M1, M2, M3, RESET, and SYNC) *must* be pulled up/down to V_{DD} or ground. If those unused pins are left open, the device malfunctions.
- Unused logic output pins (Mo, FLAG) *must* be kept open.

TRUTH TABLES

Common Input Pins

The following truth table is valid for the common input pins of both models of the SLA7070M series

Truth Table for Common Input Pins
Applicable both series models; PR and R products

Pin Name	Low Level	High Level	Clock
			POS Edge
Reset	Normal operation	Logic reset	–
F/R	Forward	Reverse	
M1	Commutation / Sleep2 function		
M2			
M3			
Ref/Sleep1	Normal operation	Sleep1 function	–
Sync	Non-sync PWM control	Sync PWM control	–

- The Reset function is asynchronous. If the input on the Reset pin is High, the internal logic circuit is reset. At this point, if the Ref pin stays Low, then the DMOS outputs turn on at the starting point of excitation. Note that the Disable control is not available with the Reset pin signal.
- The Sync function is active only at "2-phase excitation timing." If this function is used at other than 2-phase excitation timing, an overall balance might collapse because PWM off-time and set current are different in each phase A and phase B control scenario. (2-phase excitation timing is a point where the step reference current ratio of both phase A and phase B is Mode 8.)

Sleep Functions

The Hold mode stops motor rotation when applying current into a motor, and the device remains in Active status. Sleep1 is a sleep operation when logic circuits operate according to input signals. Sleep2 is a sleep operation in which the status of the logic circuits do not vary, but instead, they keep the same state as before the sleep function is initiated.

Sleep1 Function Setting Voltage at the REF/SLEEP1 pin controls the PWM current and the Sleep1 function. For normal operation, V_{REF} should be below 1.5 V (Low level). Applying a voltage greater than 2.0 V (High level) to the REF/SLEEP1 pin disables the outputs and puts the motor in a free state (coast).

This function is used to minimize power consumption when the device is not in use. Although it disables much of the internal circuitry, including the output MOSFETs and regulator, the sequencer/translator circuit is active. Therefore, a microcontroller can set the step starting point for the next operation during the Sleep1 function.

Commutation/Sleep2 Function Setting The following truth table is valid for the common Mx pins of both models of the SLA7070M series.

Truth Table for Commutation/Sleep2 Function
Applicable both series models; PR and R products

Pin Name			Full/Half Step	Microstepping
M1	M2	M3		
L	L	L	Full step (Mode 8 fixed)	Full step (Mode 8 fixed)
H	L	L	Full step (Mode F fixed)	Full step (Mode F fixed)
L	H	L	Half step	Half step
H	H	L	Half step (Mode F fixed)	Half step (Mode F fixed)
L	L	H	Sleep2 function	Quarter step
H	L	H		Eighth step
L	H	H		Sixteenth step
H	H	H		Sleep2 function

In the Sleep2 function, the outputs are disabled and the driver supply current (I_{BB}) is reduced. However, unlike the Sleep1 function, the logic circuitry is put into a "standby" state and therefore the sequencer/translator is not activated, even if a step command signal occurs on the CLOCK input pin.

Monitor Output Pin

The pin used to monitor the device output is different between these configurations:

- Microstepping products: Mo (2-phase excitation timing)
- PR products: Flag (Protection circuit operation timing)

Note that PR products with microstepping have both of the monitor output pins.

Truth Table for Monitor Outputs

Pin Name	Low Level	High Level
Mo	Other than 2-phase excitation timing	2-phase excitation timing
FLAG	Normal operation	Protection circuit operation

The outputs turn off at the point where the protection circuit starts operating. To release the protection state, reinput the logic supply voltage.

LOGIC INPUT PINS

The low pass filter incorporated with the logic input pins (RESET, CLOCK, F/R, M1, M2, M3, and SYNC) improves noise rejection. The logic inputs are CMOS input compatible, and therefore they are in high impedance state. Use the IC at a fixed input level, either Low or High.

Input Logic Timing

CLOCK signal. This device includes clock-in type of control that simplifies the interface.

- Pulse characteristics

A low-to-high and high-to-low transition on the CLOCK input sequences the translator/sequencer. Clock pulse width should be set at 2 µs in both positive and negative polarities. Therefore, clock response frequency becomes 250 kHz.

- Set-up and hold times before and after Clock pulse

With regard to the input logic of the F/R, M1, M2, and M3 pins, a 1 µs delay should occur both before and after the pulse edges, as set-up and hold times. The sequencer logic circuitry might malfunction if the logic polarity is changed during these set-up and hold times. Refer to the figure below.

RESET input

- RESET input pulse width

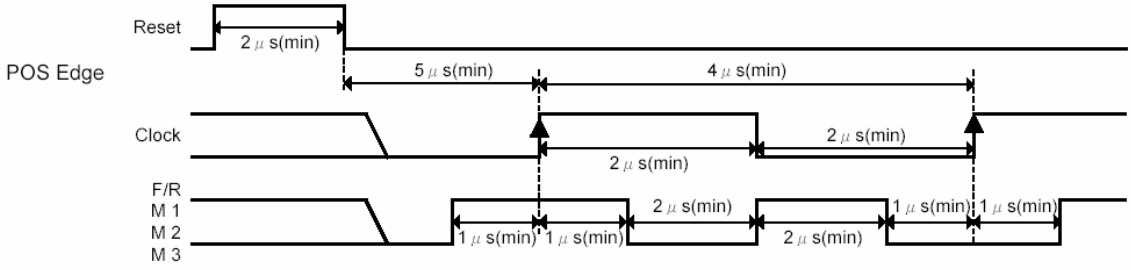
The Reset pulse width is equivalent to the high pulse level hold time. It should be greater than the 2 µs CLOCK input pulse width.

- Reset release and CLOCK input timing

The RESET input sets the translator/sequencer to a predefined Home state and turns off all of the DMOS outputs. A low pass filter is incorporated into the Reset circuit; therefore, a greater than 5 µs delay is required between the falling edge of the RESET input and the rising edge of the CLOCK input.

F/R, M1, M2, and M3 logic change

Logic level inputs on F/R, M1, M2, and M3 set the translator step direction (F/R) and step mode (M1, M2, and M3; refer to the Commutation Truth Table). Changes to these inputs do not take effect until the rising edge of the CLOCK input. However, depending on the type and state of a motor, there may be errors in motor operation. A thorough evaluation on the changes of sequence should be carried out.



Logic Input Timing

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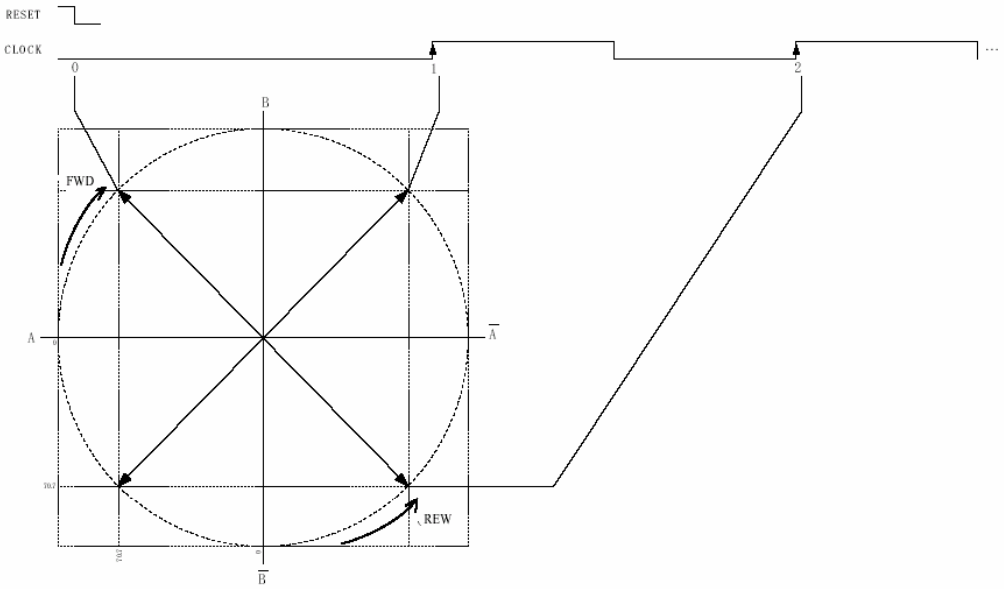
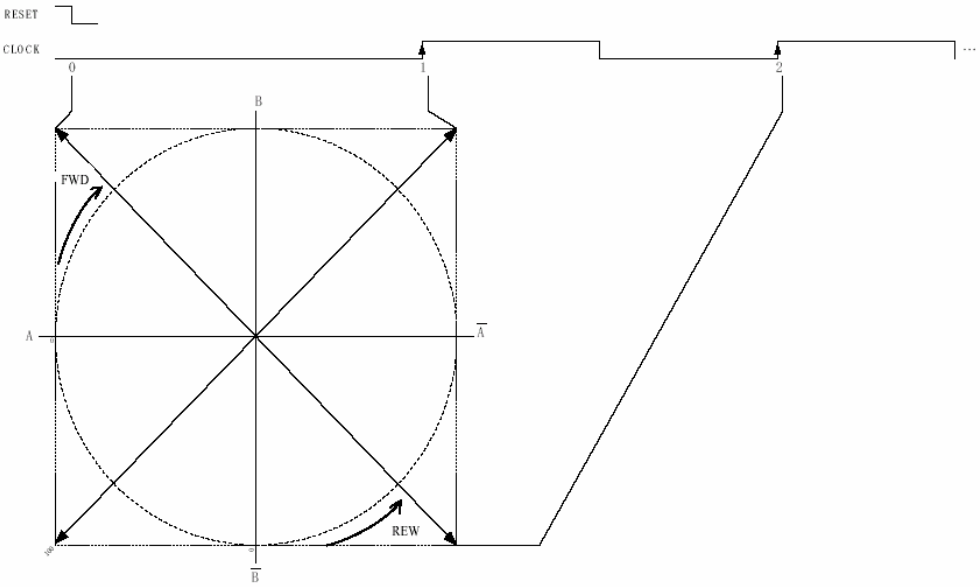
STEP SEQUENCING

All illustrations in this section are based on step sequencing at the POS (Positive) edge.

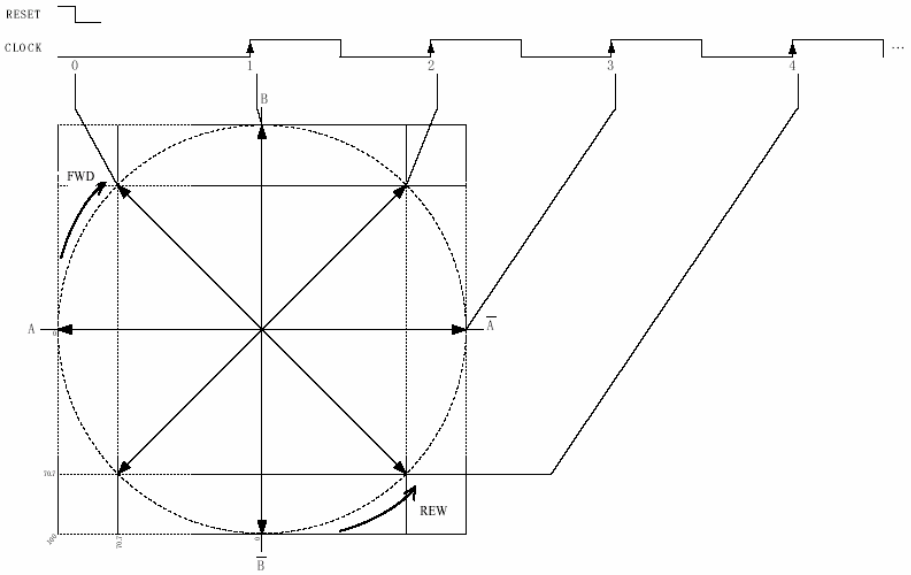
Full step; for both microstepping and full/half step products
M1: L, M2: L, M3: L (Mode 8)



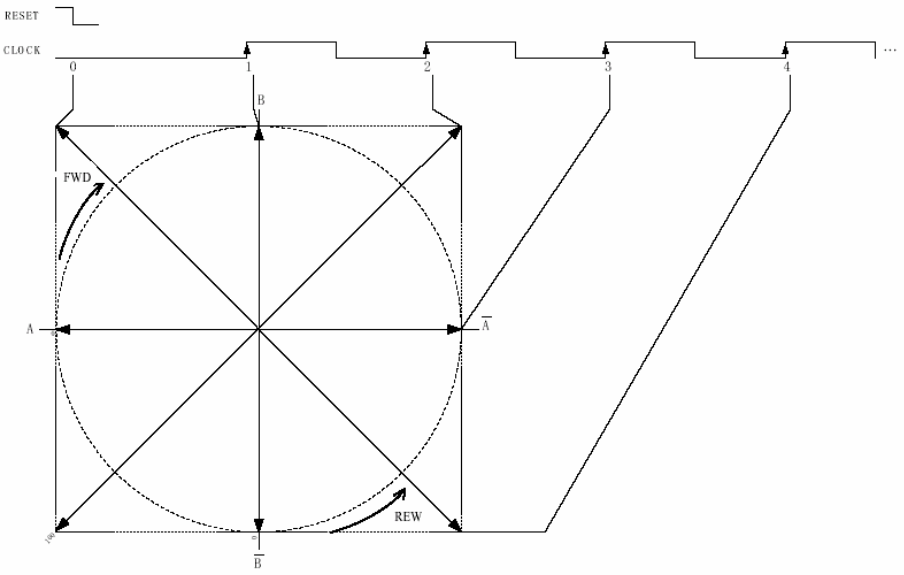
M1: H, M2: L, M3: L (Mode F)



Half step; for both microstepping and full/half step products
M1: L, M2: H, M3: L (Mode 8, F)



M1: H, M2: H, M3: L (Mode F)



SLA7070M(P)R through SLA7078M(P)R

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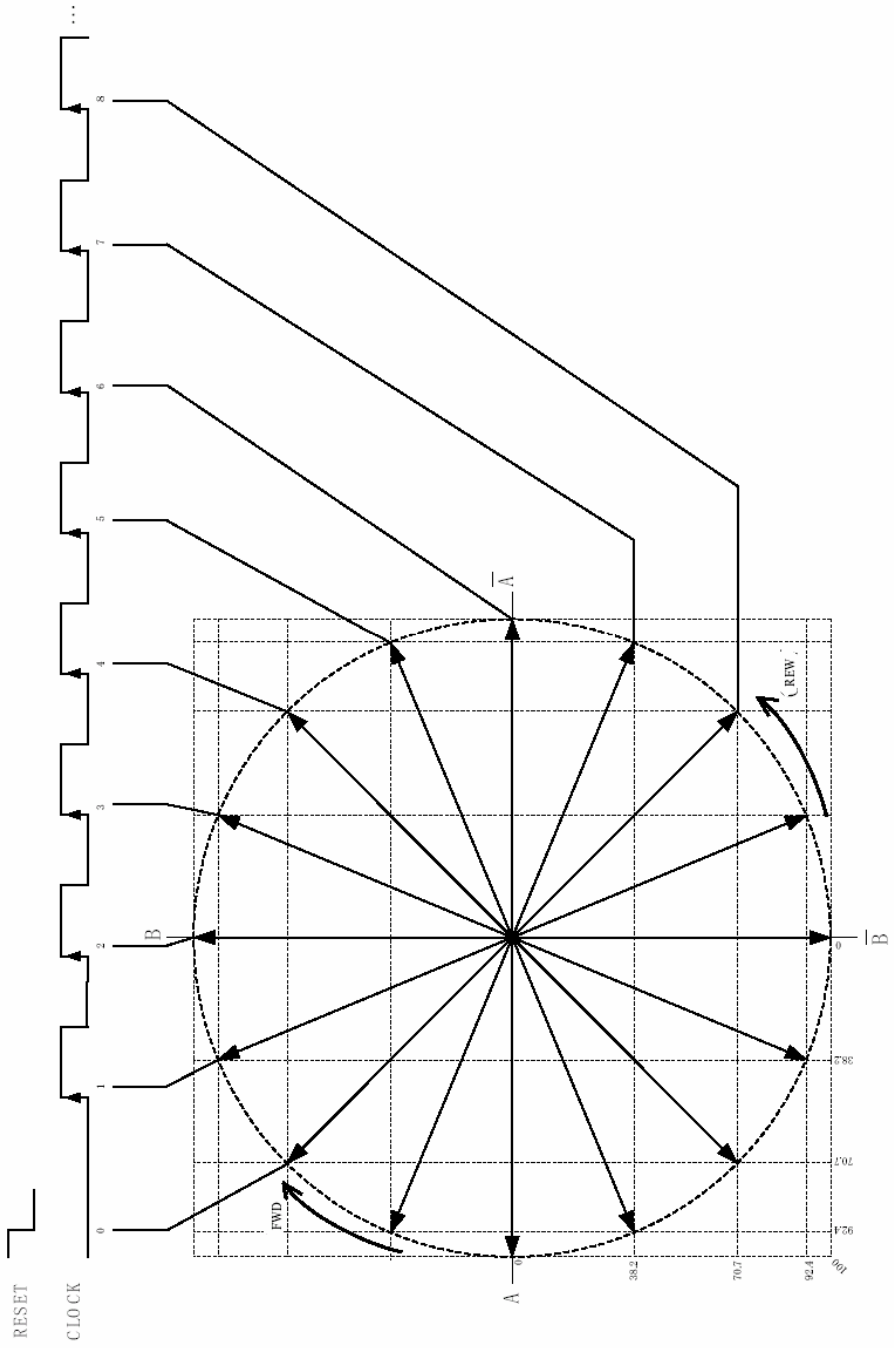
Quarter step; for microstepping products
M1: L, M2: L, M3: H



SLA7070M(P)R through SLA7078M(P)R

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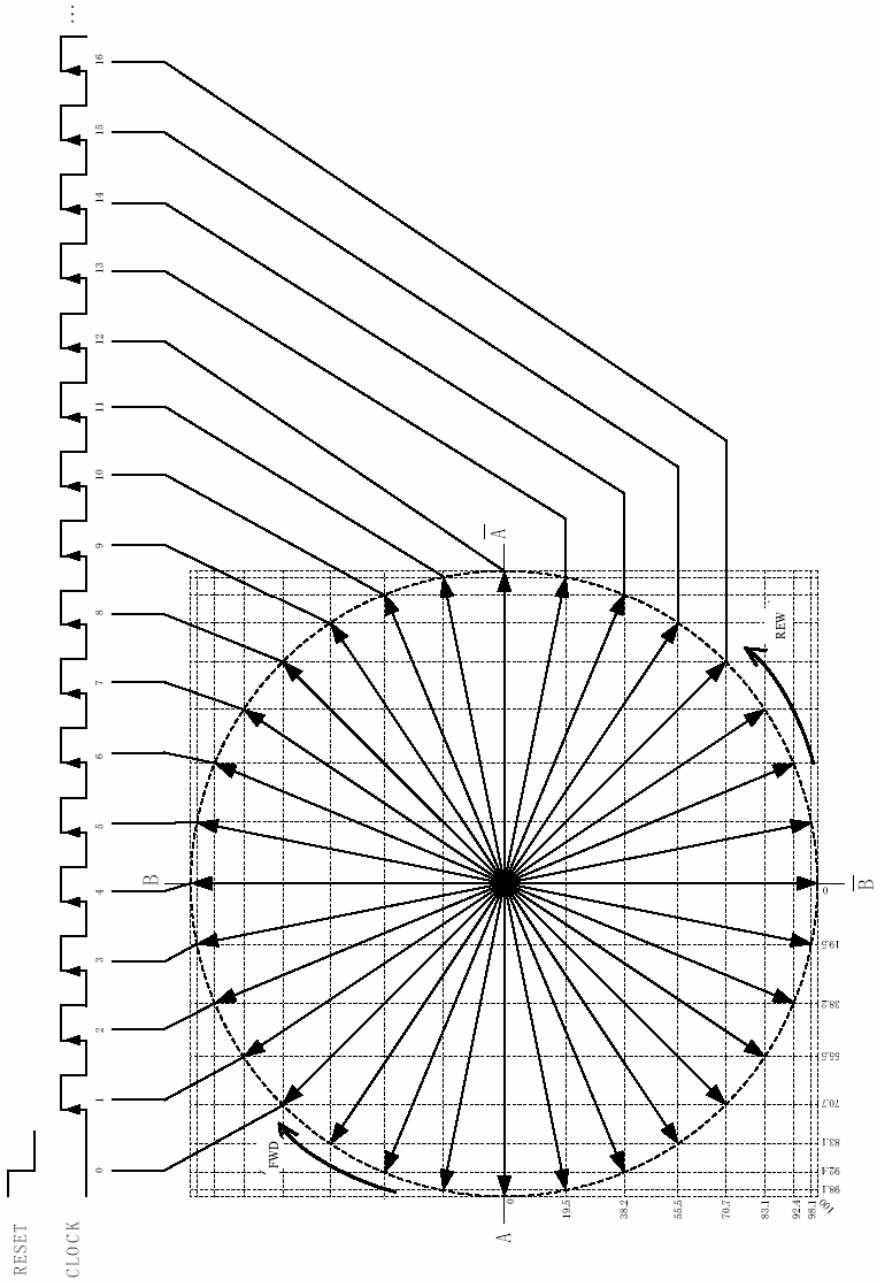
Eighth step; for microstepping products
M1: H, M2: L, M3: H



SLA7070M(P)R through SLA7078M(P)R

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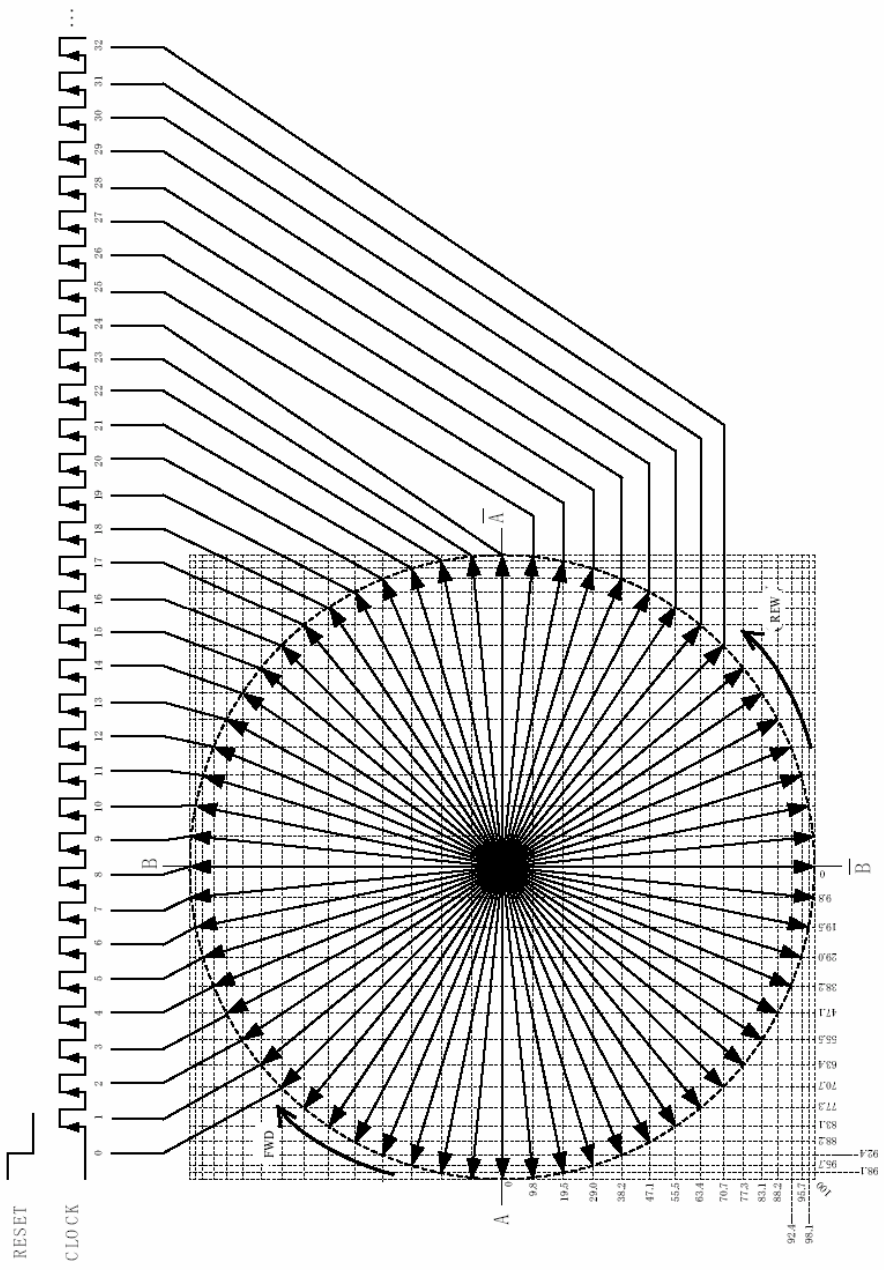
Sixteenth step; for microstepping products
M1: L, M2: H, M3: H



SLA7070M(P)R through SLA7078M(P)R

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Excitation Change Sequence

The change behavior is determined by the settings of the excitation pin (M1, M2, and M3) before and after the step signal.

Excitation Mode State Table

Direction	Internal Sequence State				Step Sequencing						
	Phase A		Phase B		Full Step		Half Step		1/4 Step	1/8 Step	1/16 Step
	PWM	Mode	PWM	Mode	Mode 8	Mode F	Mode 8, F	Mode F			
Rev. ▲	A	8	B	8	X	X*	X	X*	X	X	X
	A	7	B	9							X
	A	6	B	A						X	X
	A	5	B	B							X
	A	4	B	C					X	X	X
	A	3	B	D							X
	A	2	B	E						X	X
	A	1	B	F							X
	–	–	B	F			X	X	X	X	X
	$\bar{A}$	1	B	F							X
	$\bar{A}$	2	B	E						X	X
	$\bar{A}$	3	B	D							X
	$\bar{A}$	4	B	C					X	X	X
	$\bar{A}$	5	B	B							X
	$\bar{A}$	6	B	A						X	X
	$\bar{A}$	7	B	9							X
	$\bar{A}$	8	B	8	X	X*	X	X*	X	X	X
	$\bar{A}$	9	B	7							X
	$\bar{A}$	A	B	6						X	X
	$\bar{A}$	B	B	5							X
	$\bar{A}$	C	B	4					X	X	X
	$\bar{A}$	D	B	3							X
	$\bar{A}$	E	B	2						X	X
	$\bar{A}$	F	B	1							X
	$\bar{A}$	F	–	–			X	X	X	X	X
	$\bar{A}$	F	$\bar{B}$	1							X
	$\bar{A}$	E	$\bar{B}$	2						X	X
	$\bar{A}$	D	$\bar{B}$	3							X
	$\bar{A}$	C	$\bar{B}$	4					X	X	X
	$\bar{A}$	B	$\bar{B}$	5							X
	$\bar{A}$	A	$\bar{B}$	6						X	X
	$\bar{A}$	9	$\bar{B}$	7							X
	$\bar{A}$	8	$\bar{B}$	8	X	X*	X	X*	X	X	X
	$\bar{A}$	7	$\bar{B}$	9							X
	$\bar{A}$	6	$\bar{B}$	A						X	X
	$\bar{A}$	5	$\bar{B}$	B							X
	$\bar{A}$	4	$\bar{B}$	C					X	X	X
	$\bar{A}$	3	$\bar{B}$	D							X
	$\bar{A}$	2	$\bar{B}$	E						X	X
	$\bar{A}$	1	$\bar{B}$	F							X
	–	–	$\bar{B}$	F			X	X	X	X	X
	A	1	$\bar{B}$	F							X
	A	2	$\bar{B}$	E						X	X
	A	3	$\bar{B}$	D							X
	A	4	$\bar{B}$	C					X	X	X
	A	5	$\bar{B}$	B							X
	A	6	$\bar{B}$	A						X	X
	A	7	$\bar{B}$	9							X
	A	8	$\bar{B}$	8	X	X*	X	X*	X	X	X
	A	9	$\bar{B}$	7							X
	A	A	$\bar{B}$	6						X	X
	A	B	$\bar{B}$	5							X
	A	C	$\bar{B}$	4					X	X	X
	A	D	$\bar{B}$	3							X
	A	E	$\bar{B}$	2						X	X
	A	F	$\bar{B}$	1							X
	A	F	–	–			X	X	X	X	X
Fwd. ▼	A	F	B	1							X
	A	E	B	2						X	X
	A	D	B	3							X
	A	C	B	4					X	X	X
	A	B	B	5							X
	A	A	B	6						X	X
	A	9	B	7							X

* Sequence state is Mode 8, but step reference current ratio is Mode F. Mode F has step reference current ratio of 100%, and PWM off-time of 12 µs.

SLA7070M(P)R through SLA7078M(P)R

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INDIVIDUAL CIRCUIT DESCRIPTION

Monolithic IC (MIC)

The descriptions of the monolithic IC (MIC) elements in this section are applicable to both models of products: PR and R. However, the blanking time differs among some options, and current value in low current mode will vary according to the minimum on-time difference.

• Sequencer Logic

The single CLOCK input is used for step timing. Direction is controlled by the F/R input.

Commutation mode is controlled by the combination of the M1, M2, and M3 logic levels. For details, refer to the Commutation Truth Table on page 13.

• PWM Current Control

Each pair of outputs is controlled by a fixed off-time PWM current-control circuit. The internal oscillator (OSC) sets the off-time. Its operation mechanism is identical to that of the SLA7060M family. Refer to the Functional Description section for further details.

• Synchronous Operation Mode

This function prevents occasional motor noise during Hold mode, which normally results from asynchronous PWM operation of both motor phases. A logic high at the SYNC input sets synchronous operation. A logic low sets asynchronous operation. The use of synchronous operation during normal stepping is not recommended because it produces less motor torque and can cause motor vibration due to staircase current.

The use of synchronous operation when the motor is not in operation is allowed only in full/half step sequence timing, due to the difference in the current controlled and PWM off-time at other step sequence timings.

• DAC (D-to-A Converter)

In microstep sequencing, the current at each step is set by the value of a sense resistor (R_{SInt}), a reference voltage (V_{REF}), and the output voltage of the DACs, controlled by the output of the sequencer (translator). Refer to the Stepping Characteristics table on page 5.

• Regulator Circuit

The integrated regulator circuit is used in driving the output MOSFET gates and powering other internal linear circuits.

• Protection Circuit

A built-in protection circuit against motor coil opens or shorts is available in the PR products. Protection is activated by sensing voltage on the internal R_{SInt} resistors; therefore, an overcurrent condition cannot be detected which results from the the OUT pins or SENSE*x* pins, or both, shorting to GND.

Protection against motor coil opens is available only during PWM operation; therefore, it does not work at constant voltage driving, when the motor is rotating at high speed.

Operation of the protection circuit disables all of the DMOS outputs. To come out of protection mode, cycle the logic supply, VDD.

Output MOSFET Chip

The value of the built-in output DMOS chip varies according to which of the four different output current ratings has been selected.

Sense Resistor

Sense resistors are incorporated in the PR and R products to detect motor current. The resistance varies according to which of the four different output current ratings has been selected, as follows:

Output Current (A)	R_{SInt} Resistance (Ω Typ.)
1	0.305
1.5	0.305
2	0.205
3	0.155

Each resistance shown above includes the inherent resistance (approximately 5 mΩ) in the resistor itself.

SLA7070M(P)R through SLA7078M(P)R

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FUNCTIONAL DESCRIPTION

PWM Current Control

The description in this section is applicable to the PR and R products.

• Blanking time

The actual operating waveforms on the SENSE*x* pins when driving a motor are shown in figure 1. Immediately after PWM turns OFF, ringing (or spike) noise on the SENSE*x* pins is observed for a few µs. Ringing noise can be generated by various causes, such as capacitance between motor coils and inappropriate motor wiring.

Each pair of outputs is controlled by a fixed off-time (7 to 12 µs, depending on stepping mode) PWM current-control circuit that limits the load current to a desired value, I_{TRIP}. Initially, an output is enabled and current flows through the motor winding and the current-sense resistors. When the voltage across the current-sense resistor equals the DAC output voltage, V_{TRIP}, the current-sense comparator resets the PWM latch. This turns off the driver for the fixed off-time, during which the load inductance causes the current to recirculate for the off-time period. Therefore, if the ringing noise on the sense resistor equals and surpasses V_{TRIP}, PWM turns off.

To prevent this phenomenon, the blanking time is set to override signals from the current-sense comparator for a certain period right after PWM turns on (figure 2).

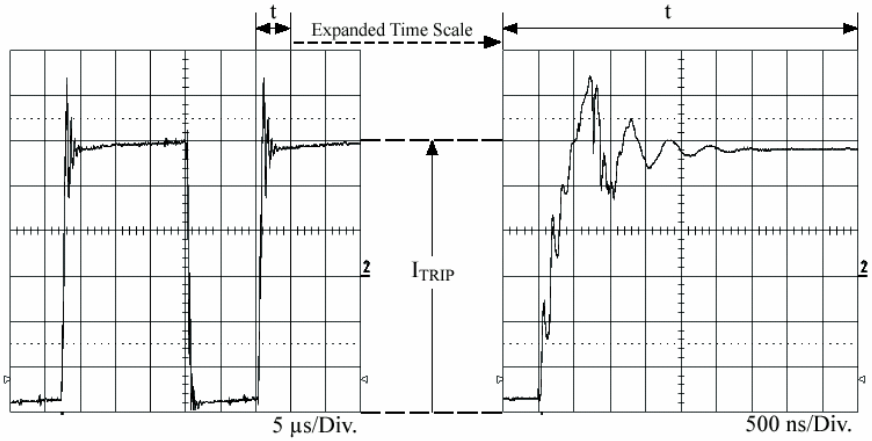

Figure 1. Operating waveforms on the SENSE*x* pins during PWM chopping

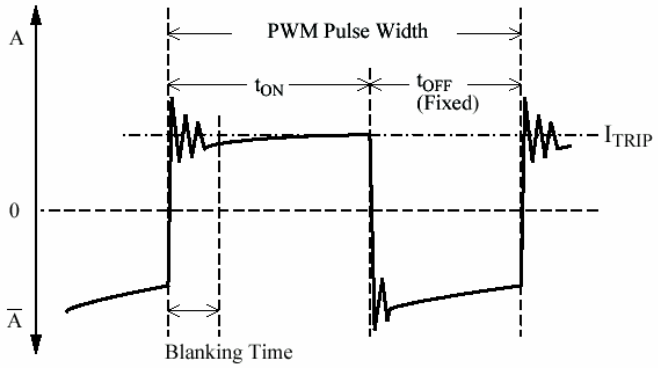

Figure 2. SENSE*x* pins pattern during PWM control

SLA7070M(P)R through SLA7078M(P)R

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PWM Off Period

The PWM off-time for the SLA7070M series is controlled as a fixed time by an internal oscillator. It also is switched in 3 levels by current proportion (see the Electrical Characteristics table).

In addition, the SLA7070M series provide a function that decreases losses occurring when the PWM turns off. This function dissolves back EMF stored in the motor coil at MOSFET turn-on, as well as at PWM turn-on (synchronous rectification operation).

Figure 3 shows the difference in back EMF generative system between the SLA7060M series and SLA7070M series. The SLA7060M series performs on–off operations using only the MOSFET on the PWM-on side, but the SLA7070M series also performs on–off operations using only the MOSFET on the PWM-off side. To prevent simultaneous switching of the MOSFETs at synchronous rectification operation, the IC has a dead time of approximately 0.5 µs. During dead time, the back EMF flows through the body diode on the MOSFET.

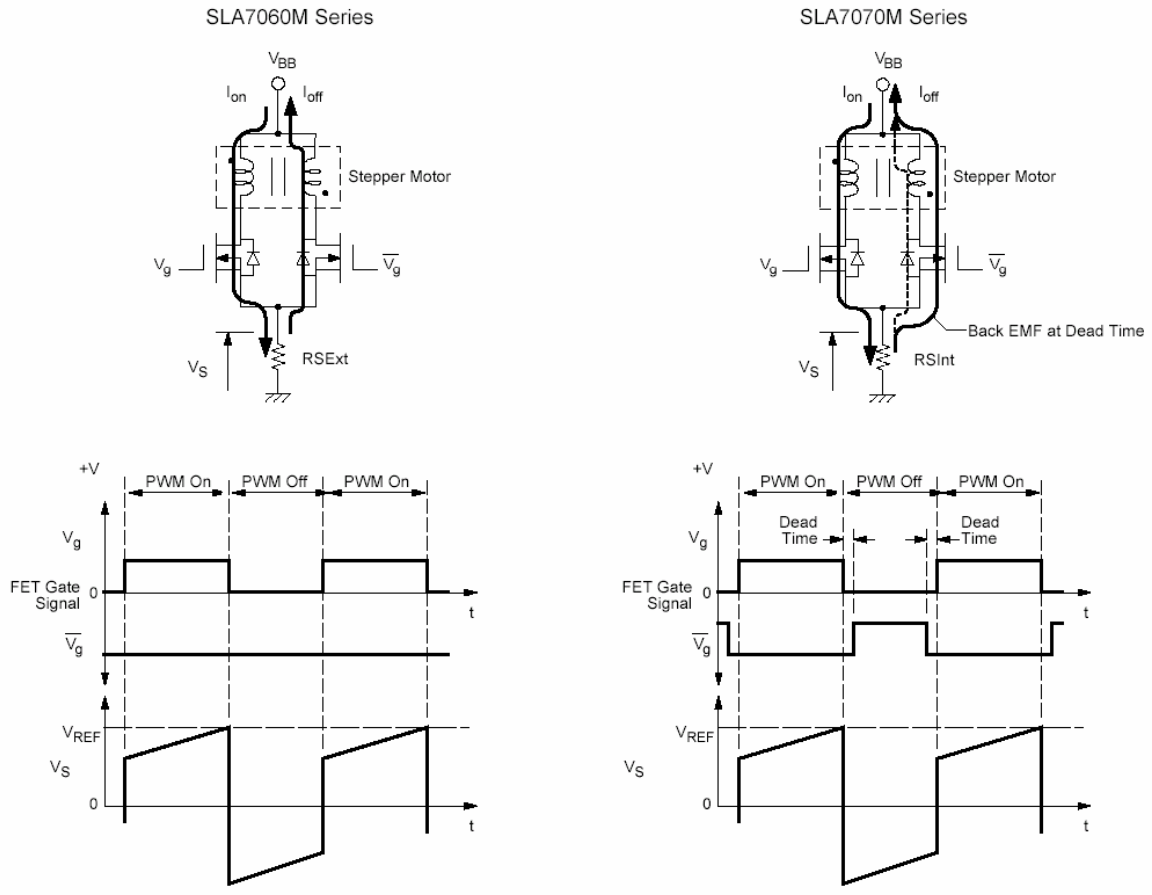

Figure 3. Synchronous rectification operation. During Dead Time, the Back EMF flows through the body diode of the MOSFET

Protection Functions: PR Types

The PR types of the SLA7070M series include a motor coil short-circuit protection circuit and a motor coil open protection circuit. They are described in this section.

• Motor Coil Short-Circuit Protection (Load Short) Circuit

This protection circuit, embedded in the SLA7070M series, begins to operate when the device detects an increase in the voltage level on the sense resistor, V_{SInt}.

The voltage at which motor coil short-circuit protection starts its operation, V_{OCP}, is set at approximately 0.7 V. The output is disabled at the time the protection circuit starts.

In order for the motor coil short-circuit protection circuit to operate, V_{SInt} must be greater than V_{OCP}.

Overcurrent that flows without passing the sense resistor is undetectable. To resume the circuit after protection operates, VDD must be cycled.

• Motor Coil Open Protection

Details of this functions is not disclosed yet due to our patent policy.

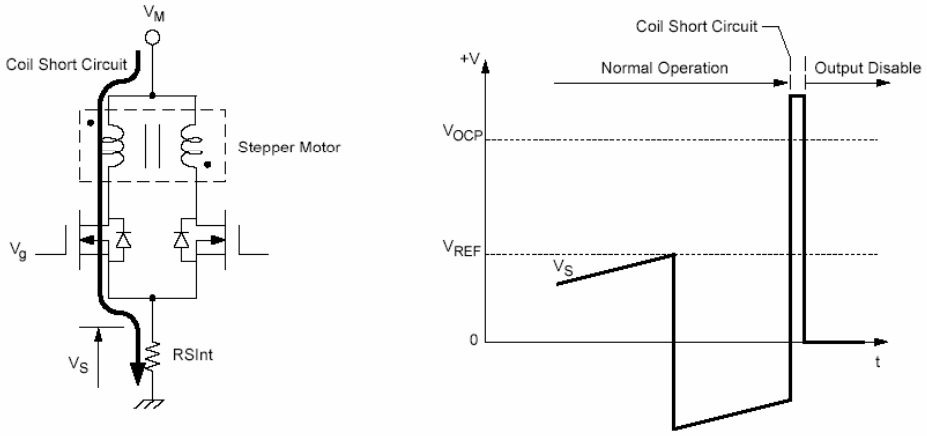

Figure 4. Motor coil short circuit protect circuit operation. Overcurrent that flows without passing the sense resistor is undetectable. To recover the circuit after protection operates, VDD must be cycled and started up again.

APPLICATION INFORMATION

Motor Current Ratio Setting (R_1, R_2, R_{SInt})

The setting calculation of motor current I_{OUT} on SLA7070M series is determined by the ratios of external components R1, R_2, and R_{SInt} (refer to the application example circuit on page 12). The following is a formula for calculating I_{OUT}:

$$I_{OUT} = \frac{R_2}{R_1 + R_2} \times V_{DD} \Big/ R_{SInt} \quad (1)$$

when V_{REF} is within specification. If V_{REF} is set less than 0.1 V, variation or impedance of the wiring pattern may influence the IC and the possibility of less accurate current sensing becomes high.

The standard voltage of current I_{TRIP} that SLA7070M series controls is partially divided by the internal DAC:

$$I_{TRIP} = \frac{V_{REF}}{R_{SInt}} \times Mode\ Proportion \quad (2)$$

For R_{SInt} value, see Sense Resistor section, page 21.

Lower Limit of Control Current

The SLA7070M series uses a self-oscillating PWM current control topology in which the off- time is fixed. As energy stored in motor coil is eliminated within fixed the PWM off-time, coil current flows intermittently, as shown in figure 5.

Thus, average current decrease and motor torque also decrease. The point intermissive current starts flowing to the coil is considered as the lower limit of the control current. The lower limit of control current differs by conditions of motor or other factors, but it is calculated from the following formula.

$$I_{OUT(min)} = \frac{V_M + R_{DS(on)} \times I_{OUT}}{R_M} + \exp\left(\frac{t_{OFF}}{T_C}\right)^{-1} - 1 \quad (3)$$

where:

$$T_C = R_M \times L_M, \text{ and} \quad (4)$$

V_M is the motor supply voltage,

$R_{DS(on)}$ is the MOSFET on resistance,

I_{OUT} is the target current level,

R_M is the motor winding resistance,

L_M is the motor winding reactance, and

t_{OFF} is the PWM off-time.

Even if the control current value is set at less than the lower limit of the control current, there is no setting at which the IC fails to operate. However, control current will worsen against setting current.

Avalanche Energy

In the unipolar topology of the SLA7070M series, a surge voltage (ringing noise) that exceeds the MOSFET capacity to withstand might be applied to the IC. To prevent damage, the SLA7070M series is designed a MOSFET having sufficient avalanche resistance to withstand this surge voltage. Therefore, even if surge voltages occur, users will be able to use the IC without any problems. However, in cases in which the motor harness is long or the IC is used above its rated current or voltage, there is a possibility that an avalanche energy could be applied that exceeds Sanken design expectations. Thus, users must test the avalanche energy applied to the IC under actual application conditions.

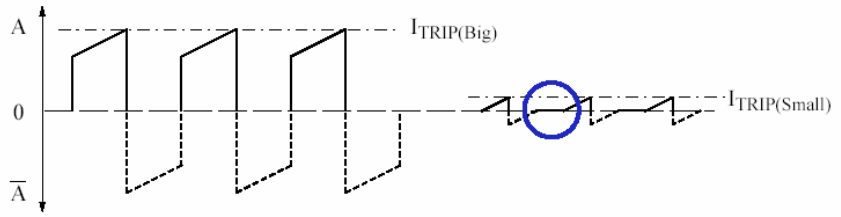

Figure 5. Control current lower limit model waveform. The circled area indicates interval when the coil current generated is 0 A.

The following procedure can be used to check the avalanche energy in an application. The schematic in figure 6 illustrates the location for the voltage test points and circuit characteristics. The timing diagram illustrates the waveform characteristics resultant.

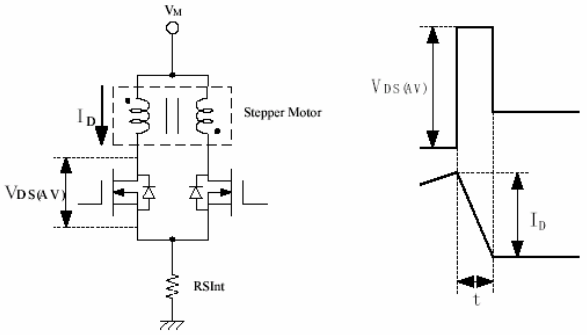

Figure 6. Test points and characteristics (left panel) and breakdown waveform (right).

Given:

$V_{DS(AV)}$ = 1 A,

I_D = 1 A, and

t = 0.5 µs.

The avalanche energy, E_{AV}, can be calculated using the following formula:

$$E_{AV} = V_{DS(AV)} \times 0.5 \times I_D \times t \quad (5)$$

$$= 140\ V \times 0.5 \times 1A \times 10^{-6}$$

$$= 0.035\ mJ$$

By comparing the E_{AV} calculated with the graph shown in figure 9, the application can be evaluated if it is safe for the IC by being within the avalanche energy-tolerated dose range of the MOSFET.

On-Off Sequence of Power Supply (VBB and VDD)

There is no restriction of the on-off sequence of the main power supply, VBB, and the logic supply, VDD.

Motor Supply Voltage (V_M) and Main Power Supply Voltage (V_{BB})

Because the SLA7070M series has a structure that separates the control IC (MIC) and the power MOSFETs as shown in the schematics on pages 10 and 11, motor supply and main power supply are separated. Therefore, it is possible to drive the IC with using different power supplies and different voltages for motor supply and main power supply. However, extra caution is needed because the supply voltage ranges differ among power supplies.

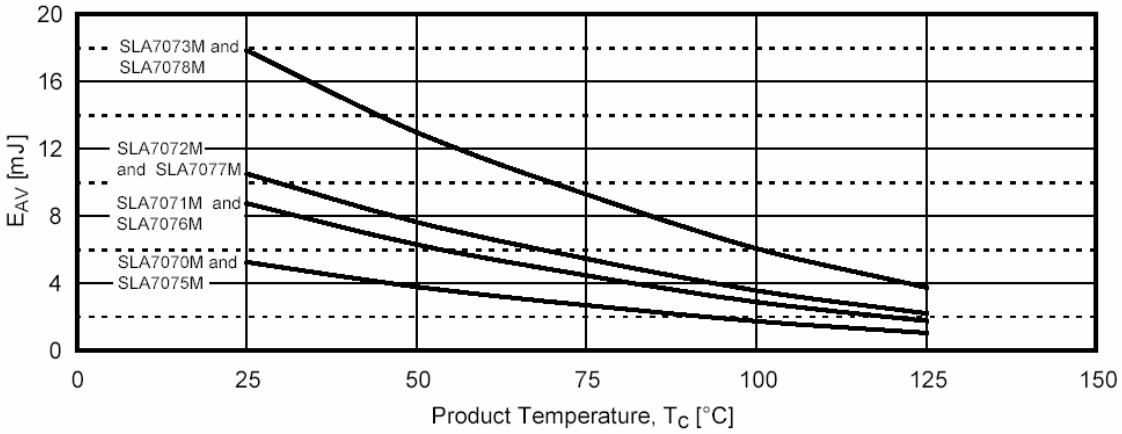

Figure 7. SLA7070M series iterated avalanche energy tolerated dose, $E_{AV(max)}$.

Internal Logic Circuits

• Reset

The sequencer circuit of this product is initialized after logic supply (V_{DD}) is applied, and the power on reset function operates. To initialize the sequencer, the output immediately after power-on indicates that the status that the power circuits are in the home state. In a case where the sequencer must be reset after motor has been operating, a reset signal must be inputted on the RESET pin. In a case in which external reset control is not necessary, the RESET pin is not used, and must be fixed at a logic low level on the application circuit board.

• CLOCK Input

When the CLOCK input signal stops, excitation changes to the motor Hold state. At this time, there is no difference if the CLOCK input signal is at the low level or the high level. The SLA7070M series is designed to move 1 step at a time, when a Clock pulse edge is detected.

• Chopping Synchronous Circuit

The SLA7070M series has a chopping synchronous function to protect from abnormal noises that may occasionally occur during the motor-Hold state. This function can be operated by setting the SYNC terminal at high level. However, if this function is used during motor rotation, control current does not stabilize, and therefore this may cause reduction of motor torque or increased vibration. So, Sanken does not recommend using this function while the motor is rotating. In addition, the synchronous circuit should be disabled in order to control motor current properly in case it is used other than in dual excitation state (Modes 8 and F) or single excitation Hold state.

In normal operation, generally the input signal for switching can be sent from an external microcomputer. However, in applications where the input signal cannot be transmitted adequately due to limitations of the port, the following method can be taken to use the functions.

The schematic diagram in figure 8 shows how the IC is designed so that the Sync signal can be determined by the CLOCK input signal. When a logic high signal is received on the CLOCK pin, the internal capacitor, C, is charged, and the Sync signal is set to logic low level. However, if the Clock signal cannot rise above logic low level (such as when the circuit between the microcomputer and the IC is not adequate), the capacitor is discharged by the internal resistor, R, and the Sync signal is set to logic high, causing the IC to shift to synchronous mode.

The RC time constant in the circuit should be determined by the minimum clock frequency used. In the case of a sequence that keeps the CLOCK input signal at logic high, an inverter circuit must be added. In a case where the Clock signal is set at an undetermined level, an edge detection circuit (figure 9) can be used to prepare the signal for the CLOCK input, allowing correct processing by the circuit shown in figure 8.

• Output Disable (Sleep1 and Sleep2) Circuits

There are two methods to set this IC at motor free-state (coast, with outputs disabled). One is to set the REF/SLEEP1 pin to more than 2 V (Sleep1), and the other (Sleep2) is to set the excitation signals (pins M1, M2, and M3). In either way, the IC will change to Sleep mode, stopping the main power supply at the same time, and decreasing circuit current. The difference between the two methods is that, in the first way, the internal sequencer remains in an enabled state, and in the latter method, the IC enters the Hold state. Moreover, in the method using

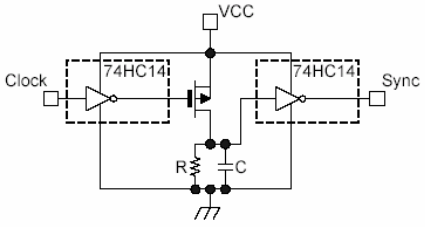

Figure 8. Clock signal shutoff detection circuit, using 74HC14s.

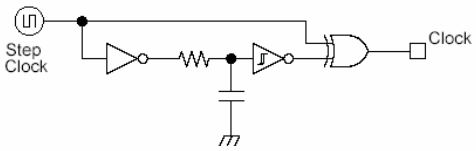

Figure 9. Clock signal edge detection circuit, inputs to example circuit shown in figure 8.

the excitation signals (Sleep2), excitation timing remains in a "standby" state, even if a signal is inputted on the CLOCK pin during Sleep mode.

When awaking to normal operating mode (motor rotation) from disabled (Sleep1 or Sleep2) mode, set an appropriate delay time from cancellation of the disable mode to the initial CLOCK input edge. In doing so, consider not only of rise time for the IC, but also of the rise time for the motor excitation current, is important (see figure 10).

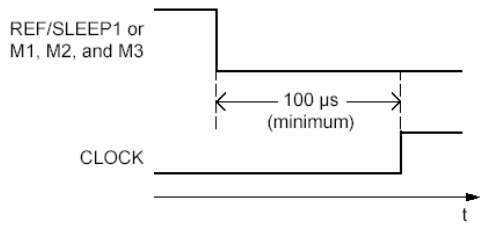

Figure 10. Timing delay between disable cancellation and the next Clock input

• REF/SLEEP1 Pin

The REF/SLEEP1 pin provides access to the following functions:

- Standard voltage setting for output current level setting
- Output enable-disable control input

These functions are further described in the Truth Tables section (page 13), and in the discussion of output disabling, above.

The figure in the Reference Voltage Setting section (page 7), shows the general relationship between the reference voltage, V_{REF}, (REF/SLEEP1 pin) setting voltage and performance. There are, however, situations in which extra caution should be exercised. These are shown in figure 11:

Range A. In this range, control current value also varies in accordance with V_{REF}. Therefore, losses in the IC and the sense resistors must be given extra consideration.

Range B. In this range, the voltage that switches output enable and disable (Sleep mode) exists. At enable, the same cautions apply as in range A. In addition, for some cases, there are possibilities that the output status will become unstable as a result of iteration between enable and disable.

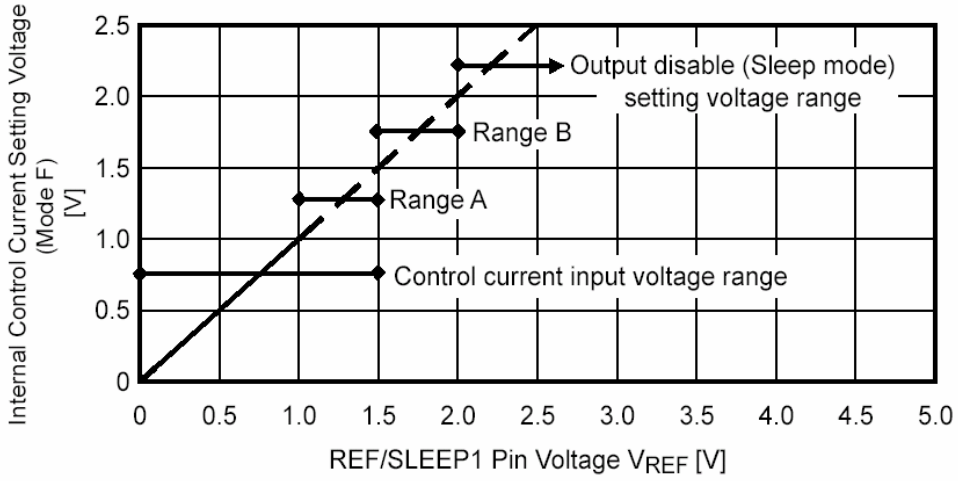

Figure 11. Relationship between external and internal reference voltages and performance. Ensure that the absolute maximum current level is not reached.

• Logic Input Pins

If a logic input pin (CLOCK, RESET, F/R, M1, M2, M3, or SYNC) is not used (fixed logic level), the pin must be tied to VDD or GND. Please do not leave them floating, because there is possibility of undefined effects on IC performance when they are left open.

• Output Pins

The Mo and FLAG output pins are designed as monitor outputs, and inside of the IC is an output inverter (see figure 12). Therefore, let these pins float if they are not used.

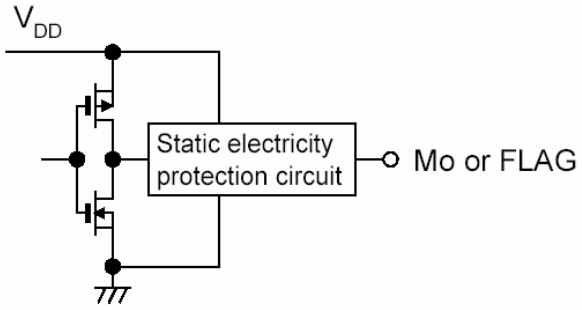

Figure 12. Mo pin (SLA 7075M through SLA 7078M models only) and FLAG pin general internal circuit layout

THERMAL DESIGN INFORMATION

It is not practical to calculate the power dissipation of SLA7070M series accurately, because that would require factors that are variable during operation, such as time periods and excitation modes during motor rotation, input frequencies and sequences, and so forth. Given this situation, it is preferable to perform an approximate calculation at worst conditions. The following is a simplified formula for calculation of power dissipation:

$$P_D = I^2_{OUT} \times (R_{DS(on)} + R_{SInt}) \times 2 \quad (6)$$

where:

P_D is the power dissipation in the IC,

I_{OUT} is the operating output current,

$R_{DS(on)}$ is the on resistance of the output MOSFET, and

R_{SInt} is current sense resistance.

Based on the P_D calculated using the above formulas, the expected increase in operating junction temperature, ΔT_J, of the IC can be estimated using figure 13. This result must be added to the worst case ambient temperature when operating, $T_{A(max)}$. Based on the calculation, there is no problem unless $T_{A(max)} + \Delta T_J > 150°C$.

However, final confirmation must be made by measuring the IC temperature during operation and then verifying power dissipation and junction temperature in the corresponding graph.

When the IC is used with a heat sink attached, device package thermal resistance, $R_{\theta JA}$, is a variable used in calculating ΔTj-a.

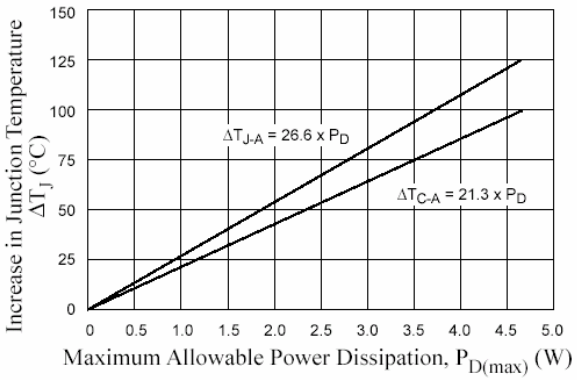

Figure 13. Temperature increase

The value of $R_{\theta JA}$ is calculated from the following formula:

$$R_{\theta JA} \approx R_{\theta JC} + R_{\theta Fin} = R_{\theta JA} - R_{\theta CA} + R_{\theta Fin} \quad (7)$$

where $R_{\theta Fin}$ is the thermal resistance of the heat sink.

ΔT_{JA} can be calculated with using the value of $R_{\theta JA}$:

$$\Delta T_J \approx \Delta T_{JC} + P_D \times R_{\theta JC} \quad (8)$$

The following procedure should be used to measure product temperature in actual operation and then estimate junction temperature:

1. Measure the ambient temperature, T_A.
2. With the device mounted but not operating, measure the temperature of the device case at the center (pin 12).
3. Power-on the device, and after it reaches operating temperature, take the measurement again.
4. Subtract the value found in step 2 from the value found in step 3. This will provide a value for ΔT_{CA}.
5. Refer to figure 13 and locate the value found in step 4 on the ΔT_{CA} trace.
6. Determine the corresponding power dissipation, P_D.
7. Substitute the values into equation 8.

CAUTION

The SLA7070M series is designed as a multichip, with separate power elements (MOSFET), control IC (MIC), and sense resistance. Consequently, because the control IC cannot accurately detect the temperature of the power elements (which are the primary sources of heat), the ICs do not provide a protection function against overheating. For thermal protection, users must conduct sufficient thermal evaluations to be able to ensure that the junction temperature does not exceed the warranty level (150°C).

This thermal design information is provided for preliminary design estimations only. The thermal performance of the IC will be significantly determined by the conditions of the application, in particular the state of the mounting PCB, heat sink, and the ambient air. Before operating the IC in an application, the user must experimentally determine the actual thermal performance.

The maximum recommended case temperatures (at the center, pin 12) for the IC are:

- With no external heat sink connection: 90°C
- With external heat sink connection: 80°C

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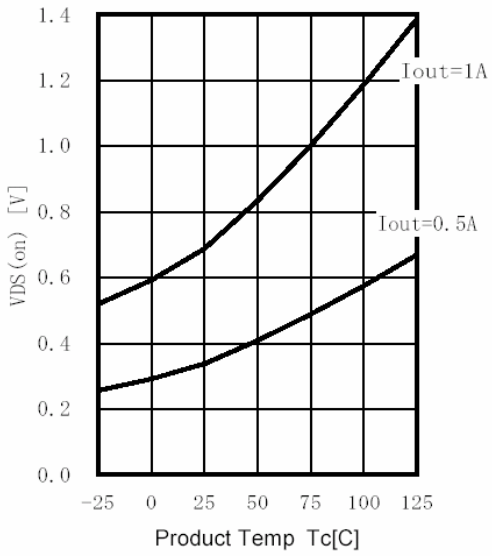
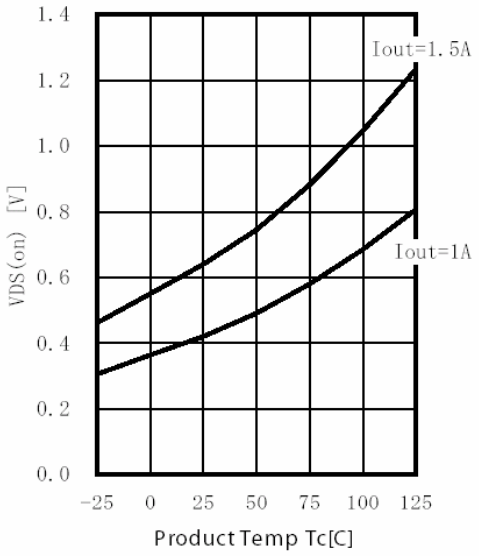
CHARACTERISTIC DATA

Output MOSFET On-Voltage, $V_{DS(on)}$

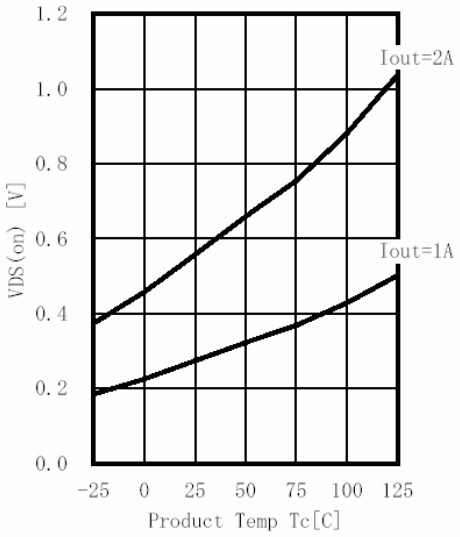
SLA7070M/SLA7075M



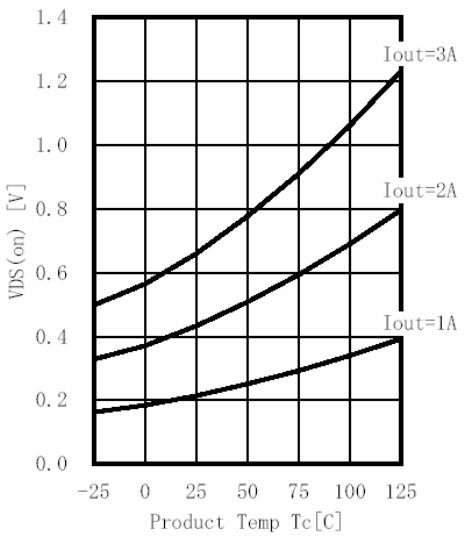
SLA7071M/SLA7076M



SLA7072M/SLA7077M



SLA7073M/SLA7078M



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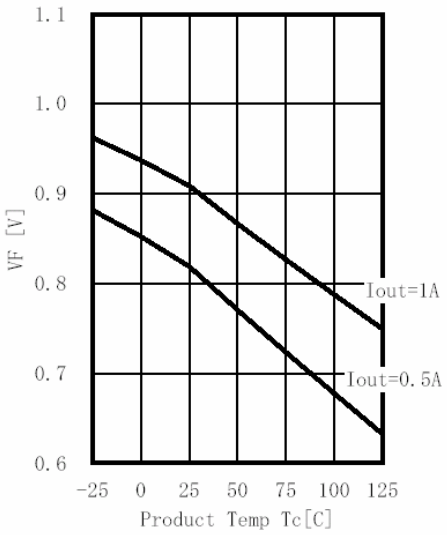
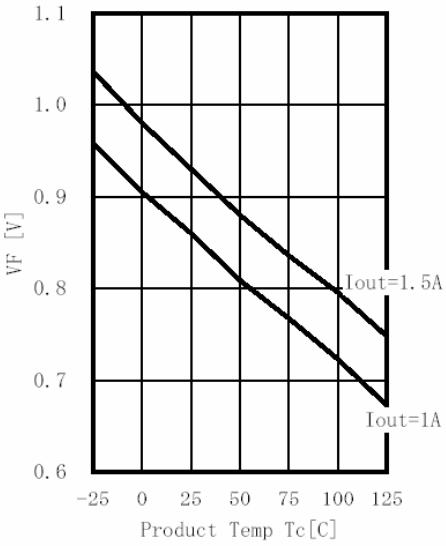
Output MOSFET Body Diodes Forward Voltage, V_F

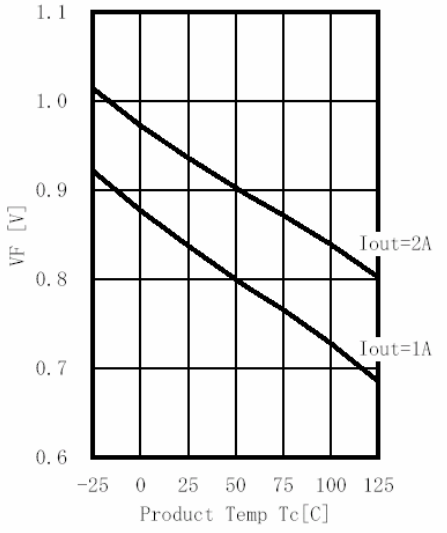
SLA7070M/SLA7075M



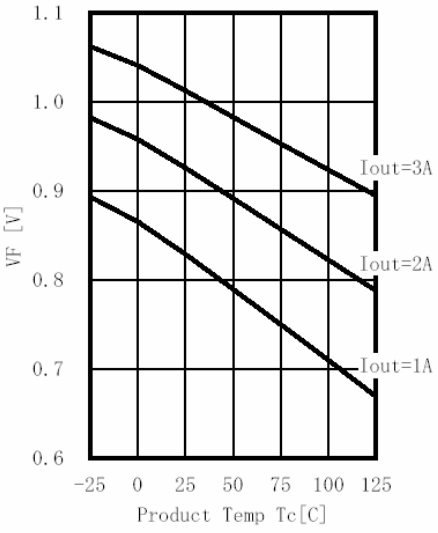
SLA7071M/SLA7076M



SLA7072M/SLA7077M



SLA7073M/SLA7078M



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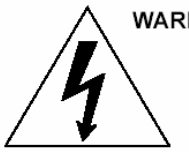

WARNING — These devices are designed to be operated at lethal voltages and energy levels. Circuit designs that embody these components must conform with applicable safety requirements. Precautions must be taken to prevent accidental contact with power-line potentials. Do not connect grounded test equipment.

The use of an isolation transformer is recommended during circuit development and breadboarding.

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