

1-Mbit (64K x 16) Static RAM

Features

- High speed: 45 ns
- Temperature ranges
 - Industrial: -40°C to +85°C
 - Automotive: -40°C to +125°C
- Wide voltage range: 2.2V to 3.6V
- Pin compatible with CY62126DV30
- Ultra low standby power
 - Typical standby current: 1 μA
 - Maximum standby current: 4 μA
- Ultra low active power
 - Typical active current: 1.3 mA at f = 1 MHz
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Offered in Pb-free 48-ball VFBGA and 44-pin TSOP II packages

Functional Description

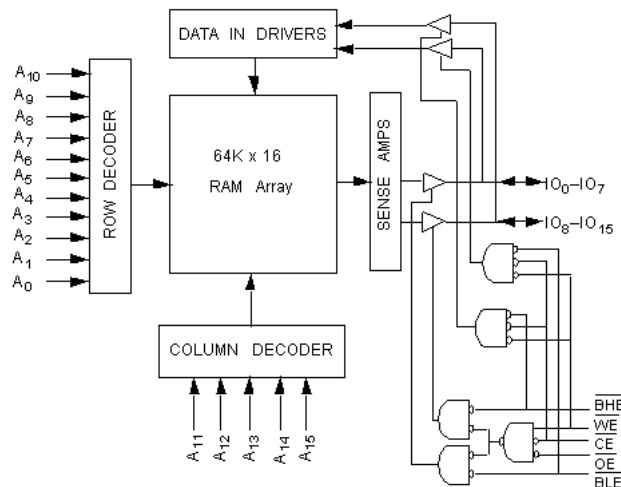
The CY62126EV30 is a high performance CMOS static RAM organized as 64K words by 16 bits^[1]. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL[®]) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device in standby mode reduces power consumption by more than 99 percent when deselected (\overline{CE} HIGH). The input and output pins (IO₀ through IO₁₅) are placed in a high impedance state when:

- Deselected (\overline{CE} HIGH)
- Outputs are disabled (\overline{OE} HIGH)
- Both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , \overline{BLE} HIGH)
- Write operation is active (\overline{CE} LOW and \overline{WE} LOW)

To write to the device, take Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from IO pins (IO₀ through IO₇) is written into the location specified on the address pins (A₀ through A₁₅). If Byte High Enable (\overline{BHE}) is LOW, then data from IO pins (IO₈ through IO₁₅) is written into the location specified on the address pins (A₀ through A₁₅).

To read from the device, take Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appear on IO₀ to IO₇. If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on IO₈ to IO₁₅. See the “Truth Table” on page 9 for a complete description of read and write modes.

Logic Block Diagram



Note

1. For best practice recommendations, refer to the Cypress application note [AN1064, SRAM System Guidelines](#).

Pin Configurations

Figure 1. 44-Ball VFBGA (Top View)

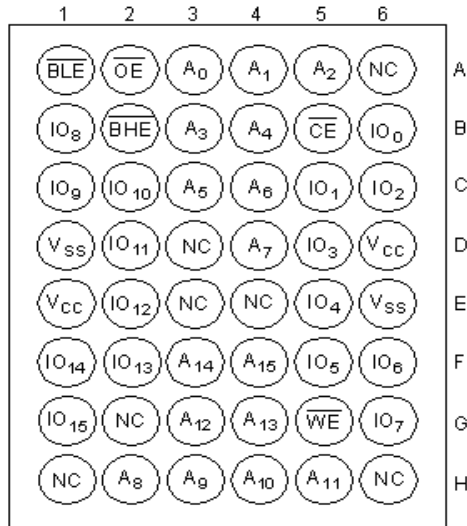


Figure 2. 44-Pin TSOP II (Top View)^[2]

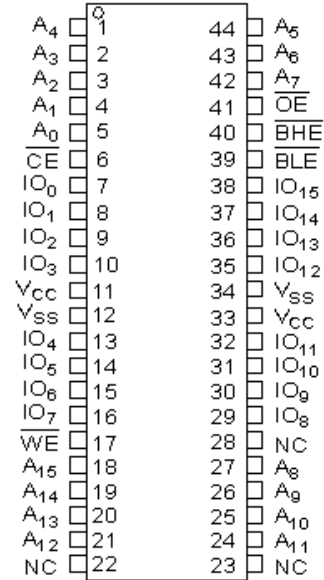


Table 1. Product Portfolio

Product	Range	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating, I _{CC} (mA)				Standby, I _{SB2} (μA)	
		f = 1 MHz		f = f _{max}							
		Min	Typ ^[3]	Max		Typ ^[3]	Max	Typ ^[3]	Max	Typ ^[3]	Max
CY62126EV30LL	Industrial	2.2	3.0	3.6	45	1.3	2	11	16	1	4
CY62126EV30LL	Automotive	2.2	3.0	3.6	55	1.3	4	11	35	1	30

Notes

- NC pins are not connected on the die.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25°C.

Maximum Ratings

Exceeding maximum ratings may shorten the battery life of the device. These user guidelines are not tested.

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential.....	-0.3V to 3.6V ($V_{CCmax} + 0.3V$)
DC Voltage Applied to Outputs in High-Z State ^[4, 5]	-0.3V to 3.6V ($V_{CCmax} + 0.3V$)

DC Input Voltage ^[4, 5]	-0.3V to 3.6V ($V_{CCmax} + 0.3V$)
Output Current into Outputs (LOW).....	20 mA
Static Discharge Voltage.....	> 2001V (MIL-STD-883, Method 3015)
Latch up Current.....	> 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} ^[6]
CY62126EV30LL	Industrial	-40°C to +85°C	2.2V to 3.6V
	Automotive	-40°C to +125°C	

Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	45 ns (Industrial)			55 ns (Automotive)			Unit
			Min	Typ ^[1]	Max	Min	Typ ^[1]	Max	
V_{OH}	Output HIGH Voltage	$I_{OH} = -0.1$ mA	2.0			2.0			V
		$I_{OH} = -1.0$ mA, $V_{CC} \geq 2.70V$	2.4			2.4			V
V_{OL}	Output LOW Voltage	$I_{OL} = 0.1$ mA			0.4			0.4	V
		$I_{OL} = 2.1$ mA, $V_{CC} \geq 2.70V$			0.4			0.4	V
V_{IH}	Input HIGH Voltage	$V_{CC} = 2.2V$ to $2.7V$	1.8		$V_{CC} + 0.3$	1.8		$V_{CC} + 0.3$	V
		$V_{CC} = 2.7V$ to $3.6V$	2.2		$V_{CC} + 0.3$	2.2		$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage	$V_{CC} = 2.2V$ to $2.7V$	-0.3		0.6	-0.3		0.6	V
		$V_{CC} = 2.7V$ to $3.6V$	-0.3		0.8	-0.3		0.8	V
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		+1	-4		+4	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled	-1		+1	-4		+4	μA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{max} = 1/t_{RC}$		11	16		11	35	mA
		$f = 1$ MHz		1.3	2.0		1.3	4.0	
I_{SB1}	Automatic CE Power down Current —CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, $V_{IN} \leq 0.2V$) $f = f_{max}$ (Address and Data Only), $f = 0$ (OE, BHE, BLE and WE), $V_{CC} = 3.60V$		1	4		1	35	μA
I_{SB2} ^[7]	Automatic CE Power down Current —CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0$, $V_{CC} = 3.60V$		1	4		1	30	μA

Capacitance

For all packages. Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ C$, $f = 1$ MHz, $V_{CC} = V_{CC}(typ)$	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes

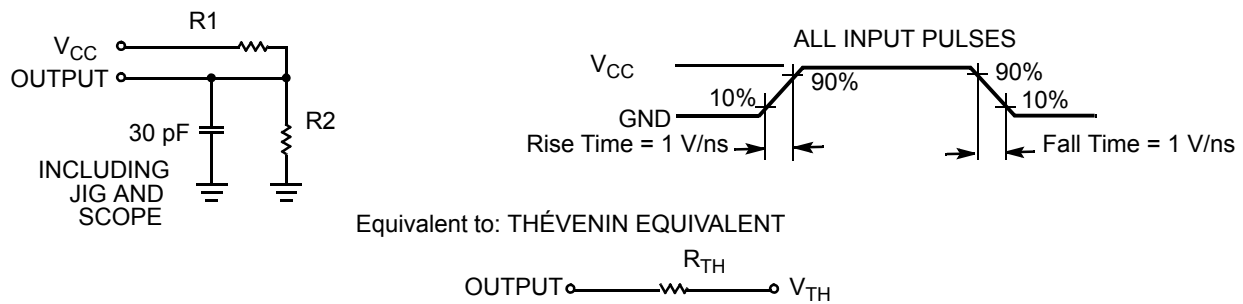
- $V_{IL(min)}$ = -2.0V for pulse durations less than 20 ns.
- $V_{IH(max)}$ = $V_{CC} + 0.75V$ for pulse durations less than 20 ns.
- Full device AC operation assumes a 100 μs ramp time from 0 to $V_{CC}(min)$ and 200 μs wait time after V_{CC} stabilization.
- Only chip enable (CE) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	VFBGA Package	TSOP II Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, two-layer printed circuit board	58.85	28.2	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		17.01	3.4	°C/W

Figure 3. AC Test Loads and Waveforms



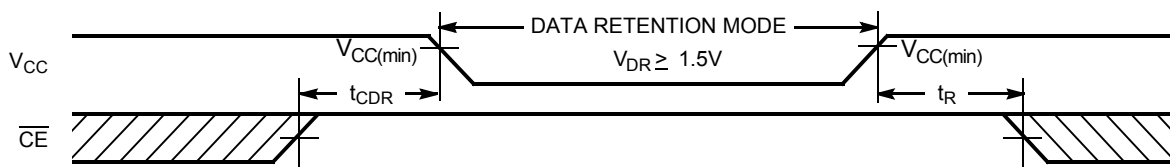
Parameters	2.2V - 2.7V	2.7V - 3.6V	Unit
R1	16600	1103	Ohms
R2	15400	1554	Ohms
R _{TH}	8000	645	Ohms
V _{TH}	1.2	1.75	Volts

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[1]	Max	Unit
V _{DR}	V _{CC} for Data Retention		1.5			V
I _{CCDR} ^[7]	Data Retention Current	V _{CC} = V _{DR} , $\overline{CE} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V			3	μA
		Automotive			30	μA
t _{CDR} ^[8]	Chip Deselect to Data Retention Time		0			ns
t _R ^[9]	Operation Recovery Time		t _{RC}			ns

Figure 4. Data Retention Waveform



Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Full device AC operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} > 100 μs.

Switching Characteristics

 Over the Operating Range ^[10, 11]

Parameter	Description	45 ns (Industrial)		55 ns (Automotive)		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read Cycle Time	45		55		ns
t_{AA}	Address to Data Valid		45		55	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	\overline{CE} LOW to Data Valid		45		55	ns
t_{DOE}	\overline{OE} LOW to Data Valid		22		25	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[12]	5		5		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[12, 13]		18		20	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[12]	10		10		ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[12, 13]		18		20	ns
t_{PU}	\overline{CE} LOW to Power Up	0		0		ns
t_{PD}	\overline{CE} HIGH to Power Down		45		55	ns
t_{DBE}	\overline{BHE} / \overline{BLE} LOW to Data Valid		22		25	ns
t_{LZBE}	\overline{BHE} / \overline{BLE} LOW to Low Z ^[12]	5		5		ns
t_{HZBE}	\overline{BHE} / \overline{BLE} HIGH to High Z ^[12, 13]		18		20	ns
Write Cycle ^[14]						
t_{WC}	Write Cycle Time	45		55		ns
t_{SCE}	\overline{CE} LOW to Write End	35		40		ns
t_{AW}	Address Setup to Write End	35		40		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Setup to Write Start	0		0		ns
t_{PWE}	\overline{WE} Pulse Width	35		40		ns
t_{BW}	\overline{BHE} / \overline{BLE} Pulse Width	35		40		ns
t_{SD}	Data Setup to Write End	25		25		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[12, 13]		18		20	ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[12]	10		10		ns

Notes

10. Test conditions assume signal transition time of 3 ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
11. AC timing parameters are subject to byte enable signals (\overline{BHE} or \overline{BLE}) not switching when chip is disabled. See [application note AN13842](#) for further clarification.
12. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
13. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
14. The internal write time of the memory is defined by the overlap of \overline{WE} , $CE = V_{IL}$, \overline{BHE} , \overline{BLE} or both = V_{IL} . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must refer to the edge of signal that terminates write.

Switching Waveforms

Figure 5. Read Cycle No. 1(Address transition controlled)^[15, 16]

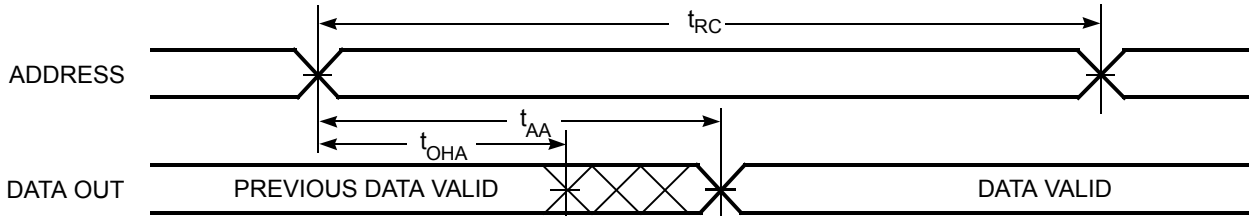
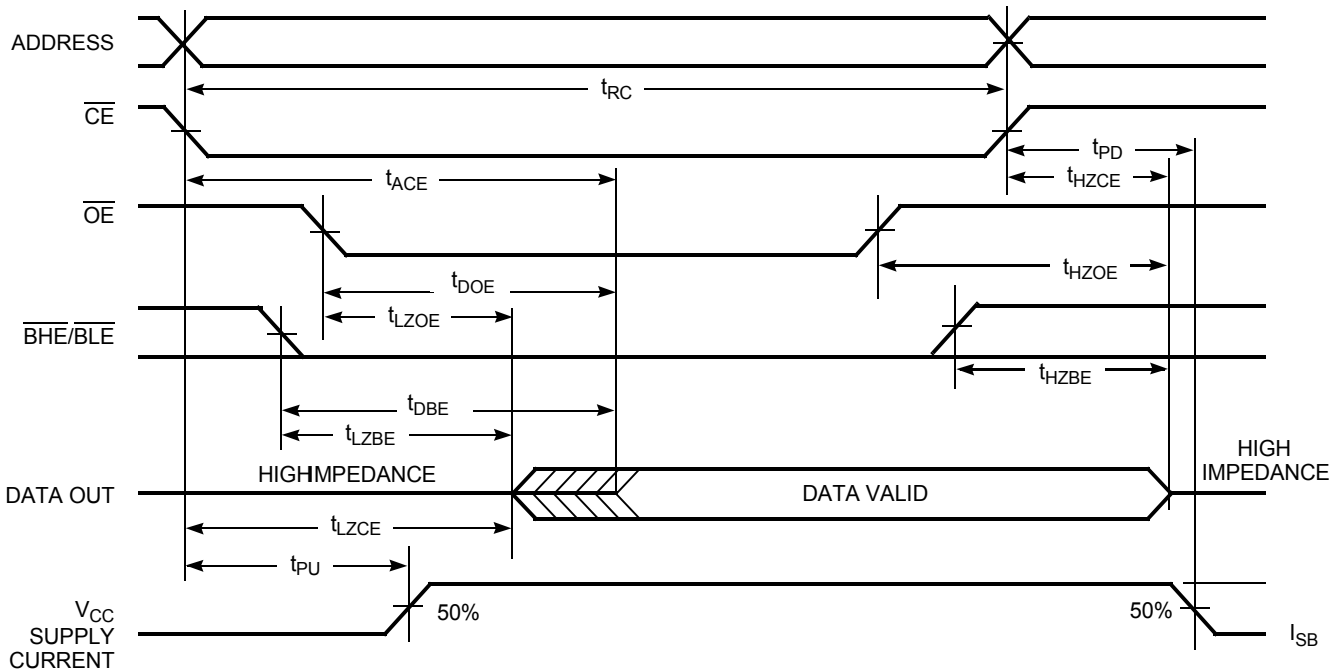


Figure 6. Read Cycle No. 2 (\overline{OE} controlled)^[16, 17]



Notes

- 15. The device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} , or both = V_{IL} .
- 16. \overline{WE} is HIGH for read cycle.
- 17. Address valid before or similar to \overline{CE} and \overline{BHE} , \overline{BLE} transition LOW.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 (\overline{WE} controlled)^[14, 18, 19]

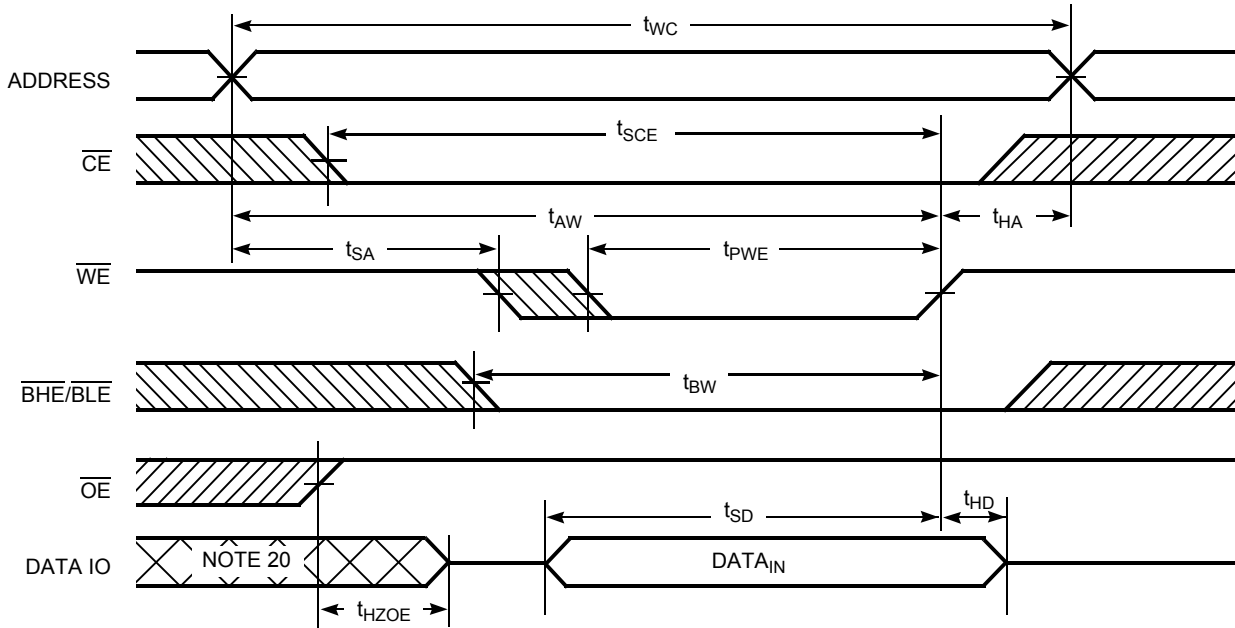
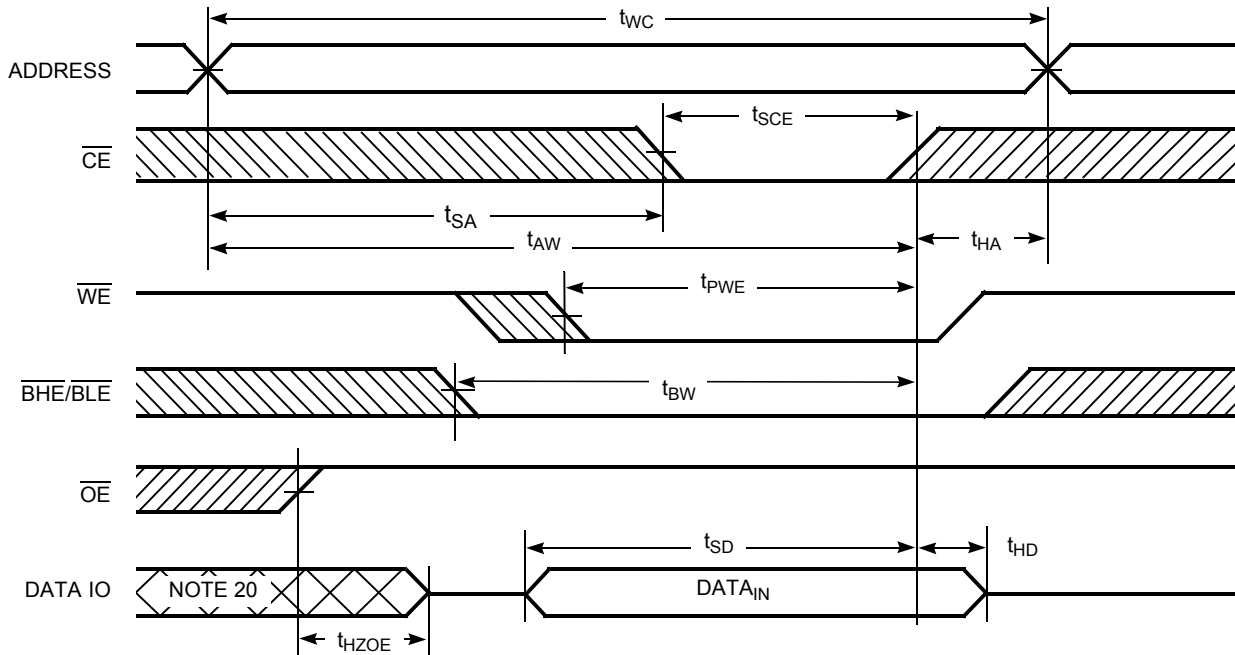


Figure 8. Write Cycle No. 2 (\overline{CE} controlled)^[14, 18, 19]



Notes

- 18. Data IO is high impedance if $\overline{OE} = V_{IH}$.
- 19. If \overline{CE} goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 20. During this period, the IOs are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW)^[19]

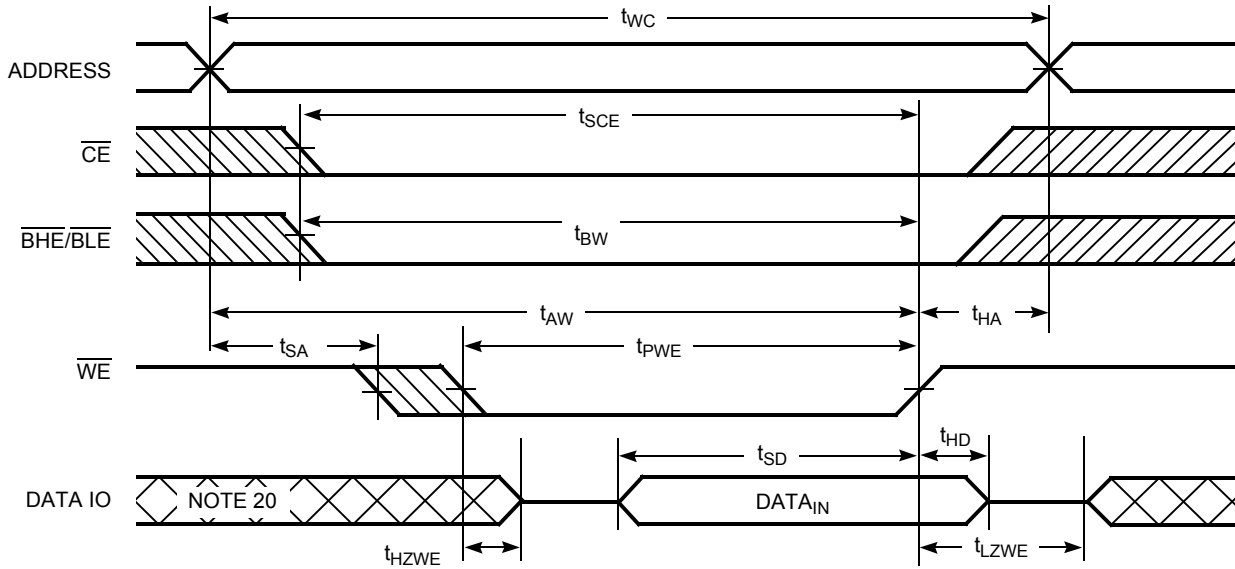
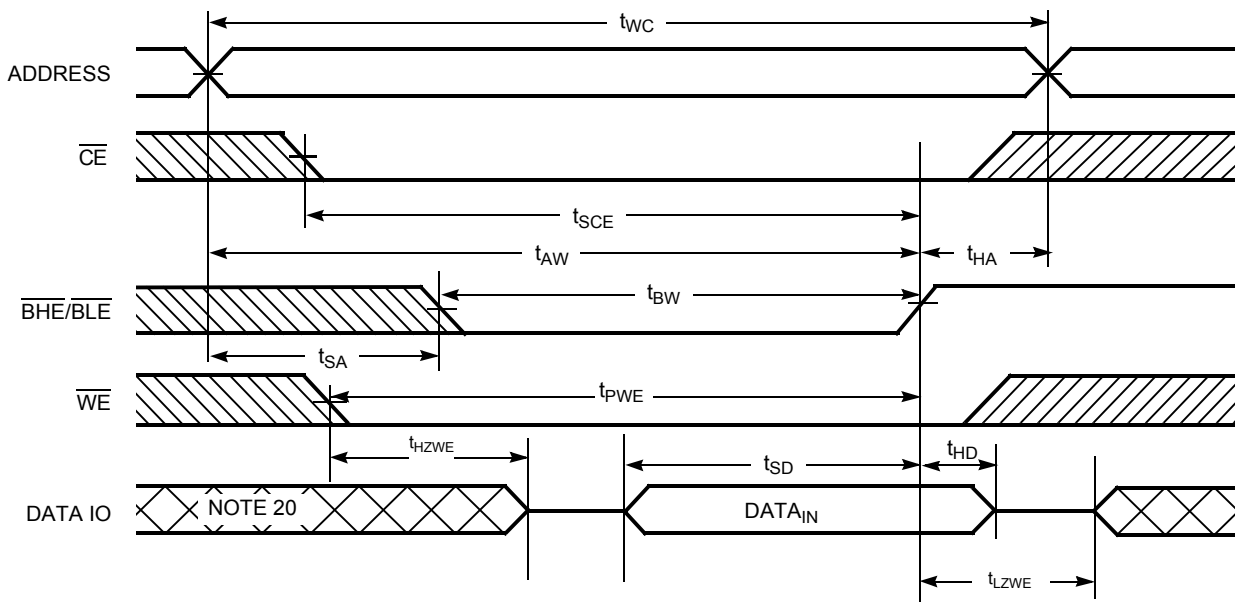


Figure 10. Write Cycle No. 4 ($\overline{BHE/BLE}$ controlled, \overline{OE} LOW)^[19]



Truth Table

\overline{CE}	\overline{WE}	\overline{OE}	\overline{BHE}	\overline{BLE}	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power Down	Standby (I_{SB})
L	X	X	H	H	High Z	Output Disabled	Active (I_{CC})
L	H	L	L	L	Data Out (IO_0 - IO_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (IO_0 - IO_7); IO_8 - IO_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (IO_8 - IO_{15}); IO_0 - IO_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (IO_0 - IO_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (IO_0 - IO_7); IO_8 - IO_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (IO_8 - IO_{15}); IO_0 - IO_7 in High Z	Write	Active (I_{CC})

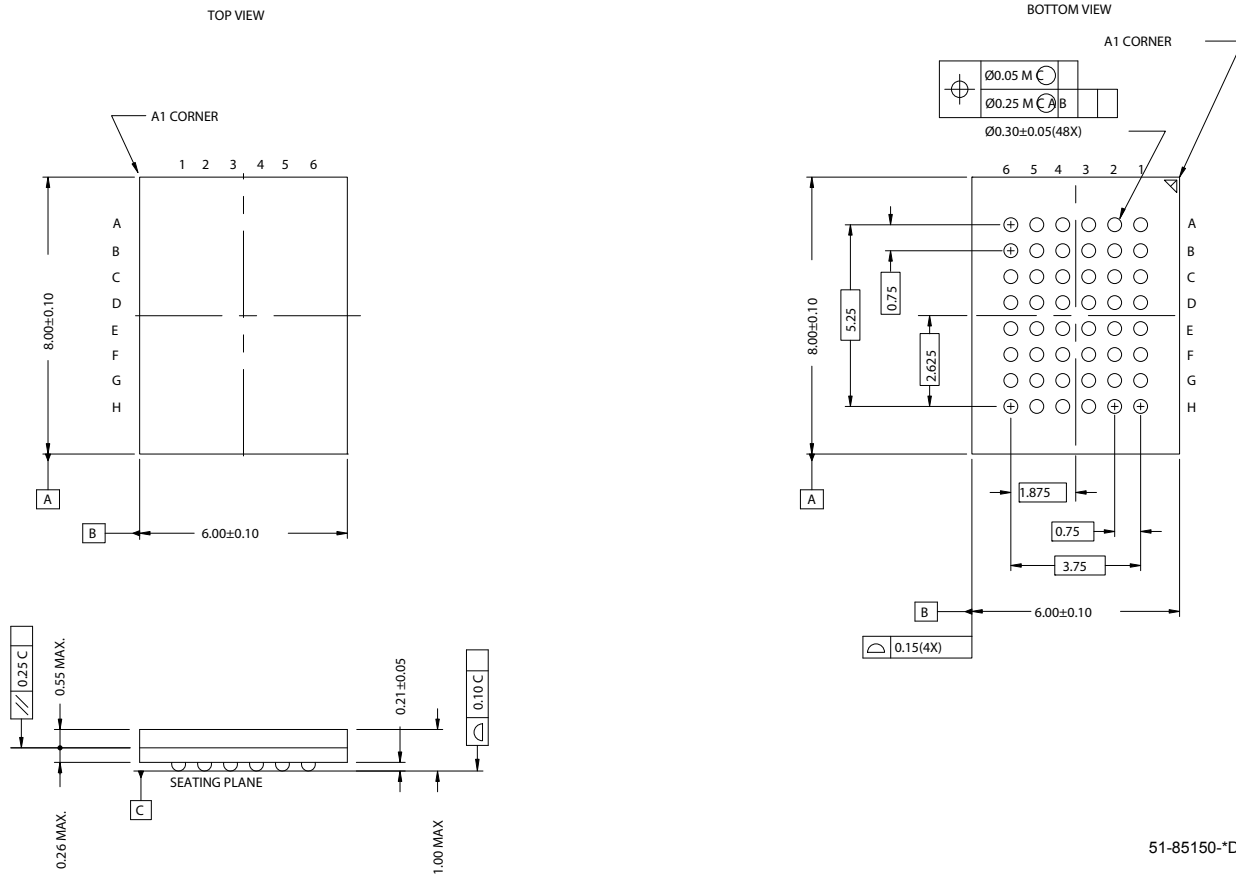
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62126EV30LL-45BVXI	51-85150	48-ball Very Fine Pitch Ball Grid Array (Pb-free)	Industrial
	CY62126EV30LL-45ZSXI	51-85087	44-pin Thin Small Outline Package II (Pb-free)	
55	CY62126EV30LL-55BVXE	51-85150	48-ball Very Fine Pitch Ball Grid Array (Pb-free)	Automotive
	CY62126EV30LL-55ZSXE	51-85087	44-pin Thin Small Outline Package II (Pb-free)	

Contact your local Cypress sales representative for availability of other parts.

Package Diagrams

Figure 11. 48-Ball VFBGA (6 x 8 x 1 mm) (51-85150)

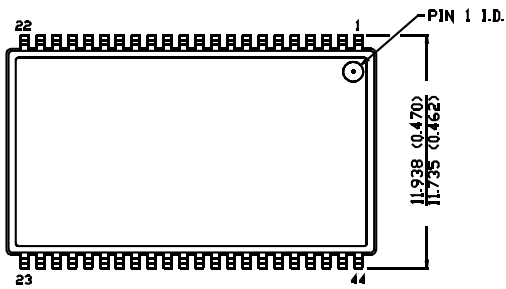


51-85150-*D

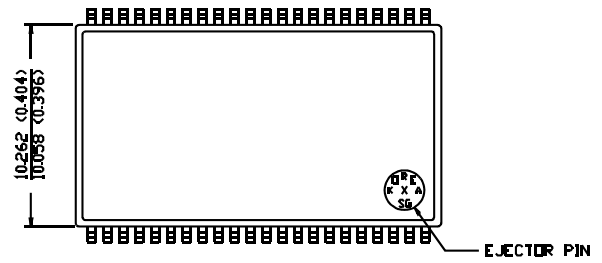
Package Diagrams (continued)

Figure 12. 44-Pin TSOP II (51-85087)

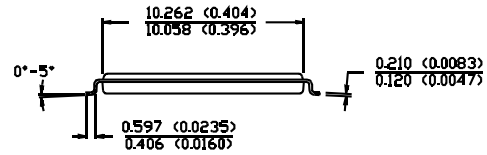
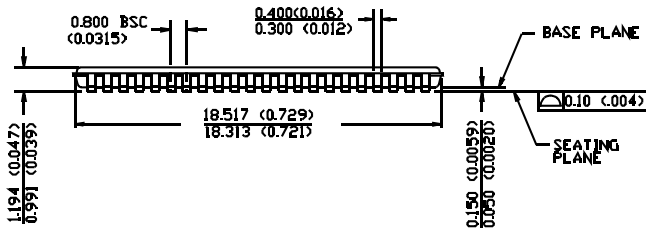
DIMENSION IN MM (INCH)
MAX
MIN



TOP VIEW



BOTTOM VIEW



51-85087-*A

Document History Page

Document Title: MoBL [®] CY62126EV30, 1-Mbit (64K x 16) Static RAM				
Document Number: 38-05486				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	202760	See ECN	AJU	New data sheet
*A	300835	See ECN	SYT	<p>Converted from Advance Information to Preliminary</p> <p>Specified Typical standby power in the Features Section</p> <p>Changed E3 ball from DNU to NC in the Pin Configuration for the FBGA Package and removed the footnote associated with it on page #2</p> <p>Changed t_{OHA} from 6 ns to 10 ns for both 35- and 45-ns speed bins, respectively</p> <p>Changed t_{DOE}, t_{SD} from 15 to 18 ns for 35-ns speed bin</p> <p>Changed t_{HZOE}, t_{HZBE}, t_{HZWE} from 12 and 15 ns to 15 and 18 ns for the 35- and 45-ns speed bins, respectively</p> <p>Changed t_{HZCE} from 12 and 15 ns to 18 and 22 ns for the 35- and 45-ns speed bins, respectively</p> <p>Changed t_{SCE}, t_{BW} from 25 and 40 ns to 30 and 35 ns for the 35- and 45-ns speed bins, respectively</p> <p>Changed t_{AW} from 25 to 30 ns and 40 to 35 ns for 35 and 45-ns speed bins respectively</p> <p>Changed t_{DBE} from 35 and 45 ns to 18 and 22 ns for the 35 and 45 ns speed bins respectively</p> <p>Removed footnote that read "$\overline{BHE}.\overline{BLE}$ is the AND of both \overline{BHE} and \overline{BLE}. Chip can be deselected by either disabling the chip enable signals or by disabling both BHE and BLE" on page # 4</p> <p>Removed footnote that read "If both \overline{BHE} and \overline{BLE} are toggled together, then t_{LZBE} is 10 ns" on page # 5</p> <p>Added Pb-free package information</p>
*B	461631	See ECN	NXR	<p>Converted from Preliminary to Final</p> <p>Removed 35 ns Speed Bin</p> <p>Removed "L" version of CY62126EV30</p> <p>Changed $I_{CC(Typ)}$ from 8 mA to 11 mA and $I_{CC(max)}$ from 12 mA to 16 mA for $f = f_{max}$</p> <p>Changed $I_{CC(max)}$ from 1.5 mA to 2.0 mA for $f = 1$ MHz</p> <p>Changed I_{SB1}, $I_{SB2(max)}$ from 1 μA to 4 μA</p> <p>Changed I_{SB1}, $I_{SB2(Typ)}$ from 0.5 μA to 1 μA</p> <p>Changed $I_{CCDR(max)}$ from 1.5 μA to 3 μA</p> <p>Changed the AC Test load Capacitance value from 50 pF to 30 pF</p> <p>Changed t_{LZOE} from 3 to 5 ns</p> <p>Changed t_{LZCE} from 6 to 10 ns</p> <p>Changed t_{HZCE} from 22 to 18 ns</p> <p>Changed t_{LZBE} from 6 to 5 ns</p> <p>Changed t_{PWE} from 30 to 35 ns</p> <p>Changed t_{SD} from 22 to 25 ns</p> <p>Changed t_{LZWE} from 6 to 10 ns</p> <p>Updated the Ordering Information table.</p>
*C	925501	See ECN	VKN	<p>Added footnote #7 related to I_{SB2} and I_{CCDR}</p> <p>Added footnote #11 related AC timing parameters</p>
*D	1045260	See ECN	VKN	<p>Added Automotive information</p> <p>Updated Ordering Information table</p>
*E	2631771	01/07/09	NXR/PYRS	<p>Changed CE condition from X to L in Truth table for Output Disable mode</p> <p>Updated template</p>

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