8 Port 10/100 Ethernet Integrated Switch

Features

- Support 1k MAC address
- 512k bits packet buffer memory
- Support auto-polarity for 10 Mbps
- Support filter/ forward special DA option
- Support broadcast storm protection
- Auto MDI-MDIX option
- Support port security option to lock the first MAC address
- Support one MII/RMII port, which works at 100 Mbps full duplex for router application
- Support port base VLAN & tag VLAN
- Support CoS
- Support SMART MAC function
- Support spanning tree protocol
- Support max forwarding packet length 1552/ 1536 bytes option
- Support 8-level bandwidth control
- Support SCA
- Support two fiber ports with far end fault function for **IP178CH** only
- Built in linear regulator control circuit
- Support Lead Free package (Please refer to the Order Information)

Note – some features need CPU support, please refer to the detail description inside this data sheet

General Description

IP178C/IP178CH integrates a 9-port switch controller, SSRAM, and 8 10/100 Ethernet transceivers. Each of the transceivers complies with the IEEE802.3, IEEE802.3u, and IEEE802.3x specifications. The transceivers are designed in DSP approach in 0.18um technology; they have high noise immunity and robust performance.

IP178C/IP178CH operates in store and forward mode. It supports flow control, auto MDI/MDI-X, CoS, port base VLAN, bandwidth control, DiffServ, SMART MAC and LED functions, etc. Each port can be configured as auto-negotiation or forced 10 Mbps/100 Mbps, full/half duplex mode. Using an EEPROM or pull up/down resistors on specific pins can configure the desired options.

Besides an 8-port switch application, **IP178C/IP178CH** supports one MII/RMII ports for router application, which supports 7 LAN ports and one WAN port. The external MAC can monitor or configure **IP178C/IP178CH** by accessing MII registers through SMI.

MII/RMII port also can be configured to be MAC mode. It is used to interface an external PHY to work as an 8+1 switch.

IP178CH supports two fiber ports with far end fault function.

Table Of Contents

Features 1
General Description 1
Table Of Contents 2
Revision History 3
Pin diagram (IP178C) 10
1 Pin description 15
Pin description (continued) 16
Pin description (continued) 18
Pin description (continued) 19
Pin description (continued) 20
Pin description (continued) 21
Pin description (continued) 22
Pin description (continued) 24
Pin description (continued) 25
Pin description (continued) 26
Pin description (continued) 27
Pin description (continued) 28
2 Functional Description 29
2.1 Flow control 32
2.2 Broadcast storm protection 33
2.3 Port locking 34
2.4 Port base VLAN 35
2.5 Tag VLAN/ Tag and un-tag function 36
2.6 Tag VLAN 36
2.7 Tag VLAN in router application 37
2.8 Smart MAC 38
2.9 CoS 42
2.9.1 Port base priority 42
2.9.2 Frame base priority 42
2.10 Spanning tree 44
2.11 Static MAC address table 46
2.12 Serial management interface 47
2.13 SCA 48
2.14 Bandwidth control 48
2.15 Register descriptions 49
3 Electrical Characteristics 86
3.1 Absolute Maximum Rating 86
3.2 DC Characteristic 86
3.3 AC Timing 87
3.3.1 PHY Mode MII Timing 87
3.3.2 MAC Mode MII Timing 88
3.3.3 RMII Timing 89
3.3.4 SMI Timing 90
3.3.5 EEPROM Timing 91
3.4 Thermal Data 91
4 Order information 92
5 Package Detail 93

Revision History

Revision #	Change Description
IP178C-DS-R01	Initial release.
IP178C-DS-R02	1. Modify Pin diagram in page 9, pin_89 from HASH_MODE[1]/LINK_LED7 to MLT3_DET/LINK_LED7,pin 84 from LOW_10M_DIS to SCA_DIS, pin_36 from SCA to NC, VCTRL to REG_OUT 2. Replace VCTRL with REG_OUT 3. Modify HASH_MODE [1] to MLT3_DET in page 17, 54 & 55 4. Modify pin 84 from LOW_10M_DIS to SCA_DIS, pin_36 from SCA to NC 5. Change BF_STM_THR_SEL [1:0] from 01: 128 frames to 126 frames in page 74 6. Modify EXT MII Pin description in page 21, 22, 23 7. "100M" change to "100 Mbps" and "10M" change to "10 Mbps". 8. Modify PHY mode for only support one MIICLK on page 25 9. Add in Thermal Data on page 85 10. Add in power consumption on page 80 11. P.54 PHY30.1[12] Default value=0, P.56 PHY30.2[7] Default value=0, P.56 PHY30.2[0] 爲 FORCE_MODE -> BI_COLOR 12. 1.8V change 1.95V
IP178C-DS-R03	1. Modify FILTER_DA, 01-80-c2-00-00-00 to 01-80-c2-00-00-02 on page 19 2. Modify VLAN_ON function when Pin 53EXTMII_EN=1 on page 18 3. Modify long packet enable function description on page 55 4. Modify Backpressure type selection on page 54 5. Modify RESETB CKT on page 14 6. Modify HASH_MODE [0] to LDPS_DIS on page 17, 54 7. Modify Pin type description on page 13 8. Modify Pin 84 from SCA_DIS to LOW_10M_DIS or SCA_DIS on page 14 9. Modify Pin 73 from LINK_Q to SEL_SCA on page 18 10. Modify Pin diagram on page 9, pin_87 from HASH_MODE [0] to LDPS_DIS,pin 84 from SCA_DIS to LOW_10M_DIS or SCA_DIS, pin_73 from LINK_Q to SEL_SCA
IP178C-DS-R04	1. Modify broadcast storm protection function on page 18, page 30, page 75 2. Add BW control value setting on page 81 3. Add BW control description on page 45 4. Rearrange Index 5. Add special_add_forward description on page 81 6. Add “The function is valid only if pin 53 EXTMII_EN is pulled low.” To pin 75, 76, 77, 78, 85, 86, 87 7. Add Note on page 1 for CPU support
IP178C-DS-R05	1. Add the order information for lead free package
IP178C-DS-R06	1. Add IP178C.RX_DV connect to MAC.RX_DV and MAC.CRS on page 27
IP178C-DS-R07	1. All ports unlink on page 84 for VCC 2. Modify VCC min form 1.85V to 1.80V on page 84 3. Modify regulator description on page 1 & 13
IP178C-DS-R08	1. Revise the pin description. 2. Modify Pin diagram of pin 85, 86, 96 and 97. 3. Modify application diagram on page 10.
IP178C-DS-R09	1. Add FXSD7 on page 26 FXSD6 on page 15 2. Add fiber application for order information on page 90 3. Add IP178CH Pin diagram on page 10
IP178C-DS-R10	1. Modify Pin diagram of pin 85, 86, 96 and 97 (IP178CH)

Revision History

Revision #	Change Description
	2. Modify Pin description on page 21 for (IP178CH) 3. Modify initial setting on page 5 for (IP178CH)
IP178Cx-DS-R11	1. Modify SCA Table on page 48 2. Replace with new SCA register table 3. Replace IP178C with **IP178C/IP178CH** 4. Modify the difference of the definition in pin 36 and 57 between IP178B and **IP178C/IP178CH** on page 5 and 6 5. Modify application blocks on page 12, 13 and 14 6. Add "**IP178CH** support two fiber " to feature list and general description on page 1
IP178Cx-DS-R12	1. Modify from "register 0" to "register 5" on page 74 2. Modify flow control description on page 32 3. Modify IPL/IPH description on page 15 4. Add 2.5V VCC_O DC description on page 86 5. Modify Bi-color LED definition on page 19 6. Replace PHY0 register 1.1 IP113A to IP178C/IP178CH & add RO/LH on page 51 7. Modify OP0 OP1 to FX enable/half on page 60 8. Add FXSDx DC on page 86 9. Modify LED Flash behavior on page 31 10. Add X1 VIL & X1 VIH on page 86 11. Add 512k bits packet buffer memory on page 1

The difference in pin definition between IP178B and IP178C/IP178CH (MII port disabled: EXTMII_EN=0)

Pin	IP178B			IP178C/IP178CH		
	Function	Configure	Type	Function	Configure	Type
36	NC		I	NC(IP178C) FXSD6(IP178CH)		IPL
52	REG_OUT		I	REG_OUT		O
53	OSCGND		--		EXTMII_EN=0	IPL
56	OSCVCC		--	RXCLK		IPH
57	GND			GND(IP178C) FXSD7(IP178CH)		
72	SPEED_LED1	DIRECT_LED	IPL	SPEED_LED1		IPL
73	SPEED_LED0			SPEED_LED0	SEL_SCA	IPL
75	FDX_LED7			FDX_LED7	X_EN	IPH
76	FDX_LED6			FDX_LED6	AGING	IPH
77	FDX_LED5			FDX_LED5	BCSTF	IPL
78	FDX_LED4			FDX_LED4	FILTER_DA	IPL
79	FDX_LED3	VLAN_ON	IPL	FDX_LED3	VLAN_ON	IPL
80		LED_SEL [1]	IPH		LED_SEL [1]	IPH
81		LED_SEL [0]	IPH		LED_SEL [0]	IPH
84		AGING	IPH	LOW_10M_DIS/ SCA_DIS		IPH
85	FDX_LED2	OP1 [1]	IPL	FDX_LED2	FX7_EN (for IP178CH only)	IPL
86	FDX_LED1	OP1 [0]	IPL	FDX_LED1	FX7_HALF (for IP178CH only)	IPL
87	FDX_LED0	HASH_MODE [0]	IPL	FDX_LED0	LDPS_DIS	IPL
90		MID_MDIX_EN	IPL		MID_MDIX_EN	IPH
95		FORCE_MODE	IPL		BI_COLOR	IPL
96	LINK_LED3	OP0 [0]	IPL	LINK_LED3	FX6_EN (for IP178CH only)	IPL
97	LINK_LED2	OP0 [1]	IPL	LINK_LED2	FX6_HALF (for IP178CH only)	IPL
101		UPDATE_R4_EN	IPH	TXCLK	LONG_PKT_DIS	IPH
102	EEDI		IPL	MDIO		IPH
103	EEDO		IPL	MDC		IPL
104	EECS		IPL	SCL		IPL
105	EESK		IPL	SDA		IPH

The difference in pin definition between IP178B and IP178C/IP178CH (MII port enabled: EXTMII_EN=1)

Pin	IP178B			IP178C/IP178CH		
	Function	Configure	Type	Function	Configure	Type
36	NC		I	NC(IP178C) FXSD6(IP178CH)		IPL
52	REG_OUT		I	REG_OUT		O
53	OSCGND		--		EXTMII_EN=1	IPL
56	OSCVCC		--	RMII_CLK_IN		IPH
57	GND			GND(IP178C) FXSD7(IP178CH)		
72	SPEED_LED1	DIRECT_LED	IPL	SPEED_LED1	RMII_ MII	IPL
73	SPEED_LED0			SPEED_LED0	SEL_SCA	IPL
75	FDX_LED7			RXDV	X_EN	IPH
76	FDX_LED6			RMII_CLK_OUT	AGING	IPH
77	FDX_LED5			RXD2	BCSTF	IPL
78	FDX_LED4			RXD1	FILTER_DA	IPL
79	FDX_LED3	VLAN_ON	IPL	RXD0	VLAN_ON	IPL
80		LED_SEL [1]	IPH	TXEN	LED_SEL [1]	IPH
81		LED_SEL [0]	IPH	TXD3	LED_SEL [0]	IPH
84		AGING	IPH		LOW_10M_DIS/ SCA_DIS	IPH
85	FDX_LED2	OP1 [1]	IPL	TXD2	(note1) (for IP178CH only)	IPL
86	FDX_LED1	OP1 [0]	IPL	TXD1	(note1) (for IP178CH only)	IPL
87	FDX_LED0	HASH_MODE [0]	IPL	TXD0	LDPS_DIS	IPL
90		MID_MDIX_EN	IPL		MID_MDIX_EN	IPH
95		FORCE_MODE	IPL		BI_COLOR	IPL
96	LINK_LED3	OP0 [0]	IPL	LINK_LED3	FX6_EN (for IP178CH only)	IPL
97	LINK_LED2	OP0 [1]	IPL	LINK_LED2	FX6_HALF (for IP178CH only)	IPL
101		UPDATE_R4_EN	IPH	TXCLK	LONG_PKT_DIS	IPH
102	EEDI		IPL	MDIO		IPH
103	EEDO		IPL	MDC		IPL
104	EECS		IPL	SCL	MII_MAC	IPL
105	EESK		IPL	SDA		IPH

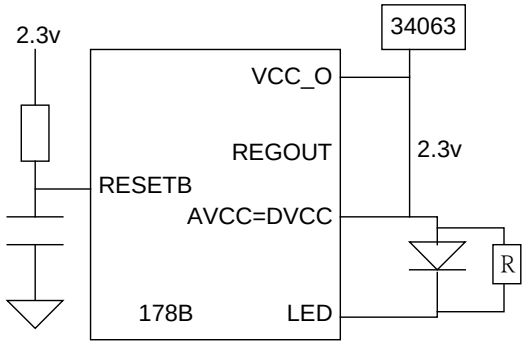
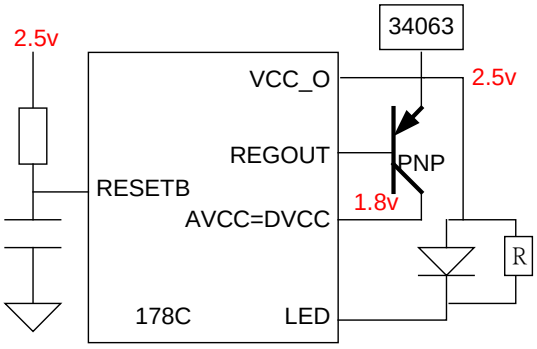
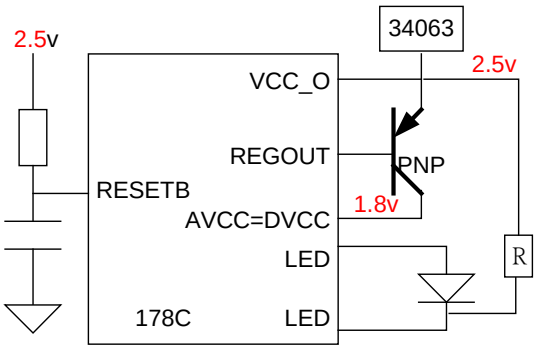
Note1: FX7_EN & FX7_HALH only can be updated by EEPORM or MDC/MDIO when EXTMII_EN = 1

Features comparison between IP178B and IP178C/IP178CH

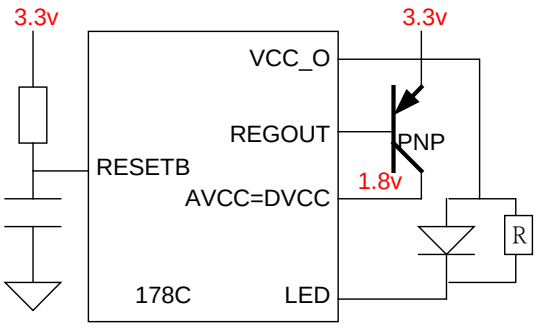
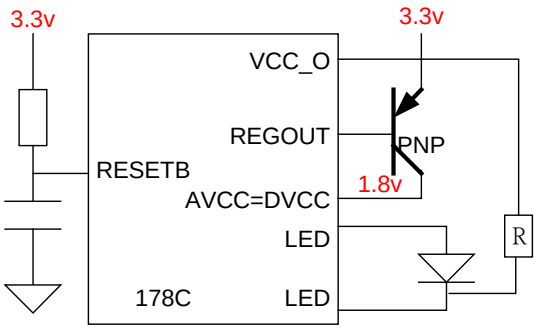
Function	IP178B	IP178C/IP178CH	
EEPROM	93C46	24C01A	
SCA (Smart Cable Analysis)	X	O	
UPDATE_R4_EN	O	X	
8 TP + 1* MII (9 port switch)	8 TP	8 TP + 1* MII (9 port switch)	
		Disable MII port (pin 53 EXTMII_EN=0)	Enable MII port (pin 53 EXTMII_EN=1)
LED pins	Link, Speed, Duplex	Link, Speed, Duplex	Link, Speed
Link quality LED	X	Pin 73	Default on (note1)
VLAN_ON	Pin 79	Pin 79	Default off (note1)
Filter reserved address option	Fixed on	Pin 78	Default off (note1)
Broadcast frame option	X	Pin 77	Default off (note1)
Aging option	Pin 84	Pin 76	Default on (note1)
Flow control option	Fixed on	Pin 75	Default on (note1)
Max packet length option	X	Pin 101	Default off (note1)
MII port speed/ duplex	X	X	Fixed 100 Mbps full
RMII/MII option	X	X	Pin 72
MII MAC mode/ PHY mode	X	X	Pin 104
MII register, MDC/MDIO	X	X	O
Built in regulator	X	2.5v → 1.95V	3.3V → 1.95V

Note1: The default value can be updated by EEPORM or MDC/MDIO.
Note2: It is UPDATE_R4_EN in IP178B.

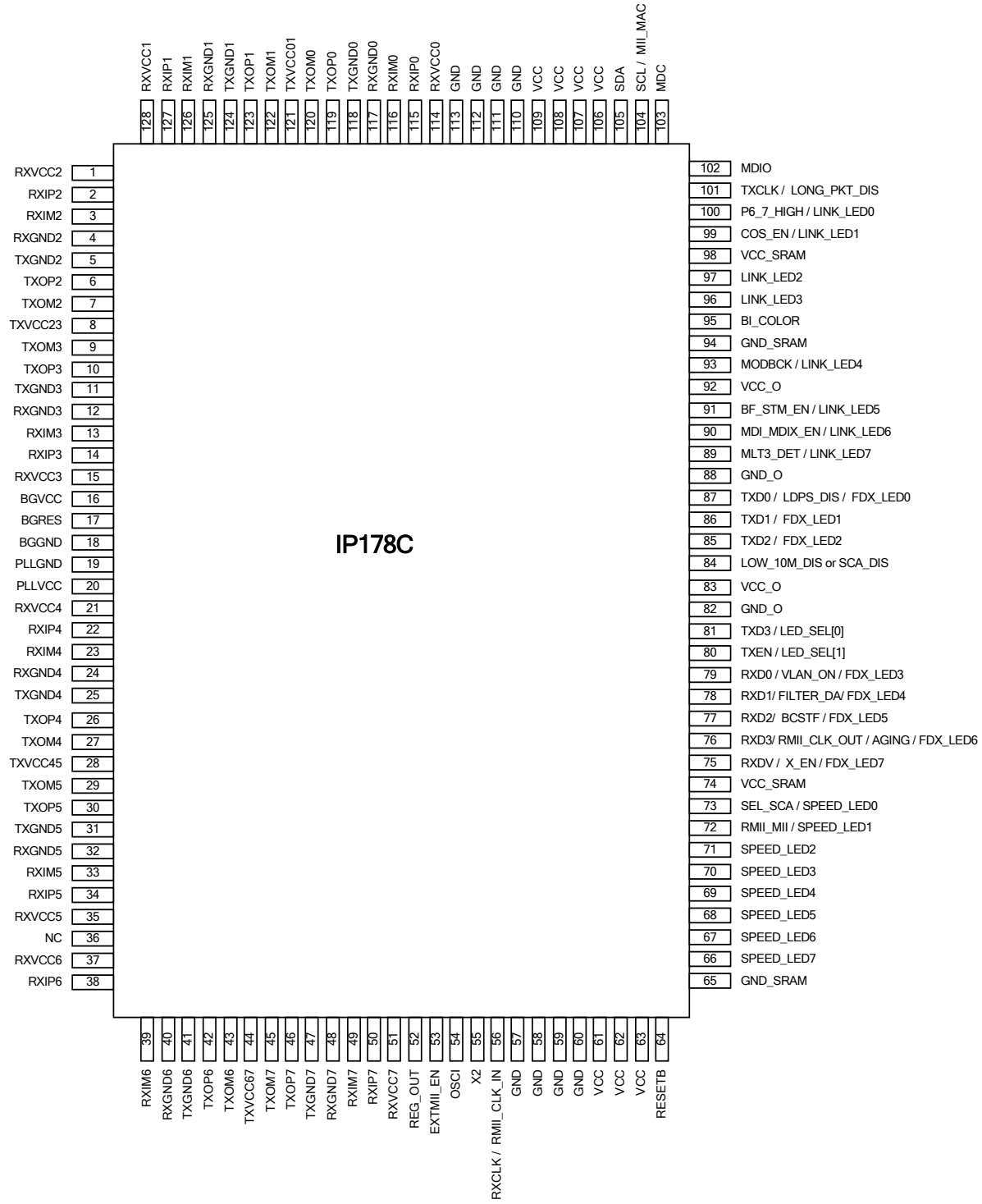
The differences in application circuit between IP178B and IP178C/IP178CH

IP178B	IP178C/IP178CH
A. Dumb switch	A. Dumb switch (EXTMII_EN=0, BI_COLOR=0)
	 Note: R is a pull up resistor for configuration. It should be connected to VCC_O.
	B. Dumb switch (EXTMII_EN=0, BI_COLOR=1)
NA	 Note: R is a pull up resistor for configuration. It should be connected to VCC_O.

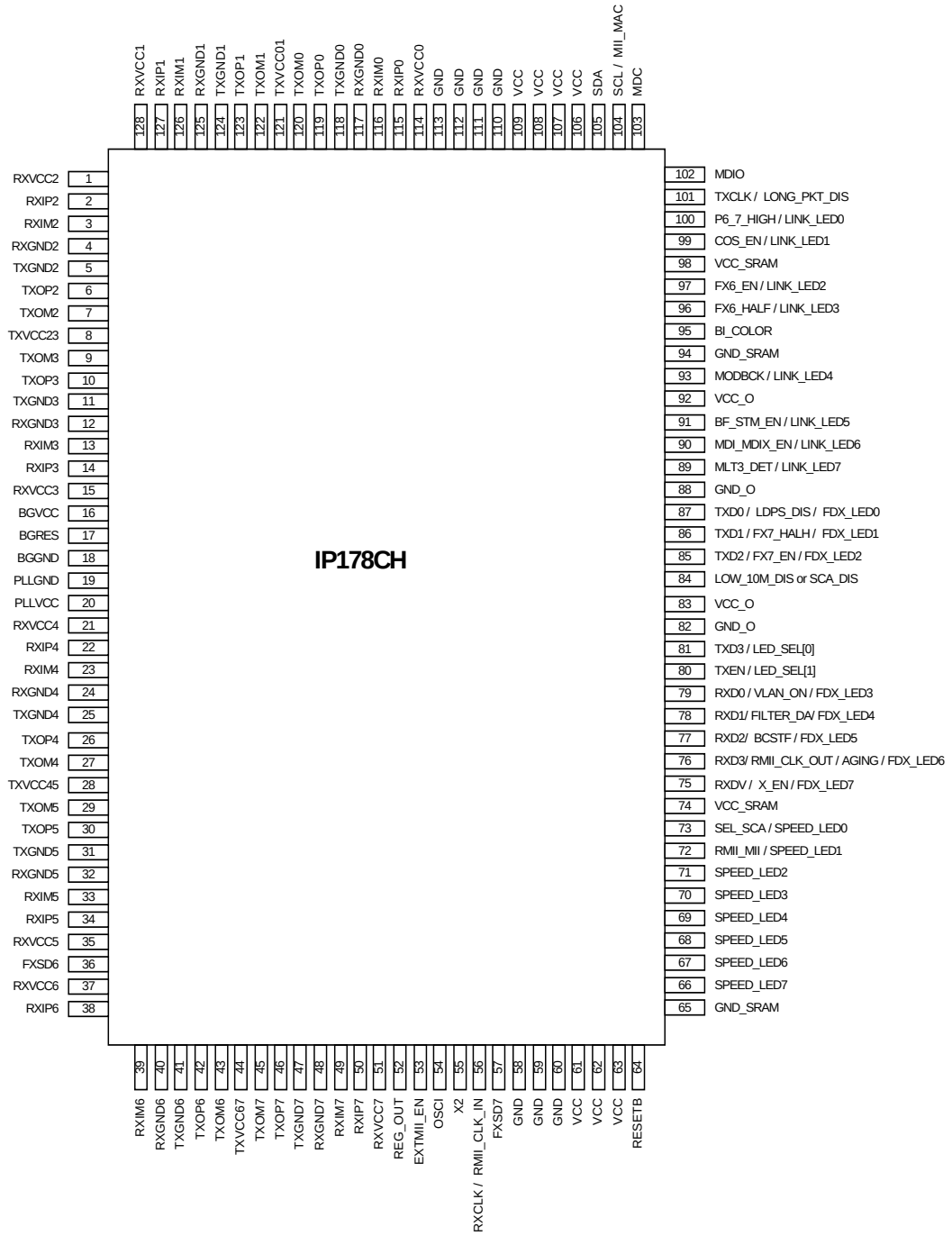
The differences in application circuit between IP178B and IP178C/IP178CH (continued)

IP178B	IP178C/IP178CH
	C. Router (EXTMII_EN=1, BI_COLOR=0)
NA	 Note: R is a pull up resistor for configuration. It should be connected to VCC_O.
	D. Router (EXTMII_EN=1, BI_COLOR=1)
NA	 Note: R is a pull up resistor for configuration. It should be connected to VCC_O.

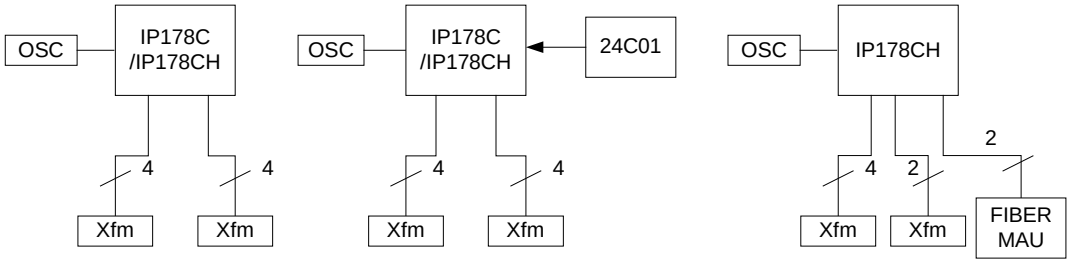
Pin diagram (IP178C)



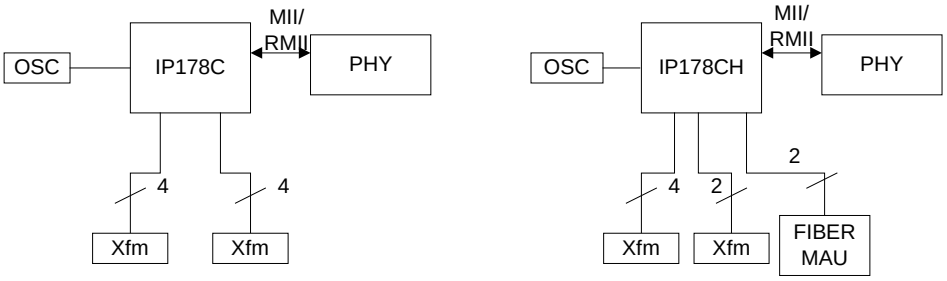
Pin diagram (IP178CH)



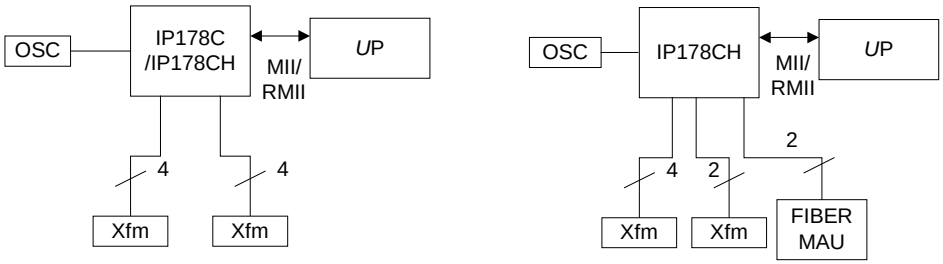
An 8-port switch



A 9-port switch



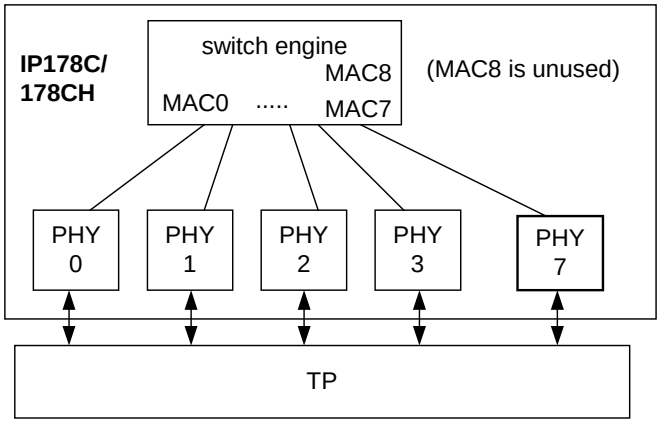
An 8-port router



IP178C/IP178CH applications: (continued)

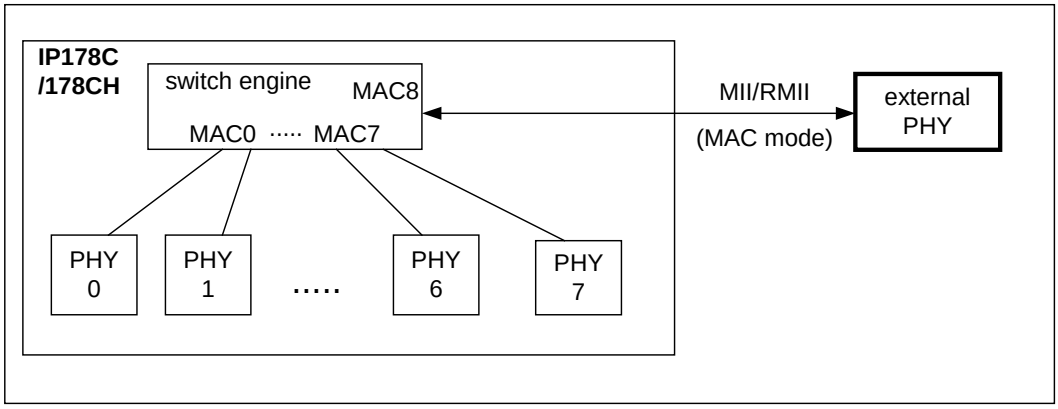
An 8-port switch application

If pin 53 EXTMII_EN is pulled low, then MII/ RMII interface is disabled. **IP178C/IP178CH** is not connected to a CPU and works as an 8-port switch. The ninth switch port MAC8 is unused in this application.



A 9-port switch application

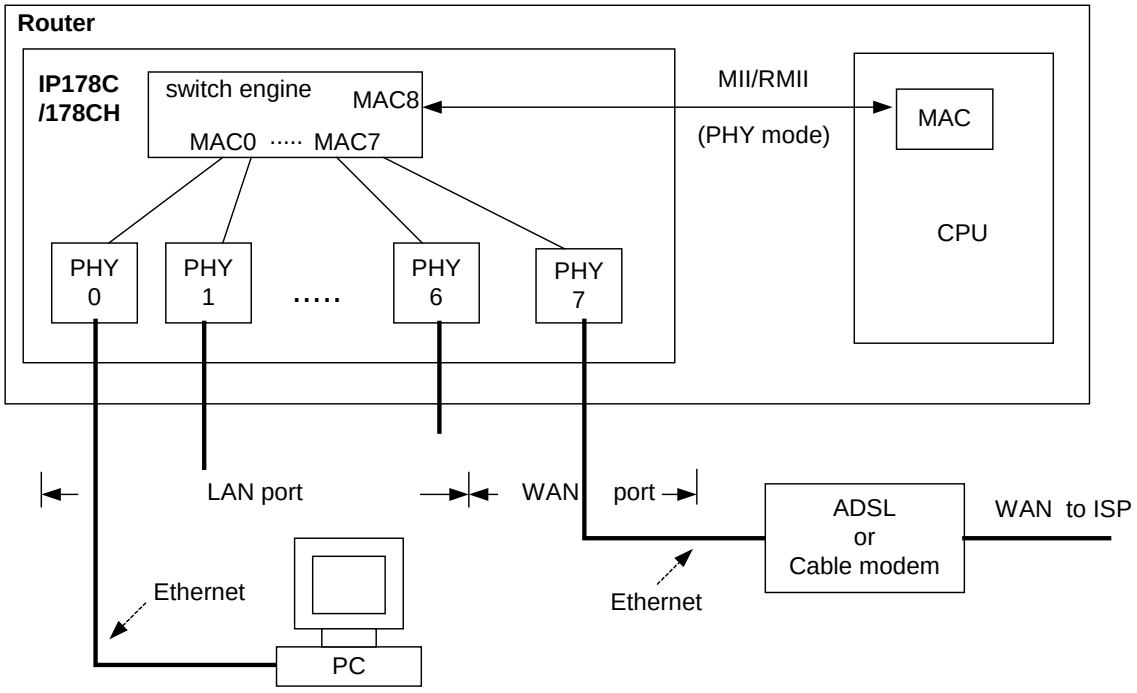
If pin 53 EXTMII_EN is pulled high, then MII/ RMII interface is enabled. The ninth switch port MAC8 is connected to a PHY through the MII/RMII interface. **IP178C/IP178CH** works as a 9-port switch. Because **IP178C/IP178CH** doesn't access the MII register of the external PHY through SMI, MII/RMII interface should be MAC mode and full duplex in this application.



IP178C/IP178CH applications: (continued)

An 8-port router application

IF pin 53 EXTMII_EN is pulled high, then MII/RMII interface is enabled. **IP178C/IP178CH** is connected to a CPU through MII/ RMII interface. **IP178C/IP178CH** works as an 8-port router. MII/RMII interface is set to be PHY mode and 100 Mbps full duplex in this application.



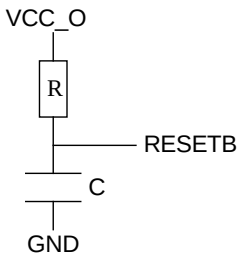
1 Pin description

Type	Description
I	Input pin
O	Output pin
IPL	Input pin with internal pull low 50M ohm
IPH	Input pin with internal pull high 50M ohm

Type	Description
IPL1	Input pin with internal pull low 22.8k ohm
IPH1	Input pin with internal pull high 22.8k ohm
IPL2	Input pin with internal pull low 92.6k ohm
IPH2	Input pin with internal pull high 113.8k ohm

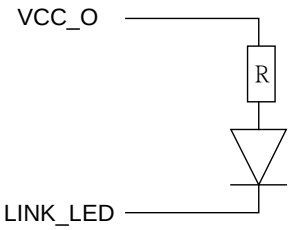
Pin No.	Label	Type	Description
Analog			
52	REG_OUT	O	Regulator output voltage The internal regulator uses pin83/pin92 VCC_O as reference voltage to control external transistor to generate a voltage source between 1.80v ~ 2.05v.. If pin 53 EXTMII_EN is pulled high, then pin83/pin92 VCC_O should be connected to 3.3v to generate 1.80v ~ 2.05v voltage source. If pin 53 EXTMII_EN is pulled low, then pin83/pin92 VCC_O should be connected to 2.5v to generate 1.80v ~ 2.05v voltage source.
17	BGRES	I	Band gap resister It is connected to GND through a 6.19k (1%) resistor in application circuit.
115, 116, 127, 126, 2, 3, 14, 13, 22, 23, 34, 33, 38, 39, 50, 49	RXIP0~7 RXIM0~7	I	TP receive
119, 120, 123, 122, 6, 7, 10, 9, 26, 27, 30, 29, 42, 43, 46, 45	TXOP0~7 TXOM0~7	O	TP transmit

Pin description (continued)

Pin No.	Label	Type	Description
Misc.			
36	NC (FXSD6)		(for IP178CH only)
54	OSCI	I	25Mhz system clock It is recommended to connect OSCI and X2 to a 25M crystal. If the clock source is from another chip or oscillator, the clock should be active at least for 1ms before pin 64 RESETB de-asserted. Pin 55 X2 should be left open in this application.
55	X2	O	Crystal pin A 25Mhz crystal can be connected to OSCI and X2.
64	RESETB	I	Reset It is low active. It must be hold for more than 1ms. It is Schmitt trigger input. If a R/C reset circuit is used, the capacitor should be connected to VCC_O as shown in the figure. 
84	LOW_10M_DIS Or SCA_DIS	IPH2	LOW_10M_DIS or SCA_DIS If pin 73 SEL_SCA is pull low, then pin 84 is LOW_10M_DIS. If pin 73 SEL_SCA is pull high, then pin 84 is SCA_DIS. For LOW_10M_DIS 1: disable power saving mode, the 10M transmit amplitude is depressed in this mode. (default) 0: enable power saving mode For SCA_DIS 1: Disable smart cable analysis function (default). 0: Enable smart cable analysis function.
EEPROM			
104	SCL	IPL2 /O	Clock of EEPROM After reset, it is used as clock pin SCL of EEPROM. After reading EEPROM, this pin becomes an input pin. Its period is longer than 10us. **IP178C/IP178CH** stops reading the rest data in EEPROM if the first two bytes in EEPROM aren't 55AA.

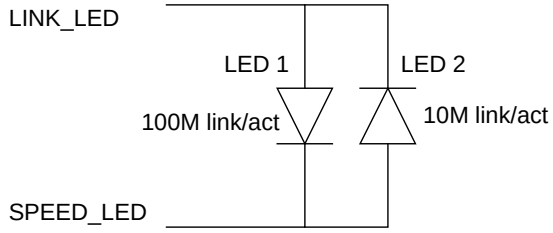
105	SDA	IPH2 /O	Data of EEPROM After reset, it is used as data pin SDA of EEPROM. After reading EEPROM, this pin becomes an input pin.

Pin description (continued)

Pin no.	Label	Type	Description
LED.			
89, 90, 91, 93, 96, 97, 99, 100	LINK_LED [7:0]	O	LINK LED The detail functions are illustrated in the following table. It should be connected to VCC_O through a LED and a resistor. Application circuit 
66, 67, 68, 69, 70, 71, 72, 73	SPEED_LED [7:0]	O	SPEED LED The detail functions are illustrated in the following table. It should be connected to VCC_O through a LED and a resistor.
75, 76, 77, 78, 79, 85, 86, 87	FDX_LED [7:0]	O	FDX LED The detail functions are illustrated in the following table. It should be connected to VCC_O through a LED and a resistor. The function is valid only if pin 53 EXTMII_EN is pulled low.
80, 81	LED_SEL [1:0]	IPH2	LED function selection The data on these pins are latched at the end of reset to select LED modes. The default value is mode 3. The detail functions are illustrated in the following table. After reset, these two pins becomes MII interface TXEN and TXD3 if pin 53 EXTMII_EN is pulled high.

LED_SEL [1:0]	LED mode	LINK_LED [7:0]	SPEED_LED [7:0]	FDX_LED [7:0]
00	Mode 0	Off: link fail On: 10 Mbps link ok Flash: Tx/Rx	Off: link fail On: 100 Mbps link ok Flash: Tx/Rx	Off: half duplex On: full duplex
01	Mode 1	Off: link fail On: link ok Flash: Rx	Off: 10 Mbps On: 100 Mbps	Off: half duplex On: full duplex Flash: collision
10	Mode 2	Off: link fail On: 10 Mbps link ok Flash: Tx/Rx	Off: link fail On: 100 Mbps link ok Flash: Tx/Rx	Off: half duplex On: full duplex Flash: collision
11 (default)	Mode 3	Off: link fail On: link ok Flash: Tx/Rx	Off: 10 Mbps On: 100 Mbps	Off: half duplex On: full duplex Flash: collision

Pin description (continued)

Pin no.	Label	Type	Description
LED.			
95	BI_COLOR	IPL2	Bi-color LED mode enable 1: Bi-color mode LED enabled. LED_LINK [7:0] and LED_SPEED [7:0] are used to drive dual color LED. The functions are defined in the following table. The behavior of FDX_LED [7:0] is the same as that in mode3 on the previous page. 0: Bi-color mode LED disabled. Please refer to pin description of LED_SEL [1:0] for LED functions. This pin takes precedence of LED_SEL [1:0]. Application circuit 

Bi-color LED definition

Status	LINK_LED [7:0]	SPEED_LED [7:0]	LED 1	LED 2
Link off	1	1	Off	Off
100 Mbps link ok	1	0	On	Off
100 Mbps link ok/ activity	1	Clock	Flash	Off
10 Mbps link ok	0	1	Off	On
10 Mbps link ok/ activity	Clock	1	Off	Flash

Pin description (continued)

Pin no.	Label	Type	Description
Basic operation parameter setting of switch			
87	LDPS_DIS	IPL1	Disable link down power saving mode 0: enable link down power saving mode (default) 1: disable link down power saving mode LDPS_DIS is full duplex LED of port 0 after reset. The function is valid only if pin 53 EXTMII_EN is pulled low.
89	MLT3_DET	IPL1	Ability for detecting MLT3 (for 10 Mbps switch to 100 Mbps) 0: disable MLT3 detection ability (default) 1: enable MLT3 detection ability MLT3_DET is link LED of port 7 after reset.
91	BF_STM_EN	IPL1	Broadcast storm enable 1: enable, 0: disable (default) A port begins to drop packets if it receives broadcast packets more than the threshold defined in MII register 31.9[15:14] bq_stm_thr_sel [1:0] or EEPROM register 83[7:6].
93	MODBCK	IPH1 / O	Aggressive back off enable **IP178C/IP178CH** adopts modified (aggressive) back off algorithm if this function is enabled. The maximum back off period is limited to 8-slot time. It makes **IP178C/IP178CH** have higher transmission priority in a collision event. 1: aggressive mode enable (default), 0: standard back off It is link LED of port 4 after reset.
76	AGING	IPH1	Aging enable 1: enable 300s aging timer (default) 0: disable aging function The function is valid only if pin 53 EXTMII_EN is pulled low.
73	SEL_SCA	IPL1	Select SCA function Function selection for PIN_84 0: PIN_84 is LOW_10M_DIS (default) 1: PIN_84 is SCA_DIS
75	X_EN	IPH1 /O	Flow control enable 1: enable IEEE802.3x & back pressure (default), 0: disable IEEE802.3x & back pressure The function is valid only if pin 53 EXTMII_EN is pulled low.

Pin description (continued)

<table>
<tr><th>Pin no.</th><th>Label</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="4">Advance operation parameter setting of switch engine</td></tr>
<tr><td>100</td><td>P6_7_HIGH</td><td>IPL1
/O</td><td>Port6 port7 are set to be high priority port

Packets received from port6 or port7 are handled as high priority packets if the function is enabled.
1: enable,
0: disabled (default)

It is an input signal during reset and its value is latched at the end of reset. It acts as a link LED of port 0 after reset.</td></tr>
<tr><td>99</td><td>COS_EN</td><td>IPL1
/O</td><td>Class of service enable

Packets with high priority tag are handled as high priority packets if the function is enabled.
1: enable,
0: disabled (default)

It is an input signal during reset and its value is latched at the end of reset. It acts as a link LED of port 1 after reset.</td></tr>
<tr><td>79</td><td>VLAN_ON</td><td>IPL1
/O</td><td>Turn on VLAN

Enable a specific configuration of port base VLAN.

0: disabled (default),
1: enable

IP178C/IP178CH are separated into 7 VLANs if this function is enabled and MII port is disabled.

The VLAN group is as follows.
<table>
<tr><td></td><td>Pin 53 EXTMII_EN=0</td><td>Pin 53EXTMII_EN=1</td></tr>
<tr><td>VLAN 1</td><td>port 0, port 7</td><td>port 0~7 & MII port</td></tr>
<tr><td>VLAN 2</td><td>port 1, port 7</td><td>port 0~7 & MII port</td></tr>
<tr><td>VLAN 3</td><td>port 2, port 7</td><td>port 0~7 & MII port</td></tr>
<tr><td>VLAN 4</td><td>port 3, port 7</td><td>port 0~7 & MII port</td></tr>
<tr><td>VLAN 5</td><td>port 4, port 7</td><td>port 0~7 & MII port</td></tr>
<tr><td>VLAN 6</td><td>port 5, port 7</td><td>port 0~7 & MII port</td></tr>
<tr><td>VLAN 7</td><td>port 6, port 7</td><td>port 0~7 & MII port</td></tr>
<tr><td>VLAN 8</td><td>NA</td><td>port 0~7 & MII port</td></tr>
</table>
It is an input signal during reset and its value is latched at the end of reset. It acts as a full duplex LED of port 3 after reset.

The configuration can be updated by programming EEPROM register. Please refer to EEPROM register 66~78 for detail information.</td></tr>
</table>

Pin description (continued)

Pin no.	Label	Type	Description
Advance operation parameter setting of switch engine			
77	BCSTF	IPL1	Broadcast frame option 1: Packets with DA equal to FFFFFFFF are handled as broadcast frame in broadcast protection function, 0: Packets with DA equal to FFFFFFFF or multi-cast frames are handled as broadcast frame in broadcast protection function. The function is valid only if pin 53 EXTMII_EN is pulled low. Programming MII register 31.30.12 will overwrite the setting.
78	FILTER_DA	IPL1	Reserved address forward option Filter packets with specific DA from 01-80-c2-00-00-02 to 01-80-c2-00-00-0f. Packets with specific DA equal to 01-80-c2-00-00-01 are always filtered regardless the setting of this pin. 1: filter, 0: forward (default) The function is valid only if pin 53 EXTMII_EN is pulled low.
101	LONG_PKT_DIS	IPH2	Max packet size option 1: Drop packets with length longer than 1536 bytes 0: Drop packets with length longer than 1552 bytes
TP/ Fiber setting			
90	MDI_MDIX_EN	IPH1 /O	MDI/MDI-X enable MDI/MDI-X auto cross over 1: enable (default), 0:disable It is an input signal during reset and its value is latched at the end of reset to set auto MDI/MDIX function. It is link LED of port 6 after reset.
85	FX7_EN	IPL1	Port 7 mode selection (for IP178CH only) 1: port7 is a fiber port, 0: port7 is a TP port The function is valid only if pin 53 EXTMII_EN is pulled low.
86	FX7_HALF	IPL1	Port7 fiber port half duplex (for IP178CH only) 1: port7 is half duplex, 0: port7 is full duplex It is valid only if pin 85 FX7_EN is pulled high. The function is valid only if pin 53 EXTMII_EN is pulled low.

97	FX6_EN	IPL1	Port 6 mode selection (for IP178CH only) 1: port6 is a fiber port, 0: port6 is a TP port
96	FX6_HALF	IPL1	Port6 fiber port half duplex (for IP178CH only) 1: port6 is half duplex, 0: port6 is full duplex It is valid only if pin 97 FX6_EN is pulled high.

Pin description (continued)

Pin no.	Label	Type	Description
MII configuration pins			
53	EXTMII_EN	IPL2	MII port enable 1: enable MII port, 0: disable MII port This pin53 also determines the regulator output voltage. Please see pin 52 REG_OUT for detail information.
104	MII_MAC	IPL2 /O	MII mode selection It is latched as MII MAC/ PHY mode selection at the end of reset. It should be pull high if pin 72 RMII_MII is pulled high. 1: MAC mode, 0: PHY mode After reset, it is used as clock pin SCL of EEPROM
72	RMII_MII	IPL1 /O	MII RMII selection It is latched as RMII_MII selection at the end of reset. It is valid only if pin 53 EXTMII_EN is pulled high. Pin 104 MII_MAC should be pull high RMII is enabled. 1: RMII, 0:MII After reset, it is used as SPPED_LED1.
SMI			
103, 102	MDC, MDIO	IPL2 , IPH2 /O	SMI The external MAC device uses the interface to access the registers of **IP178C/IP178CH**. **IP178C/IP178CH** doesn't access the MII registers of external PHY.

Pin description (continued)

Pin no.	Label	Type	Description
MII interface/ PHY mode (Pin 53 EXTMII_EN =1, pin104 MII_MAC=0 and Pin72 RMII_MII =0)			
101	MIICLK	IPL2/ O	MII transmit & receive clock It is an output signal when MII works at PHY mode. It should be connected to MII TXCLK & RXCLK of an external MAC device.
87,86,85 ,81	TXD0~TXD3	IPL1 IPL1 IPL1 IPH2	MII transmit data They are input signals when MII works at PHY mode. They are sampled at the rising edge of MIICLK. They should be connected to MII TXD of an external MAC device.
80	TXEN	IPH2	MII transmit enable It is an input signal when MII works at PHY mode. It is used to frame TXD [3:0]. It is sampled at the rising edge of MIICLK. It should be connected to MII TXEN of an external MAC device.
75	RXDV	IPH1/ O	MII receive data valid It is an output signal when MII works at PHY mode. It is used to frame RXD [3:0]. It is sent out at the falling edge of MIICLK. It should be connected to MII RXDV of an external MAC device.
79, 78, 77, 76	RXD0~RXD4	IPL1/ O, IPL1/ O, IPL1/ O, IPH1/ O	MII receive data They are output signals when MII works at PHY mode. They are sent out at the falling edge of MIICLK. They should be connected to MII RXD of an external MAC device.
56	NC	IPH2	This pin should be left open

Pin description (continued)

Pin no.	Label	Type	Description
MII interface/ MAC mode (Pin 53 EXTMII_EN =1, pin104 MII_MAC=1 and Pin72 RMII_MII =0)			
101	TXCLK	IPL2	MII transmit clock It is an input signal when MII works at MAC mode. It should be connected to MII RXCLK of an external PHY.
87,86,85,81	TXD0~TXD3	IPL1 IPL1 IPL1 IPH2	MII transmit data They are input signals when MII works at MAC mode. They are sampled at the rising edge of TXCLK. They should be connected to MII RXD of an external PHY.
80	TXEN	IPH2	MII transmit enable It is an input signal when MII works at MAC mode. It is used to frame TXD [3:0]. It is sampled at the rising edge of TXCLK. It should be connected to MII RXDV of an external PHY.
75	RXDV	IPH1/O	MII receive data valid It is an output signal when MII works at MAC mode. It is used to frame RXD [3:0]. It is sent out at the falling edge of RXCLK. It should be connected to MII TXEN of an external PHY.
79, 78, 77, 76	RXD0~RXD4	IPL1/O, IPL1/O, IPL1/O, IPH1/O	MII receive data They are output signals when MII works at MAC mode. They are sent out at the falling edge of RXCLK. They should be connected to MII TXD of an external PHY.
56	RXCLK	IPH2	MII receive clock It is an input signal when MII works at MAC mode. It should be connected to MII TXCLK of an external PHY. This pin should be left open when MII/RMII is disabled.

Pin description (continued)

Pin no.	Label	Type	Description
RMII interface (Pin 53 EXTMII_EN =1, pin104 MII_MAC=0 and Pin72 RMII_MII =1)			
76	RMII_CLK_OUT	O	RMII reference clock source
56	RMII_CLK_IN	IPH2	RMII reference clock input
87,86	TXD0, TXD1	IPL1	RMII transmit data It is sampled at the rising edge of RMII_CLK_IN.
80	TXEN	IPH2	RMII transmit enable It is used to frame TXD [1:0]. It is sampled at the rising edge of RMII_CLK_IN.
75	RXDV	IPH1/ O	RMII receive data valid It is used to frame RXD [1:0]. It is sent out at the rising edge of RMII_CLK_IN.
79, 78	RXD0, RXD1	IPL1/ O	RMII receive data It is sent out at the rising edge of RMII_CLK_IN.

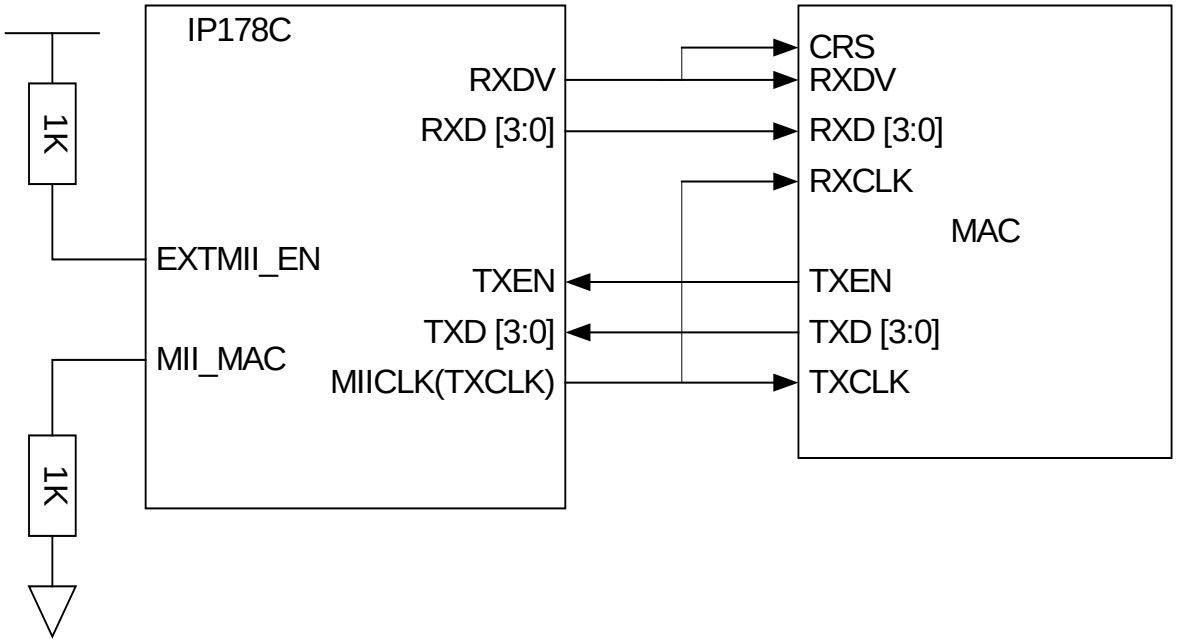
Pin description (continued)

Pin no.	Label	Type	Description
Power			
16	BGVCC	I	Power of band gap circuit
18	BGGND	I	Power of band gap circuit
19	PLLGND	I	Ground of PLL circuit
20	PLLVCC	I	Power of PLL circuit
59, 60, 110, 111, 112, 113,	GND	I	Ground of internal logic
57	GND (FXSD7)		(for IP178CH only)
58	GND		
61, 62, 63, 106, 107, 108, 109,	VCC	I	Power of internal logic
65, 94,	GND_SRAM	I	Ground of internal SRAM
74, 98,	VCC_SRAM	I	Power of internal SRAM
82, 88,	GND_O	I	Ground for LED, MII and EEPROM
83, 92,	VCC_O	I	Power for LED, MII and EEPROM
114, 128, 1, 15, 21, 35, 37, 51	RXVCC0~7	I	Power of analog receive block
117, 125, 4, 12, 24, 32, 40, 48,	RXGND0~7	I	Ground of analog receive block
118, 124, 5, 11, 25, 31, 41, 47,	TXGND0~7	I	Ground of analog transmit buffer
121, 8, 28, 44,	TXVCC01 TXVCC23 TXVCC45 TXVCC67	I	Power of analog transmit buffer

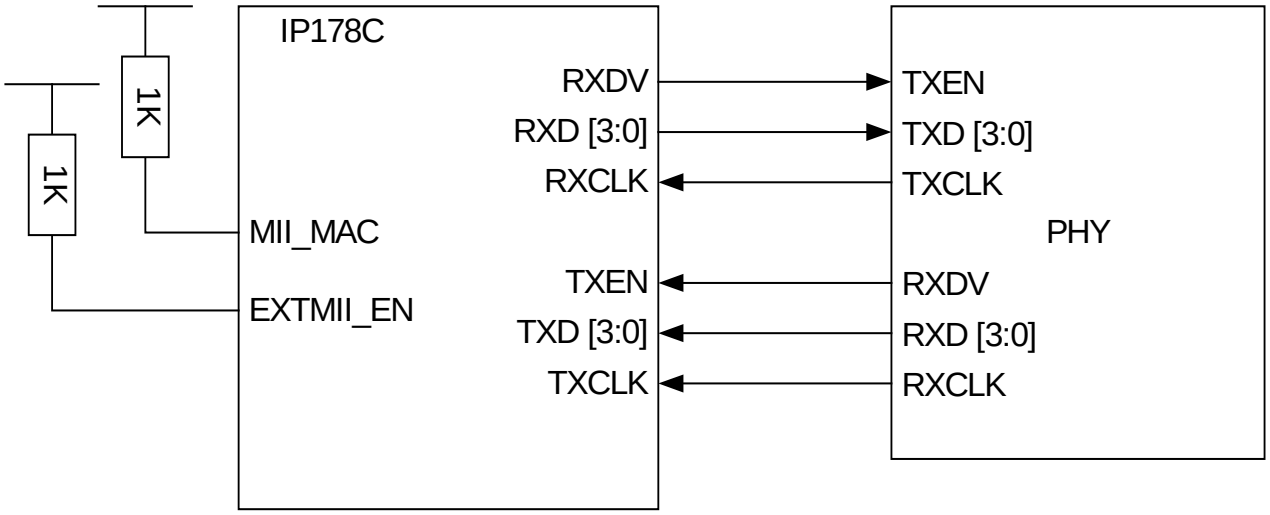
2 Functional Description

100 Mbps full MII (RMII) port (pin EXTMII_EN=1)

MII PHY mode (MII_MAC=0)

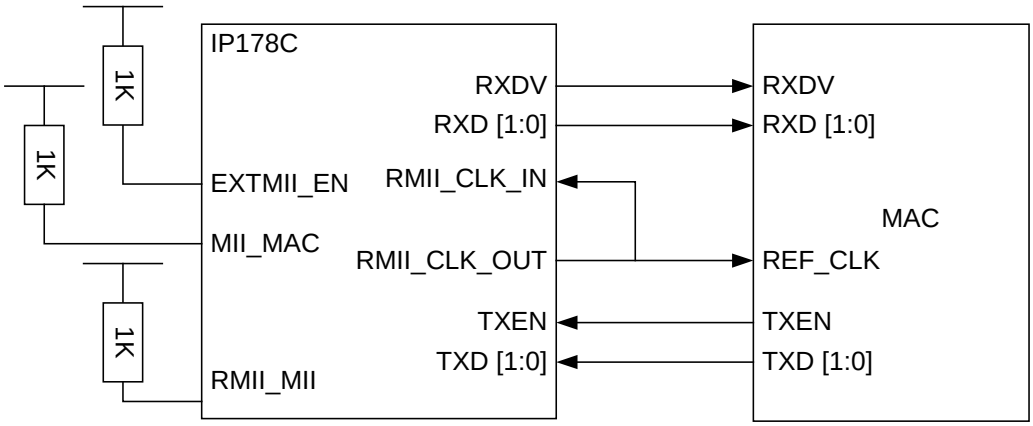


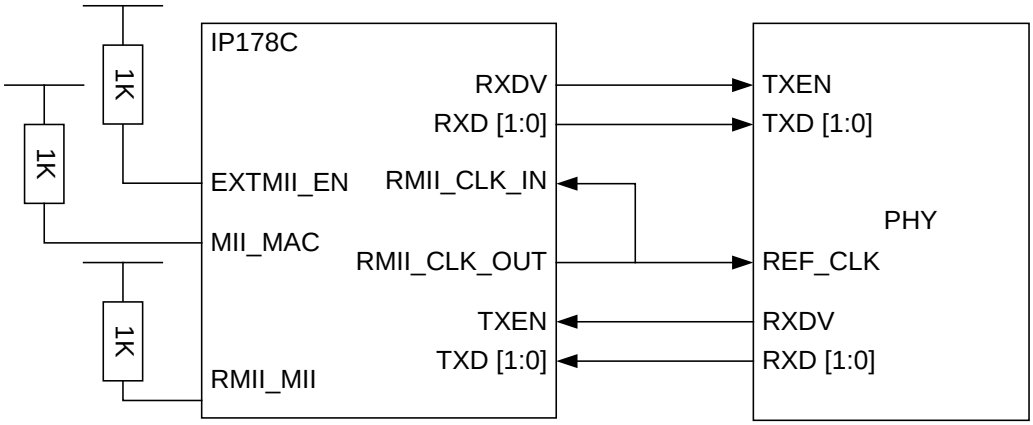
MII MAC mode (MII_MAC=1)



RMII mode (EXTMII_EN=1, RMII_MII=1, MII_MAC=1)

MII_MAC should be pulled high in spite of IP178C connecting to a MAC or a PHY.





LED display (normal operation)

Normal operation			
LED_O_SEL	LinK_LED	SPEED_LED	FDX_LED
00	Off: link fail On: 10 Mbps link ok Flash: Tx/Rx	Off: link fail On: 100 Mbps link ok Flash: Tx/Rx	Off: half duplex On: full duplex
01	Off: link fail On: link ok Flash: Rx	Off: 10 Mbps On: 100 Mbps	Off: half duplex On: full duplex Flash: collision
10	Off: link fail On: 10 Mbps link ok Flash: Tx/Rx	Off: link fail On: 100 Mbps link ok Flash: Tx/Rx	Off: half duplex On: full duplex Flash: collision
11	Off: link fail On: link ok Flash: Tx/Rx	Off: 10 Mbps On: 100 Mbps	Off: half duplex On: full duplex Flash: collision
Flash behavior: On 44ms → Off 176ms → On 44ms → …			
When link quality is poor			
LED_O_SEL	LinK_LED	SPEED_LED	FDX_LED
Don't care	Flash		
Flash behavior: Off 2s → On 2s →Off 2s → …			
SCA	See SCA paragraph for detail information		

2.1 Flow control

IP178C/IP178CH jams or pauses a port, which causes output queue over the threshold. Its link partner will defer transmission after detecting the jam or pause frame. A port of **IP178C/IP178CH** defers transmission when it receives a jam or a pause frame.

IP178C/IP178CH issues pause control frame (Pause On, time slot count = 0xffff) to remote station when the output queue of the destination port is higher than high water mark threshold. When the output queue of the destination port is lower than low water mark threshold, **IP178C/IP178CH** issues pause control frame (Pause Off, time slot count = 0) to restart transmition. Besides, **IP178C/IP178CH** provides an additional protect function, when it issues continuous 16 times of Pause ON frame (network abnormal), no more Pause ON frame will be send.

When CoS is enabled, **IP178C/IP178CH** may disable the flow control function for a short term to guarantee the bandwidth of high priority packets. A port disables its flow control function for 2 ~ 3 seconds when it receives a high priority packet. It doesn't transmit pause frame or jam pattern during the period but it still responses to pause frame or jam pattern.

The flow control function can be enabled by pulling up pin 75 X_EN or by programming MII register 30.1.10.

2.2 Broadcast storm protection

A port of **IP178C/IP178CH** begins to drops broadcast packets if the received broadcast packets are more than the threshold defined in MII register 31.9[15:14] or EEPROM register 83[7:6] bq_stm_thr_sel [1:0] in 10ms (100Mbps) or 100ms (10Mbps)

The function can be enabled by pulling high pin 91 BF_STM_EN or programming MII register 30.1.[6].

IP178C/IP178CH handles multicast frame as a broadcast frame in broadcast storm protection function if pin 77 BCSTF is pulled low.

2.3 Port locking

IP178C/IP178CH supports port locking. Each port can be configured individually by programming MII register 30.31[8:0] or EEPROM 63[0] and 62[7:0]. User has to reset **IP178C/IP178CH** by writing 16'h55AA to MII register 30.0 after enabling this function. **IP178C/IP178CH** locks first MAC address if the function is enabled. Any packet with MAC address not equal to the locked one will be dropped.

User has to turn off aging function when using the port locking function. Aging function can be disabled by pulling low pin 76 AGING or programming register 30.1[3:2].

2.4 Port base VLAN

IP178C/IP178CH supports port base VLAN functions. It separates **IP178C/IP178CH** into some groups (VLAN). A port is limited to communicate with other ports within the same group when the function is enabled. Frames will be limited in a VLAN group and will not be forwarded out of this VLAN group. A port can be assigned to one or more VLAN groups. The members (ports) of a VLAN group are assigned by programming EEPROM register 64[7:0]~81[7:0], or MII register 31.0[8:0]~31.8[8:0].

The VLAN function can be active even if there is no EEPROM. **IP178C/IP178CH** supports an easy way to enable a sub set VLAN function without programming registers. A default configuration of VLAN is adopted if pin 79 VLAN_ON is pulled high. The VLAN duration is shown in the following table. The setting in register takes precedence of the setting on pins.

VLAN_ON	EXTMII_EN	Configuration
0	X	Function disabled
1	0	VLAN groups: (P0, P7), (P1, P7), (P2, P7), (P3, P7), (P4, P7), (P5, P7), (P6, P7)
1	1	VLAN groups: (P0, MII), (P1, MII), (P2, MII), (P3, MII), (P4, MII), (P5, MII), (P6, MII), (P7, MII)

Note: P0 means port 0. P7 means port7. MII means MII port.

2.5 Tag VLAN/ Tag and un-tag function

Tag and un-tag function

IP178C/IP178CH inserts or removes a tag of a frame if tagging/ un-tagging function is enabled. The operation is illustrated as follows. The tag information is defined in MII register 30.3~30.11 and EEPROM register 6~22.

Frame type of the received packet	The operation of a port which forwards the packet	
	Forward to a untagged filed	**Forward to a tagged field**
Untagged	Forward the packet without modification	Insert a tag using the default VLAN tag value of the source port Calculate new CRC The default VLAN tag value is defined in the MII register 30.3~30.11.
Priority-tagged (VLAN ID=0)	Strip tag Calculate new CRC	Keep priority field. Replace the tag with the default VLAN tag value of the source port Calculate new CRC The default VLAN tag value is defined in the MII register 30.3~30.11.
VLAN-tagged	Strip tag Calculate new CRC	Forward the packet without modification

2.6 Tag VLAN

If tag VLAN function is enabled (MII register 30.13[3] TAG_VLAN_EN is logic high), **IP178C/IP178CH** forwards a packet according to MAC address table and one of the sixteen VLAN output port masks, defined in MII register 30.14~30.29. One of the sixteen VLAN output mask is selected by VID index, which is four bits selected from VID field in a tag. VID index is defined in MII register 30.13[2:0] VID_SEL. For example, VLAN output port mask 1 is selected if VID index selected by VID_SEL is equal to 1.

IP178C/IP178CH handles an un-tagged packet using the default VLAN tag value of its source port. A packet with VID equal to 12'b0 will be handled as un-tag frame.

2.7 Tag VLAN in router application

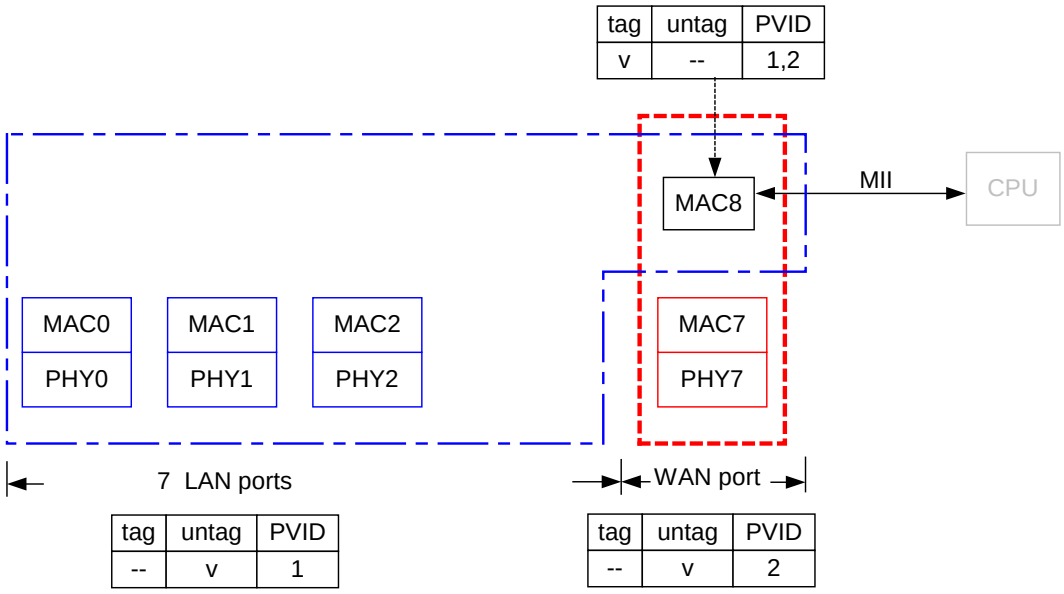
In a router application, MII port is defined as a tagged port and the other ports are defined as un-tagged ports. **IP178C/IP178CH** inserts VLAN tag into packets according to its source port when it forwards the packets to MII port. The pre-defined VLAN tag value is defined in register 30.3~11. CPU can identify the source port of a packet from MII by examining the VLAN tag.

CPU inserts VLAN tag into packets when it sends packets to MII port. **IP178C/IP178CH** forwards a packet from MII to the appropriate port according to the MAC address and VLAN tag. **IP178C/IP178CH** removes the VLAN tag when it forwards the packet.

2.8 Smart MAC

IP178C/IP178CH supports SMART MAC function to solve locked Card's ID issue. The following system configuration and operation illustrate the behavior of **IP178C/IP178CH** SMART MAC function. The SMART MAC setting is defined in MII register 30[11:0].

System configuration



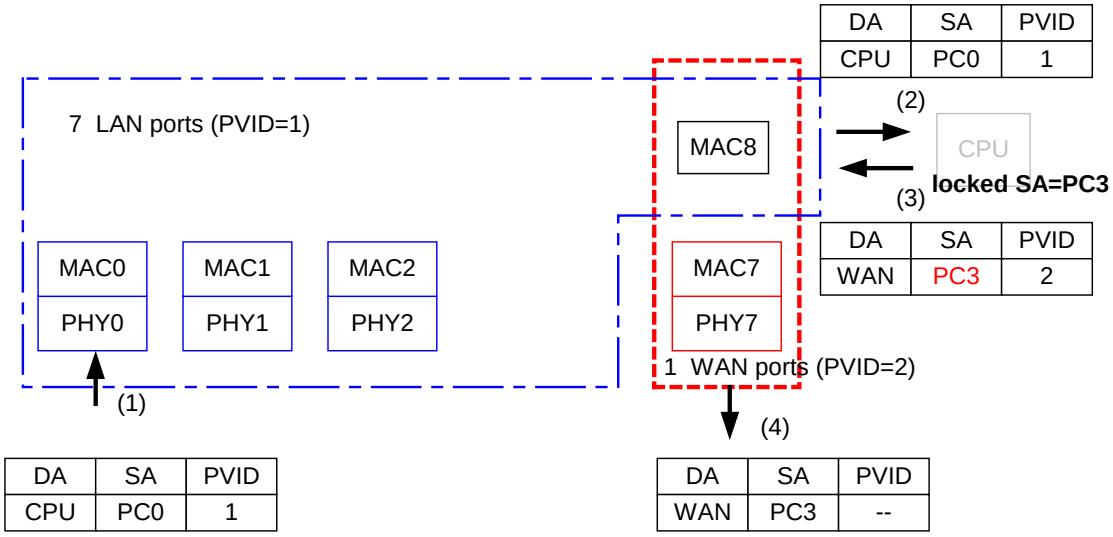
A programming example of SMART MAC

Register	Content	Description
Tag/ un-tag function setup		
30.13[12]	0	MII0 doesn't strip the tag of an outgoing packet.
30.12[8]	1	MII0 adds a tag to an outgoing packet.
30.13[11:4]	111_1111	Port0~7 strip the tag of an outgoing packet.
30.12[7:0]	000_0000	Port0~7 doesn't add a tag to an outgoing packet.
PVID function setup		
30.3~30.9	16'h0001	Define PVID of port0~port6
30.10	16'h0002	Define PVID of port7
30.11	16'h0002	Define PVID of MII0
VLAN Mask function setup		
30.14[8:0]	9'h1ff	TAG_VLAN_MASK_1
30.15[8:0]	9'h17f	TAG_VLAN_MASK_2
SMART MAC function setup		
30.30[10:8]	001	Define 1 LAN group
30.30[11]	1	Enable router function
30.13[2:0]	000	Define VID index as 000
30.13[3]	1	Enable tag VLAN
30.30[7:0]	100_0000	Define port 7 as a WAN port

Operation

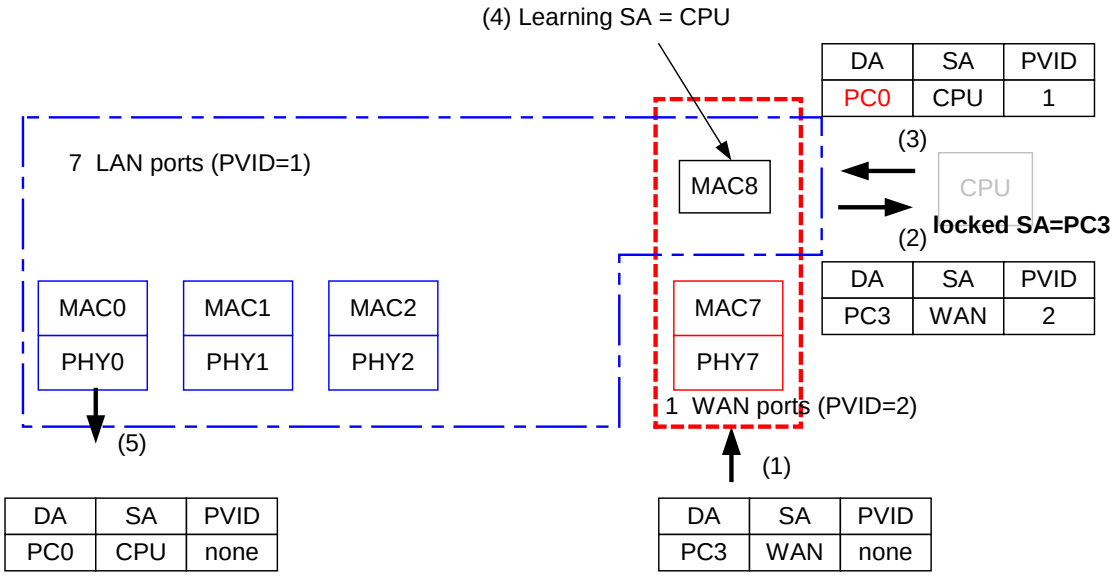
1. Packet from LAN to WAN

1.1. PC0 sends a packet to a LAN port with SA equal to PC0 and PVID equal to 1.
1.2. **IP178C/IP178CH** forwards the packet to CPU with PVID equal to 1.
1.3. CPU replaces the SA with locked address PC3, replaces PVID with 2 and sends it to **IP178C/IP178CH**.
1.4. **IP178C/IP178CH** forwards the packet to port7 (WAN port).



2. Packet from WAN to LAN

2.1. WAN port receives a packet with locked address PC3.
2.2. **IP178C/IP178CH** adds a PVID equal to 2 and forwards the packet to CPU.
2.3. CPU updates the DA, replaces PVID with 1 and sends it to **IP178C/IP178CH**.
2.4. **IP178C/IP178CH** learns the SA.
2.5. **IP178C/IP178CH** forwards the packet to port0 according to the DA.



2.9 CoS

IP178C/IP178CH supports two type of CoS. One is port base priority function and the other is frame base priority function. **IP178C/IP178CH** supports two levels of priority queues. A high priority packet will be queued to the high priority queue to share more bandwidth. The ratio of bandwidth of high priority and low priority queue is defined in MII register 30.1[15] or EEPROM 3[7].

2.9.1 Port base priority

The packets received from high priority port will be handled as high priority frames if the port base priority is enabled. It is enabled by programming the corresponding bit in MII register 31.0[9]~31.8[9] or EEPROM register 65[1] ~81[1]. Each port of **IP178C/IP178CH** can be configured as a high priority port individually.

2.9.2 Frame base priority

VLAN tag and TCP/IP TOS

IP178C/IP178CH examines the specific bits of VLAN tag and TCP/IP TOS for priority frames if the frame base priority is enabled. The packets will be handled as high priority frames if the tag value meets the high priority requirement, that is, VLAN tag bigger than 3 or TCP/IP TOS field not equal to 3'b000. It is enabled by programming the corresponding bit in MII register 31.0[10]~31.8[10] or EEPROM register 65[2]~81[2]. The frame base priority function of each port can be enabled individually.

IP178C/IP178CH supports an easy way to enable a sub set of CoS function without programming EEPROM or MII registers. Port 6 and port 7 can be set as high priority ports if pin 100 P6_7_HIGH is pulled high. Frame base priority function of all ports is enabled if pin 99 COS_EN is pulled high. The setting in register takes precedence of the setting on pins.

VLAN field

	TYPE = 8100	TCI (tag control information)
byte	12~13	14~15

TCI definition:

Bit[15:13]: User Priority 7~0
Bit 12: Canonical Format Indicator (CFI)
Bit[11~0]: VLAN ID.
IP178C uses bit[15:13] to define priority.

TOS field

	TYPE = 0800	IP HEADER
byte	12~13	14~15

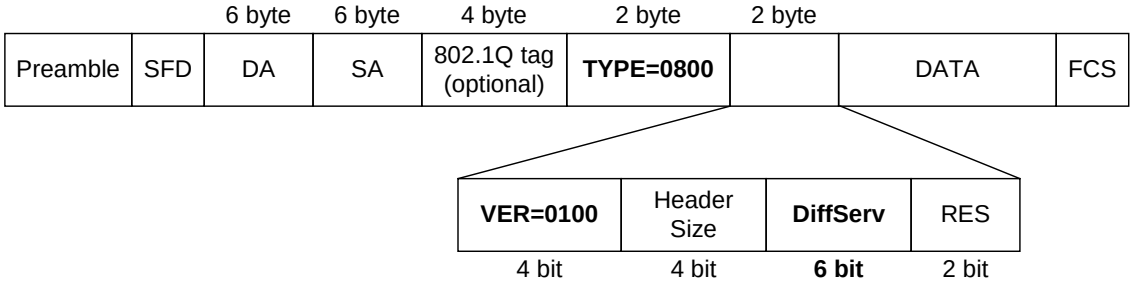
IP header definition:
Byte 14
Bit[7:0]: IP protocol version number & header length.

Byte 15: Service type
Bit[7~5]: IP Priority (Precedence) from 7~0
Bit 4: No Delay (D)
Bit 3: High Throughput
Bit 2: High Reliability (R)
Bit[1:0]: Reserved
IP178C uses bit[4:2] to define priority.

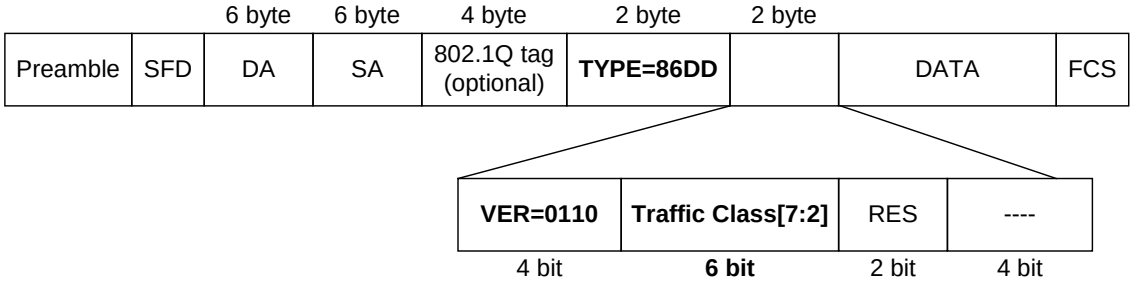
IPv4/IPv6 DiffServ

IP178C/IP178CH checks the DiffServ field of a IPv4 frame or Traffic class field [7:2] (TC[7:2]) of a IPv6 frame and uses them to decide the frame's priority if MII register 31.30.[13] DIFFSERV_EN is enabled. **IP178C/IP178CH** uses DiffServ or TC [7:2] as index to select one of 64 bits defined in the MII register 31.22~25 DSCP[63:0]. If the bit is "1", the received frame is handled as a high priority frame.

IPv4 frame format



IPv6 frame format



2.10 Spanning tree

IP178C/IP178CH supports spanning tree function with the following features:
1. Detect BPDU frames by examining multicast address (01-80-c2-00-00-00).
2. Forward BPDU packets to CPU through MII and add special tag for source port information.
Forward BPDU packets from CPU according to the special tag in a frame.
Please refer to section “Tag VLAN / Tag and un-tag function”.

Port states

To support spanning tree protocol, each port of **IP178C/IP178CH** provides five port states shown in the following table. Port 0~7 of **IP178C/IP178CH** can be configured in one of the five spanning tree states individually by programming MII register 31.13 to enable (disable) forwarding and learning function. Port 8 (MII) is dedicated for CPU.

State	Fwd BPDU packet to CPU	Fwd BPDU packet from CPU	Address learning	Fwd all packet normally	(Forward enable, Learning enable)
Disable	X (note 2)	X (note 2)	X	X	(0,0)
Blocking	O	X (note 3)	X	X	(0,0)
Listening	O	O	X	X	(0,0)
Learning	O	O	O	X	(0,1)
Forwarding	O	O	O	O	(1,1)

Note1: O: enabled, X: disabled
Note2: CPU should not send packets to **IP178C/IP178CH** and should discard packets from **IP178C/IP178CH**.
Note3: CPU should not send packets to **IP178C/IP178CH**.

Special tag

IP178C/IP178CH supports special tag function to exchange switching information with CPU without involving VLAN tag information. The special tag function is enabled by programming MII register 31.30[14] STAG_EN.

From CPU to switch

When special tag function is enabled, **IP178C/IP178CH** forwards packets from MII (CPU) by checking special tag added by CPU. The tag definition is shown in the following table. **IP178C/IP178CH** will remove the special tag 81XX and re-calculate CRC when it forwards the packet to a un-tag field. **IP178C/IP178CH** will update the special tag to 81XX and re-calculate CRC when it forwards the packet to a tag field.

Preamble	SFD	DA	SA	81XX(special tag)	Data	CRC

Special tag 81XX		
bit [15:12]	bit[11:8]	bit[7:0]
8	1	0000_0001: instruct 178C forwards the packet to port 0 0000_0010: instruct 178C forwards the packet to port 1 0000_0100: instruct 178C forwards the packet to port 2 0000_1000: instruct 178C forwards the packet to port 3 0001_0000: instruct 178C forwards the packet to port 4 0010_0000: instruct 178C forwards the packet to port 5 0100_0000: instruct 178C forwards the packet to port 6 1000_0000: instruct 178C forwards the packet to port 7

From switch to CPU

When special tag function is enabled, **IP178C/IP178CH** sends packets to MII (CPU) with source port information by adding special tag to the frame. **IP178C/IP178CH** will add the special tag 81XX and re-calculate CRC when it receives the packet from a un-tag field. **IP178C/IP178CH** will update the tag 8100 to 81XX and re-calculate CRC when it receives the packet from a tag field. The tag definition is shown in the following table.

Bit[15:12]	**bit[11:8]**	**bit[7:0]**
8	1	0000 0001: the source port of the packet is port 0 0000 0010: the source port of the packet is port 1 0000 0100: the source port of the packet is port 2 0000 1000: the source port of the packet is port 3 0001 0000: the source port of the packet is port 4 0010 0000: the source port of the packet is port 5 0100 0000: the source port of the packet is port 6 1000 0000: the source port of the packet is port 7

2.11 Static MAC address table

User can setup the static MAC address table to force the switching behavior of **IP178C/IP178CH** by programming MII register 31.14 ~ 30.21. When **IP178C/IP178CH** receives packets, which match pre-defined MAC address in the table (static_mac_0, static_mac_1), it forwards the packet to MII port (CPU). The static MAC address table has precedence over the dynamic DA look up result.

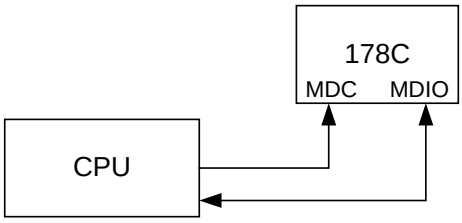
In a spanning tree application, the MII register 31.17[10] static_override_0 is "1", MII register 31.17[9] static_valid_0 is "1", the MII register 31.14~31.16 MAC address field is 01-80-c2-00-00-00 and the MII register 31.17[8:0] static_port_mask_0 is 9'b1_0000_0000 (MII). That is, **IP178C/IP178CH** only forwards BPDU to MII (CPU) and in spite of the port states.

MII register	R/W	Description	Default
31.17.10	R/W	override_0 1: override the transmission, receiving and learning setting in MII register 31.13. 0: not override	1
31.17.9	R/W	state_valid_0 1: the entry is valid 0: the entry is not valid	0
31.17[8:0]	R/W	state_port_mask_0 Bit 8: forward to port 8 (MII) Bit 7: forward to port 7 Bit 6: forward to port 6 Bit 5: forward to port 5 Bit 4: forward to port 4 Bit 3: forward to port 3 Bit 2: forward to port 2 Bit 1: forward to port 1 Bit 0: forward to port 0	9'b1_0000_0000
31.14 – 16	R/W	state_mac_0	01-80-C2-00-00-00

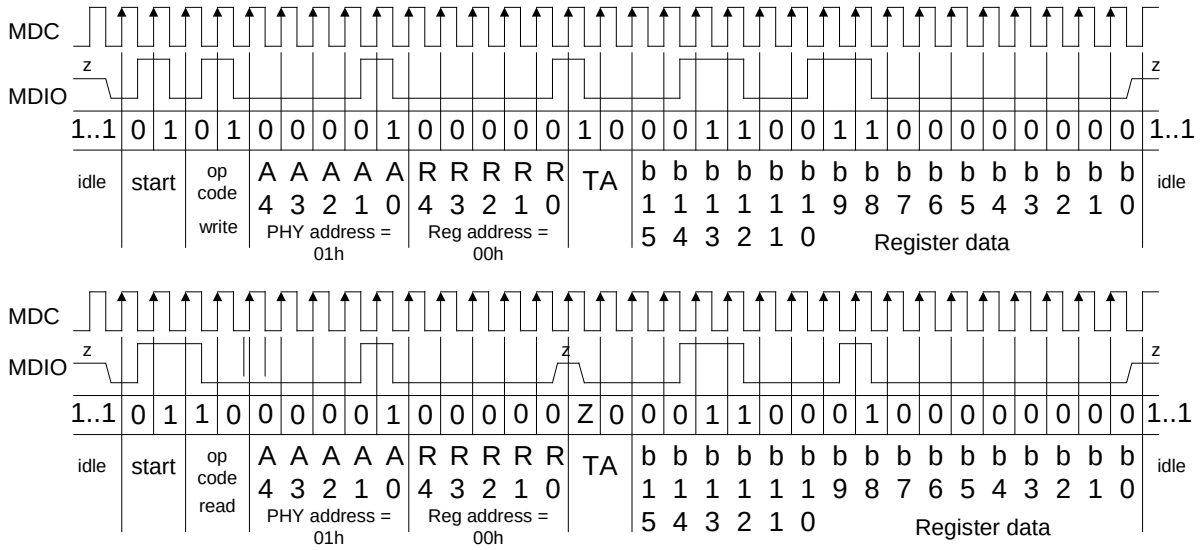
2.12 Serial management interface

User can access **IP178C/IP178CH**'s MII registers through serial management interface with pin MDC and MDIO. Its format is shown in the following table. To access MII register in **IP178C/IP178CH**, MDC should be at least one more cycle than MDIO. That is, a complete command consists of 32 bits MDIO data and at least 33 MDC clocks. When the SMI is idle, MDIO is in high impedance.

Syatem diagram



Frame format	**<Idle><start><op code><PHY address><Registers address><turnaround><data><idle>**
Read Operation	<Idle><01><10><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><Z0> <b_{15} b_{14} b_{13} b_{12} b_{11} b_{10} b_9 b_8 b_7 b_6 b_5 b_4 b_3 b_2 b_1b_0><Idle>
Write Operation	<Idle><01><01><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><10> <b_{15} b_{14} b_{13} b_{12} b_{11} b_{10} b_9 b_8 b_7 b_6 b_5 b_4 b_3 b_2 b_1b_0><Idle>



2.13 SCA

IP178C/IP178CH performs SCA on each port and shows the test result on LED pins whenever pin SCA is pulled high. The LED display is independent of LED_SEL pins. The following table shows the LED behavior of a port performing SCA.

	LinK_LED	SPEED_LED	FDX_LED
SCA initiation (under testing)	Scan port by port	Scan port by port	Scan port by port
	Running Horse LED: On 286ms -> Off 2s -> On 286ms -> Off 2s		
Test fail	On-Off-On-Off	On-Off-On-Off	Off
An open cable with length shorter than 50m open	Off	On	Off
An open cable with length between 50m and 100m	On	Off	Off
An open cable with length between 100m and 150m	On	On	Off
An shorted cable with length shorter than 50m	Off	Flash	Off
An shorted cable with length between 50m and 100m	Flash	Off	Off
An shorted cable with length between 100m and 150m	Flash	Flash	Off
Cable is normal	Off	Off	Off

2.14 Bandwidth control

IP178C/IP178CH provides the bandwidth control mechanism to manage or control the data rate on a limited bandwidth network. By controlling the ingress data rate and the egress data rate, it provides a bandwidth management solution for local area networks and also provides quick and easy allocation of uplink or downlink speeds to meet and guarantee a wide range of customer bandwidth requirements.
IP178C/IP178CH provides the easiest way to allocate bandwidth for each port, which defined in MII registers 31.26 ~ 31.29 or EEPROM registers 116 ~ 123. The ingress/egress data rate control range is from 128 kbps to 8 Mbps for each port.

2.15 Register descriptions

R/W = Read/Write, SC = Self-Clearing, RO = Read Only, LL = Latching Low, LH = Latching High

Basic MII registers of port 0

PHY	MII	ROM	R/W	Description	Default
MII control register (address 00)					
0	0.15	--		Reset	0
0	0.14	--	R/W	Loop back 1 = Loop back mode 0 = normal operation When this bit set, **IP178C/IP178CH** will be isolated from the network media, that is, the assertion of TXEN at the MII will not transmit data on the network. All MII transmission data will be returned to MII receive data path in response to the assertion of TXEN.	0
0	0.13	--	RW	Speed Selection 1 = 100 Mbpsbps 0 = 10 Mbpsbps It is valid only if bit 0.12 is set to be 0.	1
0	0.12	--	RW	Auto-Negotiation Enable 1 = Auto-Negotiation Enable 0 = Auto-Negotiation Disable	1
0	0.11	--	R/W	Power Down	0
0	0.10	--		Isolate	0
0	0.9	--	RW SC	Restart Auto- Negotiation 1 = re-starting Auto-Negotiation 0 = Auto-Negotiation re-start complete Setting this bit to logic high will cause **IP178C/IP178CH** to restart an Auto-Negotiation cycle, but depending on the value of bit 0.12 (Auto-Negotiation Enable). If bit 0.12 is cleared then this bit has no effect, and it is Read Only. This bit is self-clearing after Auto-Negotiation process is completed.	0
0	0.8	--	R/W	Duplex mode 1 = full duplex 0 = half duplex It is valid only if bit 0.12 is set to be 0.	0
0	0.7	--	R/W	Collision test	0
0	0[6:0]	--	R/W	Write as 0, ignore on read	-

PHY	MII	ROM	R/W	Description	Default
MII status register (address 01)					
0	1.15	--	RO	100Base-T4 capable 1 = 100Base-T4 capable 0 = not 100Base-T4 capable **IP178C/IP178CH** does not support 100Base-T4. This bit is fixed to be 0.	0
0	1.14	--	RO	100Base-X full duplex Capable 1 = 100Base-X full duplex capable 0 = not 100Base-X full duplex capable The default of this bit will change depend on the external setting of **IP178C/IP178CH**. If external pin setting without 100Base-X full duplex support, then this bit will change default to logic 0.	1
0	1.13	--	RO	100Base-X half duplex Capable 1 = 100Base-X half duplex capable 0 = not 100Base-X half duplex capable The default of this bit will change depend on the external setting of **IP178C/IP178CH**. If external pin setting without 100Base-X half duplex support, then this bit will change default to logic 0	1
0	1.12	--	RO	10Base-T full duplex Capable 1 = 10Base-T full duplex capable 0 = not 10Base-T full duplex capable The default of this bit will change depend on the external setting of **IP178C/IP178CH**. If external pin setting without 100Base-T full duplex support, then this bit will change default to logic 0	1
0	1.11	--	RO	10Base-T half duplex Capable 1 = 10Base-T half duplex capable 0 = not 10Base-T half duplex capable The default of this bit will change depend on the external setting of **IP178C/IP178CH**. If external pin setting without 100Base-X full duplex support, then this bit will change default to logic 0	1
0	1[10:7]	--	RO	Reserved Ignore on read	-
0	1.6	--	RO	MF preamble Suppression 1 = preamble may be suppressed 0 = preamble always required	1
0	1.5	--	RO	Auto-Negotiation Complete 1 = Auto-Negotiation complete 0 = Auto-Negotiation in progress When read as logic 1, indicates that the Auto-Negotiation process has been completed, and the contents of register 4 and 5 are valid. When read as logic 0, indicates that the Auto-Negotiation process has not been completed, and the contents of register 4 and 5 are meaningless. If Auto-Negotiation is disabled (bit 0.12 set to logic 0), then this bit will always read as logic 0.	0

PHY	MII	ROM	R/W	Description	Default
MII status register (address 01)					
0	1.4	--	RO LH	Remote fault 1 = remote fault detected 0 = not remote fault detected When read as logic 1, indicates that **IP178C/IP178CH** has detected a remote fault condition. This bit is set until remote fault condition gone and before reading the contents of the register. This bit is cleared after **IP178C/IP178CH** reset.	0
0	1.3	--	RO	Auto-Negotiation Ability 1 = Auto-Negotiation capable 0 = not Auto-Negotiation capable When read as logic 1, indicates that **IP178C/IP178CH** has the ability to perform Auto-Negotiation. The value of this bit will depend on the external mode setting of **IP178C/IP178CH** operation mode.	1
0	1.2	--	RO LL	Link Status 1 = Link Pass 0 = Link Fail When read as logic 1, indicates that **IP178C/IP178CH** has determined a valid link has been established. When read as logic 0, indicates the link is not valid. This bit is cleared until a valid link has been established and before reading the contents of this registers.	0
0	1.1	--	RO LH	Jabber Detect 1 = jabber condition detected 0 = no jabber condition detected When read as logic 1, indicates that **IP178C/IP178CH** has detected a jabber condition. This bit is always 0 for 100 Mbps operation and is cleared after **IP178C/IP178CH** reset. This bit is set until jabber condition is cleared and reading the contents of the register.	0
0	1.0	--	RO	Extended capability 1 = Extended register capabilities 0 = No extended register capabilities **IP178C/IP178CH** has extended register capabilities.	1

PHY	MII	ROM	R/W	Description	Default
PHY Identifier (address 02)					
0	2	--	RO	**IP178C/IP178CH** OUI (Organizationally Unique Identifier) ID, the msb is 3rd bit of **IP178C/IP178CH** OUI ID, and the lsb is 18th bit of **IP178C/IP178CH** OUI ID. **IP178C/IP178CH** OUI is 0090C3.	0243h

PHY	MII	ROM	R/W	Description	Default
PHY Identifier (address 03)					
0	3[15:10]	--	RO	PHY identifier **IP178C/IP178CH** OUI ID, the msb is 19th bit of **IP178C/IP178CH** OUI ID, and lsb is 24th bit of **IP178C/IP178CH** OUI ID.	3h
0	3[9:4]	--	RO	Manufacture's Model Number **IP178C/IP178CH** model number	18h
0	3[3:0]	--	RO	Revision Number **IP178C/IP178CH** revision number	0

PHY	MII	ROM	R/W	Description	Default
Auto-Negotiation Advertisement register (address 04)					
0	4.15	--		Next Page Not supported	0
0	4.14	--	RW	Reserved by IEEE, write as 0, ignore on read	0
0	4.13	--	R/W	Remote Fault Not supported	0
0	4[12:11]	--	RO	Reserved for future IEEE use, write as 0, ignore on read	0
0	4.10	--	RW	Pause 1 = Advertises that this device has implemented pause function 0 = No pause function supported	0
0	4.9	--	RW	100BASE-T4 Not supported	0
0	4.8	--	R/W	100BASE-TX full duplex 1 = 100BASE-TX full duplex is supported 0 = 100BASE-TX full duplex is not supported	1
0	4.7	--	R/W	100BASE-TX 1 = 100BASE-TX is supported 0 = 100BASE-TX is not supported	1
0	4.6	--	R/W	10BASE-T full duplex 1 = 10BASE-T full duplex is supported 0 = 10BASE-T full duplex is not supported	1
0	4.5	--	R/W	10BASE-T 1 = 10BASE-T is supported 0 = 10BASE-T is not supported	1
0	4[4:0]	--	R/W	Selector Field Use to identify the type of message being sent by Auto-Negotiation.	00001

PHY	MII	ROM	R/W	Description	Default
Link partner ability register (address 05) Base Page					
0	5.15		RO	Next Page 1 = Next Page ability is supported by link partner 0 = Next Page ability does not supported by link partner	0
0	5.14		RO	Acknowledge 1 = Link partner has received the ability data word 0 = Not acknowledge	0
0	5.13		RO	Remote Fault 1 = Link partner indicates a remote fault 0 = No remote fault indicate by link partner If this bit is set to logic 1, then bit 1.4 (Remote fault) will set to logic 1.	0
0	5[12:11]	--	RO	Reserved by IEEE for future use, write as 0, read as 0.	0
0	5.10	--	RO	Pause 1 = Link partner support IEEE802.3x 0 = Link partner does not support IEEE802.3x **IP178C/IP178CH** will reload the default value after rest or link failure.	1
0	5.9	--	RO	100BASE-T4 1 = Link partner support 100BASE-T4 0 = Link partner does not support 100BASE-T4	0
0	5.8	--	RO	100BASE-TX full duplex 1 = Link partner support 100BASE-TX full duplex 0 = Link partner does not support 100BASE-TX full duplex	0
0	5.7	--	RO	100BASE-TX 1 = Link partner support 100BASE-TX 0 = Link partner does not support 100BASE-TX	0
0	5.6	--	RO	10BASE-T full duplex 1 = Link partner support 10BASE-T full duplex 0 = Link partner does not support 10BASE-T full duplex	0
0	5.5	--	RO	10BASE-T 1 = Link partner support 10BASE-T 0 = Link partner does not support 10BASE-T	0
0	5[4:0]	--	RO	Selector Field Protocol selector of the link partner	00000

PHY	MII	ROM	R/W	Description	Default
During SCA_mode, the SCA result for each port will be stored at MII_reg_05: Auto-Negotiation Link Partner Base Page Ability. SCA setting register					
0	5[15:14]	--	RO	SCA_line_state These two bits indicate the cable status measured by SCA operation. 3: test fail (not complete) 2: line okay 1: line open 0: line short	
	5[13:8]	--	RO	SCA_peak_val These bits indicate the absolute value and the maximum value of peak amplitude measured by SCA operation.	
	5[7:2]	--	RO	SCA_peak_pos[7:2]These bits indicate the position of peak amplitude measured by SCA operation. When cable status is open or short, the failure position is approximated as (SCA_peak_pos[7:2] * 4) meters. Ex: SCA_peak_pos[7:2] = 6'b011001, the failure position is 25*4 = 100 meters	
	5[1:0]		RO	SCA_txsel These two bits indicate the TX phase of SCA operation.	

Basic MII registers of port 1-7

PHY	MII	ROM	R/W	Description	Default
Port 1 MII register 0~5					
1	0~5	--		Please refer to MII registers 0.0~0.5.	

PHY	MII	ROM	R/W	Description	Default
Port 2 MII register 0~5					
2	0~5	--		Please refer to MII registers 0.0~0.5.	

PHY	MII	ROM	R/W	Description	Default
Port 3 MII register 0~5					
3	0~5	--		Please refer to MII registers 0.0~0.5.	

PHY	MII	ROM	R/W	Description	Default
Port 4 MII register 0~5					
4	0~5	--		Please refer to MII registers 0.0~0.5.	

PHY	MII	ROM	R/W	Description	Default
Port 5 MII register 0~5					
5	0~5	--		Please refer to MII registers 0.0~0.5.	

PHY	MII	ROM	R/W	Description	Default
Port 6 MII register 0~5					
6	0~5	--		Please refer to MII registers 0.0~0.5.	

PHY	MII	ROM	R/W	Description	Default
Port 7 MII register 0~5					
7	0~5	--		Please refer to MII registers 0.0~0.5.	

PHY	MII	ROM	R/W	Description	Default
EEPROM enable register / Software reset register					
30	--	1, 0		EEPROM enable register This register should be filled with 55AA in EERPOM register 0 and 1. **IP178C/IP178CH** will examine the specified pattern to confirm if there is a valid EEPROM. The initial setting is updated with the content of EEPROM only if the specified pattern 55AA is found.	
30	0	--	W	Software reset register MII register 0 is software reset register. User can reset **IP178C/IP178CH** by writing 55AA to this register.	
30	0.15	--	R	bfll_full, free buffer is full 1: full, 0: not full This bit is for debug only.	
30	0.14	--	R	extmii_en_in 1: pin EXTMII_EN is latched high, 0: pin EXTMII_EN is latched low This bit is for debug only.	
30	0.13	--	R	Empty, all output queue is empty 1: empty 0: not empty This bit is for debug only.	

PHY	MII	ROM	R/W	Description	Default
Switch control register 1					
30	1[15]	3[7]		PRIORITY_RATE 1: 8 packets 0: 4 packets Output Queue Scheduling: high priority packet rate	1'b0
30	1[14:13]	3[6:5]		LED_O_SEL LED mode selection	P(1,1)

	LinK_LED	SPEED_LED	FDX_LED
00	Off: link fail On: 10 Mbps link ok Flash: Tx/Rx	Off: link fail On: 100 Mbps link ok Flash: Tx/Rx	Off: half duplex On: full duplex
01	Off: link fail On: link ok Flash: Rx	Off: 10 Mbps On: 100 Mbps	Off: half duplex On: full duplex Flash: collision
10	Off: link fail On: 10 Mbps link ok Flash: Tx/Rx	Off: link fail On: 100 Mbps link ok Flash: Tx/Rx	Off: half duplex On: full duplex Flash: collision
11	Off: link fail On: link ok Flash: Tx/Rx	Off: 10 Mbps On: 100 Mbps	Off: half duplex On: full duplex Flash: collision

30	1[12]	3[4]		Reserved	1'b0
30	1[11]	3[3]		Drop16 1: enable, 0:disable	1'b0
30	1[10]	3[2]		X_EN, IEEE 802.3x flow control enable 1: enable, 0:disable	P(1)
30	1[9]	3[1]		EXT_MII_X_EN, MII port IEEE 802.3x flow control enable 1: enable, 0:disable	1'b1
30	1[8]	3[0]		BK_EN, Backpressure enable 1: enable, 0: disable	P(1)
30	1[7]	2[7]		BP_KIND, Backpressure type selection It is valid only if Bk_en is set to 1'b1. 0: carrier base backpressure 1: reserved	1'b0
30	1[6]	2[6]		BF_STM_EN, Broadcast storm enable 1: enable **IP178C/IP178CH** drops the incoming packet if the number of broadcast packet in queue is over the threshold. 0: disable	P(0)
30	1[4]	2[4]		LDPS_DIS Disable link down power saving mode 0: enable link down power saving mode (default) 1: disable link down power saving mode	P(0)

<table>
<tr><th>PHY</th><th>MII</th><th>ROM</th><th>R/W</th><th>Description</th><th>Default</th></tr>
<tr><td>30</td><td>1[5]</td><td>2[5]</td><td></td><td>MLT3_DET
Ability for detecting MLT3 (for 10 Mbps switch to 100 Mbps)
0: disable MLT3 detection ability (default)
1: enable MLT3 detection ability.</td><td>P(0)</td></tr>
<tr><td>30</td><td>1[3:2]</td><td>2[3:2]</td><td></td><td>AGING. Aging time of address table selection
An address tag in hashing table will be removed if this function is turned on and its aging timer expires.
<table>
<tr><td></td><td>Aging time</td><td>note</td></tr>
<tr><td>00</td><td>no aging</td><td></td></tr>
<tr><td>01</td><td>30s</td><td></td></tr>
<tr><td>10</td><td>300s</td><td>default</td></tr>
<tr><td>11</td><td>reserved</td><td></td></tr>
</table></td><td>P(1,0)</td></tr>
<tr><td>30</td><td>1[1]</td><td>2[1]</td><td></td><td>MODBCK. Turn on modified back off algorithm
The maximum back off period is limited to 8-slot time if this function is turned on.
1: turn on, 0: turn off</td><td>P(1)</td></tr>
<tr><td>30</td><td>1[0]</td><td>2[0]</td><td></td><td>Drop extra long packet
Max forwarded packet length

0: 1536 bytes (default)
1: 1552 bytes</td><td>P(0)</td></tr>
</table>

PHY	MII	ROM	R/W	Description	Default
Switch control register 2					
30	2[15:10]	5[7:2]		TMODE_SEL. Test mode selection This function is for testing only. The default value must be adopted for normal operation.	6'b0
30	2[9]	5[1]		MDI_MDIX_EN. Auto MDIMDIX enable 1: Auto MDIMDIX (default) 0: fixed MDI Note: **IP178C/IP178CH** always uses a MDIX transformer.	P(1)
30	2[8]	5[0]		Reserved	P(0)
30	2[7]	4[7]		Reserved	1'b0
30	2[6]	4[6]		MAC_MODE_EN. External MAC mode 1: MAC mode 0: PHY mode	P(0)
30	2[5]	4[5]		RMII_EN. External MII mode 1: RMII 0: MII	P(0)
30	2[4]	4[4]		FX7_en (for IP178CH only) Fiber port 7 enable 1: enable 0: disable	P(0)
30	2[3]	4[3]		FX7_half (for IP178CH only) Fiber port 7 duplex mode 1: half duplex 0: full duplex	P(0)
30	2[2]	4[2]		FX6_en (for IP178CH only) Fiber port 6 enable 1: enable 0: disable	P(0)
30	2[1]	4[1]		FX6_half (for IP178CH only) Fiber port 6 duplex mode 1: half duplex 0: full duplex	P(0)
30	2[0]	4[0]		BI_COLOR	P(0)

PHY	MII	ROM	R/W	Description	Default
Tag register 1~9					
30	3	7,6		VLAN_TAG_0. Port0 default VLAN tag value This register defines the VLAN tag of an un-tagged packet from port 0.	16'h01
30	4	9,8		VLAN_TAG_1. Port1 default VLAN tag value This register defines the VLAN tag of an un-tagged packet from port 1.	16'h01
30	5	11,10		VLAN_TAG_2. Port2 default VLAN tag value This register defines the VLAN tag of an un-tagged packet from port 2.	16'h01
30	6	13, 12		VLAN_TAG_3. Port3 default VLAN tag value This register defines the VLAN tag of an un-tagged packet from port 3.	16'h01
30	7	15, 14		VLAN_TAG_4. Port4 default VALN tag value This register defines the VLAN tag of an un-tagged packet from port 4.	16'h01
30	8	17, 16		VLAN_TAG_5. Port5 default VLAN tag value This register defines the VLAN tag of an un-tagged packet from port 5.	16'h01
30	9	19, 18		VLAN_TAG_6. Port6 default VLAN tag value This register defines the VLAN tag of an un-tagged packet from port 6.	16'h01
30	10	21, 20		VLAN_TAG_7. Port7 default VLAN tag value This register defines the VLAN tag of an un-tagged packet from port 7.	16'h02
30	11	23, 22		VLAN_TAG_8. MII0 default VLAN tag value This register defines the VLAN tag of an un-tagged packet from MII port.	16'h02

PHY	MII	ROM	R/W	Description		Default
Tag register 10						
30	12[8:0]	25[0], 24[7:0]	R/W	ADD_TAG. Add VLAN tag Portx adds a VLAN tag defined in vlan_tag_x to each outgoing packet		9'h00
				Bit 0	1: port0 adds a VLAN tag to each outgoing packet. 0: port0 doesn't add a VLAN tag.	
				Bit 1	1: port1 adds a VLAN tag to each outgoing packet. 0: port1 doesn't add a VLAN tag.	
				Bit 2	1: port2 adds a VLAN tag to each outgoing packet. 0: port2 doesn't add a VLAN tag.	
				Bit 3	1: port3 adds a VLAN tag to each outgoing packet. 0: port3 doesn't add a VLAN tag.	
				Bit 4	1: port4 adds a VLAN tag to each outgoing packet. 0: port4 doesn't add a VLAN tag.	
				Bit 5	1: port5 adds a VLAN tag to each outgoing packet. 0: port5 doesn't add a VLAN tag.	
				Bit 6	1: port6 adds a VLAN tag to each outgoing packet. 0: port6 doesn't add a VLAN tag.	
				Bit 7	1: port7 adds a VLAN tag to each outgoing packet. 0: port7 doesn't add a VLAN tag.	
				Bit 8	1: MII adds a VLAN tag to each outgoing packet. 0: MII doesn't add a VLAN tag.	

PHY	MII	ROM	R/W	Description		Default
Tag register 11						
30	13[12:4]	27[4:0] 26[7:4]	R/W	REMOVE_TAG. Remove VLAN tag		9'h00
				Bit 0	1: port0 removes the VLAN tag of each outgoing packet. 0: port0 doesn't remove the VLAN tag of each outgoing packet.	
				Bit 1	1: port1 removes the VLAN tag of each outgoing packet. 0: port1 doesn't remove the VLAN tag of each outgoing packet.	
				Bit 2	1: port2 removes the VLAN tag of each outgoing packet. 0: port2 doesn't remove the VLAN tag of each outgoing packet.	
				Bit 3	1: port3 removes the VLAN tag of each outgoing packet. 0: port3 doesn't remove the VLAN tag of each outgoing packet.	
				Bit 4	1: port4 removes the VLAN tag of each outgoing packet. 0: port4 doesn't remove the VLAN tag of each outgoing packet.	
				Bit 5	1: port5 removes the VLAN tag of each outgoing packet. 0: port5 doesn't remove the VLAN tag of each outgoing packet.	
				Bit 6	1: port6 removes the VLAN tag of each outgoing packet. 0: port6 doesn't remove the VLAN tag of each outgoing packet.	
				Bit 7	1: port7 removes the VLAN tag of each outgoing packet. 0: port7 doesn't remove the VLAN tag of each outgoing packet.	
				Bit 8	1: MII removes the VLAN tag of each outgoing packet. 0: MII doesn't remove the VLAN tag of each outgoing packet.	

PHY	MII	ROM	R/W	Description		Default
Tag VLAN register 1						
30	13[3]	26[3]		TAG_VLAN_EN. Enable tag VLAN function 1: enable tag VLAN function 0: disable tag VLAN function		1'b0
30	13[2:0]	26[2:0]		VID_SEL. VID index selection Select 4 bits out of 12 bits VID as index of tag VLAN groups. The 12 bits of VID can't be all zeros; otherwise, it will be handled as an un-tagged frame. 000: VID[3:0], 001: VID[4:1], 010: VID[5:2], 011: VID[6:3], 100: VID[7:4], 101: VID[8:5], 110: VID[9:6], 111: VID[10:7] An example of vid_sel = 3'b000,		3'b000
				VLAN_0	VID[3:0] = 4'b0000	
				VLAN_1	VID[3:0] = 4'b0001	
				VLAN_2	VID[3:0] = 4'b0010	
				VLAN_3	VID[3:0] = 4'b0011	
				….	….	
				VLAN_e	VID[3:0] = 4'b1110	
				VLAN_f	VID[3:0] = 4'b1111	

PHY	MII	ROM	R/W	Description		Default
Tag VLAN register 2						
30	14[8:0]	29[0] 28[7:0]		TAG_VLAN_MASK_0[8:0]. Tag VLAN 0 output port mask The mask is valid only if MII register 13.3 TAG_VLAN_EN is logic high and VID index is 4'b0000. When **IP178C/IP178CH** receives a packet, it examines the VID index to choose a tag VLAN mask and forwards the packets according the MAC address table and the mask.		9'h1ff
				Bit0	1: port 0 belongs to VLAN 0 0: port 0 doesn't belong to VLAN 0	
				Bit1	1: port 1 belongs to VLAN 0 0: port 1 doesn't belong to VLAN 0	
				Bit2	1: port 2 belongs to VLAN 0 0: port 2 doesn't belong to VLAN 0	
				Bit3	1: port 3 belongs to VLAN 0 0: port 3 doesn't belong to VLAN 0	
				Bit4	1: port 4 belongs to VLAN 0 0: port 4 doesn't belong to VLAN 0	
				Bit5	1: port 5 belongs to VLAN 0 0: port 5 doesn't belong to VLAN 0	
				Bit6	1: port 6 belongs to VLAN 0 0: port 6 doesn't belong to VLAN 0	
				Bit7	1: port 7 belongs to VLAN 0 0: port 7 doesn't belong to VLAN 0	
				Bit8	1: MII port belongs to VLAN 0 0: MII port doesn't belong to VLAN 0	

PHY	MII	ROM	R/W	Description	Default
Tag VLAN register 3~17					
30	15[8:0]	31[0], 30[7:0]		TAG_VLAN_MASK_1[8:0]. Tag VLAN 1 output port mask	9'h17f
	16[8:0]	33[0], 32[7:0]		TAG_VLAN_MASK_2[8:0]. Tag VLAN 2 output port mask	9'h180
	17[8:0]	35[0], 34[7:0]		TAG_VLAN_MASK_3[8:0]. Tag VLAN 3 output port mask	9'h1ff
	18[8:0]	37[0], 36[7:0]		TAG_VLAN_MASK_4[8:0]. Tag VLAN 4 output port mask	9'h1ff
	19[8:0]	39[0], 38[7:0]		TAG_VLAN_MASK_5[8:0]. Tag VLAN 5 output port mask	9'h1ff
	20[8:0]	41[0], 40[7:0]		TAG_VLAN_MASK_6[8:0]. Tag VLAN 6 output port mask	9'h1ff
	21[8:0]	43[0], 42[7:0]		TAG_VLAN_MASK_7[8:0]. Tag VLAN 7 output port mask	9'h1ff
	22[8:0]	45[0], 44[7:0]		TAG_VLAN_MASK_8[8:0]. Tag VLAN 8 output port mask	9'h1ff
	23[8:0]	47[0], 46[7:0]		TAG_VLAN_MASK_9[8:0]. Tag VLAN 9 output port mask	9'h1ff
	24[8:0]	49[0], 48[7:0]		TAG_VLAN_MASK_A[8:0]. Tag VLAN a output port mask	9'h1ff
	25[8:0]	51[0], 50[7:0]		TAG_VLAN_MASK_B[8:0]. Tag VLAN b output port mask	9'h1ff
	26[8:0]	53[0], 52[7:0]		TAG_VLAN_MASK_C[8:0]. Tag VLAN c output port mask	9'h1ff
	27[8:0]	55[0], 54[7:0]		TAG_VLAN_MASK_D[8:0]. Tag VLAN d output port mask	9'h1ff
	28[8:0]	57[0], 56[7:0]		TAG_VLAN_MASK_E[8:0]. Tag VLAN e output port mask	9'h1ff
	29[8:0]	59[0], 58[7:0]		TAG_VLAN_MASK_F[8:0]. Tag VLAN f output port mask	9'h1ff

PHY	MII	ROM	R/W	Description	Default
Router control register 1					
30	30[11]	61[3]		ROUTER_EN. Enable router function at MII port 1: **SMART MAC** enabled. 0: **SMART MAC** disabled.	1'b0
	30[10:8]	61[2:0]		LAN_GROUPS[2:0]. Number of VLAN groups of LAN ports in a router application It defines the VLANs used by LAN ports. Each VLAN should contain MII port. It is valid only if router_en is enabled. 000: unsupported value 001: 1 VLAN group, (VLAN 1) 010: 2 VLAN groups, (VLAN 1~VLAN 2) 011: 3 VLAN groups, (VLAN 1~VLAN 3) 100: 4 VLAN groups, (VLAN 1~VLAN 4) 101: 5 VLAN groups, (VLAN 1~VLAN 5) 110: 6 VLAN groups, (VLAN 1~VLAN 6) 111: 7 VLAN groups, (VLAN 1~VLAN 7)	3'b001
	30[7:0]	60[7:0]		WAN_PORTS[7:0]. WAN ports for router application It is valid only if router_en is enabled. Bit0: 1: port 0 is a WAN port; 0: port 0 is not a WAN port Bit1: 1: port 1 is a WAN port; 0: port 1 is not a WAN port Bit2: 1: port 2 is a WAN port; 0: port 2 is not a WAN port Bit3: 1: port 3 is a WAN port; 0: port 3 is not a WAN port Bit4: 1: port 4 is a WAN port; 0: port 4 is not a WAN port Bit5: 1: port 5 is a WAN port; 0: port 5 is not a WAN port Bit6: 1: port 6 is a WAN port; 0: port 6 is not a WAN port Bit7: 1: port 7 is a WAN port; 0: port 7 is not a WAN port	8'h80

PHY	MII	ROM	R/W	Description		Default
Router control register 2						
30	31[8:0]	63[0], 62[7:0]		PORT_LOCK_EN[8:0]. Lock port MAC address 1: enable 0: disable User has to turn off aging function when using the port locking function. Aging function can be disabled by pulling low pin 76 AGING or programming register 30.1[3:2].		9'b00
				Bit0	1: port lock enabled in port 0 0: port lock disabled in port 0	
				Bit1	1: port lock enabled in port 1 0: port lock disabled in port 1	
				Bit2	1: port lock enabled in port 2 0: port lock disabled in port 2	
				Bit3	1: port lock enabled in port 3 0: port lock disabled in port 3	
				Bit4	1: port lock enabled in port 4 0: port lock disabled in port 4	
				Bit5	1: port lock enabled in port 5 0: port lock disabled in port 5	
				Bit6	1: port lock enabled in port 6 0: port lock disabled in port 6	
				Bit7	1: port lock enabled in port 7 0: port lock disabled in port 7	
				Bit8	1: port lock enabled in MII port 0: port lock disabled in MII port	

PHY	MII	ROM	R/W	Description	Default
Cos and port base VLAN register 0					
31	0[10]	65[2]		Port0 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port0 are handled as high priority packets.	1'b0
	0[9]	65[1]		Port0 set to be high priority port 1: enable, 0: disabled (default) Packets received from port0 are handled as high priority packets.	1'b0
	0[8:0]	65[0], 64[7:0]		Port0 VLAN look up table The register defines the ports in the same VLAN as port0. The bit 0~8 are corresponding to port 0~8. 1: a port is in the same VLAN as port0 0: a port is not in the same VLAN as port0 Bit0, don't care; Bit1=1, port 1 and port0 are in the same VLAN; Bit2=1, port 2 and port0 are in the same VLAN; Bit3=1, port 3 and port0 are in the same VLAN; Bit4=1, port 4 and port0 are in the same VLAN; Bit5=1, port 5 and port0 are in the same VLAN; Bit6=1, port 6 and port0 are in the same VLAN; Bit7=1, port 7 and port0 are in the same VLAN; Bit8=1, MII port and port0 are in the same VLAN;	9'h1ff

PHY	MII	ROM	R/W	Description	Default
Cos and port base VLAN register 1					
31	1[10]	67[2]		Port1 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port1 are handled as high priority packets.	1'b0
	1[9]	67[1]		Port1 set to be high priority port 1: enable, 0: disabled (default) Packets received from port1 are handled as high priority packets.	1'b0
	1[8:0]	67[0], 66[7:0]		Port1 VLAN look up table The register defines the ports in the same VLAN as port1. The bit 0~8 are corresponding to port 0~8. 1: a port is in the same VLAN as port1 0: a port is not in the same VLAN as port1 Bit0=1, port 0 and port1 are in the same VLAN; Bit1, don't care; Bit2=1, port 2 and port1 are in the same VLAN; Bit3=1, port 3 and port1 are in the same VLAN; Bit4=1, port 4 and port1 are in the same VLAN; Bit5=1, port 5 and port1 are in the same VLAN; Bit6=1, port 6 and port1 are in the same VLAN; Bit7=1, port 7 and port1 are in the same VLAN; Bit8=1, MII port and port1 are in the same VLAN;	9'h1ff

PHY	MII	ROM	R/W	Description	Default
Cos and port base VLAN register 2					
31	2[10]	69[2]		Port2 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port2 are handled as high priority packets.	1'b0
	2[9]	69[1]		Port2 set to be high priority port 1: enable, 0: disabled (default) Packets received from port2 are handled as high priority packets.	1'b0
	2[8:0]	69[0], 68[7:0]		Port2 VLAN look up table The register defines the ports in the same VLAN as port2. The bit 0~8 are corresponding to port 0~8. 1: a port is in the same VLAN as port2 0: a port is not in the same VLAN as port2 Bit0=1, port 0 and port2 are in the same VLAN; Bit1=1, port 1 and port2 are in the same VLAN; Bit2=1, don't care; Bit3=1, port 3 and port2 are in the same VLAN; Bit4=1, port 4 and port2 are in the same VLAN; Bit5=1, port 5 and port2 are in the same VLAN; Bit6=1, port 6 and port2 are in the same VLAN; Bit7=1, port 7 and port2 are in the same VLAN; Bit8=1, MII port and port2 are in the same VLAN;	9'h1ff

PHY	MII	ROM	R/W	Description	Default
Cos and port base VLAN register 3					
31	3[10]	71[2]		Port3 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port3 are handled as high priority packets.	1'b0
	3[9]	71[1]		Port3 set to be high priority port 1: enable, 0: disabled (default) Packets received from port3 are handled as high priority packets.	1'b0
	3[8:0]	71[0], 70[7:0]		Port3 VLAN look up table The register defines the ports in the same VLAN as port3. The bit 0~8 are corresponding to port 0~8. 1: a port is in the same VLAN as port3 0: a port is not in the same VLAN as port3 Bit0=1, port 0 and port3 are in the same VLAN; Bit1=1, port 3 and port3 are in the same VLAN; Bit2=1, port 2 and port3 are in the same VLAN; Bit3=1, don't care; Bit4=1, port 4 and port3 are in the same VLAN; Bit5=1, port 5 and port3 are in the same VLAN; Bit6=1, port 6 and port3 are in the same VLAN; Bit7=1, port 7 and port3 are in the same VLAN; Bit8=1, MII port and port3 are in the same VLAN;	9'h1ff

PHY	MII	ROM	R/W	Description	Default
Cos and port base VLAN register 4					
31	4[10]	73[2]		Port4 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port4 are handled as high priority packets.	1'b0
	4[9]	73[1]		Port4 set to be high priority port 1: enable, 0: disabled (default) Packets received from port4 are handled as high priority packets.	1'b0
	4[8:0]	73[0], 72[7:0]		Port4 VLAN look up table The register defines the ports in the same VLAN as port4. The bit 0~8 are corresponding to port 0~8. 1: a port is in the same VLAN as port4 0: a port is not in the same VLAN as port4 Bit0=1, port 0 and port4 are in the same VLAN; Bit1=1, port 1 and port4 are in the same VLAN; Bit2=1, port 2 and port4 are in the same VLAN; Bit3=1, port 3 and port4 are in the same VLAN; Bit4=1, don't care; Bit5=1, port 5 and port4 are in the same VLAN; Bit6=1, port 6 and port4 are in the same VLAN; Bit7=1, port 7 and port4 are in the same VLAN; Bit8=1, MII port and port4 are in the same VLAN;	9'h1ff

PHY	MII	ROM	R/W	Description	Default
Cos and port base VLAN register 5					
31	5[10]	75[2]		Port5 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port5 are handled as high priority packets.	1'b0
	5[9]	75[1]		Port5 set to be high priority port 1: enable, 0: disabled (default) Packets received from port5 are handled as high priority packets.	1'b0
	5[8:0]	75[0], 74[7:0]		Port5 VLAN look up table The register defines the ports in the same VLAN as port5. The bit 0~8 are corresponding to port 0~8. 1: a port is in the same VLAN as port5 0: a port is not in the same VLAN as port5 Bit0=1, port 0 and port5 are in the same VLAN; Bit1=1, port 1 and port5 are in the same VLAN; Bit2=1, port 2 and port5 are in the same VLAN; Bit3=1, port 3 and port5 are in the same VLAN; Bit4=1, port 4 and port5 are in the same VLAN; Bit5=1, don't care; Bit6=1, port 6 and port5 are in the same VLAN; Bit7=1, port 7 and port5 are in the same VLAN; Bit8=1, MII port and port5 are in the same VLAN;	9'h1ff

PHY	MII	ROM	R/W	Description	Default
Cos and port base VLAN register 6					
31	6[10]	77[2]		Port6 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port6 are handled as high priority packets.	1'b0
	6[9]	77[1]		Port6 set to be high priority port 1: enable, 0: disabled (default) Packets received from port6 are handled as high priority packets.	1'b0
	6[8:0]	77[0], 76[7:0]		Port6 VLAN look up table The register defines the ports in the same VLAN as port6. The bit 0~8 are corresponding to port 0~8. 1: a port is in the same VLAN as port6 0: a port is not in the same VLAN as port6 Bit0=1, port 0 and port6 are in the same VLAN; Bit1=1, port 1 and port6 are in the same VLAN; Bit2=1, port 2 and port6 are in the same VLAN; Bit3=1, port 3 and port6 are in the same VLAN; Bit4=1, port 4 and port6 are in the same VLAN; Bit5=1, port 5 and port6 are in the same VLAN; Bit6=1, don't care; Bit7=1, port 7 and port6 are in the same VLAN; Bit8=1, MII port and port6 are in the same VLAN;	9'h1ff

PHY	MII	ROM	R/W	Description	Default
Cos and port base VLAN register 7					
31	7[10]	79[2]		Port7 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from port7 are handled as high priority packets.	1'b0
	7[9]	79[1]		Port7 set to be high priority port 1: enable, 0: disabled (default) Packets received from port7 are handled as high priority packets.	1'b0
	7[8:0]	79[0], 78[7:0]		Port7 VLAN look up table The register defines the ports in the same VLAN as port7. The bit 0~8 are corresponding to port 0~8. 1: a port is in the same VLAN as port7 0: a port is not in the same VLAN as port7 Bit0=1, port 0 and port7 are in the same VLAN; Bit1=1, port 1 and port7 are in the same VLAN; Bit2=1, port 2 and port7 are in the same VLAN; Bit3=1, port 3 and port7 are in the same VLAN; Bit4=1, port 4 and port7 are in the same VLAN; Bit5=1, port 5 and port7 are in the same VLAN; Bit6=1, port 6 and port7 are in the same VLAN; Bit7=1, don't care; Bit8=1, MII port and port7 are in the same VLAN;	9'h1ff

PHY	MII	ROM	R/W	Description	Default
Cos and port base VLAN register 8					
31	8[10]	81[2]		MII port Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from MII port are handled as high priority packets.	1'b0
	8[9]	81[1]		MII port set to be high priority port 1: enable, 0: disabled (default) Packets received from MII port are handled as high priority packets.	1'b0
	8[8:0]	81[0], 80[7:0]		MII port VLAN look up table The register defines the ports in the same VLAN as port8. The bit 0~8 are corresponding to port 0~8. 1: a port is in the same VLAN as MII port 0: a port is not in the same VLAN as MI port Bit0=1, port 0 and MII port are in the same VLAN; Bit1=1, port 1 and MII port are in the same VLAN; Bit2=1, port 2 and MII port are in the same VLAN; Bit3=1, port 3 and MII port are in the same VLAN; Bit4=1, port 4 and MII port are in the same VLAN; Bit5=1, port 5 and MII port are in the same VLAN; Bit6=1, port 6 and MII port are in the same VLAN; Bit7=1, port 7 and MII port are in the same VLAN; Bit8=1, don't care;	9'h1ff

PHY	MII	ROM	R/W	Description	Default
Switch control register 3					
31	9[15:14]	83[7:6]		BF_STM_THR_SEL[1:0]. Broadcast storm threshold selection 00: 159 packets/10ms for 100Mbps port, or 159 packets/100ms for 10Mbps port, 01: 127 packets/10ms for 100Mbps port, or 127 packets/100ms for 10Mbps port, 10: 63 packets/10ms for 100Mbps port, or 63 packets/100ms for 10Mbps port, 11: 31 packets/10ms for 100Mbps port, or 31 packets/100ms for 10Mbps port	2'b11
	9[13:12]	83[5:4]		SHARE_FULL_THR_SEL[1;0]. Share buffer threshold selection 00: 160 units 01: 180 units 10: 140 units 11: 120 units	2'b00
	9[11:10]	83[3:2]		UNIT_DEFAULT_THR_SEL[1:0]. Output Queue minimum threshold selection 00: 40 units 01: 32 units 10: 48 units 11: 56 units	2'b00
	9[9:8]	83[1:0]		UNIT_LOW_THR_SEL	2'b00
	9[7:6]	82[7:6]		UNIT_HIGH_THR_SEL[1;0]. Output Queue Flow control ON threshold selection If share buffer is over share buffer full threshold, Output Queue Flow control ON threshold will be dynamic changed to 28. Others, 00: 50 units 01: 70 units 10: 90 units 11: 110 units	2'b00
	9[5]	82[5]		RESERVED	
	9[4]	82[4]		PREDROP_EN 1: Drop an incoming broadcast packet if any port is congested. 0: forward an incoming broadcast packet to un-congested ports instead of congested ports.	1
	9[3:2]	82[3:2]		PKT_LOW_THR_SEL[1:0]. Packet low water mark threshold selection 00: 40 units 01: 30 units 10: 20 units 11: 10 units	2'b00

PHY	MII	ROM	R/W	Description	Default
	9[1:0]	82[1:0]		PKT_HIGH_THR_SEL[1:0]. Packet high water mark threshold selection 00: 50 units 01: 40 units 10: 30 units 11: 20 units	2'b00

PHY	MII	ROM	R/W	Description	Default
Reserved register (It is for testing only and is not released to users)					
31	10[13:12]	85[5:4]		DRIVE[1:0]	
31	10[11]	85[3]		BF_STM_EN_QM	0
31	10[10]	85[2]		HP_DIS_FLOW_EN	0
31	10[9]	85[1]		TWOPART	1
31	10[8]	85[0]		ALLPASS	0
31	10[7:5]	84[7:5]		PHY PIN RESERVED[2:0]	0
31	10[4]	84[4]		BYSCR_MODE	0
31	10[3]	84[3]		DIGITAL_LPBK	0
31	10[2]	84[2]		DIGITAL_SPEED_UP	0
31	10[1]	84[1]		SPEED_UP_10	0
31	10[0]	84[0]		F_LINK_100	0
Reserved register (It is for testing only and is not released to users)					
31	11[15:0]	87[7:0], 86[7:0]		PHY_EEPROM_SETTING_1[15:0]	16'h0000
31	12[15:0]	89[7:0], 88[7:0]		PHY_EEPROM_SETTING_2[15:0]	16'h0000

PHY	MII	ROM	R/W	Description	Default
Spanning tree control registers					
31	13[15:8]	91		Forward_en 13[15]: 1: port7 forwarding enabled; 0: port7 forwarding disabled, 13[14]: 1: port6 forwarding enabled; 0: port6 forwarding disabled, 13[13]: 1: port5 forwarding enabled; 0: port5 forwarding disabled, 13[12]: 1: port4 forwarding enabled; 0: port4 forwarding disabled, 13[11]: 1: port3 forwarding enabled; 0: port3 forwarding disabled, 13[10]: 1: port2 forwarding enabled; 0: port2 forwarding disabled, 13[9]: 1: port1 forwarding enabled; 0: port1 forwarding disabled, 13[8]: 1: port0 forwarding enabled; 0: port0 forwarding disabled,	8'hff
31	13[7:0]	90		Learning_en 13[7]: 1: port7 learning enabled; 0: port7 learning disabled, 13[6]: 1: port6 learning enabled; 0: port6 learning disabled, 13[5]: 1: port5 learning enabled; 0: port5 learning disabled, 13[4]: 1: port4 learning enabled; 0: port4 learning disabled, 13[3]: 1: port3 learning enabled; 0: port3 learning disabled, 13[2]: 1: port2 learning enabled; 0: port2 learning disabled, 13[1]: 1: port1 learning enabled; 0: port1 learning disabled, 13[0]: 1: port0 learning enabled; 0: port0 learning disabled	8'hff

PHY	MII	ROM	R/W	Description	Default
Spanning tree registers					
31	14	93, 92		static_mac_0[15:0]	16'h0
31	15	95, 94		static_mac_0[31:16]	16'hc200
31	16	97, 96		static_mac_0[47:32]	8'h0180
31	17	99,98		[10]: static_overide_0 1: override the transmission, receiving and learning setting in MII register 31.13. 0: not override [9]: static_valid_0 1: the entry is valid 0: the entry is not valid [8:0]: static_port_mask_0 Bit [8]: forward to port MII Bit [7]: forward to port 7 Bit [6]: forward to port 6 Bit [5]: forward to port 5 Bit [4]: forward to port 4 Bit [3]: forward to port 3 Bit [2]: forward to port 2 Bit [1]: forward to port 1 Bit [0]: forward to port 0	16'h0500

PHY	MII	ROM	R/W	Description	Default
Spanning tree registers					
31	18	101,100		static_mac_1[15:0]	16'h0
31	19	103,102		static_mac_1[31:16]	16'h0
31	20	105		static_mac_1[47:32]	16'h0
31	21	107,106		[10]: static_overide_1 1: override the transmission, receiving and learning setting in MII register 31.13. 0: not override [9]: static_valid_1 1: the entry is valid 0: the entry is not valid [8:0]: static_port_mask_1 Bit [8]: forward to port MII Bit [7]: forward to port 7 Bit [6]: forward to port 6 Bit [5]: forward to port 5 Bit [4]: forward to port 4 Bit [3]: forward to port 3 Bit [2]: forward to port 2 Bit [1]: forward to port 1 Bit [0]: forward to port 0	16'h0100
DSCP register for IPv4/IPv6 DiffServ					
31	22	109,108		DSCP[15:0]	16'h0
31	23	111,110		DSCP[31:16]	16'h0
31	24	113,112		DSCP[47:32]	16'h0
31	25	115,114		DSCP[63:48]	16'h0

PHY	MII	ROM	R/W	Description	Default
31	26	117,116		[14:12]: bw_control_p1_tx [10:8]: bw_control_p1_rx [6:4]: bw_control_p0_tx [2:0]: bw_control_p0_rx BW Control Value Setting, 000 : no limit 100 : 1M bit 001 : 128k bit 101 : 2M bit 010 : 256k bit 110 : 4M bit 011 : 512k bit 111 : 8M bi	16'h0
31	27	119,118		[14:12]: bw_control_p3_tx [10:8]: bw_control_p3_rx [6:4]: bw_control_p2_tx [2:0]: bw_control_p2_rx	16'h0
31	28	121,120		[14:12]: bw_control_p5_tx [10:8]: bw_control_p5_rx [6:4]: bw_control_p4_tx [2:0]: bw_control_p4_rx	16'h0
31	29	123,122		[14:12]: bw_control_p7_tx [10:8]: bw_control_p7_rx [6:4]: bw_control_p6_tx [2:0]: bw_control_p6_rx	16'h0
31	30	125,124		[15]: bw_en_qm [14]: stag_en [13]: diffserv_en [12]: bf_ffff_only, 1: broadcast DA=FFFFFFFF 0: broadcast DA=FFFFFFFF and multicast frame [11:8]: special_add_forward BIT3: Reserved MAC address (0180C2000010-0180C20000FF) 1: forward (default), 0: discard. BIT2: Reserved MAC address (0180C2000002- 0180C200000F) 1: forward (default), 0: discard. The default value is the inverted value of pin 78 FILTER_RSV_DA. BIT1: Reserved MAC address (0180C2000001) 1: forward, 0: discard (default)	16'h8d00

PHY	MII	ROM	R/W	Description		Default
				BIT0	Reserved MAC address (0180C2000000) 1: forward (default), 0: discard	
				Default value		
				EXTMII_EN=1	EXTMII_EN =0	
				1101	{1, inv of pin78 FILTER_RSV_DA(0), 0, 1}	
				[6:4]: bw_control_p8_tx [2:0]: bw_control_p8_rx		
31	31	127,126		PHY_EEPROM_SETTING_3[15:0]		16'h0000

3 Electrical Characteristics

3.1 Absolute Maximum Rating

Stresses exceed those values listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional performance and device reliability are not guaranteed under these conditions. All voltages are specified with respect to GND.

Supply Voltage	–0.3V to 4.0V
Input Voltage	–0.3V to 5.0V
Output Voltage	–0.3V to 5.0V
Storage Temperature	-65°C to 150°C
Ambient Operating Temperature (Ta)	0°C to 70°C

3.2 DC Characteristic

Operating Conditions

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VCC	1.80	1.95	2.05	V	All ports unlink
Supply Voltage	VCC_O	3.135	3.3	3.465	V	3.3V IO
Supply Voltage	VCC_O	2.375	2.5	2.625	V	2.5V IO
Power Consumption			1.35		W	100 Mbps full, VCC=1.95V

Input Clock

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Frequency			25		MHz	
Frequency Tolerance		-50		+50	PPM	

I/O Electrical Characteristics

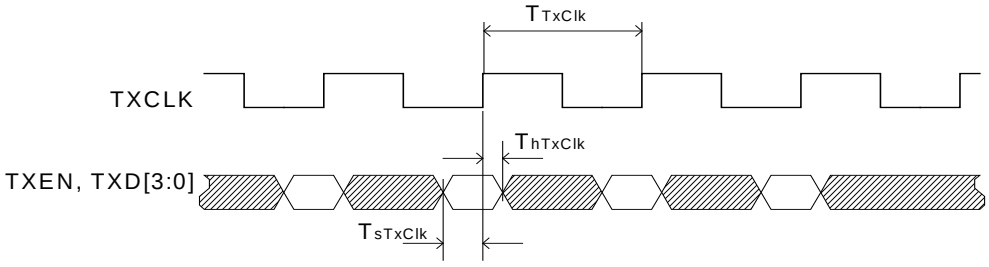
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
X1 Input Low Voltage	VIL			0.89	V	
X1 Input High Voltage	VIH	0.95			V	
Output Low Voltage	VOL			0.4	V	IOH=4mA, VCC_O_x=3.3V
Output High Voltage	VOH	2.4			V	IOL=4mA, VCC_O_x=3.3V
FXSDx Input Low Voltage	VIL			0.3	V	For IP178CH only
FXSDx Input High Voltage	VIH	1			V	For IP178CH only

3.3 AC Timing

3.3.1 PHY Mode MII Timing

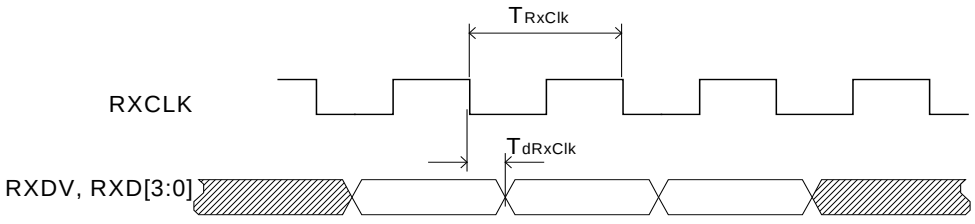
a. Transmit Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{TxClk}	Transmit clock period 100 Mbps MII	-	40	-	ns
T_{sTxClk}	TXEN, TXD to TXCLK setup time	2	-	-	ns
T_{hTxClk}	TXEN, TXD to TXCLK hold time	0.5	-	-	ns



b. Receive Timing

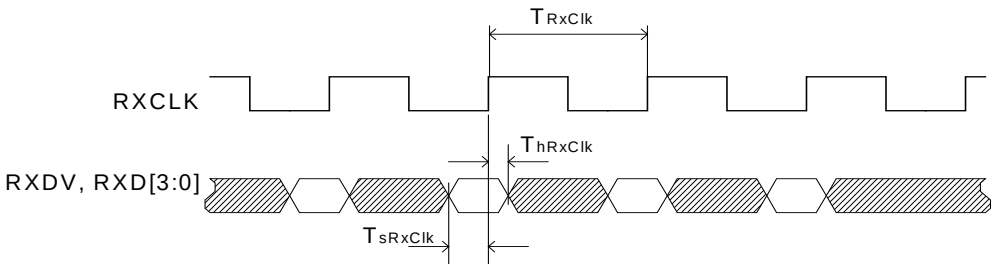
Symbol	Description	Min.	Typ.	Max.	Unit
T_{RxClk}	Receive clock period 100 Mbps MII	-	40	-	ns
T_{RxClk}	Receive clock period 10 Mbps MII	-	400	-	ns
T_{dRxClk}	RXCLK falling edge to RXDV, RXD	1	-	4	ns



3.3.2 MAC Mode MII Timing

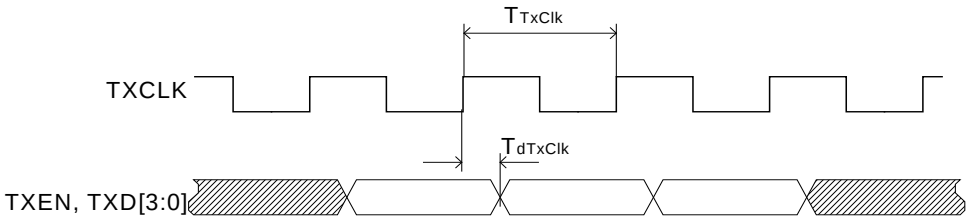
a. Receive Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{RxClk}	Receive clock period 100 Mbps MII	-	40	-	ns
T_{sRxClk}	RXDV, RXD to RXCLK setup time	2	-	-	ns
T_{hRxClk}	RXDV, RXD to RXCLK hold time	0.5	-	-	ns



b. Transmit Timing

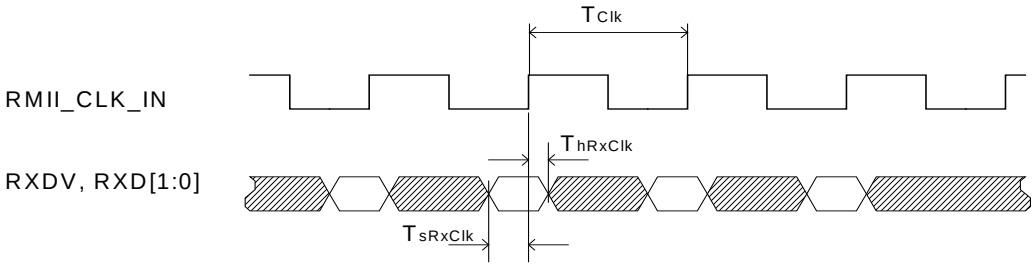
Symbol	Description	Min.	Typ.	Max.	Unit
T_{TxClk}	Transmit clock period 100 Mbps MII	-	40	-	ns
T_{dTxClk}	TXCLK rising edge to TXEN, TXD	1	-	4	ns



3.3.3 RMII Timing

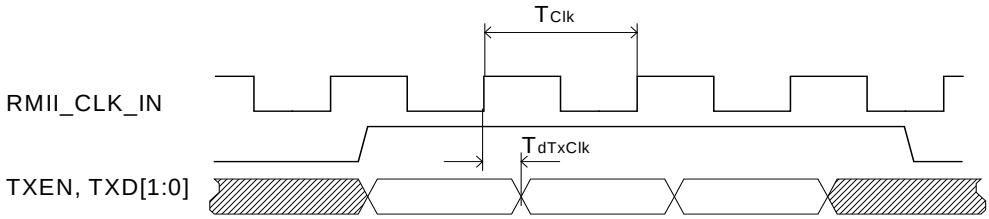
a. Receive Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{Clk}	Clock period	-	20	-	ns
T_{sRxClk}	RXDV, RXD to RMII_CLK_IN setup time	2	-	-	ns
T_{hRxClk}	RXDV, RXD to RMII_CLK_IN hold time	0.5	-	-	ns



b. Transmit Timing

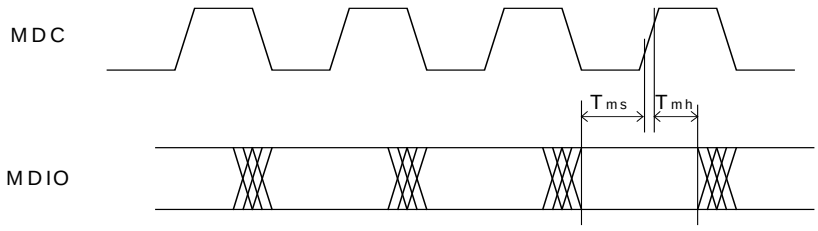
Symbol	Description	Min.	Typ.	Max.	Unit
T_{Clk}	Clock period	-	20	-	ns
T_{dTxClk}	RMII_CLK_IN rising edge to TXEN, TXD	1	-	4	ns



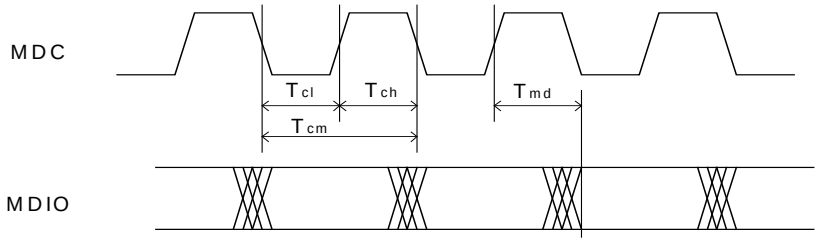
3.3.4 SMI Timing

a. MDC/MDIO Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{ch}	MDC High Time	40	-	-	ns
T_{cl}	MDC Low Time	40	-	-	ns
T_{cm}	MDC period	80	-	-	ns
T_{md}	MDIO output delay	-	-	5	ns
T_{mh}	MDIO setup time	10	-	-	ns
T_{ms}	MDIO hold time	10	-	-	ns



Write Cycle

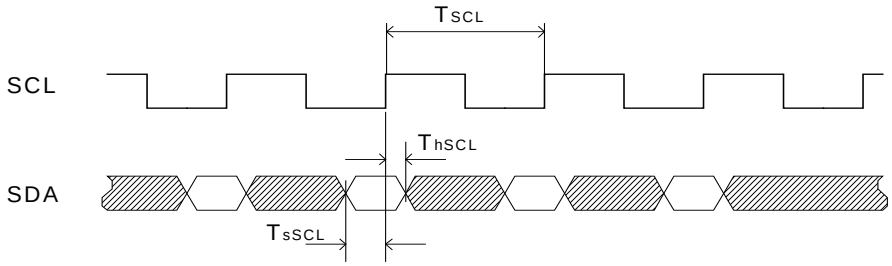


Read Cycle

3.3.5 EEPROM Timing

a.

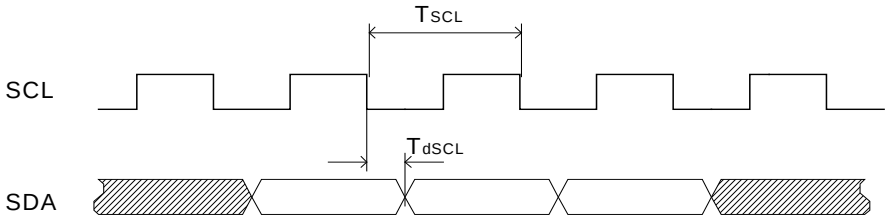
Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Receive clock period	-	20480	-	ns
T_{sSCL}	SDA to SCL setup time	2	-	-	ns
T_{hSCL}	SDA to SCL hold time	0.5	-	-	ns



Read data cycle

b.

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Transmit clock period	-	20480	-	ns
T_{dSCL}	SCL falling edge to SDA	-	-	5200	ns



Comand cycle

3.4 Thermal Data

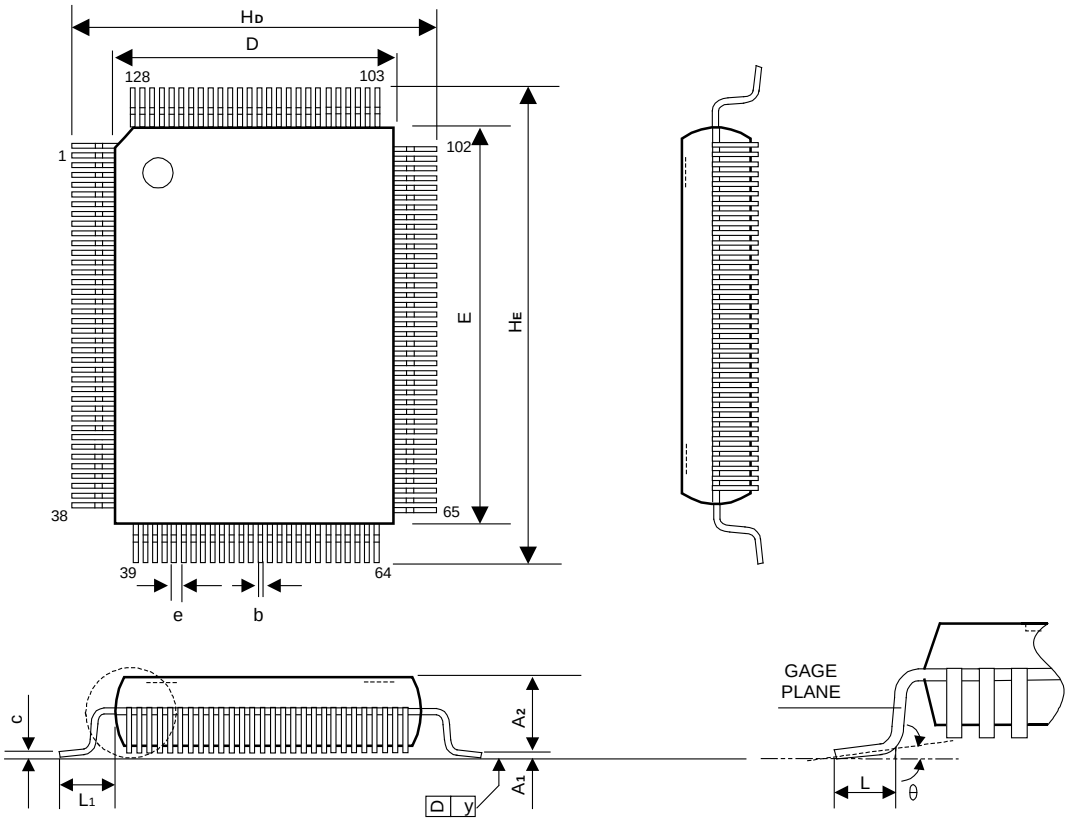
Theta Ja	Theta Jc	Conditions	Units
29.1~30.4	9.3~10.7	2 Layer PCB	^{o}C/W

4 Order information

Part No.	Package	Notice
IP178C	128-PIN PQFP	-
IP178C LF	128-PIN PQFP	Lead free
IP178CH	128-PIN PQFP	For fiber application-
IP178CH LF	128-PIN PQFP	For fiber application Lead free

5 Package Detail

128 PQFP Outline Dimensions



Symbol	Dimensions In Inches			Dimensions In mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A1	0.010	0.014	0.018	0.25	0.35	0.45
A2	0.107	0.112	0.117	2.73	2.85	2.97
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.09	0.15	0.20
HD	0.669	0.677	0.685	17.00	17.20	17.40
D	0.547	0.551	0.555	13.90	14.00	14.10
HE	0.906	0.913	0.921	23.00	23.20	23.40
E	0.783	0.787	0.791	19.90	20.00	20.10
e	-	0.020	-	-	0.50	-
L	0.025	0.035	0.041	0.65	0.88	1.03
L1	-	0.063	-	-	1.60	-
y	-	-	0.004	-	-	0.10
θ	0°	-	12°	0°	-	12°

Note:
1. Dimension D & E do not include mold protrusion.
2. Dimension B does not include dambar protrusion. Total in excess of the B dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.

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