10A Integrated FET Regulator with Programmable LDO

Features

- Input voltage — 3V to 28V
- Internal power MOSFETs — 10A
- Integrated bootstrap switch
- Smart power-save protection
- Configurable 150mA LDO with bypass capability
- TC compensated $R_{DS(ON)}$ sensed current limit
- Pseudo-fixed frequency adaptive on-time control
- Designed for use with ceramic capacitors
- Programmable V_{IN} UVLO threshold
- Independent enable for switcher and LDO
- Selectable ultra-sonic power-save (SC417)
- Selectable power-save (SC427)
- Internal soft-start and soft-shutdown at output
- Internal reference — 1% tolerance
- Over-voltage/under-voltage fault protection
- Power good output
- Lead-free 5x5mm, 32 Pin MLPQ package
- Fully WEEE and RoHS compliant

Applications

- Notebook, desktop, tablet, and server computers
- Networking and telecommunication equipment
- Printers, DSL, and STB applications
- Embedded applications
- Power supply modules
- Point of load power supplies

Description

The SC417/SC427 is a stand-alone synchronous buck power supply. It features integrated power MOSFETs, a bootstrap switch, and a programmable LDO in a space-saving MLPQ-5x5mm 32-pin package. The device is highly efficient and uses minimal PCB area. It uses pseudo-fixed frequency adaptive on-time operation to provide fast transient response.

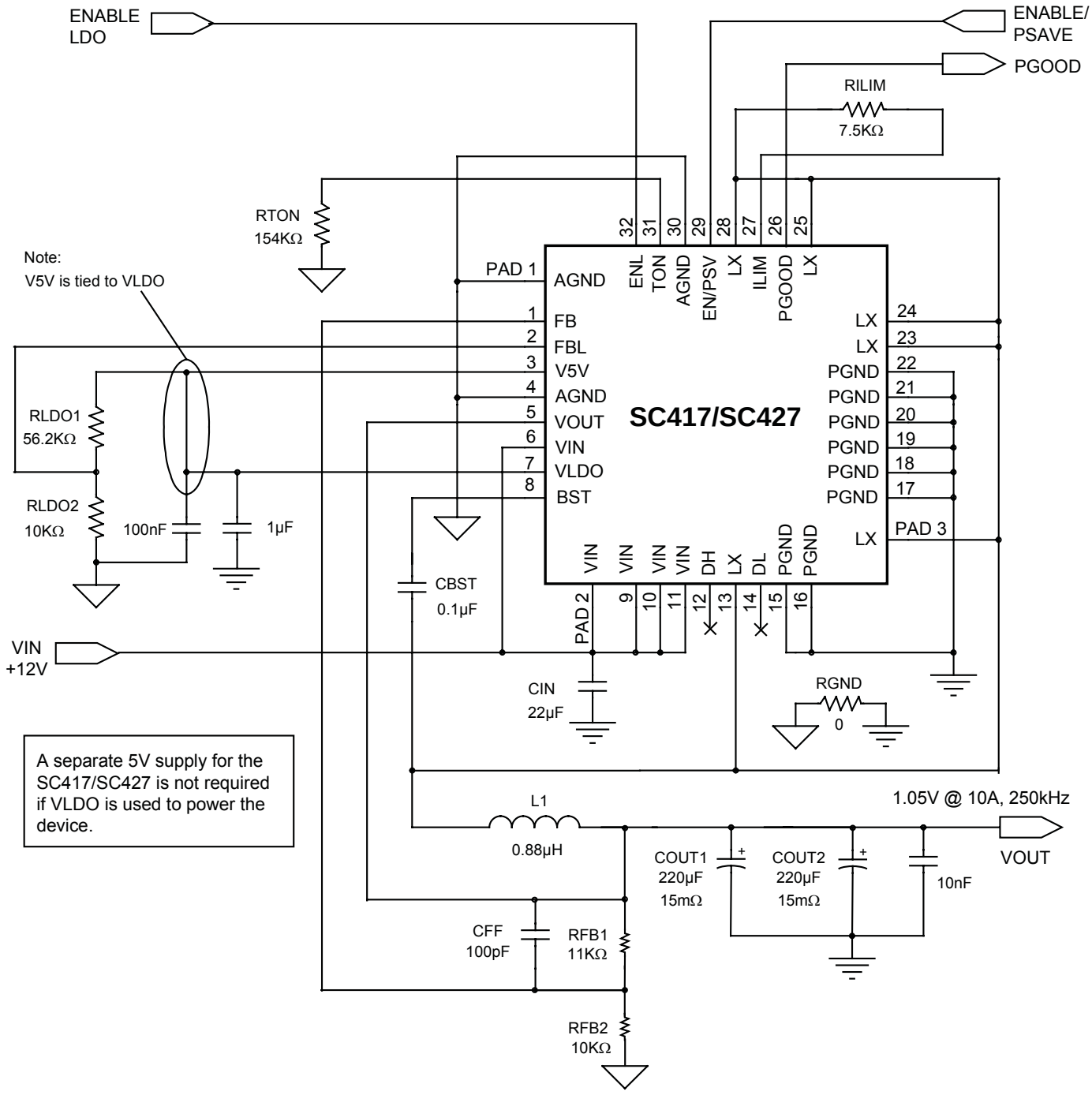
The SC417/SC427 supports using standard capacitor types such as electrolytic or special polymer in addition to ceramic, at switching frequencies up to 1MHz. The programmable frequency, synchronous operation, and selectable power-save provide high efficiency operation over a wide load range.

The LDO output is programmable from 0.75V to 5.25V using external resistors. The bias voltage for the device can be supplied by the on-chip LDO when $V_{IN} > 4.5V$, or by an external 5V supply. When a separate source is used as the bias supply, the LDO can be programmed to provide a different voltage.

Additional features include cycle-by-cycle current limit, soft-start, under and over-voltage protection, programmable over-current protection, soft shutdown, and selectable power-save. The device also provides separate enable inputs for the PWM controller and LDO as well as a power good output for the PWM controller.

The input voltage can range from 3V to 28V. The wide input voltage range, programmable frequency, and programmable LDO make the device extremely flexible and easy to use in a broad range of applications. Support is provided for single cell or multi-cell battery systems in addition to traditional DC power supply applications.

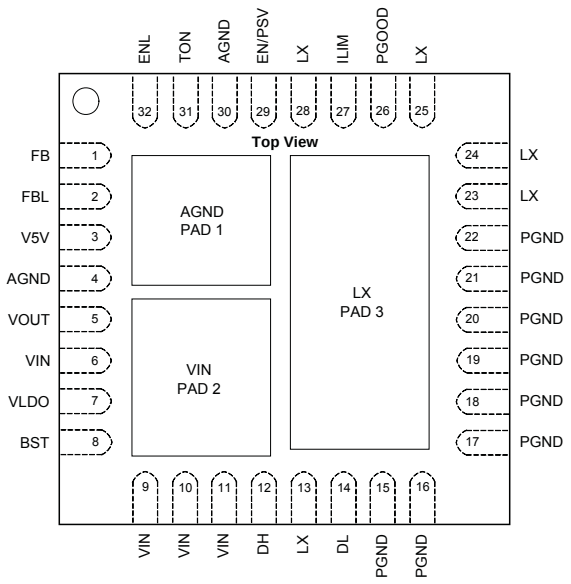
Typical Application Circuit



Key Components

Component	Value	Manufacturer	Part Number	Web
CIN	22µF/25V	Murata	GRM32ER61E226KE15L	www.murata.com
COUT1, COUT2	220µF/15mΩ/6.3V	Panasonic	EEFUE0J221R	www.panasonic.com
L1	0.88µH/20A	Vishay	IHLP4040DZERR88M11	www.vishay.com
All other small signal components (resistors and capacitors) are standard SMT devices.				

Pin Configuration



MLPQ-32; 5x5, 32 LEAD

Ordering Information

Device	Package
SC417MLTRT[1][2]	MLPQ-32 5X5
SC427MLTRT[1][2]	MLPQ-32 5X5
SC417EVB	Evaluation Board
SC427EVB	Evaluation Board

Notes:

1) Available in tape and reel only. A reel contains 3000 devices.
2) Lead-free packaging only. Device is WEEE and RoHS compliant.

Marking Information

yyww. = Date Code
xxxxxx = Semtech Lot Number
xxxxxx = Semtech Lot Number

yyww. = Date Code
xxxxxx = Semtech Lot Number
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Absolute Maximum Ratings[1]

LX to PGND (V) ..... -0.3 to +30
LX to PGND (V) (transient — 100ns) ..... -2 to +30
VIN to PGND (V) ..... -0.3 to +30
EN/PSV, PGOOD, ILIM, to GND (V) ..... -0.3 to +(V5V+0.3)
VOUT, VLDO, FB, FBL, to GND (V) ..... -0.3 to +(V5V+0.3)
V5V to PGND (V) ..... -0.3 to +6
TON to PGND (V) ..... -0.3 to +(V5V - 1.5)
ENL (V) ..... -0.3 to V_{IN}
BST to LX (V) ..... -0.3 to +6.0
BST to PGND (V) ..... -0.3 to +35
AGND to PGND (V) ..... -0.3 to +0.3

Recommended Operating Conditions

Input Voltage (V) ..... 3.0 to 28
V5V to PGND (V) ..... 4.5 to 5.5
VOUT to PGND (V) ..... 0.5 to 5.5

Thermal Information

Storage Temperature (°C) ..... -60 to +150
Maximum Junction Temperature (°C) 150
Operating Junction Temperature (°C) ..... -40 to +125
Thermal resistance, junction to ambient [2] (°C/W)
- High-side MOSFET 25
- Low-side MOSFET 20
- PWM controller and LDO thermal resistance 50

Peak IR Reflow Temperature (°C) 260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) This device is ESD sensitive. Use of standard ESD handling precautions is required.
(2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless specified: V_{IN} =12V, T_A = +25°C for Typ, -40 to +85 °C for Min and Max, T_J < 125°C, V5V = +5V, Typical Application Circuit

Parameter	Conditions	Min	Typ	Max	Units
Input Supplies					
Input Supply Voltage		3		28	V
V5V Voltage		4.5		5.5	V
VIN UVLO Threshold[1]	Sensed at ENL pin, rising edge	2.40	2.60	2.95	V
	Sensed at ENL pin, falling edge	2.235	2.40	2.565	
VIN UVLO Hysteresis	EN/PSV = High		0.2		V
V5V UVLO Threshold	Measured at V5V pin, rising edge	3.7	3.9	4.1	V
	Measured at V5V pin, falling edge	3.5	3.6	3.75	
V5V UVLO Hysteresis			0.3		V
VIN Supply Current	ENL , EN/PSV = 0V, V_{IN} = 28V		8.5	20	µA
	Standby mode; ENL=V5V, EN/PSV = 0V		130		

Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
Input Supplies (continued)					
V5V Supply Current	ENL , EN/PSV = 0V		3	7	µA
	SC417, EN/PSV = V5V, no load (f_{SW} = 25kHz), V_{FB} > 500mV[2]		2		mA
	SC427, EN/PSV = V5V, no load, V_{FB} > 500mV[2]		0.7		
	f_{SW} = 250kHz, EN/PSV = floating , no load[2]		10		
FB On-Time Threshold	static V_{IN} and load, 0 to +85 °C	0.496	0.500	0.504	V
	static V_{IN} and load, -40 to +85 °C	0.495		0.505	V
Frequency Range	continuous mode operation	200		1000	kHz
	minimum f_{SW}, (SC417 only), EN/PSV = V5V, no load		25		
Bootstrap Switch Resistance			10		Ω
Timing					
On-Time	continuous mode operation, V_{IN} = 15V, V_{OUT} = 5V, f_{SW}= 300kHz, R_{TON} = 133kΩ	999	1110	1220	ns
Minimum On-Time [2]			50		ns
Minimum Off-Time [2]			250		ns
Soft-Start					
Soft-Start Ramp Time [2]			850		µs
Analog Inputs/Outputs					
VOUT Input Resistance			500		kΩ
Current Sense					
Zero-Crossing Detector Threshold	LX - PGND	-3	0	+3	mV
Power Good					
Power Good Threshold	upper limit, V_{FB} > internal 500mV reference		+20		%
	lower limit, V_{FB} < internal 500mV reference		-10		%
Start-Up Delay Time			2		ms
Fault (noise immunity) Delay Time[2]			5		µs
Leakage				1	µA
Power Good On-Resistance			10		Ω

Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
Fault Protection					
Valley Current Limit	R_{ILIM} = 5.9k Ω	6	8	10	A
I_{LIM} Source Current			10		µA
I_{LIM} Comparator Offset	with respect to AGND	-10	0	+10	mV
Output Under-Voltage Fault	V_{FB} with respect to internal 500mV reference, 8 consecutive clocks		-25		%
Smart Power-save Protection Threshold (2)	V_{FB} with respect to internal 500mV reference		+10		%
Over-Voltage Protection Threshold	V_{FB} with respect to internal 500mV reference		+20		%
Over-Voltage Fault Delay(2)			5		µs
Over-Temperature Shutdown(2)	10°C hysteresis		150		°C
Logic Inputs/Outputs					
Logic Input High Voltage	EN/PSV, ENL	2.0			V
Logic Input Low Voltage	EN/PSV, ENL			0.4	V
EN/PSV Input Bias Current	EN/PSV= V5V or AGND	-10		+10	µA
ENL Input Bias Current	V_{IN} = 28V		11	18	µA
FBL, FB Input Bias Current	FBL, FB = V5V or AGND	-1		+1	µA
Linear Regulator (LDO)					
FBL Accuracy	VLDO load = 10mA	0.735	0.75	0.765	V
LDO Current Limit	Start-up and foldback, V_{IN} = 12V		85		mA
	operating current limit, V_{IN} = 12V	135	200		
VLDO to VOUT Switch-over Threshold (3)		-140		+140	mV
VLDO to VOUT Non-switch-over Threshold (3)		-450		+450	mV
VLDO to VOUT Switch-over Resistance	V_{OUT} = +5V		2		Ω
LDO Drop Out Voltage (4)	from V_{IN} to V_{VLDO}, V_{VLDO} = +5V, I_{VLDO} = 100mA		1.2		V

Notes:

(1) V_{IN} UVLO is programmable using a resistor divider from VIN to ENL to AGND. The ENL voltage is compared to an internal reference.

(2) Guaranteed by design.

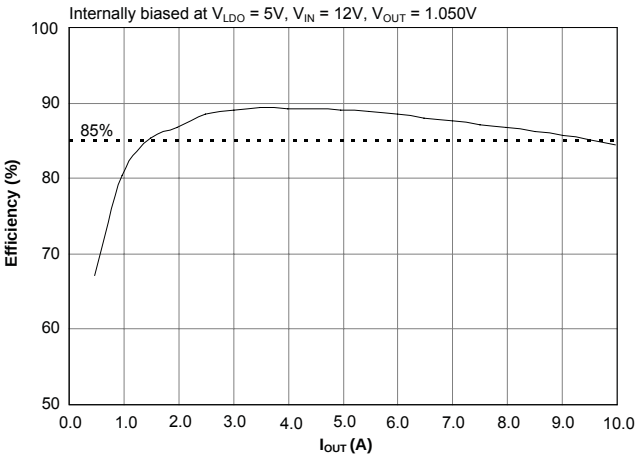
(3) The switch-over threshold is the maximum voltage differential between the VLDO and VOUT pins which ensures that VLDO will internally switch-over to VOUT. The non-switch-over threshold is the minimum voltage differential between the VLDO and VOUT pins which ensures that VLDO will not switch-over to VOUT.

(4) The LDO drop out voltage is the voltage at which the LDO output drops 2% below the nominal regulation point.

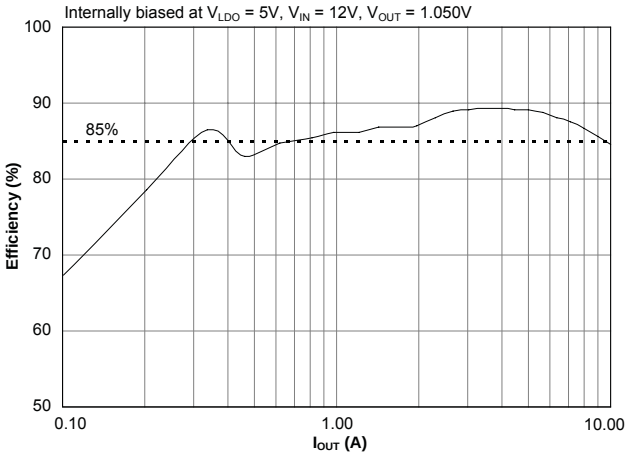
Typical Characteristics

Characteristics in this section are based on using the Typical Application Circuit on page 2 (SC417).

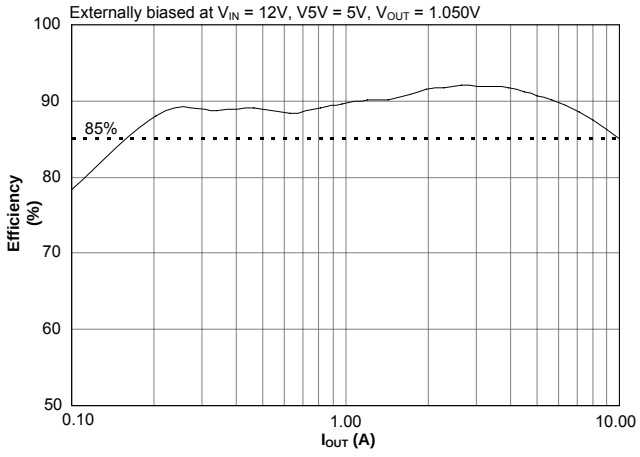
Efficiency vs. Load — Forced Continuous Mode



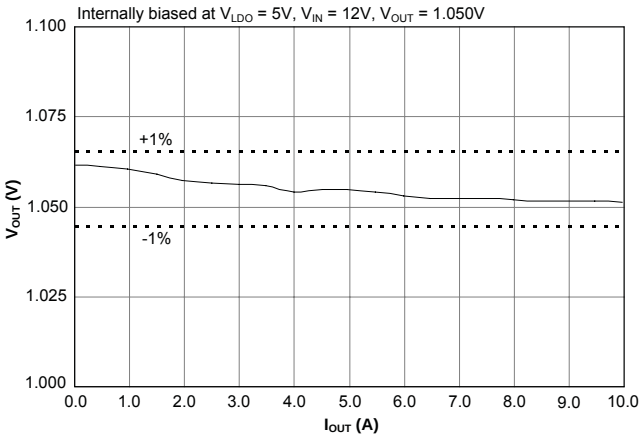
Efficiency vs. Load — Powersave Mode



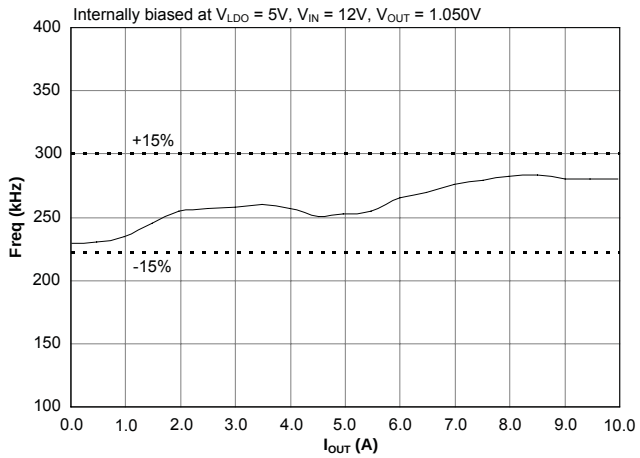
Efficiency vs. Load — Powersave Mode



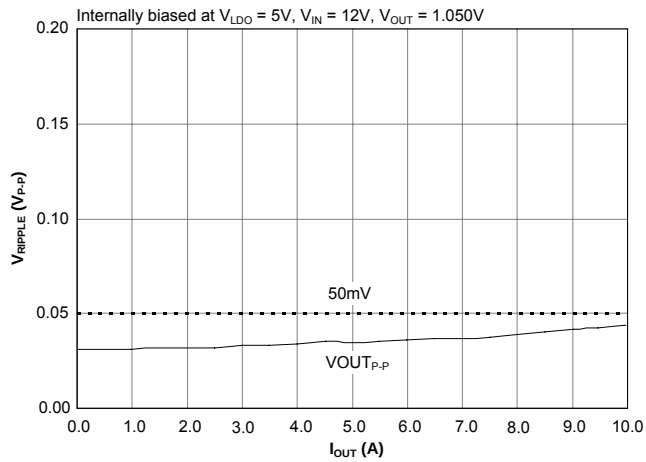
V_{OUT} vs. Load — Forced Continuous Mode



Frequency vs. Load — Forced Continuous Mode



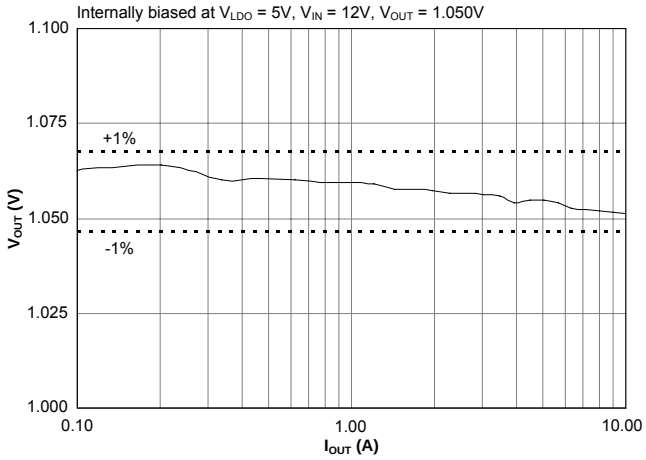
V_{RIPPLE} vs. Load — Forced Continuous Mode



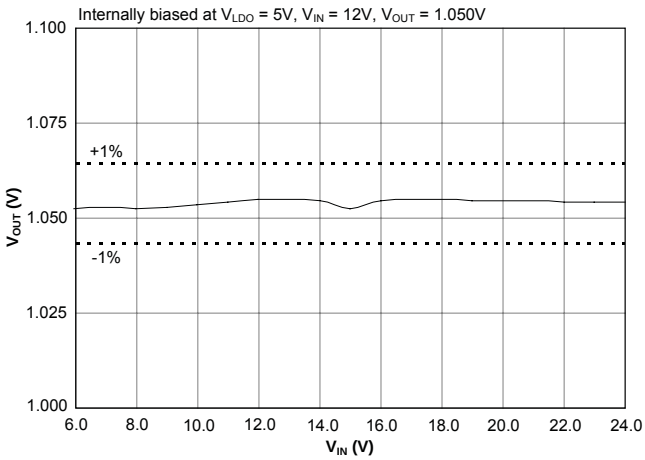
Typical Characteristics (continued)

Characteristics in this section are based on using the Typical Application Circuit on page 2 (SC417).

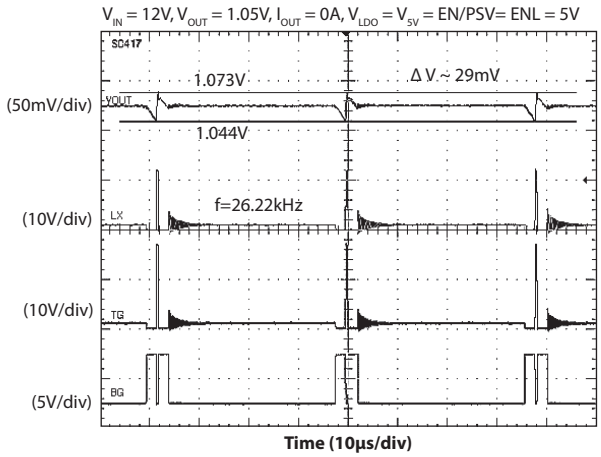
V_{OUT} vs. Load — Powersave Mode



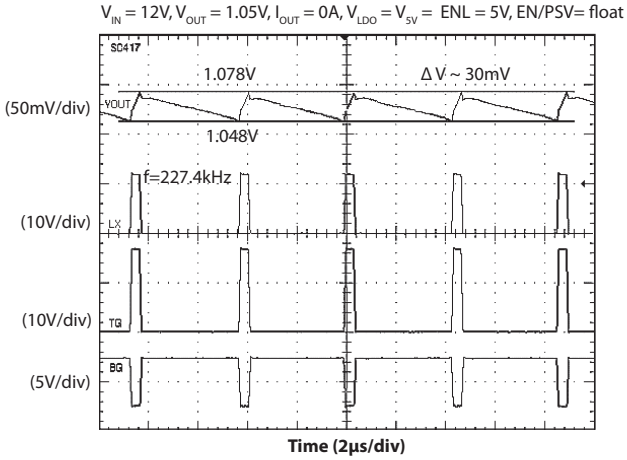
V_{OUT} vs. Line — Forced Continuous Mode



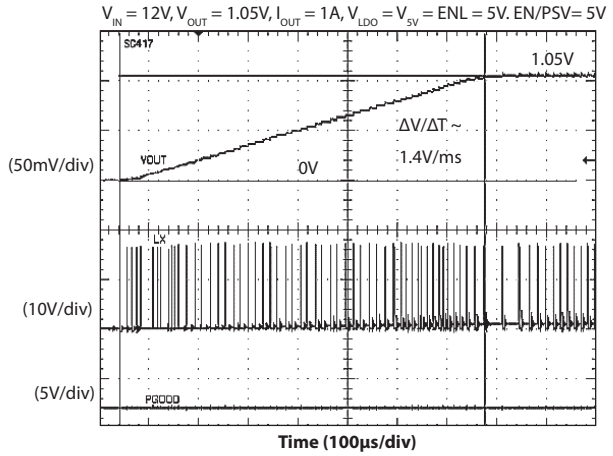
Ultrasonic Powersave Mode — No Load



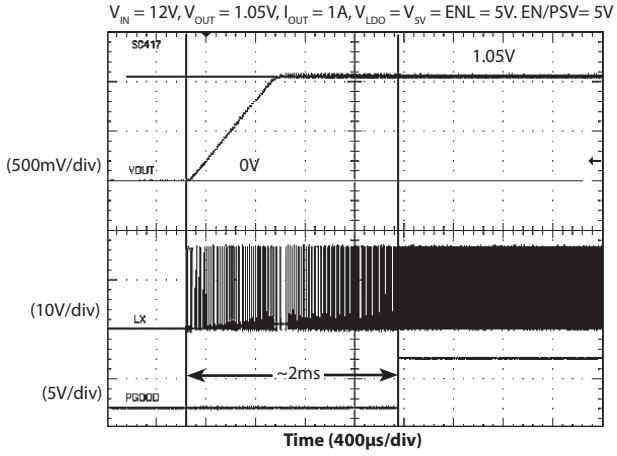
Forced Continuous Mode — No Load



Enabled Loaded Output — Full Scale



Enabled Loaded Output — Power Good True

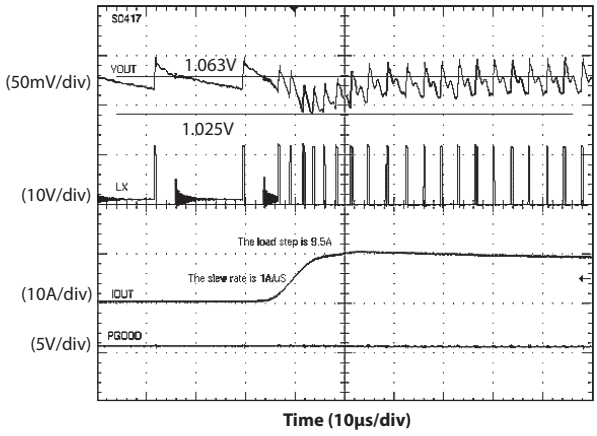


Typical Characteristics (continued)

Characteristics in this section are based on using the Typical Application Circuit on page 2 (SC417).

Transient Response — Load Rising

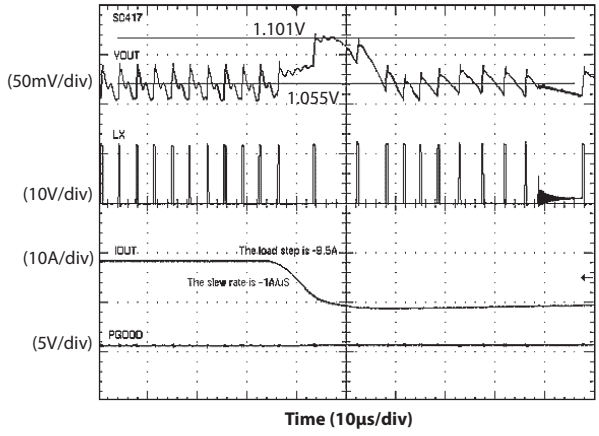
V_{IN} = 12V, V_{OUT} = 1.05V, I_{OUT} = 0A to 10A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V



Time (10µs/div)

Transient Response — Load Falling

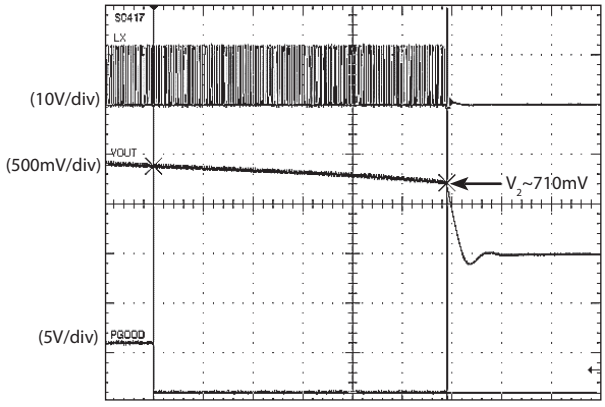
V_{IN} = 12V, V_{OUT} = 1.05V, I_{OUT} = 10A to 0A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V



Time (10µs/div)

Output Under-voltage Response — Normal Operation

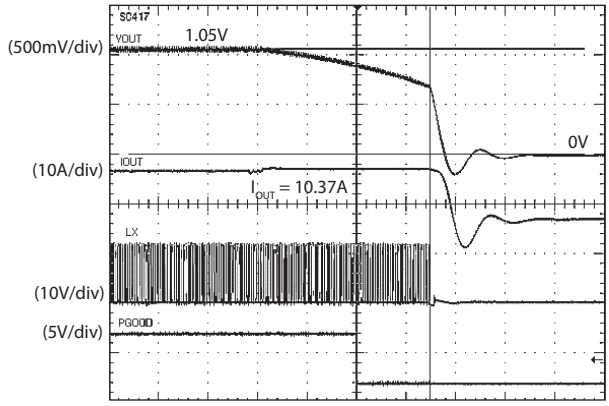
V_{IN} = 12V, V_{OUT} = 1.05V, I_{OUT} = 0A, V_{LDO} = V_{5V} = ENL = 5V, floating EN/PSV



Time (100µs/div)

Output Over-current Response — Normal Operation

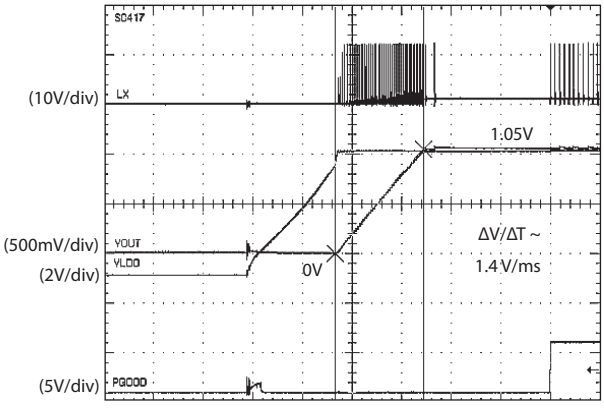
V_{IN} = 12V, V_{OUT} = 1.05V, V_{LDO} = V_{5V} = ENL = 5V, EN/PSV= floating; I_{OUT} ramped to trip point



Time (100µs/div)

Self-Biased Start-Up — Power Good True

V_{IN} = 0V to 12V step, V_{OUT} = 1.05V, I_{OUT} = 0A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V



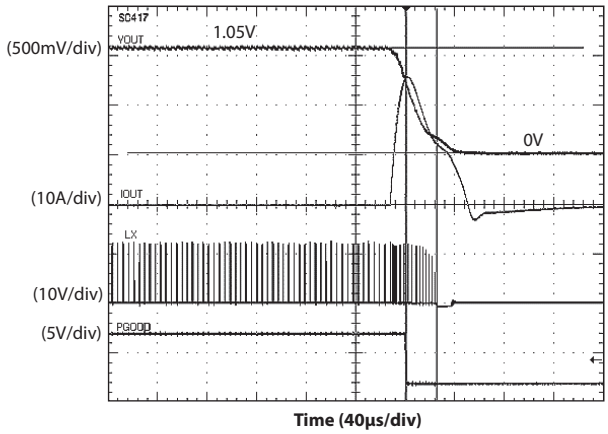
Time (400µs/div)

Typical Characteristics (continued)

Characteristics in this section are based on using the Typical Application Circuit on page 2.

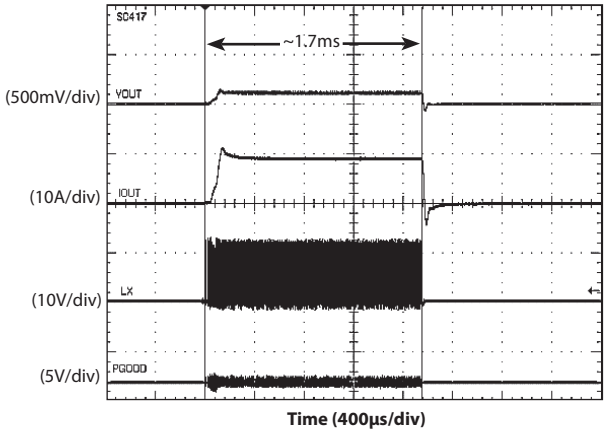
Shorted Output Response — Normal Operation

V_{IN} = 12V, V_{OUT} = 1.05V, I_{OUT} = 0A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V



Shorted Output Response — Power-UP Operation

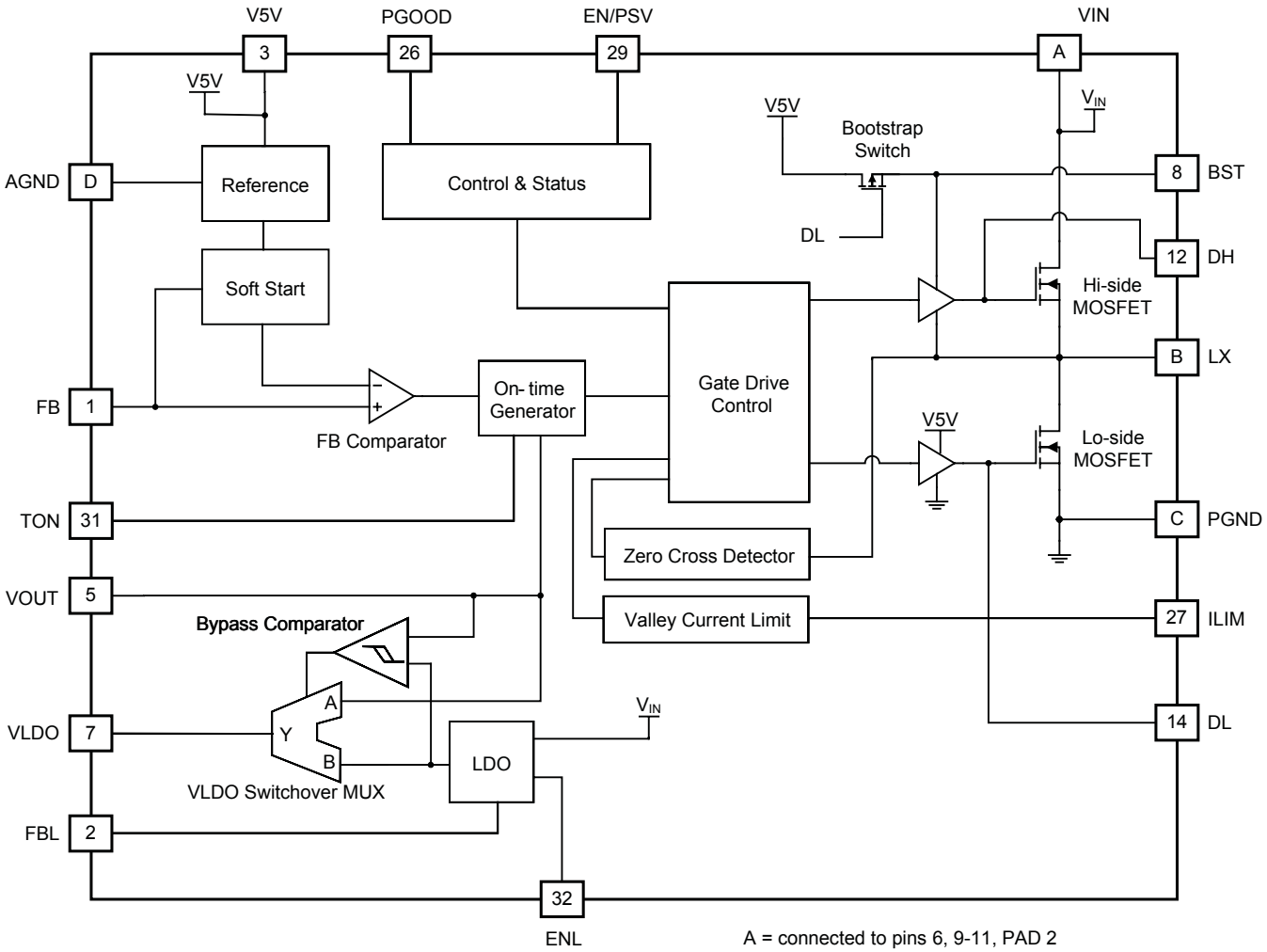
V_{IN} = 12V, V_{OUT} = 1.05V, I_{OUT} = 0A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V



Pin Descriptions

Pin #	Pin Name	Pin Function
1	FB	Feedback input for switching regulator used to program the output voltage — connect to an external resistor divider from VOUT to AGND.
2	FBL	Feedback input for the LDO — connect to an external resistor divider from VLDO to AGND — used to program the LDO output.
3	V5V	5V power input for internal analog circuits and gate drives — connect to external 5V supply or configure the LDO for 5V and connect to VLDO.
4, 30, PAD 1	AGND	Analog ground
5	VOUT	Switcher output voltage sense pin — also the input to the internal switch-over between VOUT and VLDO.
6, 9-11, PAD 2	VIN	Input supply voltage
7	VLDO	LDO output
8	BST	Bootstrap pin — connect a capacitor from BST to LX to develop the floating supply for the high-side gate drive.
12	DH	High-side gate drive — do not connect this pin
13, 23-25, 28, PAD 3	LX	Switching (phase) node
14	DL	Low-side gate drive — do not connect this pin
15-22	PGND	Power ground
26	PGOOD	Open-drain power good indicator — high impedance indicates power is good. An external pull-up resistor is required.
27	ILIM	Current limit sense pin — used to program the current limit by connecting a resistor from ILIM to LX.
29	EN/PSV	Enable/power-save input for the switching regulator — connect to AGND to disable the switching regulator. Float to operate in forced continuous mode (power-save disabled). SC417 — connect to V5V to operate with ultra-sonic power-save mode enabled. SC427 — connect to V5V to operate with power-save mode enabled with no minimum frequency.
31	TON	On-time programming input — set the on-time by connecting through a resistor to AGND
32	ENL	Enable input for the LDO — connect ENL to AGND to disable the LDO. Drive with logic to +3V for logic control, or program the VIN UVLO with a resistor divider between VIN, ENL, and AGND.

Block Diagram



A = connected to pins 6, 9-11, PAD 2
B = connected to pins 13, 23-25, 28, PAD 3
C = connected to pins 15-22
D = connect to pins 4, 30, PAD 1

Applications Information

Synchronous Buck Converter

The SC417/SC427 is a step down synchronous DC-DC buck converter with integrated power MOSFETs and a programmable LDO. The device is capable of 10A operation at very high efficiency. A space saving 5x5 (mm) 32-pin package is used. The programmable operating frequency range of 200kHz to 1MHz enables optimizing the configuration for PCB area and efficiency.

The buck controller uses a pseudo-fixed frequency adaptive on-time control. This control method allows fast transient response which permits the use of smaller output capacitors.

Input Voltage Requirements

The SC417/SC427 requires two input supplies for normal operation: VIN and V5V. VIN operates over the wide range from 3V to 28V. V5V requires a 5V supply input that can be an external source or the internal LDO configured to supply 5V.

Psuedo-fixed Frequency Adaptive On-time Control

The PWM control method used by the SC417/SC427 is pseudo-fixed frequency, adaptive on-time, as shown in Figure 1. The ripple voltage generated at the output capacitor ESR is used as a PWM ramp signal. This ripple is used to trigger the on-time of the controller.

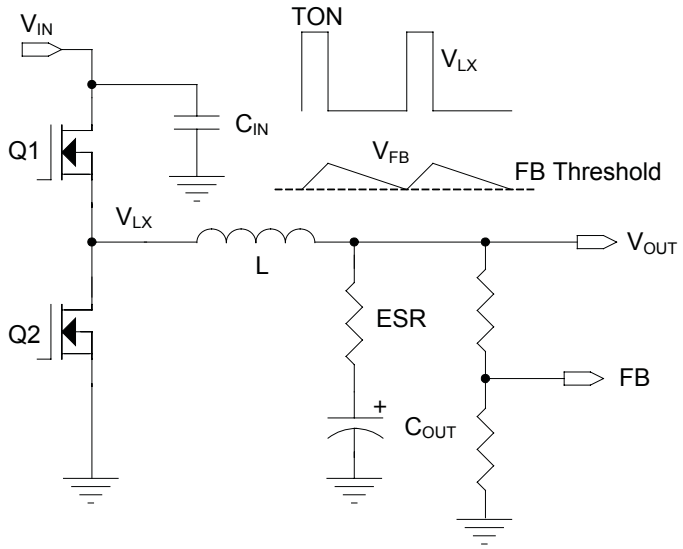


Figure 1 — PWM Control Method, V_{OUT} Ripple

The adaptive on-time is determined by an internal one-shot timer. When the one-shot is triggered by the output ripple, the device sends a single on-time pulse to the high-side MOSFET. The pulse period is determined by V_{OUT} and V_{IN}; the period is proportional to output voltage and inversely proportional to input voltage. With this adaptive on-time arrangement, the device automatically anticipates the on-time needed to regulate V_{OUT} for the present V_{IN} condition and at the selected frequency.

The advantages of adaptive on-time control are:

- Predictable operating frequency compared to other variable frequency methods.
- Reduced component count by eliminating the error amplifier and compensation components.
- Reduced component count by removing the need to sense and control inductor current.
- Fast transient response — the response time is controlled by a fast comparator instead of a typically slow error amplifier.
- Reduced output capacitance due to fast transient response

One-Shot Timer and Operating Frequency

The one-shot timer operates as shown in Figure 2. The FB Comparator output goes high when V_{FB} is less than the internal 500mV reference. This feeds into the gate drive and turns on the high-side MOSFET, and also starts the one-shot timer. The one-shot timer uses an internal comparator and a capacitor. One comparator input is connected to V_{OUT}, the other input is connected to the capacitor. When the on-time begins, the internal capacitor charges from zero volts through a current which is proportional to V_{IN}. When the capacitor voltage reaches V_{OUT}, the on-time is completed and the high-side MOSFET turns off.

Applications Information (continued)

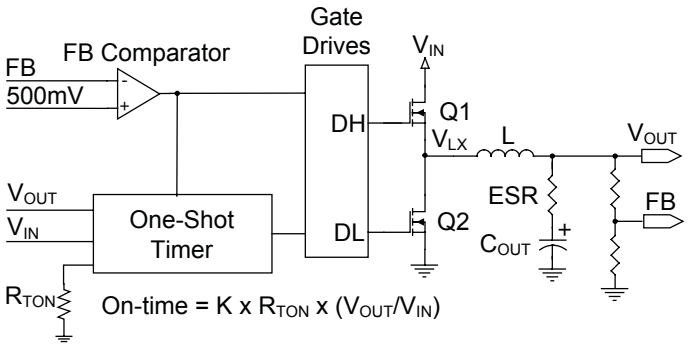


Figure 2 — On-Time Generation

This method automatically produces an on-time that is proportional to V_{OUT} and inversely proportional to V_{IN}. Under steady-state conditions, the switching frequency can be determined from the on-time by the following equation.

$$f_{SW} = \frac{V_{OUT}}{T_{ON} \times V_{IN}}$$

The SC417/SC427 uses an external resistor to set the on-time which indirectly sets the frequency. The on-time can be programmed to provide operating frequency from 200kHz to 1MHz using a resistor between the TON pin and ground. The resistor value is selected by the following equation.

$$R_{TON} = \frac{(TON - 10ns) \times V_{IN}}{25pF \times V_{OUT}}$$

The maximum R_{TON} value allowed is shown by the following equation.

$$R_{TON\_MAX} = \frac{V_{IN\_MIN}}{15\mu A}$$

V_{OUT} Voltage Selection

The switcher output voltage is regulated by comparing V_{OUT} as seen through a resistor divider at the FB pin to the internal 500mV reference voltage, see Figure 3.

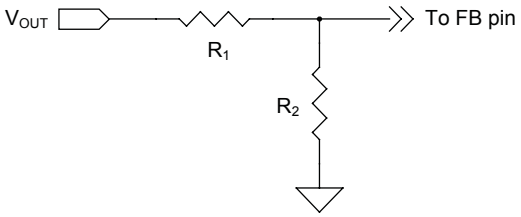


Figure 3 — Output Voltage Selection

Note that this control method regulates the valley of the output ripple voltage, not the DC value. The DC output voltage V_{OUT} is offset by the output ripple according to the following equation.

$$V_{OUT} = 0.5 \times \left(1 + \frac{R_1}{R_2}\right) + \left(\frac{V_{RIPPLE}}{2}\right)$$

Enable and Power-save Inputs

The EN/PSV and ENL inputs are used to enable or disable the switching regulator and the LDO. When EN/PSV is low (grounded), the switching regulator is off and in its lowest power state. When off, the output of the switching regulator soft-discharges the output into a 15Ω internal resistor via the V_{OUT} pin. When EN/PSV is allowed to float, the pin voltage will float to 1.5V. The switching regulator turns on with power-save disabled and all switching is in forced continuous mode.

When EN/PSV is high (above 2.0V) for SC417, the switching regulator turns on with ultra-sonic power-save enabled. The SC417 ultra-sonic power-save operation maintains a minimum switching frequency of 25kHz, for applications with stringent audio requirements.

When EN/PSV is high (above 2.0V) for SC427, the switching regulator turns on with power-save enabled. The SC427 power-save operation is designed to maximize efficiency at light loads with no minimum frequency limits. This makes the SC427 an excellent choice for portable and battery-operated systems.

The ENL input is used to control the internal LDO. This input serves a second function by acting as a V_{IN} ULVO sensor for the switching regulator.

When ENL is low (grounded), the LDO is off. When ENL is a logic high but below the VIN UVLO threshold (2.6V typical), then the LDO is on and the switcher is off. When ENL is above the VIN UVLO threshold, the LDO is enabled and the switcher is also enabled if the EN/PSV pin is not grounded.

Forced Continuous Mode Operation

The SC417/SC427 operates the switcher in Forced Continuous Mode (FCM) by floating the EN/PSV pin (see Figure 4). In this mode one of the power MOSFETs is

Applications Information (continued)

always on, with no intentional dead time other than to avoid cross-conduction. This feature results in uniform frequency across the full load range with the trade-off being poor efficiency at light loads due to the high-frequency switching of the MOSFETs.

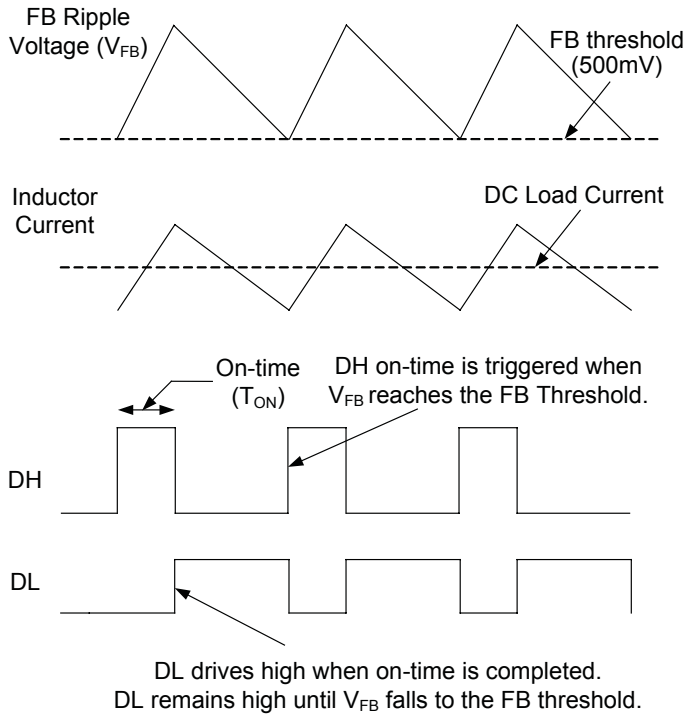


Figure 4 — Forced Continuous Mode Operation

Ultra-sonic Power-save Operation (SC417)

The SC417 provides ultra-sonic power-save operation at light loads, with the minimum operating frequency fixed at 25kHz. This is accomplished using an internal timer that monitors the time between consecutive high-side gate pulses. If the time exceeds 40µs, DL drives high to turn the low-side MOSFET on. This draws current from V_{OUT} through the inductor, forcing both V_{OUT} and V_{FB} to fall. When V_{FB} drops to the 500mV threshold, the next DH on-time is triggered. After the on-time is completed the high-side MOSFET is turned off and the low-side MOSFET turns on. The low-side MOSFET remains on until the inductor current ramps down to zero, at which point the low-side MOSFET is turned off.

Because the on-times are forced to occur at intervals no greater than 40µs, the frequency will not fall below ~25kHz. Figure 5 shows ultra-sonic power-save operation.

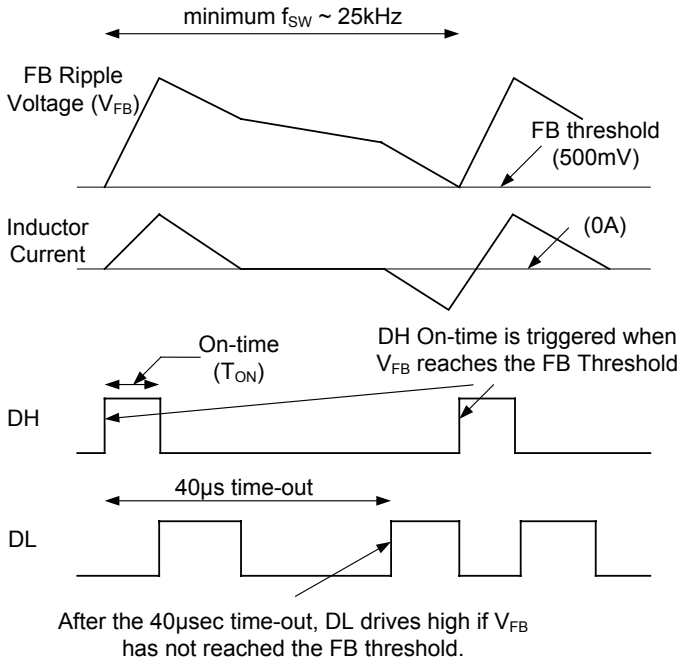


Figure 5 — Ultrasonic Power-save Operation

Power-save Mode Operation (SC427)

The SC427 provides power-save operation at light loads with no minimum operating frequency. With power-save enabled, the internal zero crossing comparator monitors the inductor current via the voltage across the low-side MOSFET during the off-time. If the inductor current falls to zero for 8 consecutive switching cycles, the controller enters power-save operation. It will turn off the low-side MOSFET on each subsequent cycle provided that the current crosses zero. At this time both MOSFETs remain off until V_{FB} drops to the 500mV threshold. Because the MOSFETs are off, the load is supplied by the output capacitor. If the inductor current does not reach zero on any switching cycle, the controller immediately exits power-save and returns to forced continuous mode. Figure 6 shows power-save operation at light loads.

Applications Information (continued)

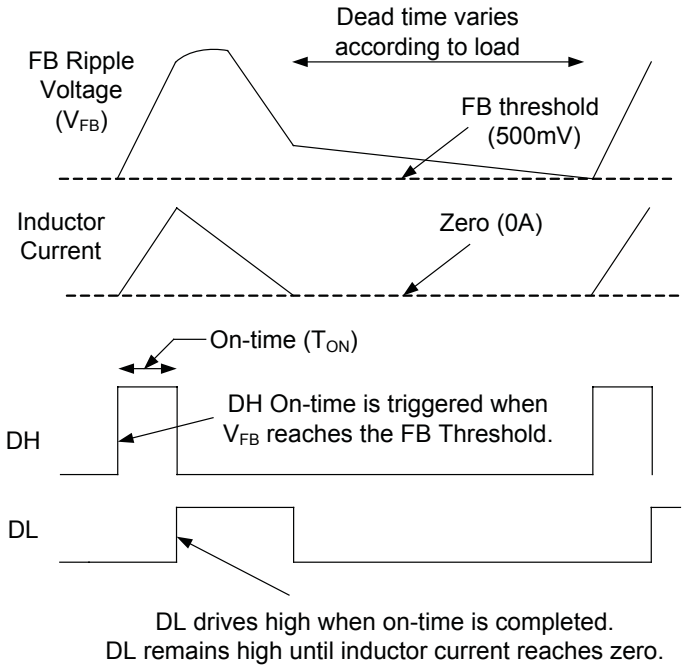


Figure 6 — Power-save Operation

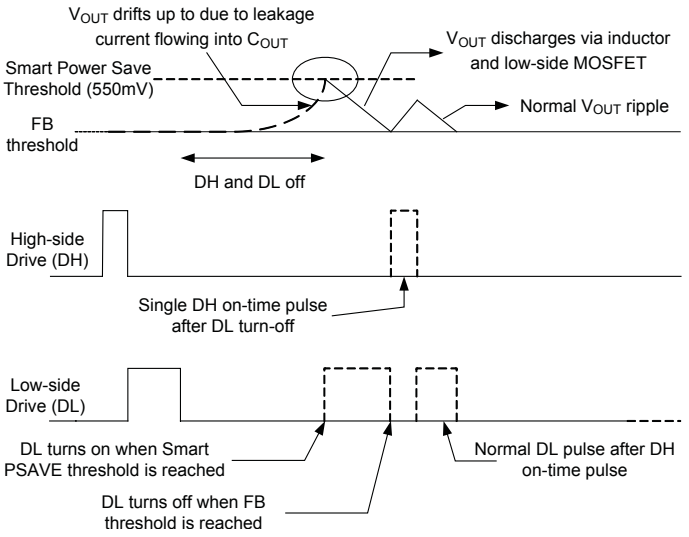


Figure 7 — Smart Power-save

Smart Power-save Protection

Active loads may leak current from a higher voltage into the switcher output. Under light load conditions with power-save enabled, this can force V_{OUT} to slowly rise and reach the over-voltage threshold, resulting in a hard shut-down. Smart power-save prevents this condition. When the FB voltage exceeds 10% above nominal (exceeds 550mV), the device immediately disables power-save, and DL drives high to turn on the low-side MOSFET. This draws current from V_{OUT} through the inductor and causes V_{OUT} to fall. When V_{FB} drops back to the 500mV trip point, a normal T_{ON} switching cycle begins. This method prevents a hard OVP shutdown and also cycles energy from V_{OUT} back to V_{IN}. It also minimizes operating power by avoiding forced conduction mode operation. Figure 7 shows typical waveforms for the Smart Power-save feature.

Current Limit Protection

The device features programmable current limiting, which is accomplished by using the RDSON of the lower MOSFET for current sensing. The current limit is set by R_{ILIM} resistor. The R_{ILIM} resistor connects from the ILIM pin to the LX pin which is also the drain of the low-side MOSFET. When the low-side MOSFET is on, an internal ~10µA current flows from the ILIM pin and through the R_{ILIM} resistor, creating a voltage drop across the resistor. While the low-side MOSFET is on, the inductor current flows through it and creates a voltage across the $RDS_{(ON)}$. The voltage across the MOSFET is negative with respect to ground. If this MOSFET voltage drop exceeds the voltage across R_{ILIM}, the voltage at the ILIM pin will be negative and current limit will activate. The current limit then keeps the low-side MOSFET on and will not allow another high-side on-time, until the current in the low-side MOSFET reduces enough to bring the ILIM voltage back up to zero. This method regulates the inductor valley current at the level shown by ILIM in Figure 8.

Applications Information (continued)

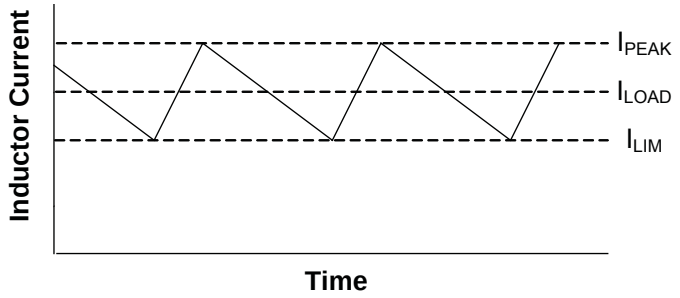


Figure 8 — Valley Current Limit

Setting the valley current limit to 10A results in a peak inductor current of 10A plus peak ripple current. In this situation, the average (load) current through the inductor is 10A plus one-half the peak-to-peak ripple current.

The internal 10µA current source is temperature compensated at 4100ppm in order to provide tracking with the $RDS_{(ON)}$.

The R_{ILIM} value is calculated by the following equation.

$$R_{ILIM} = 735 \times I_{LIM}$$

Note that because the low-side MOSFET with low $RDS_{(ON)}$ is used for current sensing, the PCB layout, solder connections, and PCB connection to the LX node must be done carefully to obtain good results. Refer to the layout guidelines for information.

Soft-Start of PWM Regulator

Soft-start is achieved in the PWM regulator by using an internal voltage ramp as the reference for the FB Comparator. The voltage ramp is generated using an internal charge pump which drives the reference from zero to 500mV in ~1.2mV increments, using an internal ~500kHz oscillator. When the ramp voltage reaches 500mV, the ramp is ignored and the FB comparator switches over to a fixed 500mV threshold. During soft-start the output voltage tracks the internal ramp, which limits the start-up inrush current and provides a controlled soft-start profile for a wide range of applications. Typical soft-start ramp time is 850µs.

During soft-start the regulator turns off the low-side MOSFET on any cycle if the inductor current falls to zero. This prevents negative inductor current, allowing the device to start into a pre-biased output.

Power Good Output

The power good (PGOOD) output is an open-drain output which requires a pull-up resistor. When the output voltage is 10% below the nominal voltage, PGOOD is pulled low. It is held low until the output voltage returns above -8% of nominal. PGOOD is held low during start-up and will not be allowed to transition high until soft-start is completed (when V_{FB} reaches 500mV) and typically 2ms has passed.

PGOOD will transition low if the V_{FB} pin exceeds +20% of nominal, which is also the over-voltage shutdown threshold (600mV). PGOOD also pulls low if the EN/PSV pin is low when V5V is present.

Output Over-Voltage Protection

Over-voltage protection becomes active as soon as the device is enabled. The threshold is set at 500mV + 20% (600mV). When V_{FB} exceeds the OVP threshold, DL latches high and the low-side MOSFET is turned on. DL remains high and the controller remains off, until the EN/PSV input is toggled or V5V is cycled. There is a 5µs delay built into the OVP detector to prevent false transitions. PGOOD is also low after an OVP event.

Output Under-Voltage Protection

When V_{FB} falls 25% below its nominal voltage (falls to 375mV) for eight consecutive clock cycles, the switcher is shut off and the DH and DL drives are pulled low to tri-state the MOSFETs. The controller stays off until EN/PSV is toggled or V5V is cycled.

V5V UVLO, and POR

Under-Voltage Lock-Out (UVLO) circuitry inhibits switching and tri-states the DH/DL drivers until V5V rises above 3.9V. An internal Power-On Reset (POR) occurs when V5V exceeds 3.9V, which resets the fault latch and soft-start counter to prepare for soft-start. The SC417/SC427 then begins a soft-start cycle. The PWM will shut off if V5V falls below 3.6V.

LDO Regulator

The device features an integrated LDO regulator with a programmable output voltage from 0.75V to 5.25V using

Applications Information (continued)

external resistors. The feedback pin (FBL) for the LDO is regulated to 750mV. There is also an enable pin (ENL) for the LDO that provides independent control. The LDO voltage can also be used to provide the bias voltage for the switching regulator.

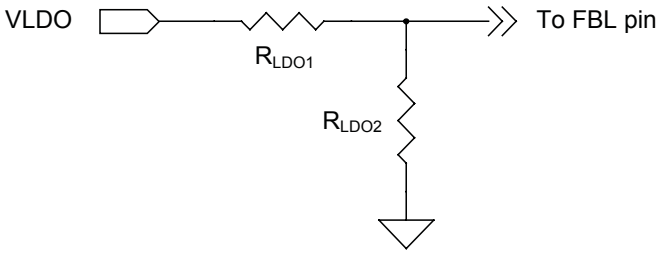


Figure 9 — LDO Start-Up

The LDO output voltage is set by the following equation.

$$VLDO = 750mV \times \left(1 + \frac{R_{LDO1}}{R_{LDO2}}\right)$$

A minimum capacitance of 1µF referenced to AGND is normally required at the output of the LDO for stability. If the LDO is providing bias power to the device, then a minimum 0.1µF capacitor referenced to AGND is required along with a minimum 1.0µF capacitor referenced to PGND to filter the gate drive pulses. Refer to the layout guidelines section.

LDO Start-up

Before start-up, the LDO checks the status of the following signals to ensure proper operation can be maintained.

1. ENL pin
2. VLDO output
3. V_{IN} input voltage

When the ENL pin is high and V_{IN} is above the UVLO point, the LDO will begin start-up. During the initial phase, when the LDO output voltage is near zero, the LDO initiates a current-limited start-up (typically 85mA) to charge the output capacitor. When V_{LDO} has reached 90% of the final value (as sensed at the FBL pin), the LDO current limit is increased to ~200mA and the LDO output is quickly driven to the nominal value by the internal LDO regulator.

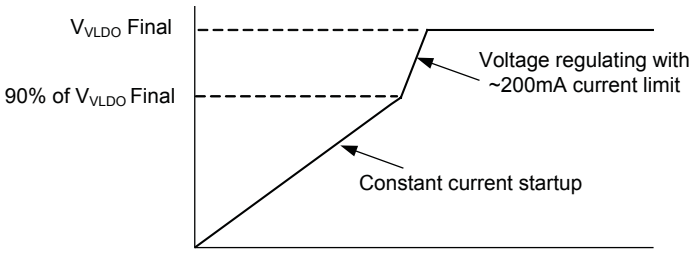


Figure 10 — LDO Start-Up

LDO Switch-Over Operation

The SC417/SC427 includes a switch-over function for the LDO. The switch-over function is designed to increase efficiency by using the more efficient DC-DC converter to power the LDO output, avoiding the less efficient LDO regulator when possible. The switch-over function connects the VLDO pin directly to the VOUT pin using an internal switch. When the switch-over is complete the LDO is turned off, which results in a power savings and maximizes efficiency. If the LDO output is used to bias the SC417/SC427, then after switch-over the device is self-powered from the switching regulator with the LDO turned off.

The switch-over logic waits for 32 switching cycles before it starts the switch-over. There are two methods that determine the switch-over of V_{LDO} to V_{OUT}.

In the first method, the LDO is already in regulation and the DC-DC converter is later enabled. As soon as the PGOOD output goes high, the 32 cycles are started. The voltages at the VLDO and VOUT pins are then compared; if the two voltages are within ±300mV of each other, the VLDO pin connects to the VOUT pin using an internal switch, and the LDO is turned off.

In the second method, the DC-DC converter is already running and the LDO is enabled. In this case the 32 cycles are started as soon as the LDO reaches 90% of its final value. At this time, the VLDO and VOUT pins are compared, and if within ±300mV the switch-over occurs and the LDO is turned off.

Applications Information (continued)

Switch-over Limitations on VOUT and VLDO

Because the internal switch-over circuit always compares the VOUT and VLDO pins at start-up, there are limitations on permissible combinations of VOUT and VLDO. Consider the case where VOUT is programmed to 1.5V and VLDO is programmed to 1.8V. After start-up, the device would connect VOUT to VLDO and disable the LDO, since the two voltage are within the ±300mV switch-over window. To avoid unwanted switch-over, the minimum difference between the voltages for VOUT and VLDO should be ±500mV.

It is not recommended to use the switch-over feature for an output voltage less than 3V since this does not provide sufficient voltage for the gate-source drive to the internal p-channel switch-over MOSFET.

Switch-over MOSFET Parasitic Diodes

The switch-over MOSFET contains parasitic diodes that are inherent to its construction, as shown in Figure 11.

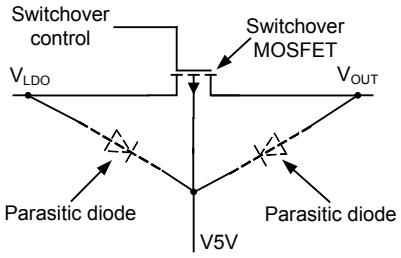


Figure 11— Switch-over MOSFET Parasitic Diodes

There are some important design rules that must be followed to prevent forward bias of these diodes. The following two conditions need to be satisfied in order for the parasitic diodes to stay off.

- $V5V \geq V_{LDO}$
- $V5V \geq V_{OUT}$

If either V_{LDO} or V_{OUT} is higher than V5V, then the respective diode will turn on and the SC417/SC427 operating current will flow through this diode. This has the potential of damaging the device.

ENL pin and VIN UVLO

The ENL pin also acts as the switcher under-voltage lockout for the V_{IN} supply. The V_{IN} UVLO voltage is programmable via a resistor divider at the VIN, ENL and AGND pins.

ENL is the enable/disable signal for the LDO. In order to implement the VIN UVLO there is also a timing requirement that needs to be satisfied.

If the ENL pin transitions low within 2 switching cycles and is < 1V, then the LDO will turn off but the switcher remains on. If ENL goes below the VIN UVLO threshold and stays above 1V, then the switcher will turn off but the LDO remains on.

The VIN UVLO function has a typical threshold of 2.6V on the VIN rising edge. The falling edge threshold is 2.4V.

Note that it is possible to operate the switcher with the LDO disabled, but the ENL pin must be below the logic low threshold (0.4V maximum).

ENL Logic Control of PWM Operation

When the ENL input is driven above 2.6V, it is impossible to determine if the LDO output is going to be used to power the device or not. In self-powered operation where the LDO will power the device, it is necessary during the LDO start-up to hold the PWM switching off until the LDO has reached 90% of the final value. This is to prevent overloading the current-limited LDO output during the LDO start-up. However, if the switcher was previously operating (with EN/PSV high but ENL at ground, and V5V supplied externally), then it is undesirable to shut down the switcher.

To prevent this, when the ENL input is taken above 2.6V (above the VIN UVLO threshold), the internal logic checks the PGOOD signal. If PGOOD is high, then the switcher is already running and the LDO will run through the start-up cycle without affecting the switcher. If PGOOD is low, then the LDO will not allow any PWM switching until the LDO output has reached 90% of it's final value.

SEMTECH

Applications Information (continued)

Using the On-chip LDO to Bias the SC417/SC427

The following steps must be followed when using the on-chip LDO to bias the device.

- Connect V5V to VLDO before enabling the LDO.
- The LDO has an initial current limit of 40mA at start-up, therefore, do not connect any external load to VLDO during start-up.
- When VLDO reaches 90% of its final value, the LDO current limit increases to 200mA. At this time the LDO may be used to supply the required bias current to the device.

Attempting to operate in self-powered mode in any other configuration can cause unpredictable results and may damage the device.

Design Procedure

When designing a switch mode supply the input voltage range, load current, switching frequency, and inductor ripple current must be specified.

The maximum input voltage (V_{INMAX}) is the highest specified input voltage. The minimum input voltage (V_{INMIN}) is determined by the lowest input voltage after evaluating the voltage drops due to connectors, fuses, switches, and PCB traces.

The following parameters define the design.

- Nominal output voltage (V_{OUT})
- Static or DC output tolerance
- Transient response
- Maximum load current (I_{OUT})

There are two values of load current to evaluate — continuous load current and peak load current. Continuous load current relates to thermal stresses which drive the selection of the inductor and input capacitors. Peak load current determines instantaneous component stresses and filtering requirements such as inductor saturation, output capacitors, and design of the current limit circuit.

The following values are used in this design.

- V_{IN} = 12V ± 10%
- V_{OUT} = 1.05V ± 4%
- f_{SW} = 250kHz
- Load = 10A maximum

Frequency Selection

Selection of the switching frequency requires making a trade-off between the size and cost of the external filter components (inductor and output capacitor) and the power conversion efficiency.

The desired switching frequency is 250kHz which results from using component selected for optimum size and cost .

A resistor (R_{TON}) is used to program the on-time (indirectly setting the frequency) using the following equation.

$$R_{TON} = \frac{(T_{ON} - 10ns) \times V_{IN}}{25pF \times V_{OUT}}$$

To select R_{TON}, use the maximum value for V_{IN}, and for T_{ON} use the value associated with maximum V_{IN}.

$$T_{ON} = \frac{V_{OUT}}{V_{INMAX} \times f_{SW}}$$

T_{ON} = 318 ns at 13.2V_{IN}, 1.05V_{OUT}, 250kHz

Substituting for R_{TON} results in the following solution.

R_{TON} = 154.9kΩ, use R_{TON} = 154kΩ

Inductor Selection

In order to determine the inductance, the ripple current must first be defined. Low inductor values result in smaller size but create higher ripple current which can reduce efficiency. Higher inductor values will reduce the ripple current/voltage and for a given DC resistance are more efficient. However, larger inductance translates directly into larger packages and higher cost. Cost, size, output ripple, and efficiency are all used in the selection process.

The ripple current will also set the boundary for power-save operation. The switching will typically enter power-save mode when the load current decreases to 1/2 of the ripple current. For example, if ripple current is 4A then Power-save operation will typically start for loads less than 2A. If ripple current is set at 40% of maximum load current, then power-save will start for loads less than 20% of maximum current.

Applications Information (continued)

The inductor value is typically selected to provide a ripple current that is between 25% to 50% of the maximum load current. This provides an optimal trade-off between cost, efficiency, and transient performance.

During the DH on-time, voltage across the inductor is (V_{IN} - V_{OUT}). The equation for determining inductance is shown next.

$$L = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{I_{RIPPLE}}$$

Example

In this example, the inductor ripple current is set equal to 50% of the maximum load current. Thus ripple current will be 50% x 10A or 5A. To find the minimum inductance needed, use the V_{IN} and T_{ON} values that correspond to V_{INMAX}.

$$L = \frac{(13.2 - 1.05) \times 318ns}{5A} = 0.77\mu H$$

A slightly larger value of 0.88µH is selected. This will decrease the maximum I_{RIPPLE} to 4.4A.

Note that the inductor must be rated for the maximum DC load current plus 1/2 of the ripple current.

The ripple current under minimum V_{IN} conditions is also checked using the following equations.

$$T_{ON\_VINMIN} = \frac{25pF \times R_{TON} \times V_{OUT}}{V_{INMIN}} + 10ns = 384ns$$

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{L}$$

$$I_{RIPPLE\_VIN} = \frac{(10.8 - 1.05) \times 384ns}{0.88\mu H} = 4.25A$$

Capacitor Selection

The output capacitors are chosen based on required ESR and capacitance. The maximum ESR requirement is controlled by the output ripple requirement and the DC tolerance. The output voltage has a DC value that is equal to the valley of the output ripple plus 1/2 of the peak-to-peak ripple. Change in the output ripple voltage will lead to a change in DC voltage at the output.

The design goal is that the output voltage regulation be ±4% under static conditions. The internal 500mV reference tolerance is 1%. Allowing 1% tolerance from the FB resistor divider, this allows 2% tolerance due to V_{OUT} ripple. Since this 2% error comes from 1/2 of the ripple voltage, the allowable ripple is 4%, or 42mV for a 1.05V output.

The maximum ripple current of 4.4A creates a ripple voltage across the ESR. The maximum ESR value allowed is shown by the following equations.

$$ESR_{MAX} = \frac{V_{RIPPLE}}{I_{RIPPLEMAX}} = \frac{42mV}{4.4A}$$

$$ESR_{MAX} = 9.5\ m\Omega$$

The output capacitance is usually chosen to meet transient requirements. A worst-case load release, from maximum load to no load at the exact moment when inductor current is at the peak, determines the required capacitance. If the load release is instantaneous (load changes from maximum to zero in < 1µs), the output capacitor must absorb all the inductor's stored energy. This will cause a peak voltage on the capacitor according to the following equation.

$$COUT_{MIN} = \frac{L\left(I_{OUT} + \frac{1}{2} \times I_{RIPPLEMAX}\right)^2}{(V_{PEAK})^2 - (V_{OUT})^2}$$

Assuming a peak voltage V_{PEAK} of 1.150 (100mV rise upon load release), and a 10A load release, the required capacitance is shown by the next equation.

$$COUT_{MIN} = \frac{0.88\mu H\left(10 + \frac{1}{2} \times 4.4\right)^2}{(1.15)^2 - (1.05)^2}$$

$$COUT_{MIN} = 595\mu F$$

If the load release is relatively slow, the output capacitance can be reduced. At heavy loads during normal switching, when the FB pin is above the 500mV reference, the DL output is high and the low-side MOSFET is on. During this time, the voltage across the inductor is approximately -V_{OUT}. This causes a down-slope or falling di/dt in the

Applications Information (continued)

inductor. If the load di/dt is not much faster than the -di/dt in the inductor, then the inductor current will tend to track the falling load current. This will reduce the excess inductive energy that must be absorbed by the output capacitor, therefore a smaller capacitance can be used.

The following can be used to calculate the needed capacitance for a given dI_{LOAD}/dt:

Peak inductor current is shown by the next equation.

$$I_{LPK} = I_{MAX} + 1/2 \times I_{RIPPLEMAX}$$

$$I_{LPK} = 10 + 1/2 \times 4.4 = 12.2A$$

$$\text{Rate of change of Load Current} = \frac{dI_{LOAD}}{dt}$$

I_{MAX} = maximum load release = 10A

$$C_{OUT} = I_{LPK} \times \frac{L \times \frac{I_{LPK}}{V_{OUT}} - \frac{I_{MAX}}{dI_{LOAD}} \times dt}{2(V_{PK} - V_{OUT})}$$

Example

$$\text{Load}\frac{dI_{LOAD}}{dt} = \frac{2.5A}{\mu s}$$

This would cause the output current to move from 10A to zero in 4µs as shown by the following equation.

$$C_{OUT} = 12.2 \times \frac{0.88\mu H \times \frac{12.2}{1.05} - \frac{10}{2.5} \times 1\mu s}{2(1.15 - 1.05)}$$

$$C_{OUT} = 379\ \mu F$$

Note that C_{OUT} is much smaller in this example, 379µF compared to 595µF based on a worst-case load release. To meet the two design criteria of minimum 379µF and maximum 9mΩ ESR, select two capacitors rated at 220µF and 15mΩ ESR.

It is recommended that an additional small capacitor be placed in parallel with C_{OUT} in order to filter high frequency switching noise.

Stability Considerations

Unstable operation is possible with adaptive on-time controllers, and usually takes the form of double-pulsing or ESR loop instability.

Double-pulsing occurs due to switching noise seen at the FB input or because the FB ripple voltage is too low. This causes the FB comparator to trigger prematurely after the 250ns minimum off-time has expired. In extreme cases the noise can cause three or more successive on-times. Double-pulsing will result in higher ripple voltage at the output, but in most applications it will not affect operation. This form of instability can usually be avoided by providing the FB pin with a smooth, clean ripple signal that is at least 10mVp-p, which may dictate the need to increase the ESR of the output capacitors. It is also imperative to provide a proper PCB layout as discussed in the Layout Guidelines section.

Another way to eliminate doubling-pulsing is to add a small (~ 10pF) capacitor across the upper feedback resistor, as shown in Figure 13. This capacitor should be left unpopulated until it can be confirmed that double-pulsing exists. Adding the C_{TOP} capacitor will couple more ripple into FB to help eliminate the problem. An optional connection on the PCB should be available for this capacitor.

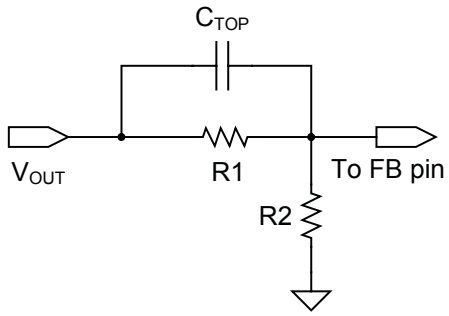


Figure 13 — Capacitor Coupling to FB Pin

ESR loop instability is caused by insufficient ESR. The details of this stability issue are discussed in the ESR Requirements section. The best method for checking stability is to apply a zero-to-full load transient and observe the output voltage ripple envelope for overshoot and ringing. Ringing for more than one cycle after the initial step is an indication that the ESR should be increased.

Applications Information (continued)

One simple way to solve this problem is to add trace resistance in the high current output path. A side effect of adding trace resistance is output decreased load regulation.

ESR Requirements

A minimum ESR is required for two reasons. One reason is to generate enough output ripple voltage to provide 10mVp-p at the FB pin (after the resistor divider) to avoid double-pulsing.

The second reason is to prevent instability due to insufficient ESR. The on-time control regulates the valley of the output ripple voltage. This ripple voltage is the sum of the two voltages. One is the ripple generated by the ESR, the other is the ripple due to capacitive charging and discharging during the switching cycle. For most applications the minimum ESR ripple voltage is dominated by the output capacitors, typically SP or POSCAP devices. For stability the ESR zero of the output capacitor should be lower than approximately one-third the switching frequency. The formula for minimum ESR is shown by the following equation.

$$ESR_{MIN} = \frac{3}{2 \times \pi \times C_{OUT} \times f_{sw}}$$

For applications using ceramic output capacitors, the ESR is normally too small to meet the above ESR criteria. In these applications it is necessary to add a small virtual ESR network composed of two capacitors and one resistor, as shown in Figure 14. This network creates a ramp voltage across C_L, analogous to the ramp voltage generated across the ESR of a standard capacitor. This ramp is then capacitively coupled into the FB pin via capacitor C_C.

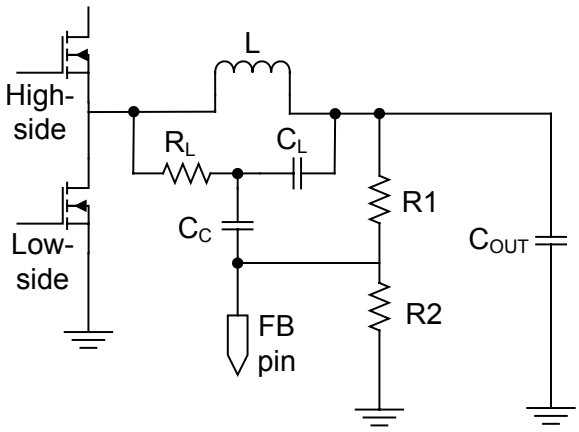


Figure 14 — Virtual ESR Ramp Current

Dropout Performance

The output voltage adjust range for continuous-conduction operation is limited by the fixed 250ns (typical) minimum off-time of the one-shot. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times.

The duty-factor limitation is shown by the next equation.

$$DUTY = \frac{T_{ON(MIN)}}{T_{ON(MIN)} + T_{OFF(MAX)}}$$

The inductor resistance and MOSFET on-state voltage drops must be included when performing worst-case dropout duty-factor calculations.

System DC Accuracy (V_{OUT} Controller)

Three factors affect V_{OUT} accuracy: the trip point of the FB error comparator, the ripple voltage variation with line and load, and the external resistor tolerance. The error comparator offset is trimmed so that under static conditions it trips when the feedback pin is 500mV, 1%.

The on-time pulse from the SC417/SC427 in the design example is calculated to give a pseudo-fixed frequency of

Applications Information (continued)

250kHz. Some frequency variation with line and load is expected. This variation changes the output ripple voltage. Because constant on-time converters regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, if the output ripple is 50mV with V_{IN} = 6 volts, then the measured DC output will be 25mV above the comparator trip point. If the ripple increases to 80mV with V_{IN} = 25V, then the measured DC output will be 40mV above the comparator trip. The best way to minimize this effect is to minimize the output ripple.

To compensate for valley regulation, it may be desirable to use passive droop. Take the feedback directly from the output side of the inductor and place a small amount of trace resistance between the inductor and output capacitor. This trace resistance should be optimized so that at full load the output droops to near the lower regulation limit. Passive droop minimizes the required output capacitance because the voltage excursions due to load steps are reduced as seen at the load.

The use of 1% feedback resistors contributes up to 1% error. If tighter DC accuracy is required, 0.1% resistors should be used.

The output inductor value may change with current. This will change the output ripple and therefore will have a minor effect on the DC output voltage. The output ESR also affects the output ripple and thus has a minor effect on the DC output voltage.

Switching Frequency Variations

The switching frequency will vary depending on line and load conditions. The line variations are a result of fixed propagation delays in the on-time one-shot, as well as unavoidable delays in the external MOSFET switching. As V_{IN} increases, these factors make the actual DH on-time slightly longer than the ideal on-time. The net effect is that frequency tends to falls slightly with increasing input voltage.

The switching frequency also varies with load current as a result of the power losses in the MOSFETs and the inductor. For a conventional PWM constant-frequency converter, as load increases the duty cycle also increases slightly to compensate for IR and switching losses in the MOSFETs and inductor. A constant on-time converter must also compensate for the same losses by increasing the effective duty cycle (more time is spent drawing energy from V_{IN} as losses increase). The on-time is essentially constant for a given V_{OUT}/V_{IN} combination, to offset the losses the off-time will tend to reduce slightly as load increases. The net effect is that switching frequency increases slightly with increasing load.

Applications Information (continued)

PCB Layout Guidelines

The optimum layout for the SC417/SC427 is shown in Figure 15. The layout highlights the device as a space saving and high performance solution. This layout shows an integrated FET buck regulator with a maximum current of 10A. The total PCB area is approximately 20 x 25 mm.

This figure shows the total area and optimum layout for the device. If optimum layout is not possible due to PCB limitations, the following generic guidelines should be followed.

Generic Layout Guidelines

One or more ground planes are recommended to minimize the effect of switching noise, resistive losses, and to maximize heat removal. The analog ground reference AGND should connect directly to the AGND pad and pins. An AGND plane or island should be used near the device. All components that are referenced to AGND should connect directly to this plane and mounted on the IC side of the PCB.

AGND should connect to PGND (power ground) using an external zero ohm resistor or using a short PCB trace. Connect AGND to PGND only at one place, as near to the AGND and PGND pins as is practical.

Power ground (PGND) should be a separate plane which is not used for routing analog traces.

All PGND connections should connect directly to the PGND plane. Indirect connections between AGND and GND which will create ground loops should be avoided.

The V5V input provides power to the internal analog circuits and the upper and lower gate drivers. The V5V supply decoupling capacitors should be tied between V5V and PGND with short traces.

The switcher power section should be connected directly to the PGND plane(s) using multiple vias as required for

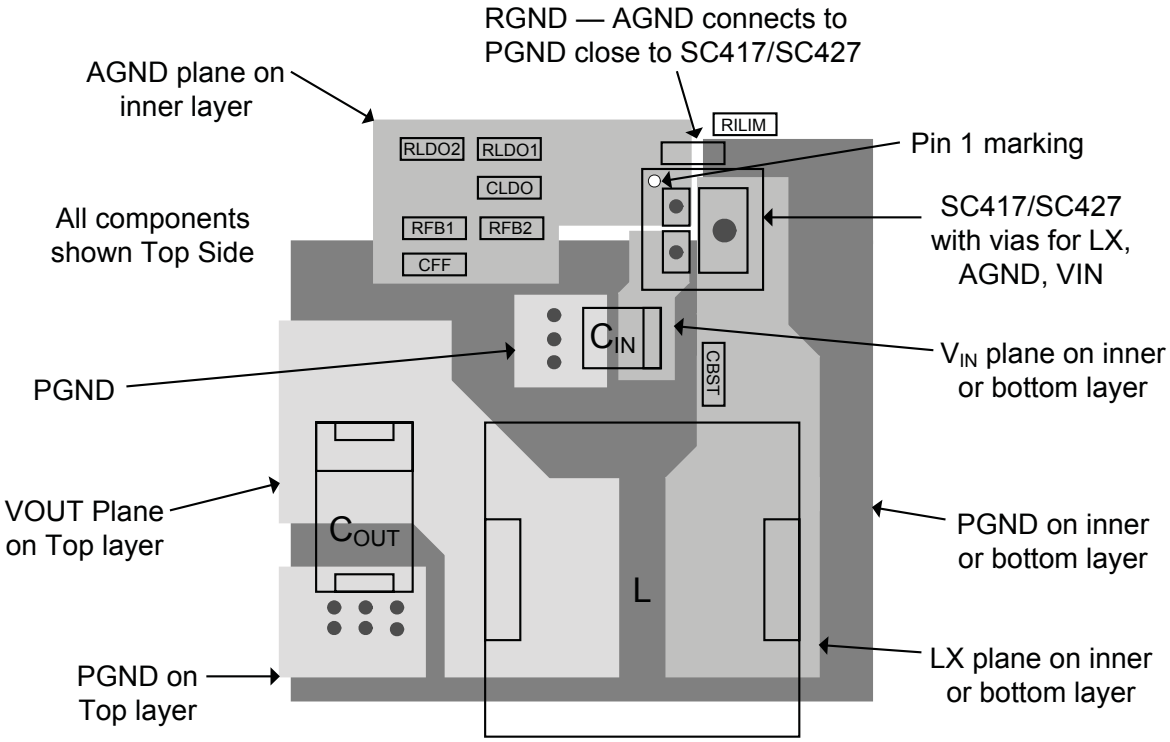


Figure 15 — PCB Layout

Applications Information (continued)

current handling (including the chip power ground connections). Power components should be placed to minimize current loops and reduce losses. Make all the power connections on one side of the PCB using wide copper areas if possible. Do not use minimum land patterns for power components.

Current Limit

Obtaining an accurate current limit for the SC417/SC427 requires careful PCB layout. The device uses the $RDS_{(ON)}$ of the low-side MOSFET for current sensing. The ILIM comparator that performs the current limit function monitors the ILIM pin with respect to AGND, but the low-side MOSFET is internally connected to PGND. The PCB layout needs to following these guidelines.

- AGND and PGND must be connected together directly at the pins of the IC and not anywhere else. This can be done through PCB copper or a zero ohm resistor. Keep the traces short and direct. The preferred connection for PGND is at pin 19. The preferred connection for AGND is at the PAD1.
- The PGND path from the device to the input and output capacitors requires a wide copper areas. Use multiple vias and copper areas if available. Do not break up these copper areas with intervening components. The goal is to minimize the IR drop between all PGND connections.
- Provide multiple vias and multiple copper areas between the LX pins and the inductor. The goal is to minimize any IR drop that might contributed to the $RDS_{(ON)}$. This is also good to carry heat away from the device.
- For the connection from the RLIM resistor to the LX node, use a direct Kelvin connection to pin 28 (LX), as near to the pin as possible. Do not connect to a place further in the copper between the LX pins and the inductor — the intervening copper will appear as increased $RDS_{(ON)}$ and will reduce the operating current limit.

The layout can be considered in two parts; the control section referenced to AGND, and the switcher power section referenced to GND.

Control Section

Locate all components referenced to AGND on the schematic and place these components near the device and on the same side if possible. Connect AGND to the AGND pad and pins using a plane or island if possible.

The device supply decoupling capacitor (V5V to PGND) should be located as close as possible to the pins. The V5V decoupling capacitor preferred placement is on the opposite side of the PCB. It should be routed with traces as short as possible, using at least two vias when connecting through the PCB.

There are two sensitive feedback-related pins at the device — VOUT and FB. Proper routing is essential to keep noise away from these signals. All components connected to FB should be located directly at the chip, and the copper area of the FB node must be minimized. The VOUT trace that feeds into the VOUT pin, which also feeds the FB resistor divider, must be kept as far away as possible from noise sources such as all switching signals (LX, DH, DL, BST) and the inductor. Route the VOUT trace in a quiet layer if possible, from the output capacitor back to the chip.

Power Section

The switcher power section key guidelines are as follows.

- There should be a very small input loop between the input capacitors, inductor, and output capacitors. Locate the input decoupling capacitors directly at the VIN pad on the device.
- The LX phase node should be a large enough to carry the required current. Careful sizing is required since this is the noisiest node.
- The PGND connection between the input capacitors, low-side MOSFET, and output capacitors should be as small as possible, with wide traces or planes and multiple vias.
- The impedance of the PGND connection between the low-side MOSFET and the PGND pin should be minimized. This connection must carry the DL drive current, which has high peaks at both rising and falling edges. Use multiple layers and multiple vias to minimize impedance and keep the distance as short as practical.

Applications Information (continued)

Connect the control and switcher power sections as follows.

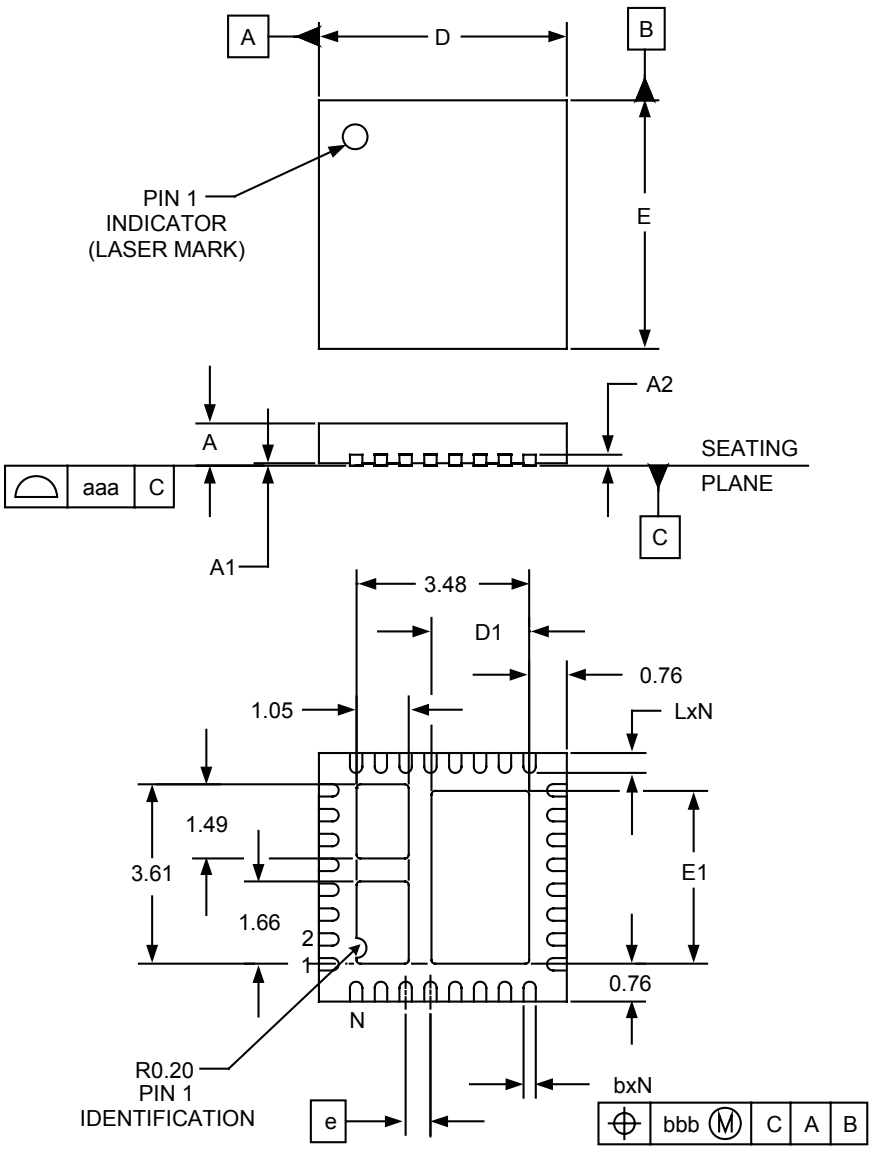
- Route the V_{OUT} feedback trace in a quiet layer, away from noise sources.
- BST is a noisy node and should be kept as short as possible. The high-side DH driver uses the boost capacitor to provide the DH drive current. The boost capacitor must be placed near the device and connected to the BST and LX pins using short, wide traces to minimize impedance.
- Connect the PGND pin on the chip to the V5V decoupling capacitor and then insert vias directly to the ground plane.

LDO Section

There are three components for the LDO that need to be optimized for this layout, the two feedback resistors and the output capacitor. Use the following guidelines to locate these components.

- The feedback resistors should be placed as close to the FBL pin as possible. This minimizes the trace length for the FBL pin.
- For the feedback divider connection, the top resistor must connect directly to the LDO output capacitor. There should be no PCB inductance between the top of the resistor divider and the LDO output capacitor.
- If VLDO is not used to power the device, then a minimum 1.0µF capacitor referenced to AGND is required.
- If VLDO is used to power-up the device by connecting it to V5V, then the LDO output capacitor also becomes the decoupling capacitor for the V5V input. A minimum 0.1µF capacitor referenced to AGND is required along with a minimum 1.0µF capacitor referenced to PGND to filter the gate drive pulses. Each capacitor should be placed near the V5V pin and connected with short, direct traces. Each capacitor should connect directly to its respective ground.

Outline Drawing — MLPQ-5x5-32

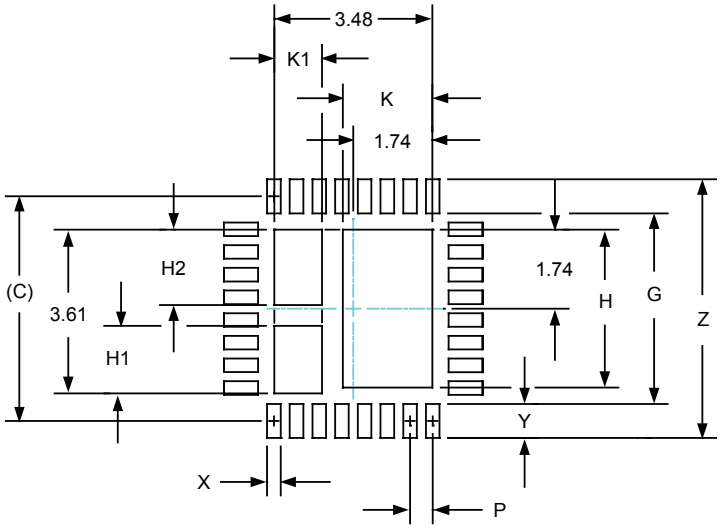


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.039	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.193	.197	.201	4.90	5.00	5.10
D1	.076	.078	.080	1.92	1.97	2.02
E	.193	.197	.201	4.90	5.00	5.10
E1	.135	.137	.139	3.43	3.48	3.53
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	32			32		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern — MLPQ-5x5-32



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.195)	(4.95)
G	.165	4.20
H	.137	3.48
H1	.059	1.49
H2	.065	1.66
K	.078	1.97
K1	.041	1.05
P	.020	0.50
X	.012	0.30
Y	.030	0.75
Z	.224	5.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD
   SHALL BE CONNECTED TO A SYSTEM GROUND PLANE.
   FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR
   FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. SQUARE PACKAGE-DIMENSIONS APPLY IN BOTH X AND Y DIRECTIONS.

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