



# MCP6L71/1R/2/4

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NOTES:

## 1.0 ELECTRICAL CHARACTERISTICS

### 1.1 Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ .....	7.0V
Current at Input Pins .....	$\pm 2$ mA
Analog Inputs ( $V_{IN+}$ and $V_{IN-}$ ) †† ..	$V_{SS} - 1.0V$ to $V_{DD} + 1.0V$
All other Inputs and Outputs .....	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Difference Input Voltage .....	$ V_{DD} - V_{SS} $
Output Short Circuit Current .....	Continuous
Current at Output and Supply Pins .....	$\pm 30$ mA
Storage Temperature .....	$-65^{\circ}C$ to $+150^{\circ}C$
Junction Temperature ( $T_J$ ) .....	$+150^{\circ}C$
ESD Protection On All Pins (HBM/MM) .....	$\geq 4$ kV/400V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 “Input Voltage and Current Limits”**.

### 1.2 Specifications

**TABLE 1-1: DC ELECTRICAL SPECIFICATIONS**

Electrical Characteristics: Unless otherwise indicated, $T_A = +25^{\circ}C$ , $V_{DD} = 5.0V$ , $V_{SS} = GND$ , $V_{CM} = V_{DD}/2$ , $V_{OUT} \approx V_{DD}/2$ , $V_L = V_{DD}/2$ and $R_L = 10$ k $\Omega$ to $V_L$ . (Refer to <a href="#">Figure 1-1</a> ).						
Parameters	Sym	Min (Note 1)	Typ	Max (Note 1)	Units	Conditions
<b>Input Offset</b>						
Input Offset Voltage	$V_{OS}$	-4	$\pm 1$	+4	mV	
Input Offset Temperature Drift	$\Delta V_{OS}/\Delta T_A$	—	$\pm 1.3$	—	$\mu V/^{\circ}C$	$T_A = -40^{\circ}C$ to $+125^{\circ}C$ ,
Power Supply Rejection Ratio	PSRR	—	89	—	dB	
<b>Input Bias Current and Impedance</b>						
Input Bias Current	$I_B$	—	1	—	pA	
	$I_B$	—	50	—	pA	$T_A = +85^{\circ}C$
	$I_B$	—	2000	—	pA	$T_A = +125^{\circ}C$
Input Offset Current	$I_{OS}$	—	$\pm 1$	—	pA	
Common Mode Input Impedance	$Z_{CM}$	—	$10^{13}  6$	—	$\Omega  pF$	
Differential Input Impedance	$Z_{DIFF}$	—	$10^{13}  3$	—	$\Omega  pF$	
<b>Common Mode</b>						
Common Mode Input Voltage Range	$V_{CMR}$	-0.3	—	+5.3	V	
Common Mode Rejection Ratio	CMRR	—	91	—	dB	$V_{CM} = -0.3V$ to $5.3V$
<b>Open-Loop Gain</b>						
DC Open-Loop Gain (Large Signal)	$A_{OL}$	—	105	—	dB	$V_{OUT} = 0.2V$ to $4.8V$ , $V_{CM} = V_{SS}$
<b>Output</b>						
Maximum Output Voltage Swing	$V_{OL}$	—	—	0.020	V	$G = +2$ V/V, 0.5V input overdrive
	$V_{OH}$	4.980	—	—	V	$G = +2$ V/V, 0.5V input overdrive
Output Short Circuit Current	$I_{SC}$	—	$\pm 25$	—	mA	

**Note 1:** For design guidance only; not tested.

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**TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)**

**Electrical Characteristics:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $V_L = V_{DD}/2$  and  $R_L = 10\text{ k}\Omega$  to  $V_L$ . (Refer to [Figure 1-1](#)).

Parameters	Sym	Min (Note 1)	Typ	Max (Note 1)	Units	Conditions
<b>Power Supply</b>						
Supply Voltage	$V_{DD}$	2.0	—	6.0	V	
Quiescent Current per Amplifier	$I_Q$	50	150	240	$\mu\text{A}$	$I_O = 0$

**Note 1:** For design guidance only; not tested.

**TABLE 1-2: AC ELECTRICAL SPECIFICATIONS**

**Electrical Characteristics:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +2.0\text{V}$  to  $+5.5\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$  and  $C_L = 60\text{ pF}$ . (Refer to [Figure 1-1](#)).

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>AC Response</b>						
Gain Bandwidth Product	GBWP	—	2.0	—	MHz	
Phase Margin	PM	—	65	—	$^\circ$	$G = +1\text{ V/V}$
Slew Rate	SR	—	0.9	—	$\text{V}/\mu\text{s}$	
<b>Noise</b>						
Input Noise Voltage	$E_{ni}$	—	4.6	—	$\mu\text{V}_{P-P}$	$f = 0.1\text{ Hz}$ to $10\text{ Hz}$
Input Noise Voltage Density	$e_{ni}$	—	19	—	$\text{nV}/\sqrt{\text{Hz}}$	$f = 10\text{ kHz}$
Input Noise Current Density	$i_{ni}$	—	3	—	$\text{fA}/\sqrt{\text{Hz}}$	$f = 1\text{ kHz}$

**TABLE 1-3: TEMPERATURE SPECIFICATIONS**

**Electrical Characteristics:** Unless otherwise indicated,  $V_{DD} = +2.0\text{V}$  to  $+5.5\text{V}$  and  $V_{SS} = \text{GND}$ .

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Temperature Ranges</b>						
Specified Temperature Range	$T_A$	-40	—	+125	$^\circ\text{C}$	
Operating Temperature Range	$T_A$	-40	—	+125	$^\circ\text{C}$	<b>Note 1</b>
Storage Temperature Range	$T_A$	-65	—	+150	$^\circ\text{C}$	
<b>Thermal Package Resistances</b>						
Thermal Resistance, 5L-SOT-23	$\theta_{JA}$	—	256	—	$^\circ\text{C}/\text{W}$	
Thermal Resistance, 8L-SOIC	$\theta_{JA}$	—	163	—	$^\circ\text{C}/\text{W}$	
Thermal Resistance, 8L-MSOP	$\theta_{JA}$	—	206	—	$^\circ\text{C}/\text{W}$	
Thermal Resistance, 14L-SOIC	$\theta_{JA}$	—	120	—	$^\circ\text{C}/\text{W}$	
Thermal Resistance, 14L-TSSOP	$\theta_{JA}$	—	100	—	$^\circ\text{C}/\text{W}$	

**Note 1:** The Junction Temperature ( $T_J$ ) must not exceed the Absolute Maximum specification of  $+150^\circ\text{C}$ .

## 1.3 Test Circuits

The circuit used for most DC and AC tests is shown in [Figure 1-1](#). This circuit can independently set  $V_{CM}$  and  $V_{OUT}$ ; see [Equation 1-1](#). Note that  $V_{CM}$  is not the circuit's common mode voltage ( $(V_P + V_M)/2$ ), and that  $V_{OST}$  includes  $V_{OS}$  plus the effects (on the input offset error,  $V_{OST}$ ) of temperature, CMRR, PSRR and  $A_{OL}$ .

### EQUATION 1-1:

$$G_{DM} = R_F/R_G$$

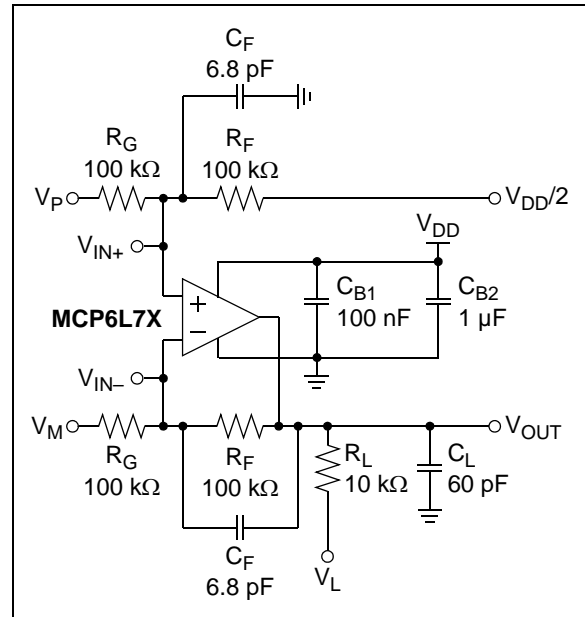
$$V_{CM} = (V_P + V_{DD}/2)/2$$

$$V_{OST} = V_{IN-} - V_{IN+}$$

$$V_{OUT} = (V_{DD}/2) + (V_P - V_M) + V_{OST}(1 + G_{DM})$$

Where:

$G_{DM}$	=	Differential Mode Gain	(V/V)
$V_{CM}$	=	Op Amp's Common Mode Input Voltage	(V)
$V_{OST}$	=	Op Amp's Total Input Offset Voltage	(mV)



**FIGURE 1-1:** AC and DC Test Circuit for Most Specifications.

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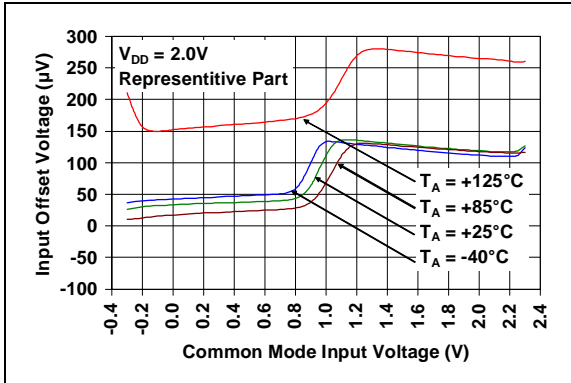
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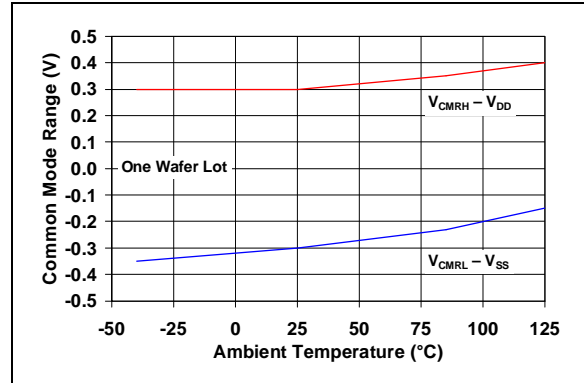
## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

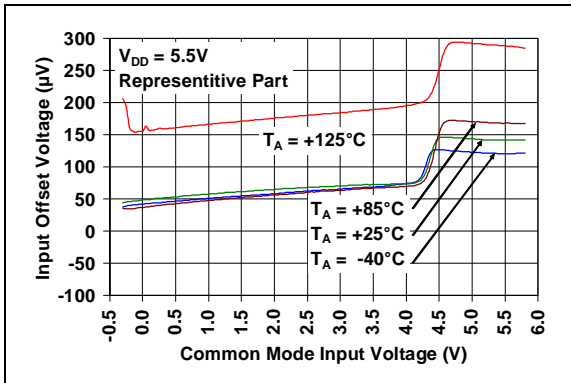
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$  and  $C_L = 60\text{ pF}$ .



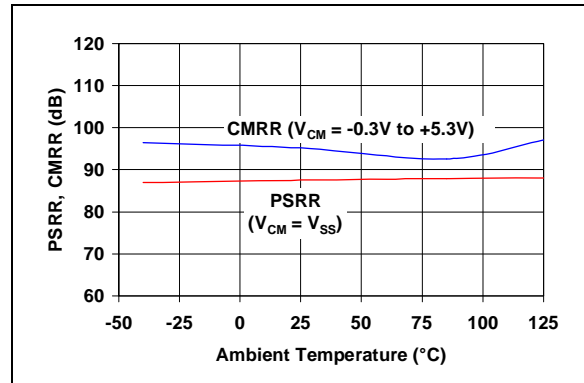
**FIGURE 2-1:** Input Offset Voltage vs. Common Mode Input Voltage at  $V_{DD} = 2.0\text{V}$ .



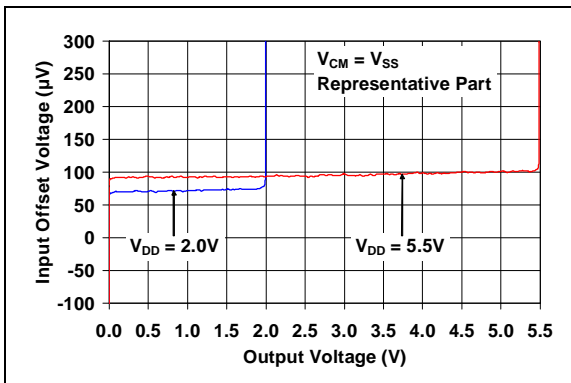
**FIGURE 2-4:** Input Common Mode Range Voltage vs. Ambient Temperature.



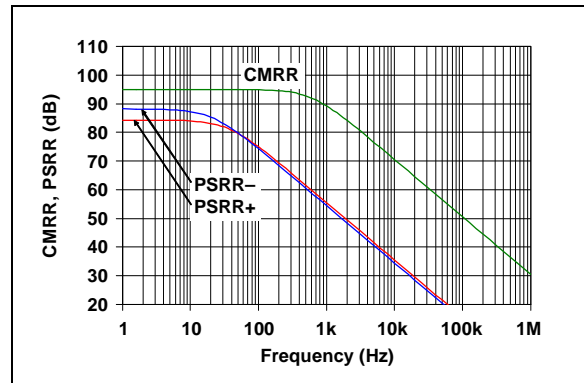
**FIGURE 2-2:** Input Offset Voltage vs. Common Mode Input Voltage at  $V_{DD} = 5.5\text{V}$ .



**FIGURE 2-5:** CMRR, PSRR vs. Temperature.



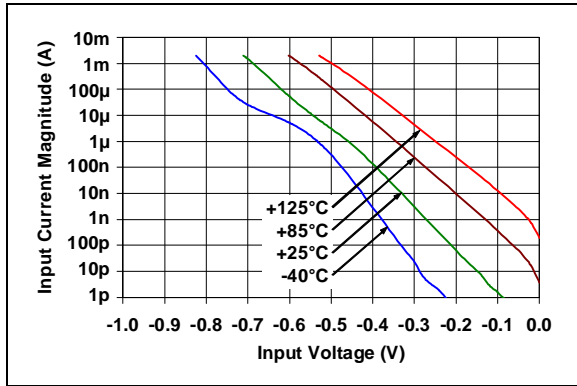
**FIGURE 2-3:** Input Offset Voltage vs. Output Voltage.



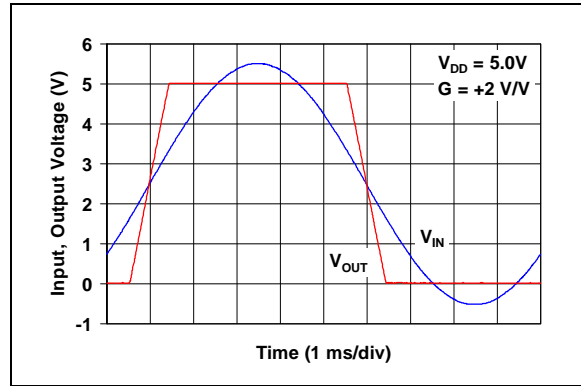
**FIGURE 2-6:** CMRR, PSRR vs. Frequency.

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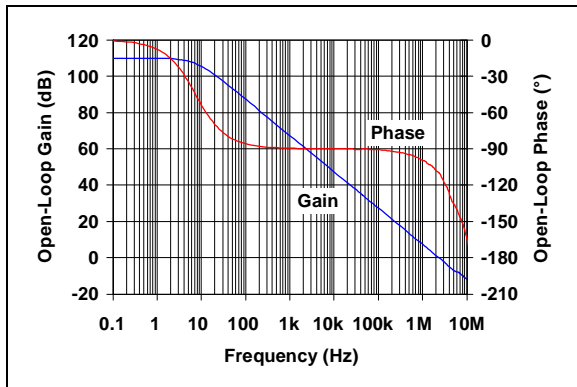
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$  and  $C_L = 60\text{ pF}$ .



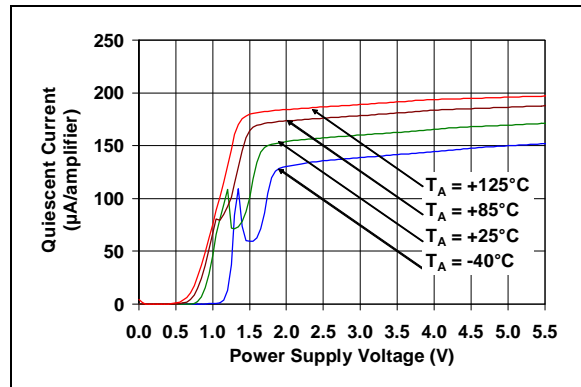
**FIGURE 2-7:** Input Current vs. Input Voltage.



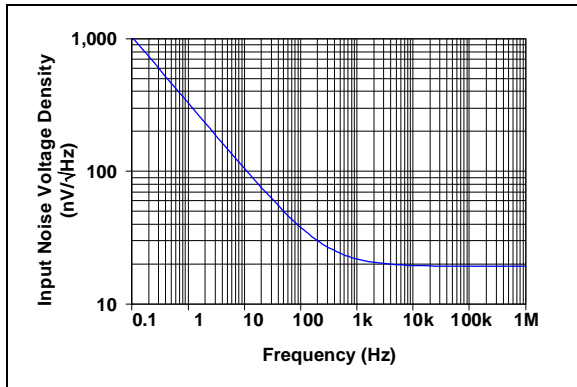
**FIGURE 2-10:** The MCP6L71/1R/2/4 Show No Phase Reversal.



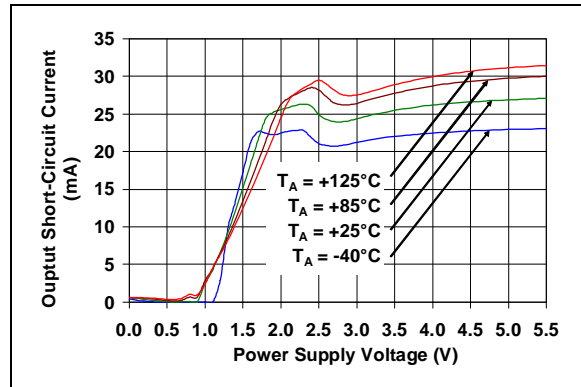
**FIGURE 2-8:** Open-Loop Gain, Phase vs. Frequency.



**FIGURE 2-11:** Quiescent Current vs. Supply Voltage.



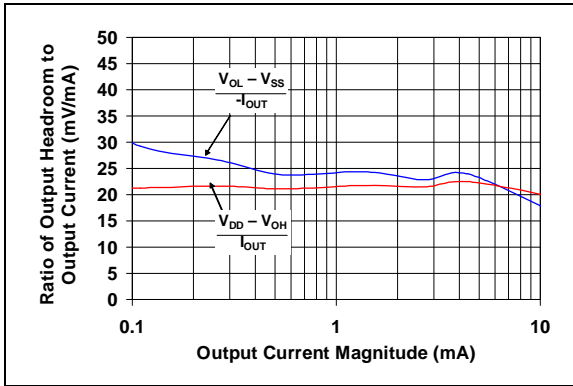
**FIGURE 2-9:** Input Noise Voltage Density vs. Frequency.



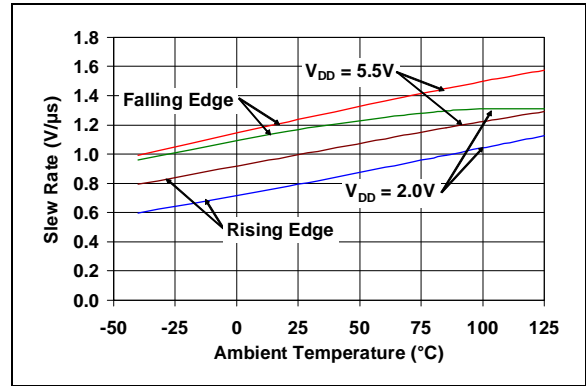
**FIGURE 2-12:** Output Short Circuit Current vs. Supply Voltage.



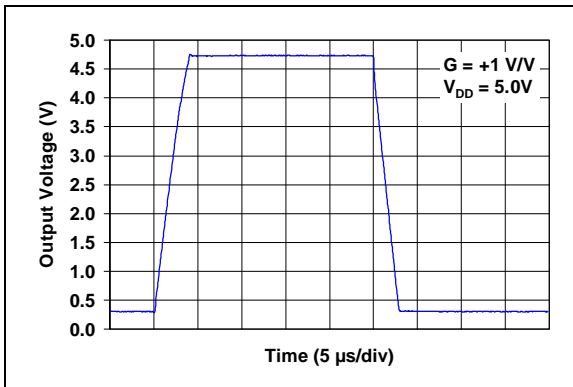
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$  and  $C_L = 60\text{ pF}$ .



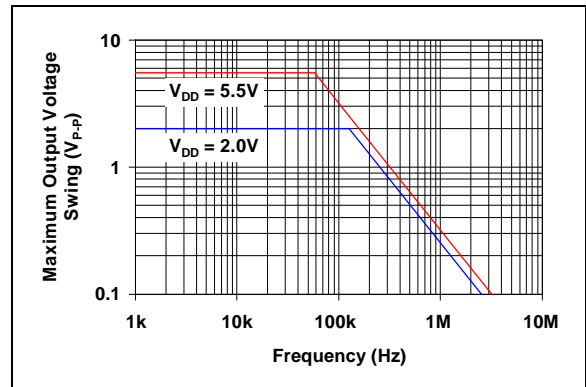
**FIGURE 2-13:** Ratio of Output Voltage Headroom vs. Output Current Magnitude.



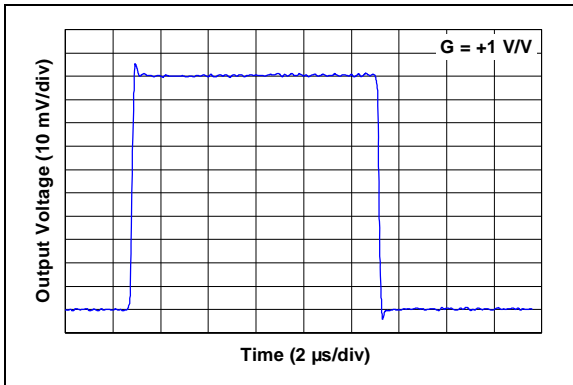
**FIGURE 2-16:** Slew Rate vs. Ambient Temperature.



**FIGURE 2-14:** Large Signal Non-inverting Pulse Response.



**FIGURE 2-17:** Maximum Output Voltage Swing vs. Frequency.



**FIGURE 2-15:** Small Signal Non-inverting Pulse Response.

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## 3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in [Table 3-1](#) (single op amps) and [Table 3-2](#) (dual and quad op amps).

**TABLE 3-1: PIN FUNCTION TABLE FOR SINGLE OP AMPS**

MCP6L71		MCP6L71R	Symbol	Description
MSOP, SOIC	SOT-23-5	SOT-23-5		
2	4	4	$V_{IN-}$	Inverting Input
3	3	3	$V_{IN+}$	Non-inverting Input
4	2	5	$V_{SS}$	Negative Power Supply
6	1	1	$V_{OUT}$	Analog Output
7	5	2	$V_{DD}$	Positive Power Supply
1,5,8	—	—	NC	No Internal Connection

**TABLE 3-2: PIN FUNCTION TABLE FOR DUAL AND QUAD OP AMPS**

MCP6L72	MCP6L74	Symbol	Description
MSOP, SOIC	SOIC, TSSOP		
1	1	$V_{OUTA}$	Analog Output (op amp A)
2	2	$V_{INA-}$	Inverting Input (op amp A)
3	3	$V_{INA+}$	Non-inverting Input (op amp A)
8	4	$V_{DD}$	Positive Power Supply
5	5	$V_{INB+}$	Non-inverting Input (op amp B)
6	6	$V_{INB-}$	Inverting Input (op amp B)
7	7	$V_{OUTB}$	Analog Output (op amp B)
—	8	$V_{OUTC}$	Analog Output (op amp C)
—	9	$V_{INC-}$	Inverting Input (op amp C)
—	10	$V_{INC+}$	Non-inverting Input (op amp C)
4	11	$V_{SS}$	Negative Power Supply
—	12	$V_{IND+}$	Non-inverting Input (op amp D)
—	13	$V_{IND-}$	Inverting Input (op amp D)
—	14	$V_{OUTD}$	Analog Output (op amp D)

### 3.1 Analog Outputs

The output pins are low impedance voltage sources.

### 3.2 Analog Inputs

The non-inverting and inverting inputs are high impedance CMOS inputs with low bias currents.

### 3.3 Power Supply Pins

The positive power supply ( $V_{DD}$ ) is 2.0V to 6.0V higher than the negative power supply ( $V_{SS}$ ). For normal operation, the other pins are at voltages between  $V_{SS}$  and  $V_{DD}$ .

Typically, these parts are used in a single (positive) supply configuration. In this case,  $V_{SS}$  is connected to ground and  $V_{DD}$  is connected to the supply.  $V_{DD}$  will need bypass capacitors.

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## 4.0 APPLICATION INFORMATION

The MCP6L71/1R/2/4 family of op amps is manufactured using Microchip's state of the art CMOS process, specifically designed for low cost, low power and general purpose applications. The low supply voltage, low quiescent current and wide bandwidth make the MCP6L71/1R/2/4 ideal for battery powered applications.

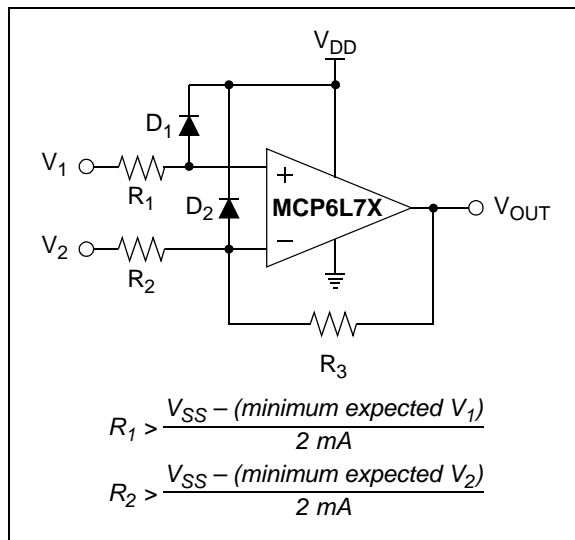
### 4.1 Rail-to-Rail Inputs

#### 4.1.1 PHASE REVERSAL

The MCP6L71/1R/2/4 op amps are designed to prevent phase inversion when the input pins exceed the supply voltages. Figure 2-10 shows an input voltage exceeding both supplies without any phase reversal.

#### 4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

In order to prevent damage and/or improper operation of these amplifiers, the circuit they are in must limit the currents (and voltages) at the input pins (see Section 1.1 "Absolute Maximum Ratings †"). Figure 4-1 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins ( $V_{IN+}$  and  $V_{IN-}$ ) from going too far below ground, and the resistors  $R_1$  and  $R_2$  limit the possible current drawn out of the input pins. Diodes  $D_1$  and  $D_2$  prevent the input pins ( $V_{IN+}$  and  $V_{IN-}$ ) from going too far above  $V_{DD}$ , and dump any currents onto  $V_{DD}$ .



**FIGURE 4-1:** Protecting the Analog Inputs.

A significant amount of current can flow out of the inputs (through the ESD diodes) when the common mode voltage ( $V_{CM}$ ) is below ground ( $V_{SS}$ ); see Figure 2-7. Applications that are high impedance may need to limit the usable voltage range.

#### 4.1.3 NORMAL OPERATIONS

The input stage of the MCP6L71/1R/2/4 op amps uses two differential CMOS input stages in parallel. One operates at low common mode input voltage ( $V_{CM}$ ), while the other at high  $V_{CM}$ . With this topology, and at room temperature, the device operates with  $V_{CM}$  up to 0.3V above  $V_{DD}$  and 0.3V below  $V_{SS}$  (typically at +25°C).

The transition between the two input stage occurs when  $V_{CM} = V_{DD} - 1.1V$ . For the best distortion and gain linearity, with non-inverting gains, avoid this region of operation.

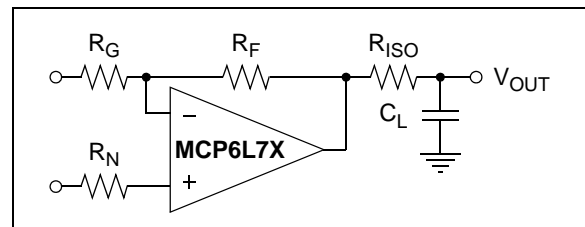
### 4.2 Rail-to-Rail Output

The output voltage range of the MCP6L71/1R/2/4 op amps is  $V_{DD} - 20 \text{ mV}$  (minimum) and  $V_{SS} + 20 \text{ mV}$  (maximum) when  $R_L = 10 \text{ k}\Omega$  is connected to  $V_{DD}/2$  and  $V_{DD} = 5.0V$ . Refer to Figure 2-13 for more information.

### 4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response.

When driving large capacitive loads with these op amps (e.g., > 100 pF when  $G = +1$ ), a small series resistor at the output ( $R_{ISO}$  in Figure 4-2) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.



**FIGURE 4-2:** Output Resistor,  $R_{ISO}$  Stabilizes Large Capacitive Loads.

Bench measurements are helpful in choosing  $R_{ISO}$ . Adjust  $R_{ISO}$  so that a small signal step response (see Figure 2-15) has reasonable overshoot (e.g., 4%).

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## 4.4 Supply Bypass

With this family of operational amplifiers, the power supply pin ( $V_{DD}$  for single supply) should have a local bypass capacitor (i.e., 0.01  $\mu\text{F}$  to 0.1  $\mu\text{F}$ ) within 2 mm for good, high frequency performance. It also needs a bulk capacitor (i.e., 1  $\mu\text{F}$  or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with nearby analog parts.

## 4.5 Unused Amplifiers

An unused op amp in a quad package (MCP6L74) should be configured as shown in Figure 4-3. These circuits prevent the output from toggling and causing crosstalk. In Circuit A,  $R_1$  and  $R_2$  produce a voltage within its output voltage range ( $V_{OH}$ ,  $V_{OL}$ ). The op amp buffers this voltage, which can be used elsewhere in the circuit. Circuit B uses the minimum number of components and operates as a comparator.

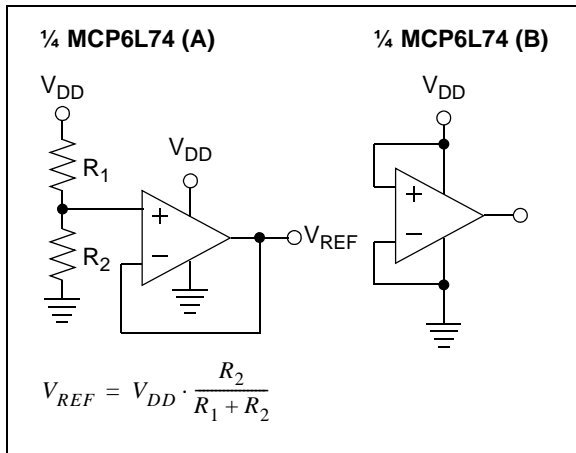


FIGURE 4-3: Unused Op Amps.

## 4.6 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is  $10^{12}\Omega$ . A 5V difference would cause 5 pA of current to flow. This is greater than the MCP6L71/1R/2/4 family's bias current at +25°C (1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. Figure 4-4 shows an example of this type of layout.

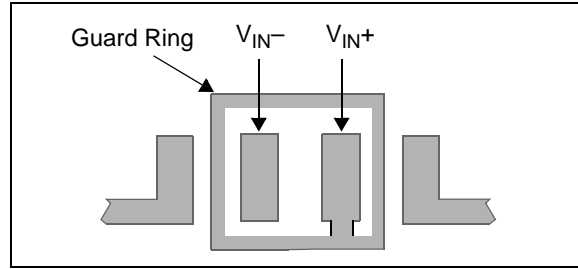


FIGURE 4-4: Example Guard Ring Layout.

1. For Inverting Gain and Transimpedance Amplifiers (convert current to voltage, such as photo detectors):
  - a) Connect the guard ring to the non-inverting input pin ( $V_{IN+}$ ). This biases the guard ring to the same reference voltage as the op amp (e.g.,  $V_{DD}/2$  or ground).
  - b) Connect the inverting pin ( $V_{IN-}$ ) to the input with a wire that does not touch the PCB surface.
2. Non-inverting Gain and Unity Gain Buffer:
  - a) Connect the guard ring to the inverting input pin ( $V_{IN-}$ ). This biases the guard ring to the common mode input voltage.
  - b) Connect the non-inverting pin ( $V_{IN+}$ ) to the input with a wire that does not touch the PCB surface.

## 4.7 Application Circuits

### 4.7.1 INVERTING INTEGRATOR

An inverting integrator is shown in Figure 4-5. The circuit provides an output voltage that is proportional to the negative time-integral of the input. The additional resistor  $R_2$  limits DC gain and controls output clipping. To minimize the integrator's error for slow signals, the value of  $R_2$  should be much larger than the value of  $R_1$ .

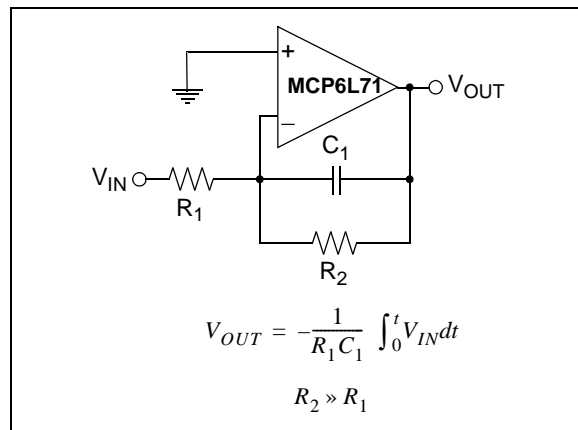


FIGURE 4-5: Inverting Integrator.

## 5.0 DESIGN TOOLS

Microchip provides the basic design tools needed for the MCP6L71/1R/2/4 family of op amps.

### 5.1 FilterLab<sup>®</sup> Software

Microchip's FilterLab<sup>®</sup> software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at [www.microchip.com/filterlab](http://www.microchip.com/filterlab), the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

### 5.2 MAPS (Microchip Advanced Part Selector)

MAPS is a software tool that helps efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip web site at [www.microchip.com/maps](http://www.microchip.com/maps), the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Data sheets, Purchase, and Sampling of Microchip parts.

### 5.3 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at [www.microchip.com/analogtools](http://www.microchip.com/analogtools).

Some boards that are especially useful are:

- MCP6XXX Amplifier Evaluation Board 1
- MCP6XXX Amplifier Evaluation Board 2
- MCP6XXX Amplifier Evaluation Board 3
- MCP6XXX Amplifier Evaluation Board 4
- Active Filter Demo Board Kit
- 5/6-Pin SOT-23 Evaluation Board, P/N VSUPEV2
- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board, P/N SOIC8EV
- 14-Pin SOIC/TSSOP/DIP Evaluation Board, P/N SOIC14EV

## 5.4 Application Notes

The following Microchip Application Notes are available on the Microchip web site at [www.microchip.com/appnotes](http://www.microchip.com/appnotes) and are recommended as supplemental reference resources.

- **ADN003:** "Select the Right Operational Amplifier for your Filtering Circuits", DS21821
- **AN722:** "Operational Amplifier Topologies and DC Specifications", DS00722
- **AN723:** "Operational Amplifier AC Specifications and Applications", DS00723
- **AN884:** "Driving Capacitive Loads With Op Amps", DS00884
- **AN990:** "Analog Sensor Conditioning Circuits – An Overview", DS00990

# MCP6L71/1R/2/4

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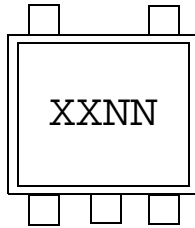
NOTES:



## 6.0 PACKAGING INFORMATION

### 6.1 Package Marking Information

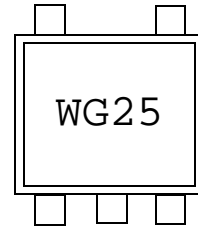
#### 5-Lead SOT-23 (MCP6L71, MCP6L71R)



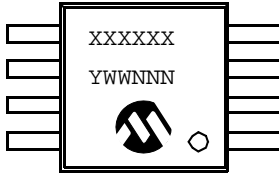
Device	Code
MCP6L71	WGNN
MCP6L71R	WFNN

**Note:** Applies to 5-Lead SOT-23

Example:



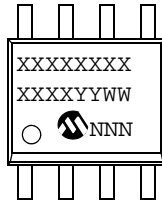
#### 8-Lead MSOP (MCP6L71, MCP6L72)



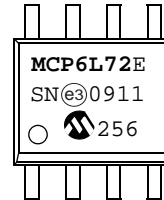
Example:



#### 8-Lead SOIC (150 mil) (MCP6L71, MCP6L72)



Example:



<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

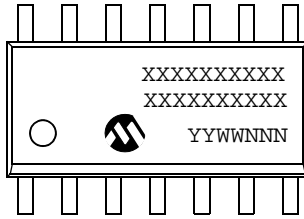
**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

# MCP6L71/1R/2/4

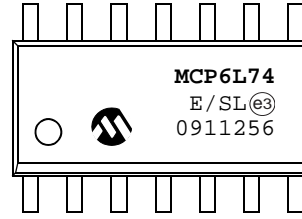
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## Package Marking Information (Continued)

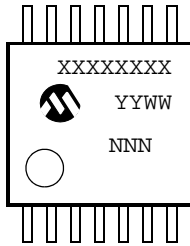
14-Lead SOIC (150 mil) (MCP6L74)



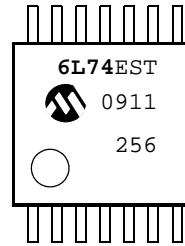
Example:



14-Lead TSSOP (MCP6L74)

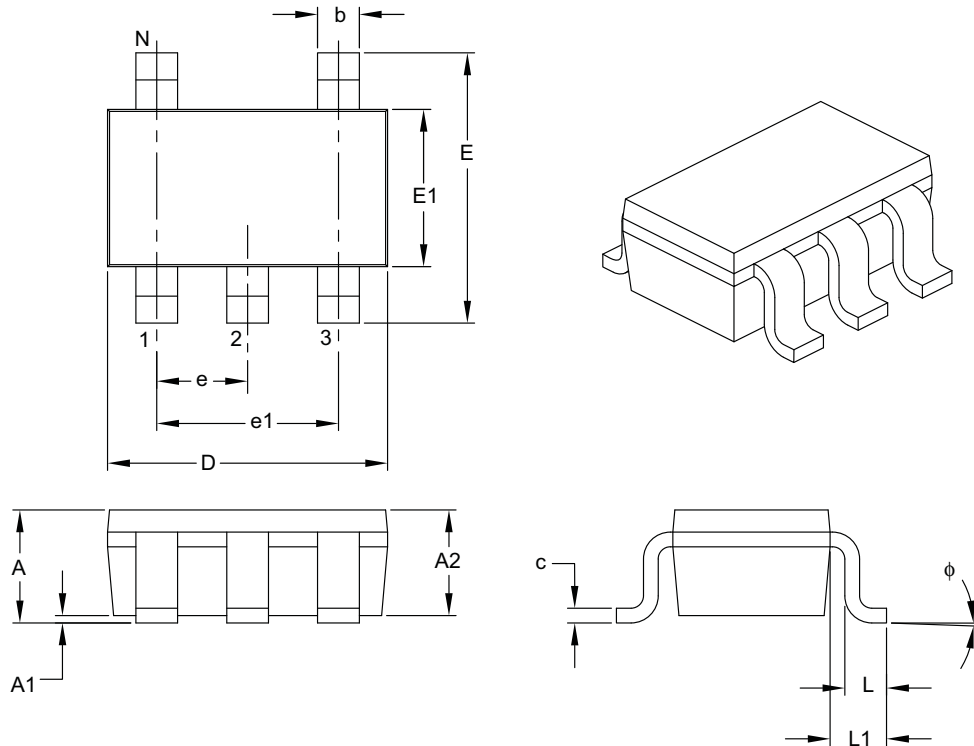


Example:



## 5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	5		
Lead Pitch	e	0.95 BSC		
Outside Lead Pitch	e1	1.90 BSC		
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	$\phi$	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

**Notes:**

- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

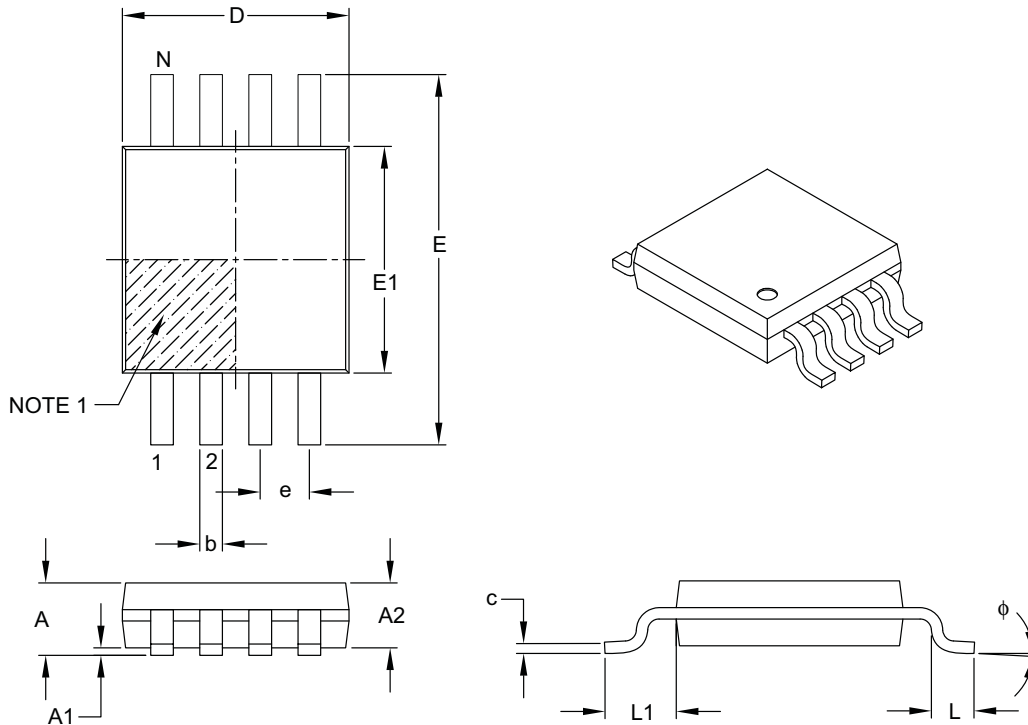
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

# MCP6L71/1R/2/4

## 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Overall Length	D	3.00 BSC		
Foot Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Foot Angle	$\phi$	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.22	–	0.40

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

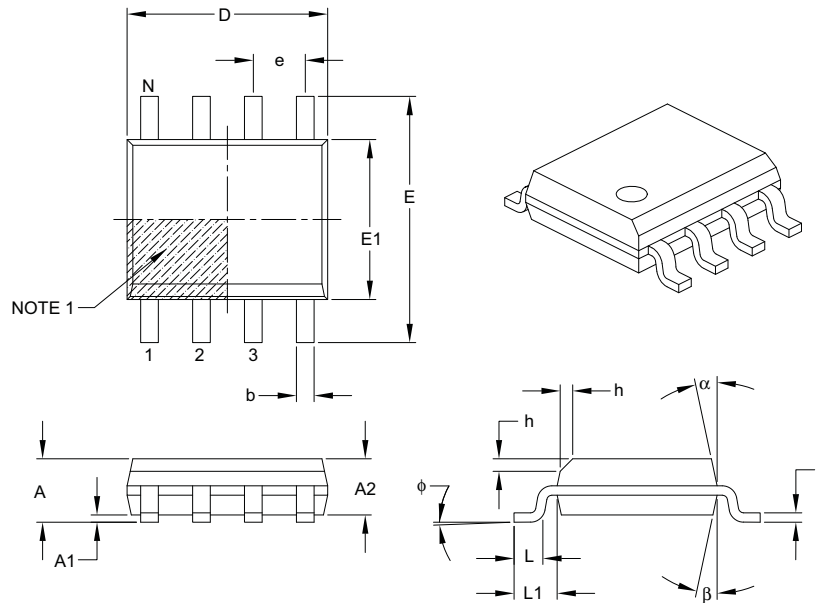
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Foot Angle	$\phi$	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	$\alpha$	5°	–	15°
Mold Draft Angle Bottom	$\beta$	5°	–	15°

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

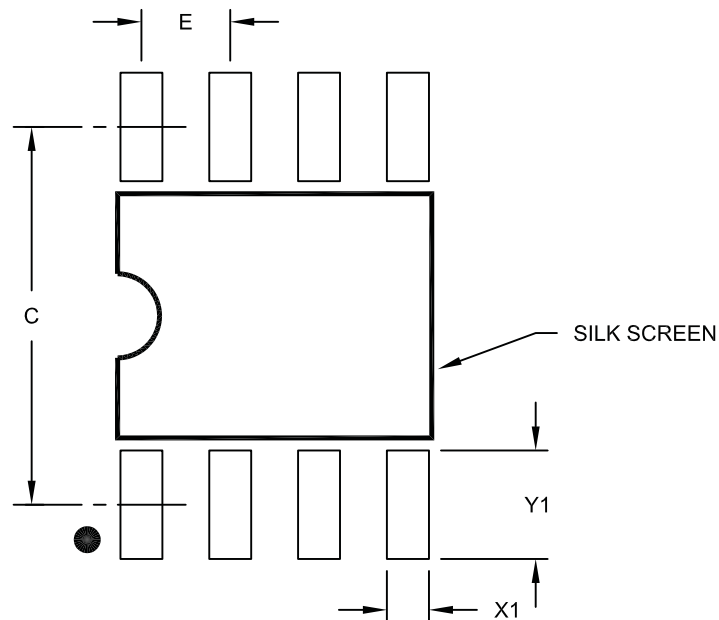
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

# MCP6L71/1R/2/4

## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

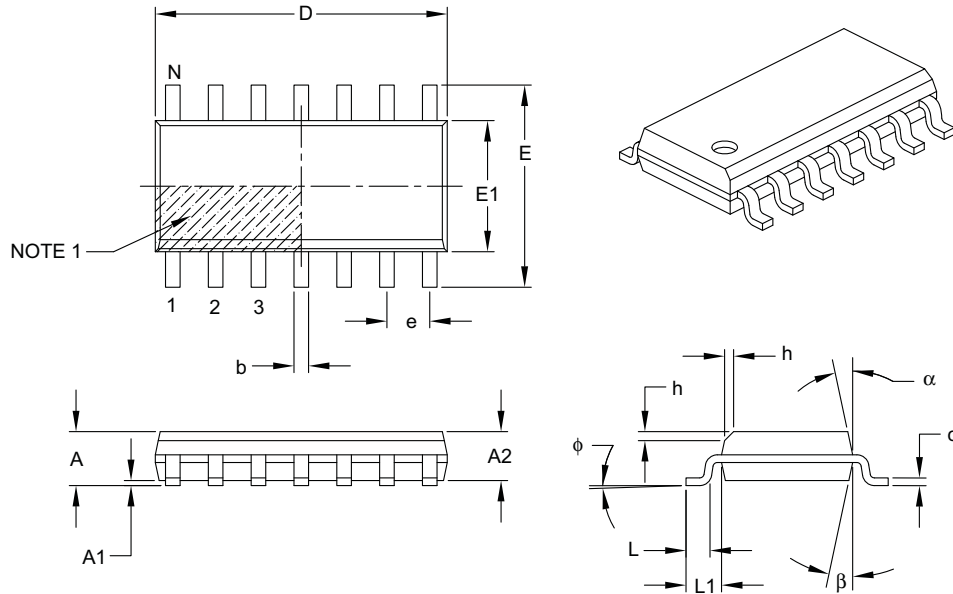
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

## 14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

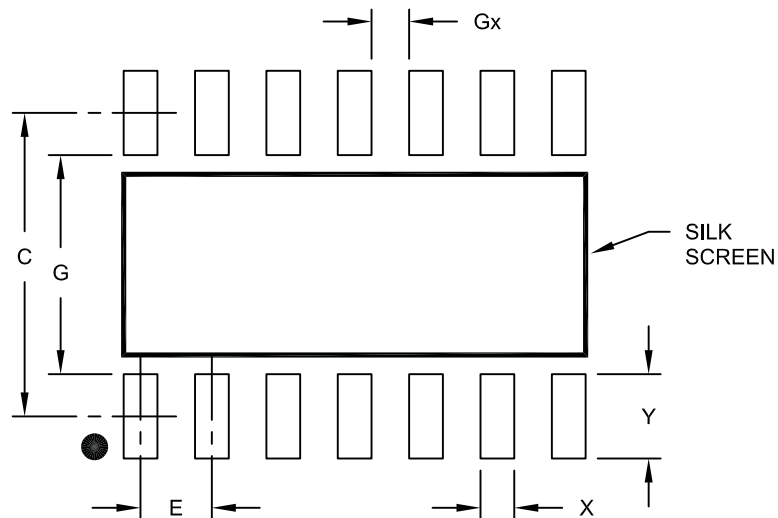
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B

# MCP6L71/1R/2/4

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

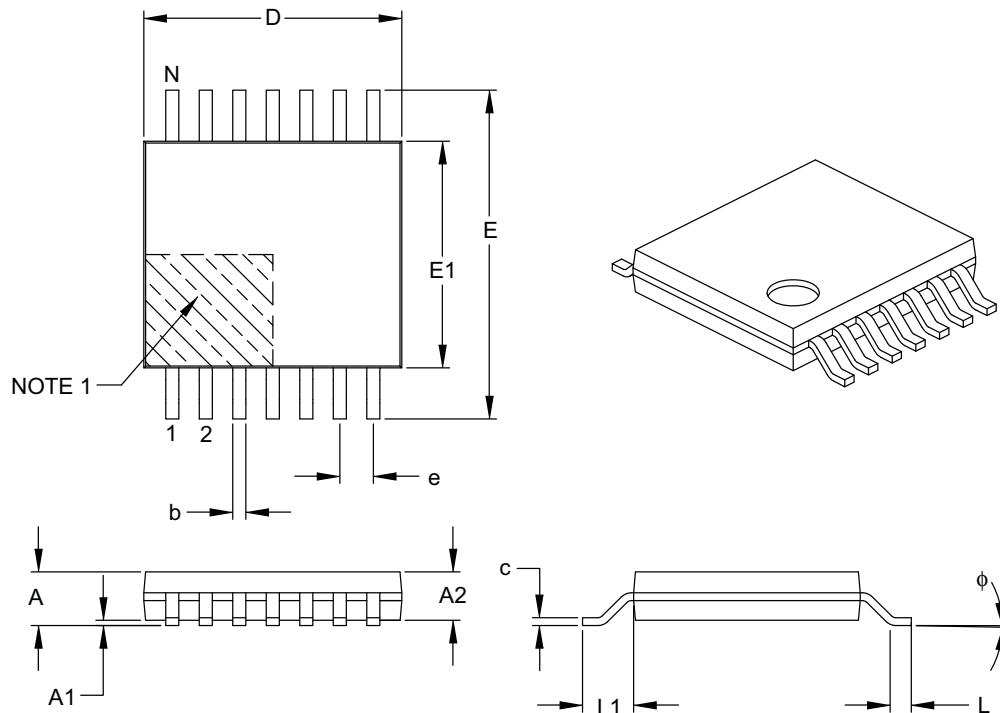
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A



## 14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		14		
Pitch	e		0.65 BSC		
Overall Height	A		–	–	1.20
Molded Package Thickness	A2		0.80	1.00	1.05
Standoff	A1		0.05	–	0.15
Overall Width	E		6.40 BSC		
Molded Package Width	E1		4.30	4.40	4.50
Molded Package Length	D		4.90	5.00	5.10
Foot Length	L		0.45	0.60	0.75
Footprint	L1		1.00 REF		
Foot Angle	$\phi$		0°	–	8°
Lead Thickness	c		0.09	–	0.20
Lead Width	b		0.19	–	0.30

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087B

# MCP6L71/1R/2/4

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NOTES:

## APPENDIX A: REVISION HISTORY

### Revision A (March 2009)

- Original data sheet release.

# MCP6L71/1R/2/4

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	—	<u>X</u>	<u>/XX</u>
Device		Temperature Range	Package
Device:	MCP6L71T:	Single Op Amp (Tape and Reel) (MSOP, SOIC, SOT-23-5)	
	MCP6L71RT:	Single Op Amp (Tape and Reel) (SOT-23-5)	
	MCP6L72T:	Dual Op Amp (Tape and Reel) (MSOP, SOIC)	
	MCP6L74T:	Quad Op Amp (Tape and Reel) (SOIC, TSSOP)	
Temperature Range:	E	= -40°C to +125°C	
Package:	OT	= Plastic Small Outline Transistor (SOT-23), 5-lead (MCP6L71, MCP6L71R)	
	MS	= Plastic MSOP, 8-lead	
	SN	= Plastic SOIC, (150 mil Body), 8-lead	
	SL	= Plastic SOIC (150 mil Body), 14-lead	
	ST	= Plastic TSSOP (4.4 mm Body), 14-lead	

Examples:	
a)	MCP6L71T-E/OT: Tape and Reel, 5LD SOT-23 package.
b)	MCP6L71T-E/MS: Tape and Reel, 8LD MSOP package.
c)	MCP6L71T-E/SN: Tape and Reel, 8LD SOIC package.
a)	MCP6L71RT-E/OT: Tape and Reel, 5LD SOT-23 package.
a)	MCP6L72T-E/MS: Tape and Reel, 8LD MSOP package.
b)	MCP6L72T-E/SN: Tape and Reel, 8LD SOIC package.
a)	MCP6L74T-E/SL: Tape and Reel, 14LD SOIC package.
b)	MCP6L74-E/ST: Tape and Reel, 14LD TSSOP package.

# MCP6L71/1R/2/4

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NOTES:

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**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

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