SC18IS600/601

SPI to I²C-bus interface

Rev. 05 — 28 July 2008 Product data sheet

1. General description

The SC18IS600/601 is designed to serve as an interface between the standard SPI of a host (microcontroller, microprocessor, chip set, etc.) and the serial I²C-bus. This allows the host to communicate directly with other I²C-bus devices. The SC18IS600/601 can operate as an I²C-bus master-transmitter or master-receiver. The SC18IS600/601 controls all the I²C-bus specific sequences, protocol, arbitration and timing.

The key distinction between the SC18IS600 and the SC18IS601 lies in the clock source: internal (SC18IS600) versus external (SC18IS601).

2. Features

- SPI slave interface
- SPI Mode 3
- Master I²C-bus controller
- General Purpose Input/Output (GPIO) pins: 4 (SC18IS600); 3 (SC18IS601)
- Two quasi-bidirectional I/O pins
- 5 V tolerant I/O pins
- High-speed SPI:
  - Up to 3 Mbit/s (SC18IS601)
  - Up to 1.2 Mbit/s (SC18IS600)
- High-speed I²C-bus: 400 kbit/s
- 96-byte transmit buffer
- 96-byte receive buffer
- 2.4 V to 3.6 V operation
- Power-down mode with $\overline{\text{WAKEUP}}$ pin
- Oscillator: internal (SC18IS600); external (SC18IS601)
- Active LOW interrupt output
- Available in very small TSSOP16 and HVQFN24 packages

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SC18IS600IPW	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
SC18IS601IPW			
SC18IS600IBS	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-3

4. Block diagram

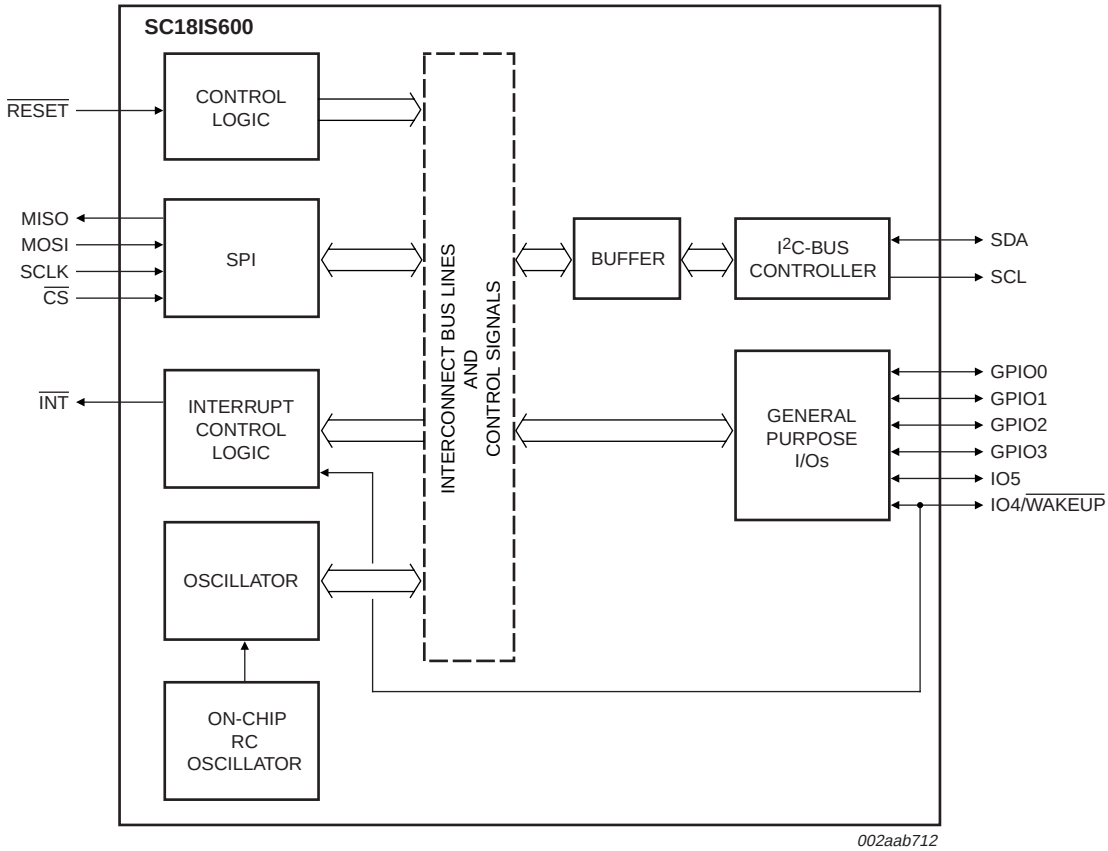


Fig 1. Block diagram of SC18IS600

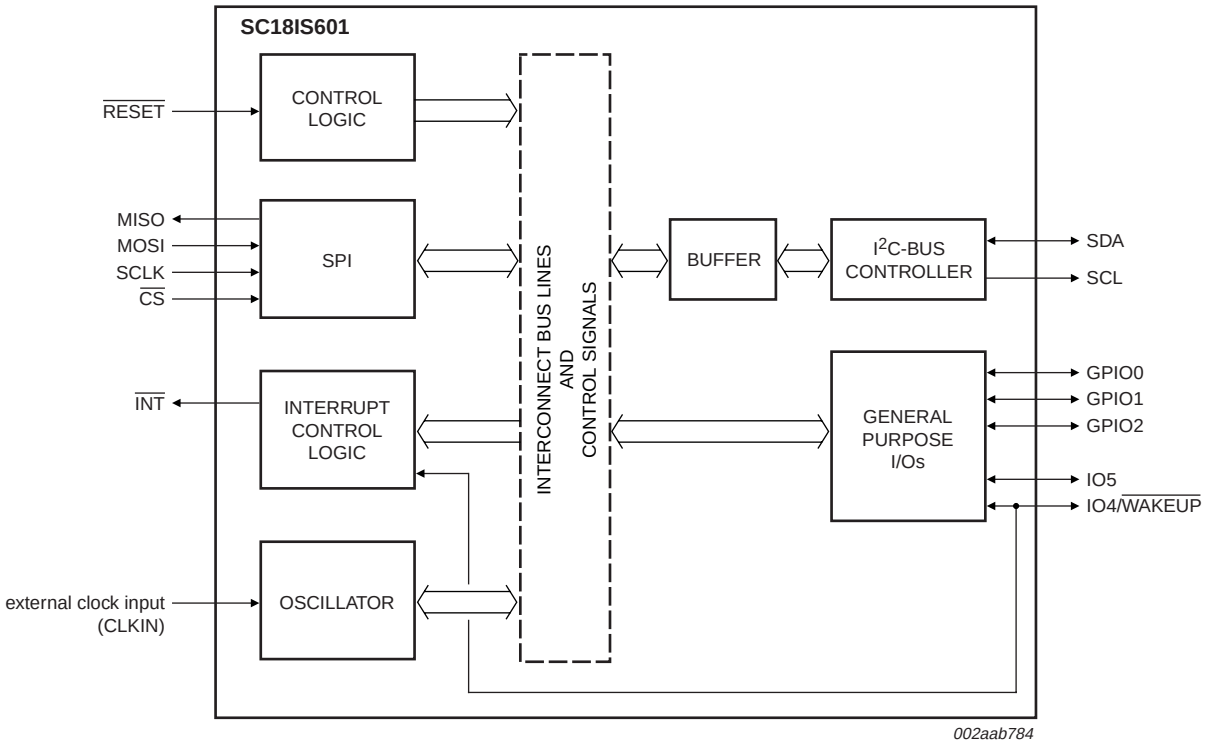


Fig 2. Block diagram of SC18IS601

5. Pinning information

5.1 Pinning

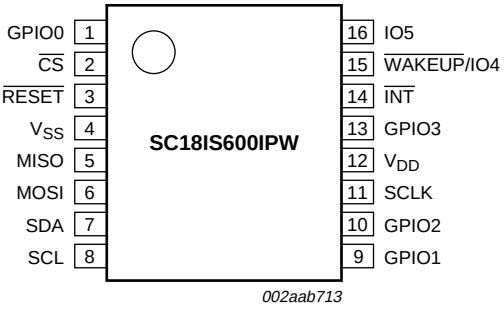


Fig 3. SC18IS600 pin configuration for TSSOP16

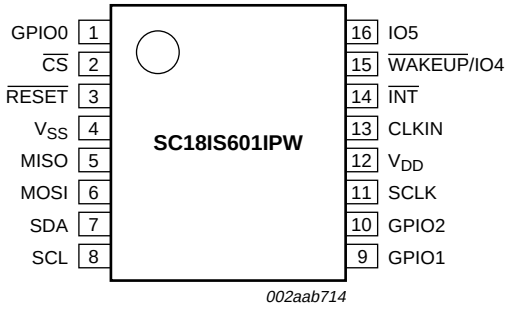


Fig 4. SC18IS601 pin configuration for TSSOP16

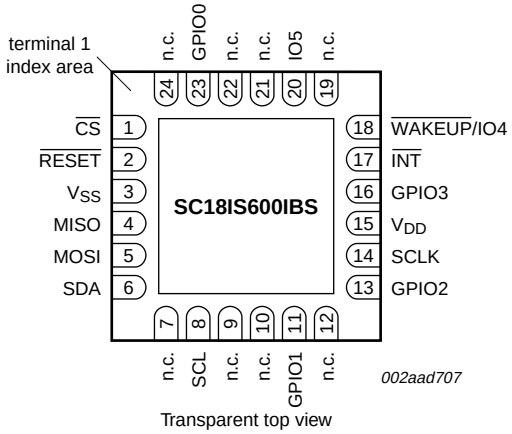


Fig 5. SC18IS600 pin configuration for HVQFN24

5.2 Pin description

Table 2. Pin description

Symbol	Pin			Type	Description
	TSSOP16		HVQFN24		
	SC18IS600	SC18IS601	SC18IS600		
GPIO0	1	1	23	I/O	programmable I/O pin
$\overline{CS}$	2	2	1	I	Chip select. When $\overline{CS}$ is LOW, the SC18IS600/601 is selected.
$\overline{RESET}$	3	3	2	I	Master Reset. When active (LOW), $\overline{RESET}$ sets internal registers to the default values, and resets the I²C-bus and SPI hardware. See Table 3.
V_{SS}	4	4	3[1]	I	ground supply voltage
MISO	5	5	4	O	SPI slave data output
MOSI	6	6	5	I	SPI slave data input
SDA	7	7	6	I/O	I²C-bus serial data input/output
SCL	8	8	8	O	I²C-bus serial clock output
GPIO1	9	9	11	I/O	programmable I/O pin
GPIO2	10	10	13	I/O	programmable I/O pin
SCLK	11	11	14	I	SPI clock input
V_{DD}	12	12	15	I	2.4 V to 3.6 V supply voltage
GPIO3	13	-	16	I/O	programmable I/O pin
CLKIN	-	13	-	I	external clock input
$\overline{INT}$	14	14	17	O	Interrupt. When active (LOW), $\overline{INT}$ informs the CPU that the SC18IS600/601 has an interrupt to be serviced. $\overline{INT}$ is reset (deactivated) either when the I2CStat register is read or as a result of a master reset ($\overline{RESET}$). This pin is an open-drain pin.
$\overline{WAKEUP}$/IO4	15	15	18	I/O	Wake up the SC18IS600/601 from the Power-down mode. Pulled LOW by the host to wake-up from low power state. This pin can also be used as a quasi-bidirectional I/O when not in a power-down state.
IO5	16	16	20	I/O	quasi-bidirectional I/O pin
n.c.	-	-	7, 9, 10, 12, 19, 21, 22, 24	-	not connected

[1] HVQFN24 package die supply ground is connected to both V_{SS} pin and exposed center pad. V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

6. Functional description

The SC18IS600/601 acts as a bridge between a SPI interface and an I²C-bus. It allows a SPI master device to communicate with I²C-bus slave devices. The SPI interface supports Mode 3 of the SPI specification and can operate up to 3 Mbit/s (SC18IS601).

6.1 Internal registers

The SC18IS600/601 provides internal registers for monitoring and control. These registers are shown in Table 3. Register functions are more fully described in the following paragraphs.

Table 3. Internal registers summary

Register address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Default value
0x00	IOConfig	IO3.1[1]	IO3.0[1]	IO2.1	IO2.0	IO1.1	IO1.0	IO0.1	IO0.0	R/W	0x00
0x01	IOState	0	0	GPIO5	GPIO4	GPIO3[2]	GPIO2	GPIO1	GPIO0	R/W	0x3F
0x02	I2CClock	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0	R/W	0x19
0x03	I2CTO	TO6	TO5	TO4	TO3	TO2	TO1	TO0	TE	R/W	0xFE
0x04	I2CStat	1	1	1	1	I2CSTAT3	I2CSTAT2	I2CSTAT1	I2CSTAT0	R	0xF0
0x05	I2CAdr	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	X	R/W	0x00

[1] For SC18IS601, these bits are ‘Don’t care’.

[2] For SC18IS601 GPIO3 is not used.

6.2 Register descriptions

6.2.1 Programmable IO port configuration register (IOConfig)

Pins GPIO0 to GPIO3 may be configured by software to one of four types. These are: quasi-bidirectional, push-pull, open-drain, and input-only. Two configuration bits per pin, located in the IOConfig register, select the IO type for each pin. Each pin has Schmitt-triggered input that also has a glitch suppression circuit. IO4 and IO5 are quasi-bidirectional pins and are not user-configurable. For SC18IS601, GPIO3 is non-existent.

Table 4 shows the configurations for the programmable I/O pins. IOx.1 and IOx.0 correspond to GPIOx.

Table 4. Pin configurations

IOx.1	IOx.0	Pin configuration
0	0	quasi-bidirectional output configuration
0	1	input-only configuration
1	0	push-pull output configuration
1	1	open-drain output configuration

6.2.1.1 Quasi-bidirectional output configuration

Quasi-bidirectional outputs can be used both as an input and output without the need to reconfigure the pin. This is possible because when the pin outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a large current. There are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

One of these pull-ups, called the ‘very weak’ pull-up, is turned on whenever the pin latch for the pin contains a logic 1. This very weak pull-up sources a very small current that will pull the pin HIGH if it is left floating.

A second pull-up, called the ‘weak’ pull-up, is turned on when the pin latch for the pin contains a logic 1 and the pin itself is also at a logic 1 level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting a 1. If this pin is pulled LOW by an external device, the weak pull-up turns off, and only the very weak pull-up remains on. In order to pull the pin LOW under these conditions, the external device has to sink enough current to overpower the weak pull-up and pull the pin below its input threshold voltage.

The third pull-up is referred to as the ‘strong’ pull-up. This pull-up is used to speed up LOW-to-HIGH transitions on a quasi-bidirectional pin when the pin latch changes from a logic 0 to a logic 1. When this occurs, the strong pull-up turns on for two system clock cycles quickly pulling the pin HIGH.

The quasi-bidirectional pin configuration is shown in Figure 6.

Although the SC18IS600/601 is a 3 V device, most of the pins are 5 V tolerant. If 5 V is applied to a pin configured in quasi-bidirectional mode, there will be a current flowing from the pin to V_{DD} causing extra power consumption. Therefore, applying 5 V to pins configured in quasi-bidirectional mode is discouraged.

A quasi-bidirectional pin has a Schmitt-triggered input that also has a glitch suppression circuit.

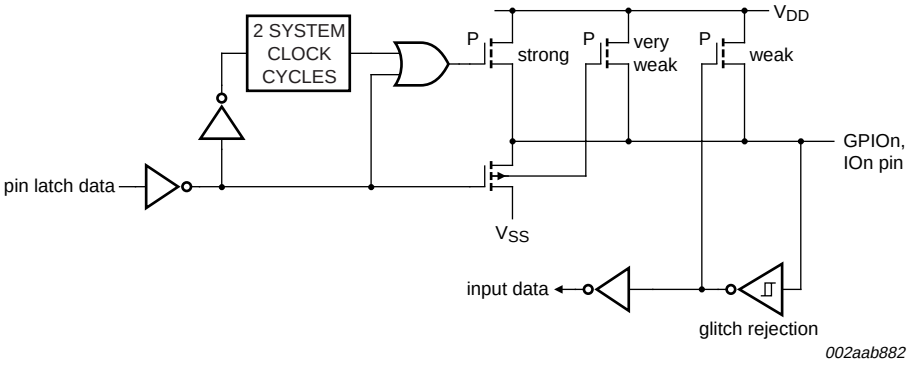


Fig 6. Quasi-bidirectional output configuration

6.2.1.2 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the pin when the pin latch contains a logic 0. To be used as a logic output, a pin configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}. The pull-down for this mode is the same as for the quasi-bidirectional mode.

The open-drain pin configuration is shown in Figure 7.

An open-drain pin has a Schmitt-triggered input that also has a glitch suppression circuit.

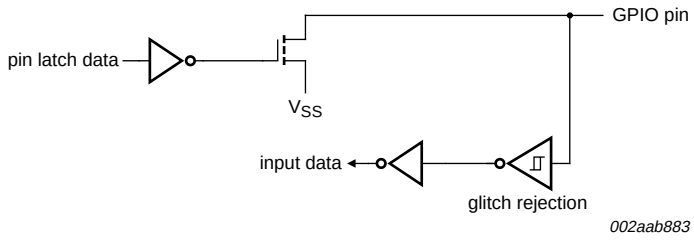


Fig 7. Open-drain output configuration

6.2.1.3 Input-only configuration

The input-only pin configuration is shown in Figure 8. It is a Schmitt-triggered input that also has a glitch suppression circuit.

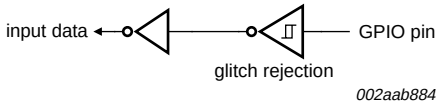


Fig 8. Input-only configuration

6.2.1.4 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the pin latch contains a logic 1. The push-pull mode may be used when more source current is needed from a pin output.

The push-pull pin configuration is shown in Figure 9.

A push-pull pin has a Schmitt-triggered input that also has a glitch suppression circuit.

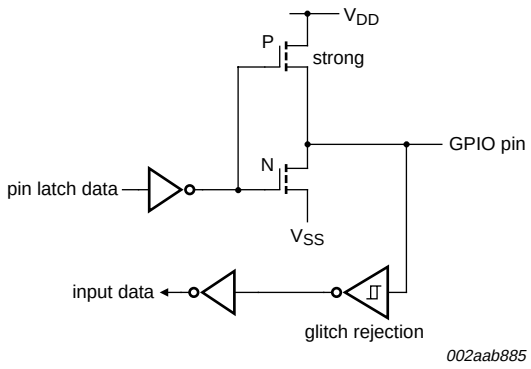


Fig 9. Push-pull output configuration

6.2.2 I/O pins state register (IOState)

When read, this register returns the actual state of all programmable and quasi-bidirectional I/O pins. When written, each register bit will be transferred to the corresponding I/O pin programmed as output.

Table 5. IOState - I/O pins state register (address 0x01) bit description

Bit	Symbol	Description
7:6	-	reserved
5	IO5	Set the logic level on the output pins.
4	IO4	Write to this register:
3	GPIO3 (SC18IS600 only)	logic 0 = set output pin to zero
2	GPIO2	logic 1 = set output pin to one
1	GPIO1	A read from this register returns states of all pins.
0	GPIO0	

6.2.3 I²C-bus address register (I2CAdr)

The contents of the register represents the device's own I²C-bus address. The most significant bit corresponds to the first bit received from the I²C-bus after a START condition. The least significant bit is not used, but should be programmed with a '0'.

I2CAdr is not needed for device operation, but should be configured so that its address does not conflict with an I²C-bus device address used by the bus master.

6.2.4 I²C-bus clock rates register (I2CClk)

This register determines the I²C-bus clock frequency. Various clock rates are shown in Table 6 for the SC18IS600. The frequency can be determined using Equation 1:

$$I^2C\text{-}bus\ clock\ frequency = \frac{7.3728 \times 10^6}{4 \times I2CClk}(Hz) \quad (1)$$

The I²C-bus clock frequency for the SC18IS601 can be determined using Equation 2:

$$I^2C\text{-}bus\ clock\ frequency = \frac{CLKIN}{4 \times I2CClk}(Hz) \quad (2)$$

Table 6. I²C-bus clock frequency example at 7.3728 MHz

I2CClk (decimal)	I²C-bus clock frequency
5 (minimum)	369 kHz
7	263 kHz
9	204 kHz
19	97 kHz
255 (maximum)	7.2 kHz

6.2.5 I²C-bus time-out register (I2CTO)

The time-out register is used to determine the maximum time that the I²C-bus master is allowed to complete a transfer before setting an I²C-bus time-out interrupt.

Table 7. I2CTO - I²C-bus time-out register (address 0x04) bit description

Bit	Symbol	Description
7:1	TO[7:1]	Time-out value
0	TE	Enable/disable time-out function logic 0 = disable logic 1 = enable

The least significant bit of I2CTO (TE bit) is used as a time-out enable/disable. A logic 1 will enable the time-out function.

On the SC18IS600 the time-out oscillator operates at 57.6 kHz. For the SC18IS601 the time-out oscillator frequency can be determined using Equation 3:

$$Time\text{-}out\ oscillator\ frequency = \frac{CLKIN}{128}(Hz) \quad (3)$$

This oscillator is fed into a 16-bit down counter. The down counter's lower nine bits are loaded with '1', while the upper seven bits are loaded with the contents of I2CTO.

Fig 10. Time-out value

The time-out value is an approximate value.

In the case of arbitration loss, the SC18IS600/601 will transmit a START condition when the bus becomes free unless the time-out condition is reached. If the time-out condition is reached, an interrupt will be generated on the $\overline{INT}$ pin. The 'I²C-bus time-out' status can be read in I2CStat.

6.2.6 I²C-bus status register (I2CStat)

This register reports the results of I²C-bus transmit and receive transaction between SC18IS600/601 and an I²C-bus slave device.

Table 8. I²C-bus status

Register value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	I²C-bus status description
0xF0	1	1	1	1	0	0	0	0	Transmission successful. The SC18IS600/601 has successfully completed an I²C-bus read or write transaction. An interrupt is generated on $\overline{INT}$. This is also the default status after reset. No interrupt is generated after reset.
0xF1	1	1	1	1	0	0	0	1	I²C-bus device address not acknowledged. No I²C-bus slave device has acknowledged the slave address that has been sent out in an I²C-bus read or write transaction. An interrupt is generated on $\overline{INT}$.
0xF2	1	1	1	1	0	0	1	0	I²C-bus device address not acknowledged. An I²C-bus slave has not acknowledged the byte that has just been transmitted by the SC18IS600/601. An interrupt is generated on $\overline{INT}$.
0xF3	1	1	1	1	0	0	1	1	I²C-bus busy. The SC18IS600/601 is busy performing an I²C-bus transaction, no new transaction should be initiated by the host. No interrupt is generated.
0xF8	1	1	1	1	1	0	0	0	I²C-bus time-out (see Section 6.2.5 "I²C-bus time-out register (I2CTO)"). The SC18IS600/601 has started an I²C-bus transaction that has taken longer than the time programmed in I2CTO register. This could happen after a period of unsuccessful arbitration or when an I²C-bus slave is (continuously) pulling the SCL clock LOW. An interrupt is generated on $\overline{INT}$.)
0xF9	1	1	1	1	1	0	0	1	I²C-bus invalid data count. The number of bytes specified in a read or write command to the SC18IS600/601. An interrupt is generated on $\overline{INT}$.

6.3 External clock input (SC18IS601)

In this device, the processor clock is derived from an external source driving the CLKIN pin. The clock rate may be from 0 Hz up to 18 MHz.

6.4 I²C-bus serial interface

I²C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I²C-bus may be used for test and diagnostic purposes.

A typical I²C-bus configuration is shown in Figure 11. The SC18IS600/601 device provides a byte-oriented I²C-bus interface that supports data transfers up to 400 kHz. (Refer to *UM10204, "I²C-bus specification and user manual"*.)

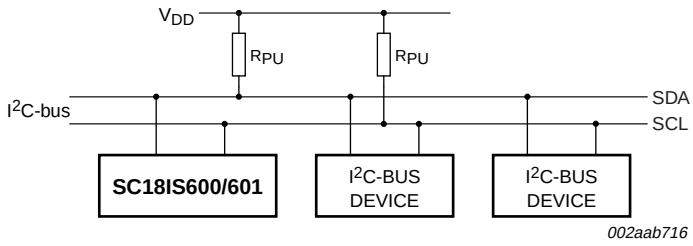


Fig 11. I²C-bus configuration

6.5 Serial Peripheral Interface (SPI)

The host communicates with the SC18IS600/601 via the SPI interface. The SC18IS600/601 operates in Slave mode up to 3 Mbit/s.

The SPI interface has four pins: SCLK, MOSI, MISO, and $\overline{CS}$.

- **SCLK**, **MOSI** and **MISO** are typically tied together between two or more SPI devices. Data flows from the master to the SC18IS600/601 on the MOSI (Master Out Slave In) pin and flows from SC18IS600/601 to the master on the MISO (Master In Slave Out) pin. The SCLK signal is an input to the SC18IS600/601.
- **$\overline{CS}$** is the slave select pin. In a typical configuration, an SPI master selects one SPI device as the current slave. An SPI slave device uses its $\overline{CS}$ pin to determine whether it is selected. The $\overline{CS}$ pin may be tied LOW if it is the only device on the bus.

Typical connections are shown in Figure 12.

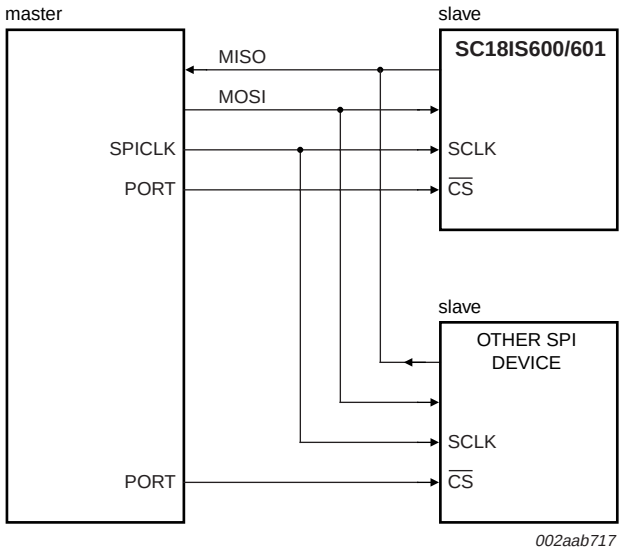


Fig 12. SPI single master multiple slaves configuration

6.6 SPI message format

6.6.1 Write N bytes to I²C-bus slave device

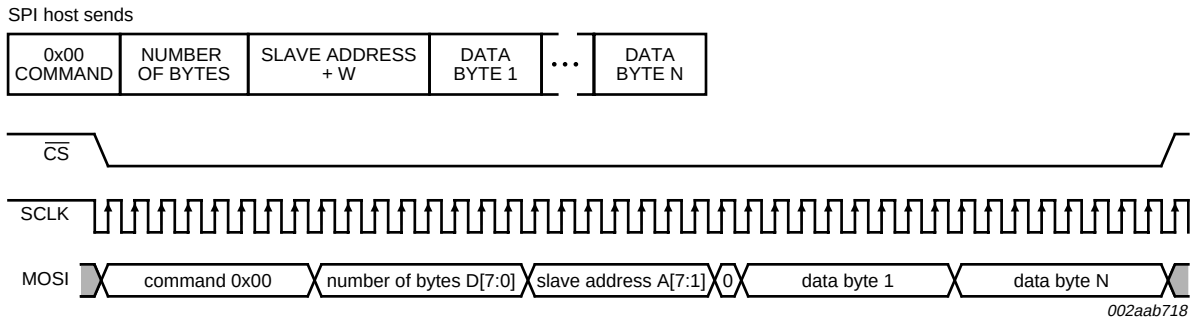


Fig 13. Write N bytes to I²C-bus slave device

The SPI host issues the write command by sending a 0x00 command followed by the total number of bytes (maximum 96 bytes excluding the address) to send and an I²C-bus slave device address followed by I²C-bus data bytes, beginning with the first byte (data byte 1) and ending with the last byte (data byte N). Once the SPI host issues this command, the SC18IS600/601 will access the I²C-bus slave device and start sending the I²C-bus data bytes.

When the I²C-bus write transaction has successfully finished, and interrupt is generated on the $\overline{\text{INT}}$ pin, and the 'transaction completed' status can be read in I2CStat.

Note that the third byte sent by the host is the device I²C-bus slave address. The SC18IS600/601 will ignore the least significant bit so a write will always be performed even if the least significant bit is a '1'.

6.6.2 Read N bytes from I²C-bus slave device

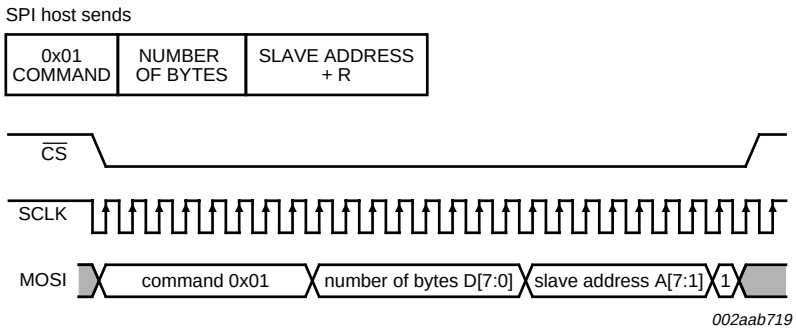


Fig 14. Read N bytes from I²C-bus slave device

Once the host issues this command, the SC18IS600/601 will start an I²C-bus read transaction on the I²C-bus to the specified slave address. Once the data is received, the SC18IS600/601 will place this data in the receiver buffer, and will generate an interrupt on the $\overline{INT}$ pin. The 'transaction completed' status can be read in the I2CStat. Note that the data is not returned until a Read Buffer command is performed (see Section 6.6.4 "Read buffer").

Note that the third byte sent by the host is the device slave address. The SC18IS600/601 will ignore the least significant bit so a read will always be performed even if the least significant bit is a '0'. The maximum number of bytes to be read is 96.

6.6.3 I²C-bus read after write

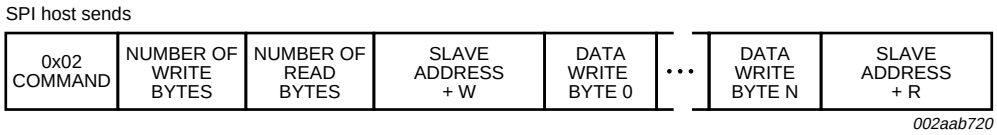


Fig 15. I²C-bus read after write

Once the host issues this command, the SC18IS600/601 will start a write transaction on the I²C-bus to the specified slave address. Once the data is written, the SC18IS600/601 will read data from the specified slave, place the data in the Receiver Buffer and generate an interrupt on the $\overline{INT}$ pin. The 'transaction completed' status can be read in I2CStat. Note that the data is not returned until a 'Read Buffer' command is performed.

6.6.4 Read buffer

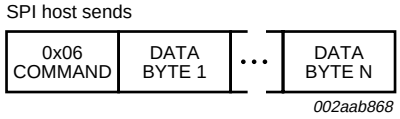


Fig 16. Read buffer

When the host issues a Read Buffer command, the SC18IS600/601 will return the data in the Read Buffer on the MISO pin. Note that the Read Buffer will be overwritten if an additional 'Read N bytes' or a 'Read after write' command is executed before the Read Buffer command.

6.6.5 I²C-bus write after write

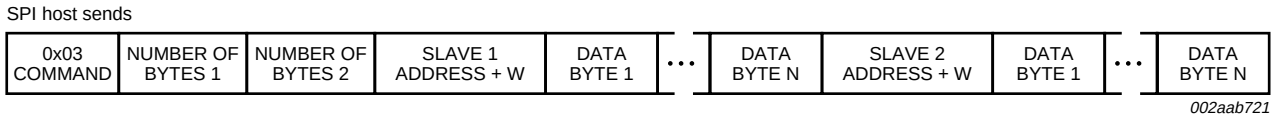


Fig 17. Write after write

When the host issues this command, the SC18IS600/601 will first write N data bytes to the I²C-bus slave 1 device followed by a write of M data bytes to the I²C-bus slave 2 device.

6.6.6 SPI configuration

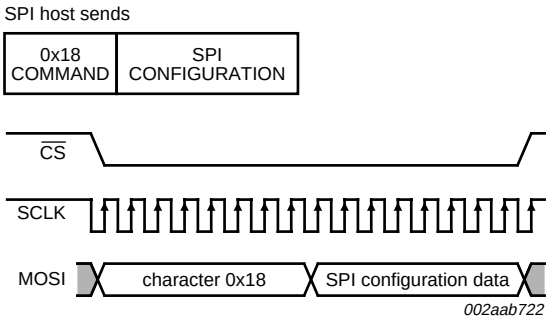


Fig 18. SPI configuration

Table 9. SPI configuration

SPI configuration	Data order
0x81	LSB first
0x42	MSB first (default)

The SPI configuration command can be used to change the order in which the bits of SPI data byte are sent on the SPI bus. In the LSB first configuration (SPI configuration data is 0x81), bit 0 is the first bit sent of any SPI byte. In MSB first (SPI configuration data is 0x42), bit 7 is the first bit sent. Table 9 shows the two possible configurations that can be programmed.

6.6.7 Write to SC18IS600/601 internal registers

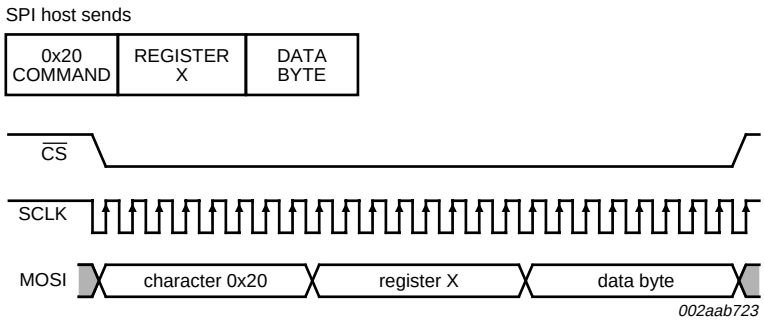


Fig 19. Write to SC18IS600/601 internal registers

A Write Register function is initiated by sending a 0x20 command followed by an internal register address to be written (see Section 6.1). The register data byte follows the register address. Only one register can be accessed in a single transaction. There is no auto-incrementing of the register address.

6.6.8 Read from SC18IS600/601 internal register

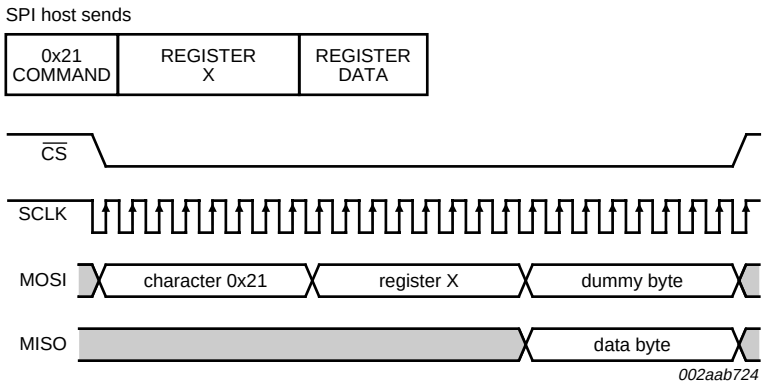


Fig 20. Read from SC18IS600/601 internal register

A Read Register function is initiated by sending a 0x21 command followed by an internal register address to be read (see Section 6.1) and a dummy byte. The data byte of the read register is returned by the SC18IS600 on the MISO pin. Only one register can be accessed in a single transaction. There is no auto-incrementing of the register address.

Note that write and read from internal registers are processed immediately as soon as the SC18IS600/601 determines the intended register.

6.6.9 Power-down mode

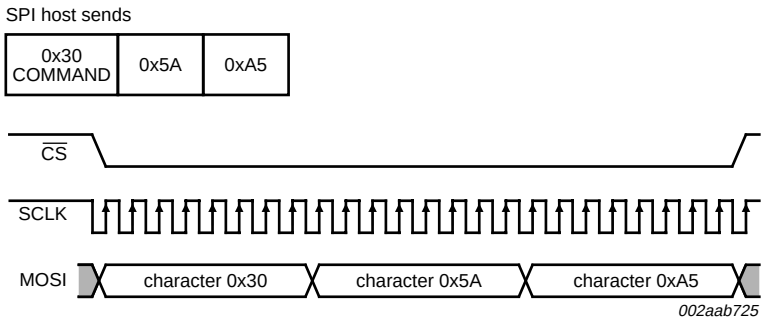


Fig 21. Power-down mode

The SC18IS600/601 can be placed in a low-power mode where the internal oscillator is stopped and it will no longer respond to SPI messages. Enter the Power-down mode by sending the power-down command (0x30) followed by the two defined bytes, which are 0x5A followed by 0xA5. If the exact message is not received, the device will not enter the power-down state.

Before entering the power-down state, $\overline{\text{WAKEUP}}$/IO4 should be placed in a HIGH state. To exit the power-down state, the $\overline{\text{WAKEUP}}$/IO4 should be brought LOW. After leaving the power-down state, the $\overline{\text{WAKEUP}}$/IO4 can once again be used as a general-purpose IO pin.

7. Limiting values

Table 10. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1][2]

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature	operating	–55	+125	°C
T_{stg}	storage temperature		–65	+150	°C
V_n	voltage on any other pin	referenced to V_{SS}	–0.5	+5.5	V
$I_{OH(I/O)}$	HIGH-level output current per input/output pin		-	8	mA
$I_{OL(I/O)}$	LOW-level output current per input/output pin		-	20	mA
$I_{I/O(tot)(max)}$	maximum total I/O current		-	120	mA
P_{tot}/pack	total power dissipation per package	[3]	-	1.5	W

[1] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

[2] Parameters are valid over the operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[3] Based on package heat transfer, not device power consumption.

8. Static characteristics

Table 11. Static characteristics

V_{DD} = 2.4 V to 3.6 V; T_{amb} = −40 °C to +85 °C (industrial); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(oper)}$	operating supply current	V_{DD} = 3.6 V; f = 12 MHz		-	7	13	mA
		V_{DD} = 3.6 V; f = 18 MHz		-	11	16	mA
$I_{DD(idle)}$	Idle mode supply current	V_{DD} = 3.6 V; f = 12 MHz		-	3.6	4.8	mA
		V_{DD} = 3.6 V; f = 18 MHz		-	4	6	mA
$I_{DD(tpd)}$	total Power-down mode supply current	V_{DD} = 3.6 V; industrial		-	< 0.1	5	µA
		V_{DD} = 3.6 V; extended		-	-	50	µA
$V_{th(HL)}$	HIGH-LOW threshold voltage	Schmitt trigger input		$0.22V_{DD}$	$0.4V_{DD}$	-	V
$V_{th(LH)}$	LOW-HIGH threshold voltage	Schmitt trigger input		-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{hys}	hysteresis voltage			-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage	all pins; I_{OL} = 20 mA		-	0.6	1.0	V
		all pins; I_{OL} = 10 mA		-	0.3	0.5	V
		all pins; I_{OL} = 3.2 mA		-	0.2	0.3	V
V_{OH}	HIGH-level output voltage	all pins; I_{OH} = −8 mA; push-pull mode		V_{DD} − 1	-	-	V
		all pins; I_{OH} = −3.2 mA; push-pull mode		V_{DD} − 0.7	V_{DD} − 0.4	-	V
		all pins; I_{OH} = −20 µA; quasi-bidirectional mode		V_{DD} − 0.3	V_{DD} − 0.2	-	V
C_{ig}	input capacitance at gate		[2]	-	-	15	pF
I_{IL}	LOW-level input current	logical 0; V_I = 0.4 V	[3]	-	-	−80	µA
I_{LI}	input leakage current	all ports; $V_I = V_{IL}$ or V_{IH}	[4]	-	-	±10	µA
I_{THL}	HIGH-LOW transition current	all ports; logical 1-to-0; V_I = 2.0 V at V_{DD} = 3.6 V	[5][6]	−30	-	−450	µA
$R_{RESET\_N(int)}$	internal pull-up resistance on pin $\overline{\text{RESET}}$			10	-	30	kΩ

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] Pin capacitance is characterized but not tested.

[3] Measured with pins in quasi-bidirectional mode.

[4] Measured with pins in high-impedance mode.

[5] Pins in quasi-bidirectional mode with weak pull-up (applies to all pins with pull-ups).

[6] Pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

9. Dynamic characteristics

Table 12. Dynamic characteristics

V_{DD} = 2.4 V to 3.6 V; T_{amb} = −40 °C to +85 °C (industrial); unless otherwise specified.[1]

Symbol	Parameter	Conditions		Variable clock		f_{osc} = 12 MHz		Unit
				Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	SC18IS600; nominal f = 7.3728 MHz; trimmed to ±1 % at T_{amb} = 25 °C		7.189	7.557	7.189	7.557	MHz
External clock input (SC18IS601); see Figure 23								
f_{osc}	oscillator frequency	V_{DD} = 2.4 V to 3.6 V		0	12	-	-	MHz
T_{CLCL}	clock cycle time			83	-	-	-	ns
t_{CHCX}	clock HIGH time			22	$T_{CLCL} - t_{CLCX}$	22	-	ns
t_{CLCX}	clock LOW time			22	$T_{CLCL} - t_{CHCX}$	22	-	ns
t_{CLCH}	clock rise time			-	8	-	8	ns
t_{CHCL}	clock fall time			-	8	-	8	ns
Glitch filter								
t_{gr}	glitch rejection time	$\overline{RESET}$ pin	[2]	-	50	-	50	ns
		any pin except $\overline{RESET}$	[2]	-	15	-	15	ns
t_{sa}	signal acceptance time	$\overline{RESET}$ pin		125	-	125	-	ns
		any pin except $\overline{RESET}$		50	-	50	-	ns
SPI slave interface								
f_{SPI}	SPI operating frequency	2.0 MHz		0	$^{fosc}/_{6}$	0	2.0	MHz
T_{SPICYC}	SPI cycle time	2.0 MHz		$^{6}/_{fosc}$	-	500	-	ns
$t_{SPILEAD}$	SPI enable lead time	2.0 MHz		4	-	4	-	µs
t_{SPILAG}	SPI enable lag time			4	-	4	-	µs
t_{SCLKH}	SCLK HIGH time			$^{3}/_{fosc}$	-	190	-	ns
t_{SCLKL}	SCLK LOW time			$^{3}/_{fosc}$	-	190	-	ns
t_{SPIDSU}	SPI data set-up time			100	-	100	-	ns
t_{SPIDH}	SPI data hold time			100	-	100	-	ns
t_{SPIA}	SPI access time			0	120	0	120	ns
t_{SPIDIS}	SPI disable time	2.0 MHz		0	240	-	240	ns
t_{SPIDV}	SPI enable to output data valid time	2.0 MHz		0	240	-	240	ns
		3.0 MHz		0	167	-	167	ns
t_{SPIOH}	SPI output data hold time			0	-	0	-	ns
t_{SPIR}	SPI rise time	SPI outputs (SCLK, MOSI, MISO)		-	100	-	100	ns
		SPI inputs (SCLK, MOSI, MISO, $\overline{CS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	SPI outputs (SCLK, MOSI, MISO)		-	100	-	100	ns
		SPI inputs (SCLK, MOSI, MISO, $\overline{CS}$)		-	2000	-	2000	ns

[1] Parameters are valid over operating temperature range unless otherwise specified. Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

[2] SCL and SDA do not have glitch suppression circuits.

Table 13. Dynamic characteristics

V_{DD} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C (industrial); unless otherwise specified.[1]

Symbol	Parameter	Conditions		Variable clock		f_{osc} = 18 MHz		Unit
				Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	SC18IS600; nominal f = 7.3728 MHz; trimmed to ±1 % at T_{amb} = 25 °C		7.189	7.557	7.189	7.557	MHz
External clock input (SC18IS601); see Figure 23								
f_{osc}	oscillator frequency			0	18	-	-	MHz
T_{CLCL}	clock cycle time			55	-	-	-	ns
t_{CHCX}	clock HIGH time			22	$T_{CLCL} - t_{CLCX}$	22	-	ns
t_{CLCX}	clock LOW time			22	$T_{CLCL} - t_{CHCX}$	22	-	ns
t_{CLCH}	clock rise time			-	5	-	5	ns
t_{CHCL}	clock fall time			-	5	-	5	ns
Glitch filter								
t_{gr}	glitch rejection time	$\overline{RESET}$ pin	[2]	-	50	-	50	ns
		any pin except $\overline{RESET}$	[2]	-	15	-	15	ns
t_{sa}	signal acceptance time	$\overline{RESET}$ pin		125	-	125	-	ns
		any pin except $\overline{RESET}$		50	-	50	-	ns
SPI slave interface								
f_{SPI}	SPI operating frequency	3.0 MHz		0	$f_{osc}/6$	0	3	MHz
T_{SPICYC}	SPI cycle time	3.0 MHz		$6/f_{osc}$	-	333	-	ns
$t_{SPILEAD}$	SPI enable lead time	3.0 MHz		4	-	4	-	µs
t_{SPILAG}	SPI enable lag time	3.0 MHz		4	-	4	-	µs
t_{SCLKH}	SCLK HIGH time			$3/f_{osc}$	-	167	-	ns
t_{SCLKL}	SCLK LOW time			$3/f_{osc}$	-	167	-	ns
t_{SPIDSU}	SPI data set-up time			100	-	100	-	ns
t_{SPIDH}	SPI data hold time			100	-	100	-	ns
t_{SPIA}	SPI access time			0	80	0	80	ns
t_{SPIDIS}	SPI disable time	3.0 MHz		0	160	-	160	ns
t_{SPIDV}	SPI enable to output data valid time	3.0 MHz		0	160	-	160	ns
t_{SPIOH}	SPI output data hold time			0	-	0	-	ns
t_{SPIR}	SPI rise time	SPI outputs (SCLK, MOSI, MISO)		-	100	-	100	ns
		SPI inputs (SCLK, MOSI, MISO, $\overline{CS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	SPI outputs (SCLK, MOSI, MISO)		-	100	-	100	ns
		SPI inputs (SCLK, MOSI, MISO, $\overline{CS}$)		-	2000	-	2000	ns

[1] Parameters are valid over operating temperature range unless otherwise specified. Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

[2] SCL and SDA do not have glitch suppression circuits.

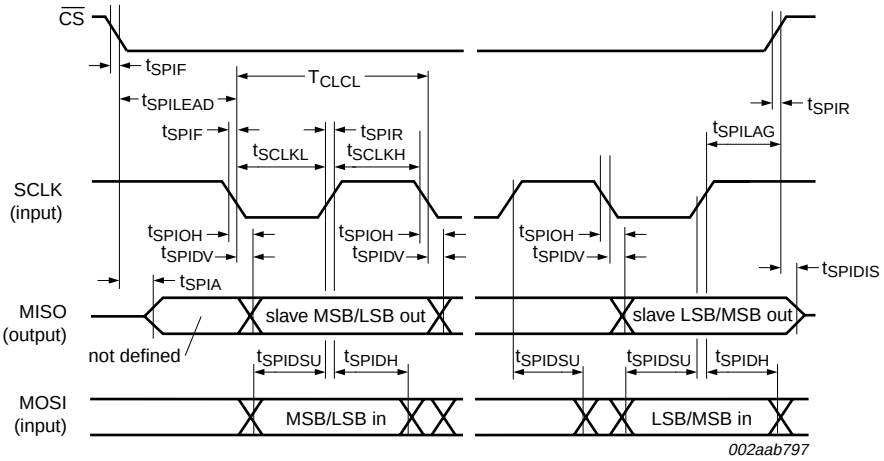


Fig 22. SPI slave timing (Mode 3)

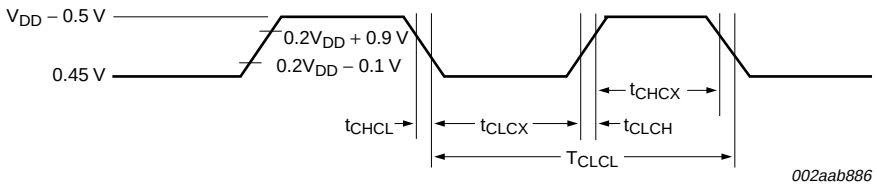


Fig 23. External clock timing

Table 14. Additional SPI AC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SPICLKW}$	SPICLK HIGH time	between two SPI bytes	8	-	-	µs
t_{CSW}	$\overline{CS}$ HIGH time	between two SPI transactions	refer to Figure 25			µs
$t_{SPILAG1}$	SPI enable lag time 1	in a SPI to I²C-bus transaction	refer to Figure 26			µs
t_d	delay time	from last SCLK pulse to SDA LOW in a SPI to I²C-bus transaction	refer to Figure 27			µs

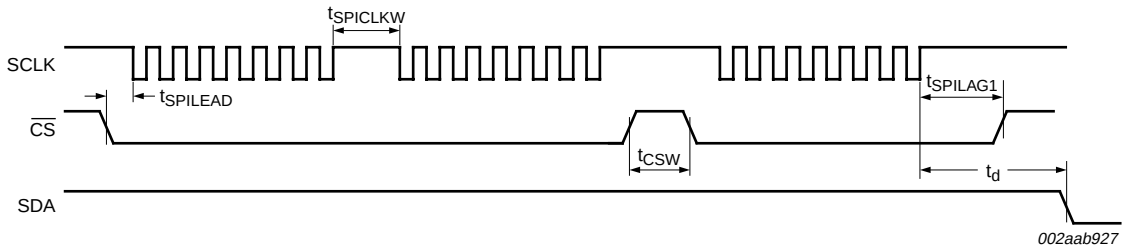


Fig 24. SPI to I²C-bus timing diagram

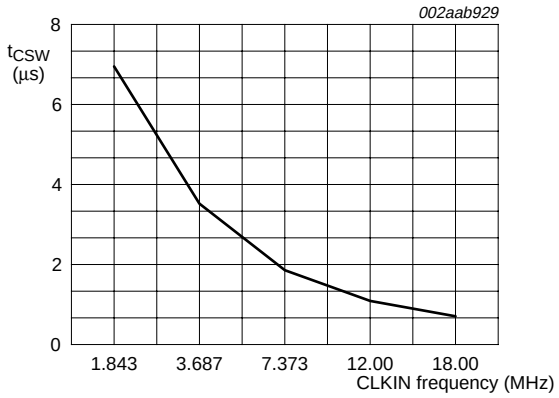


Fig 25. t_{CSW} as a function of CLKIN frequency

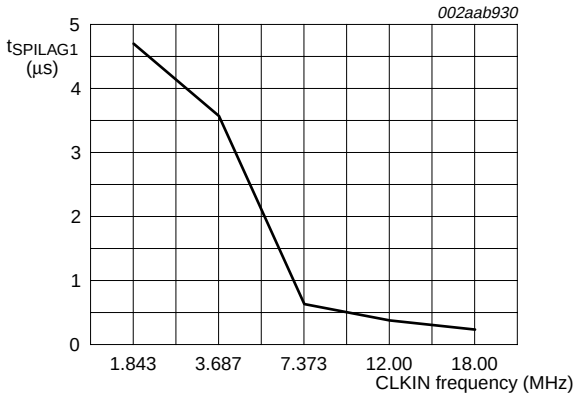


Fig 26. $t_{SPILAG1}$ as a function of CLKIN frequency

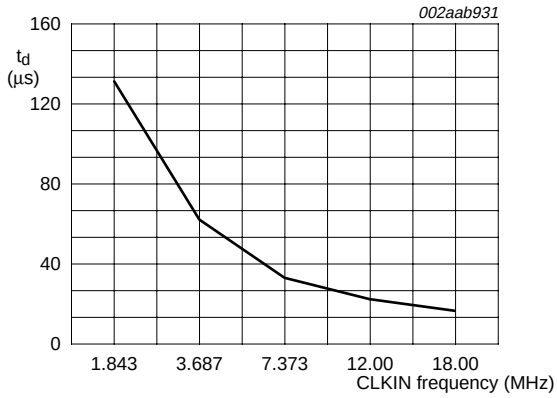
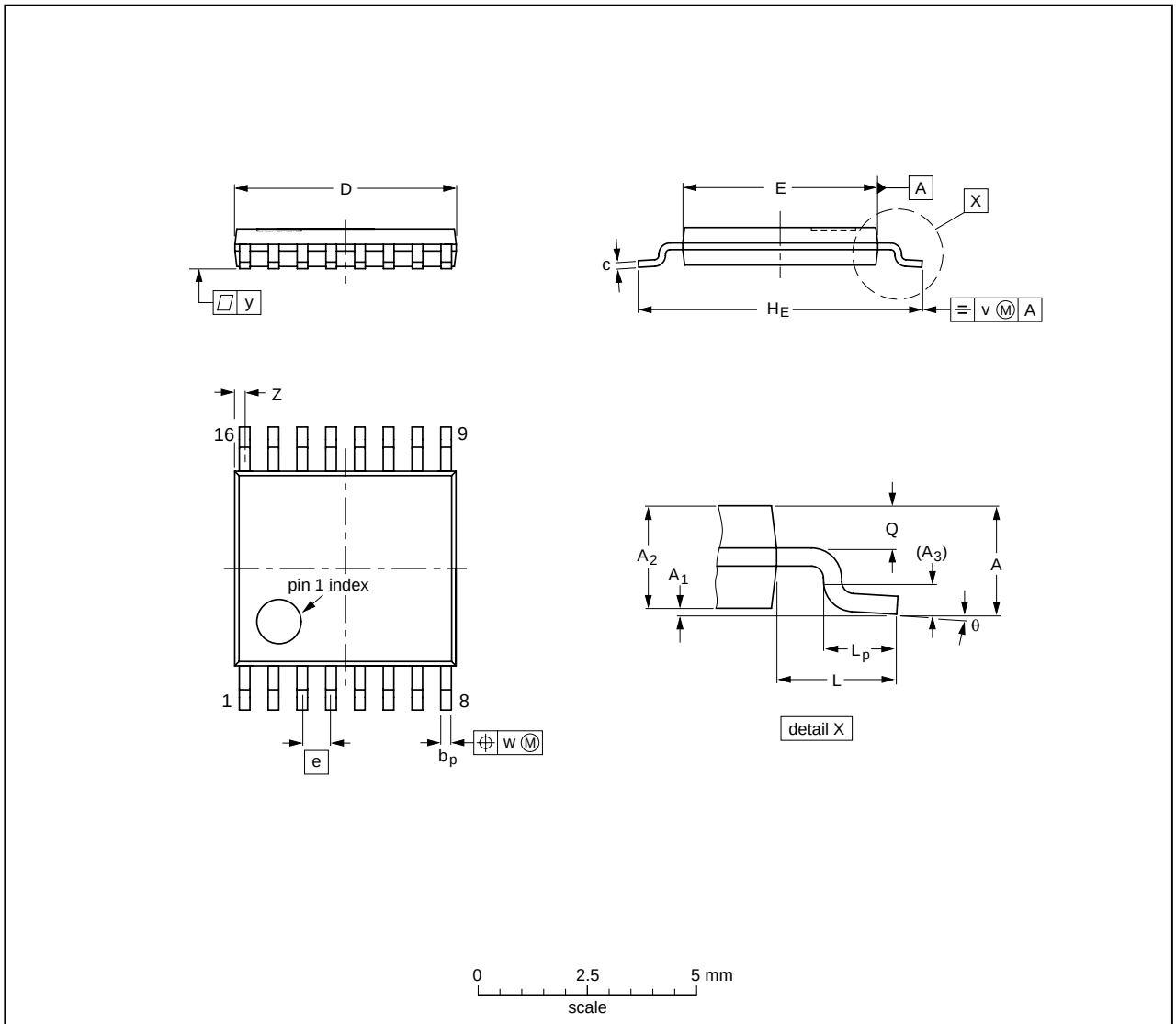


Fig 27. t_d as a function of CLKIN frequency

10. Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

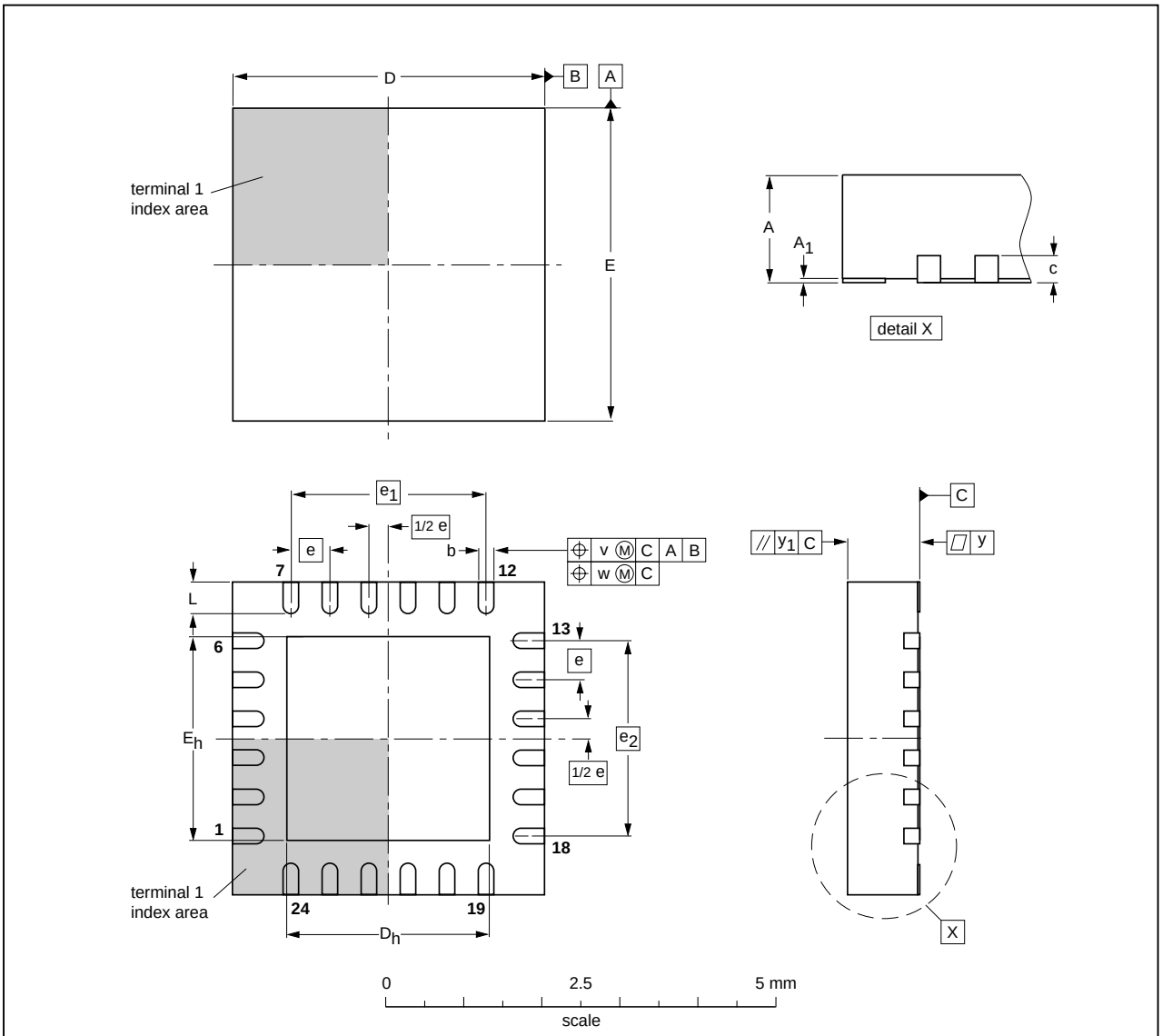
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 28. Package outline SOT403-1 (TSSOP16)

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.75 2.45	4.1 3.9	2.75 2.45	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-3	- - -	MO-220	- - -			~~04-11-19~~ 05-03-10

Fig 29. Package outline SOT616-3 (HVQFN24)

11. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

11.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

11.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

11.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

11.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 30) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 15 and 16

Table 15. SnPb eutectic process (from J-STD-020C)

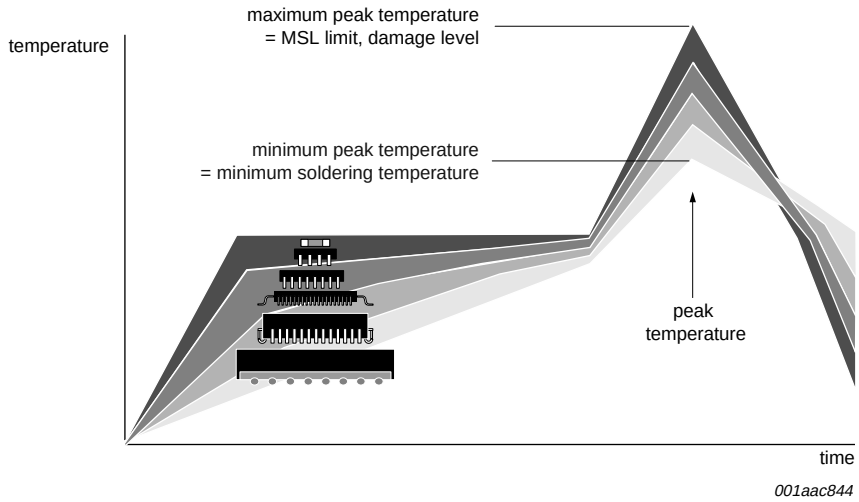
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 16. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 30.



MSL: Moisture Sensitivity Level

Fig 30. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

12. Abbreviations

Table 17. Abbreviations

Acronym	Description
ASCII	American Standard Code for Information Interchange
CPU	Central Processing Unit
GPIO	General Purpose Input/Output
I/O	Input/Output
I²C-bus	Inter-Integrated Circuit bus
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed-Circuit Board
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter

13. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SC18IS600_601_5	20080728	Product data sheet	-	SC18IS600_601_4
Modifications:	• Table 9 “SPI configuration”: – SPI configuration for LSB first data order changed from “0x42” to “0x81” – SPI configuration for MSB first data order changed from “0x81” to “0x42” • Section 6.6.6 “SPI configuration”, first paragraph: – 2nd sentence: changed from “0x42” to “0x81” – 3rd sentence: changed from “0x81” to “0x42”			
SC18IS600_601_4	20080320	Product data sheet	-	SC18IS600_601_3
SC18IS600_601_3	20061213	Product data sheet	-	SC18IS600_601_2
SC18IS600_601_2	20060811	Product data sheet	-	SC18IS600_601_1
SC18IS600_601_1	20060224	Product data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

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Date of release: 28 July 2008
Document identifier: SC18IS600_601_5