1 MEG UVEPROM

UV Erasable Programmable Read-Only Memory

AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-89614
- MIL-STD-883

FEATURES

- Organized 131,072 x 8
- Single +5V ±10% power supply
- Operationally compatible with existing megabit EPROMs
- Industry standard 32-pin ceramic dual-in-line package
- All inputs/outputs fully TTL compatible
- 8-bit output for use in microprocessor-based systems
- Very high-speed SNAP! Pulse Programming
- Power-saving CMOS technology
- 3-state output buffers
- 400mV minimum DC noise immunity with standard TTL loads
- Latchup immunity of 250 mA on all input and output pins
- No pullup resistors required
- Low power dissipation (Vcc = 5.5V)
  - ✓Active - 165 mW Worst Case
  - ✓Standby - 0.55 mW Worst Case (CMOS-input levels)

OPTIONS	MARKING	
• Timing		
120ns access	-12	
150ns access	-15	
200ns access	-20	
• Package(s)		
Ceramic DIP (600mils)	J or ECA	No. 114
• Operating Temperature Ranges		
Military (-55°C to +125°C)	M	

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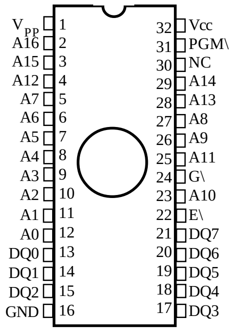
PIN ASSIGNMENT
(Top View)

32-Pin DIP (J)
(600 MIL)



Pin Name	Function
A0 - A18	Address Inputs
DA0-DQ7	Inputs (programming)/Outputs
E\	Chip Enable
G\	Output Enable
GND	Ground
PGM\	Program
V_{CC}	5V Supply
V_{PP}	13V Power Supply*

**Only in program mode.*

GENERAL DESCRIPTION

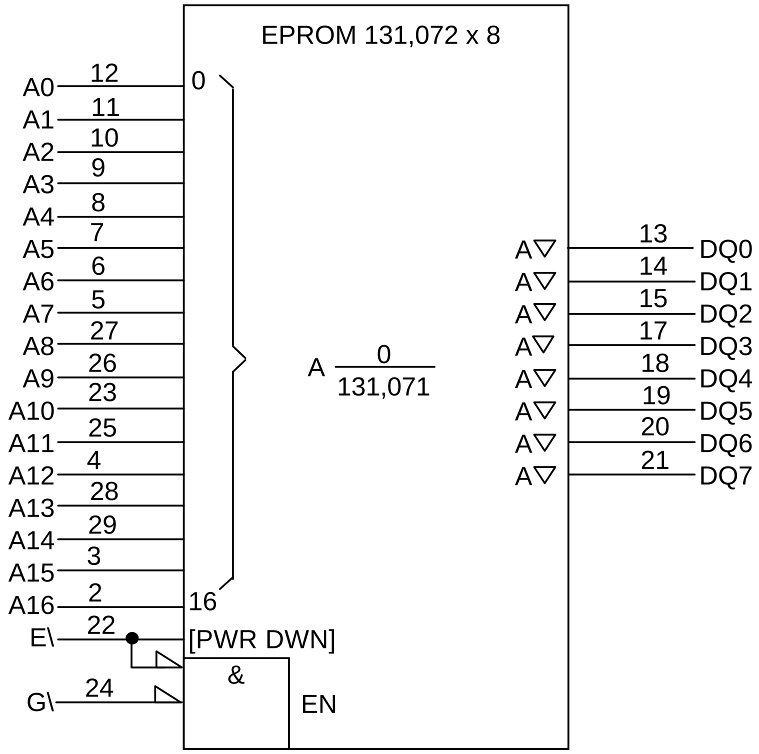
The SMJ27C010A series are 131072 by 8-bit (1048576-bit), ultaviolet (UV) light erasable, electrically programmable read-only memories (EPROMs).

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits without the use of external pullup resistors. Each output can drive one Series 54 TTL circuit without external resistors.

The SMJ27C010A EPROM is offered in a ceramic dual-in-line package (J suffix) designed for insertion in mounting-hole rows on 15.2mm (600mil) centers.

These EPROMs operate from a single 5V supply (in the read mode), and therefore, are ideal for use in microprocessor-based systems. One other 13V supply is needed for programming. All programming signals are TTL level. These devices are programmable using the SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13V and a V_{CC} of 6.5V for a nominal programming time of thirteen seconds. For programming outside the system, existing EPROM programmers can be used. Locations can be programmed singly, in blocks, or at random.

FUNCTIONAL BLOCK DIAGRAM*



* This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. J package illustrated.

OPERATION

The seven modes of operation are listed in Table 1. The read mode requires a single 5V supply. All inputs are TTL level except for V_{PP} during programming (13V for SNAP! Pulse), and 12V on A9 for signature mode.

TABLE 1. OPERATION MODES

FUNCTION	MODE*							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
E\	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
G\	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	X	V_{IL}	
PGM\	X	X	X	V_{IL}	V_{IH}	X	X	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H**	V_H**
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0-DQ7	Data Out	High-Z	High-Z	Data In	Data Out	High-Z	CODE	
							MFG	DEVICE
							97	D6

* X can be V_{IL} or V_{IH}.
**V_H = 12V ± 0.5V

READ/OUTPUT DISABLE

When the outputs of two or more SMJ27C010As are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low level signal is applied to the E\ and G\ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

LATCHUP IMMUNITY

Latchup immunity on the SMJ27C010A is a minimum of 250mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the printed circuit board level when the devices are interfaced to industry-standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

POWER DOWN

Active I_{CC} supply current can be reduced from 30mA to 500µA by applying a high TTL input on E\ and to 100µA by applying a high CMOS input on E\. In this mode all outputs are in the high-impedance state.

ERASURE

Before programming, the SMJ27C010A EPROM is erased by exposing the chip through the transparent lid to a high-intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity x exposure time) is 15-W·s/cm^2. A typical 12-mW/cm^2, filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure; therefore, when using the SMJ27C010A, the window should be covered with an opaque label. After erasure (all bits in logic high state), logic lows are programmed into the desired locations. A programmed low can be erased only by ultraviolet light.

SNAP! PULSE PROGRAMMING

The SMJ27C010A is programmed by using the SNAP! Pulse programming algorithm as illustrated by the flow chart (Figure 1). This algorithm programs in a nominal time of thirteen seconds. Actual programming time varies as a function of the programmer used.

The SNAP! Pulse programming algorithm uses an initial pulse of 100 microseconds (µs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to ten 100µs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13V, V_{CC}= 6.5V, E\ = V_{IL}, and G\ = V_{IH}. Data is presented in parallel (eight bits) on pins DQ0 through DQ7. Once addresses and data are stable, PGM\ is pulsed low.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5V ± 10%.

PROGRAM INHIBIT

Programming can be inhibited by maintaining high level inputs on the E\ or the PGM\ pins.

PROGRAM VERIFY

Programmed bits can be verified with V_{PP} = 13V when G\ = V_{IL}, and E\ = V_{IL}, and PGM\ = V_{IH}.

SIGNATURE MODE

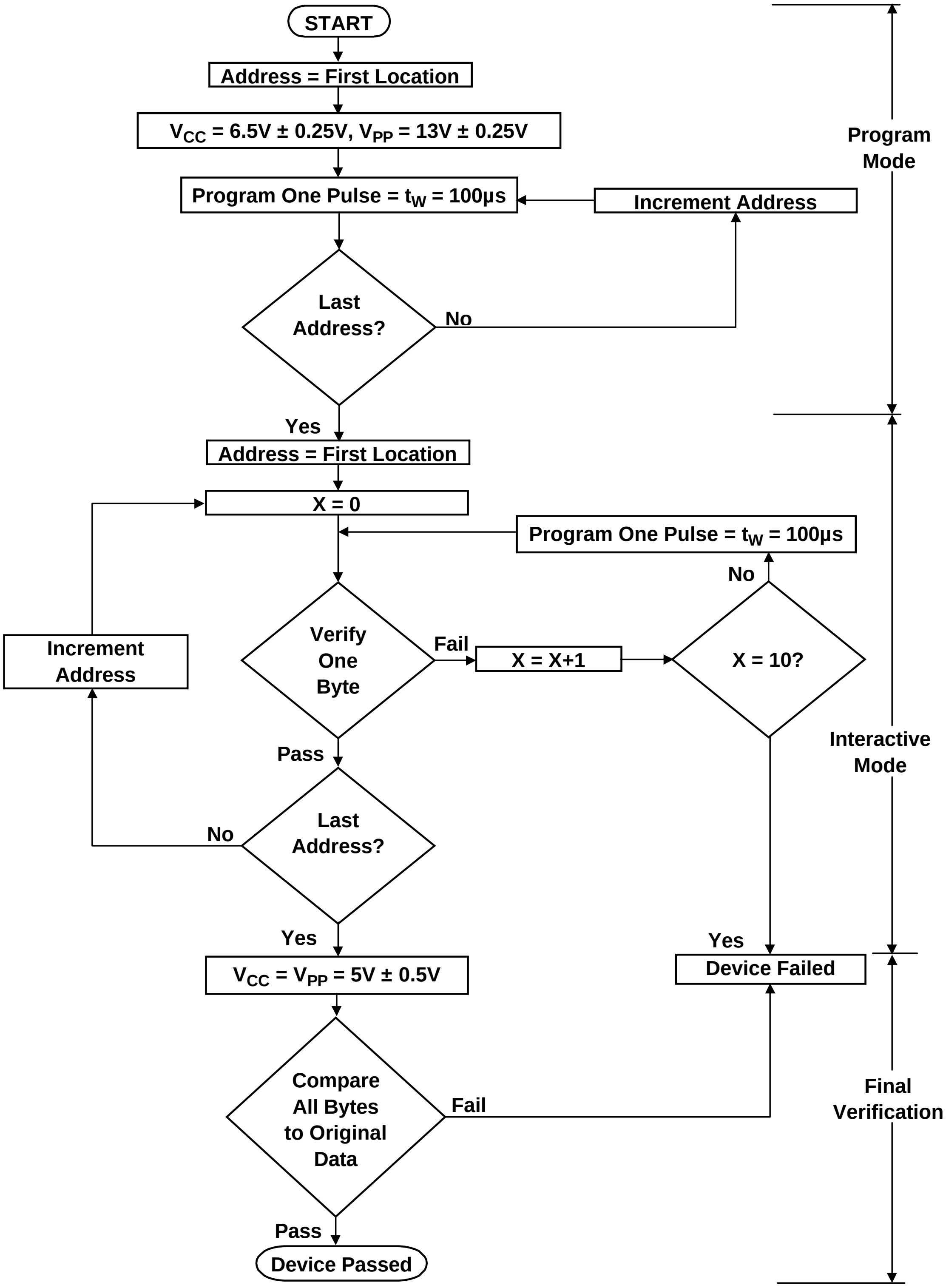
The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 26) is forced to 12V. Two identifier bytes are accessed by toggling A0. All other addresses must be held low. The signature code for these devices is 97D6. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code D6 (Hex), as shown in Table 2.

TABLE 2. SIGNATURE MODES

IDENTIFIER*	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	1	1	0	1	0	1	1	0	D6

* E\ = G\ = V_{IL}, A1 - A8 = V_{IL}, A9 = V_H, A10 - A16 = V_{IL}, V_{PP} = V_{CC}.

FIGURE 1. SNAP! PULSE PROGRAMMING FLOW CHART



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage Range, V_{CC}**...........................-0.6V to +7.0V
Supply Voltage Range, V_{pp}**.........................-0.6V to +14.0V
Input Voltage Range, All inputs except A9**..-0.6V to V_{CC}+1
A9.....-0.6V to +13.5V
Output Voltage Range,
with respect to V_{SS}**..................................-0.6V to V_{CC} +1
Operating Free-air Temperature Range, T_A....-55°C to 125°C
Storage Temperature Range, T_{stg}.....................-65°C to 150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

** All voltage values are with respect to GND.

RECOMMENDED OPERATING CONDITIONS

				MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage	Read Mode[1]		4.5	5	5.5	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	V
V_{PP}	Supply Voltage	Read Mode[2]		V_{CC}-0.6	V_{CC}	V_{CC}+0.6	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	V
V_{IH}	High-level DC input voltage		TTL	2		V_{CC}+0.5	V
			CMOS	V_{CC}-0.2		V_{CC}+0.5	V
V_{IL}	Low-level DC input voltage		TTL	-0.5		0.8	V
			CMOS	-0.5		GND+0.2	V
T_A	Operating free-air temperature			-55		125	°C

NOTES:

1. V_{CC} must be applied before or at the same time as V_{pp} and removed after or at the same time as V_{pp}. The deivce must not be inserted into or removed from the board when V_{pp} or V_{CC} is applied.
2. During programming, V_{pp} must be maintained at 13V ± 0.25V.

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level DC output voltage		I_{OH} = -20µA	V_{CC}-0.2		V
			I_{OH} = -2.5mA	3.5		
V_{OL}	Low-level DC output voltage		I_{OL} = 2.1mA		0.4	V
			I_{OL} = 20µA		0.1	
I_I	Input current (leakage)		V_I = 0V to 5.5V		±1	µA
I_O	Output current (leakage)		V_O = 0V to V_{CC}		±1	µA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5V		10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-Input Level	V_{CC} = 5.5V, E\=V_{IH}		500	µA
		CMOS-Input Level	V_{CC} = 5.5V, E\=V_{CC}±0.2V		100	
I_{CC2}	V_{CC} supply current (active) (output open)		E\=V_{IL}, V_{CC}=5.5V t_{cycle} = minimum cycle time, outputs open[1]		30	mA

NOTES:

1. Minimum cycle time = maximum access time.

CAPACITANCE OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, f = 1MHz*

PARAMETER		TEST CONDITIONS	TYP**	MAX	UNIT
C_I	Input capacitance	$V_I = 0V$, f = 1MHz	4	8	pF
C_O	Output capacitance	$V_O = 0V$, f= 1 MHz	6	10	pF

* Capacitance measurements are made on sample basis only.

** All typical values are at $T_A = 25°C$ and nominal voltages.

SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF OPERATING CONDITIONS[1,2]

PARAMETER		TEST CONDITIONS	-12		-15		-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	$C_L = 100pF$ 1 Series 74 TTL Load, Input $t_r < 20ns$, Input $t_f < 20ns$		120		150		200	ns
$t_{a(E)}$	Access time from chip enable			120		150		200	ns
$t_{en(G)}$	Output enable time from G\			55		75		75	ns
t_{dis}	Output disable time from G\ or E\, whichever occurs first[3]		0	50	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, E\, or G\, whichever occurs first[3]		0		0		0		ns

NOTES:

1. For all switching characteristics, the input pulse levels are 0.4V to 2.4V. Timing measurements are made at 2V for logic high and 0.8V for logic low. (Reference AC testing waveform)
2. Common test conditions apply for t_{dis} except during programming.
3. Value calculated from 0.5V delta to measured output level.

SWITCHING CHARACTERISTICS FOR PROGRAMMING: $V_{CC} = 6.5V$ and $V_{PP} = 13V$ (SNAP! Pulse), $T_A = 25°C$[1]

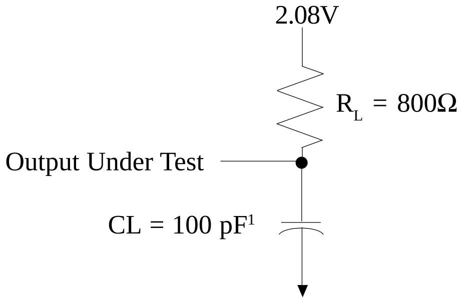
PARAMETER		MIN	MAX	UNIT
$t_{dis(G)}$	Disable, Output disable time from G\	0	130	ns
$t_{en(G)}$	Enable, Output enable time from G\		150	ns

NOTE: 1. For all switching characteristics, the input pulse levels are 0.4V to 2.4V. Timing measurements are made at 2V for logic high and 0.8V for logic low (reference AC testing waveform).

TIMING REQUIREMENTS FOR PROGRAMMING

			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Pulse duration, program	SNAP! Pulse Programming Algorithm	95	100	105	µs
$t_{su(A)}$	Setup Time, Address		2			µs
$t_{su(E)}$	Setup Time, E\		2			µs
$t_{su(G)}$	Setup Time, G\		2			µs
$t_{su(D)}$	Setup Time, Data		2			µs
$t_{su(Vpp)}$	Setup Time, V_{PP}		2			µs
$t_{su(Vcc)}$	Setup Time, V_{CC}		2			µs
$t_{h(A)}$	Hold time, address		0			µs
$t_{h(D)}$	Hold time, data		2			µs

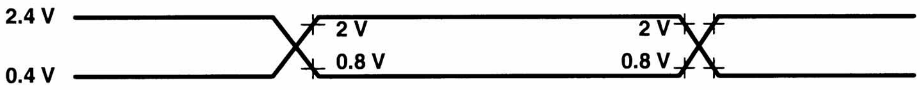
PARAMETER MEASUREMENT INFORMATION



NOTES:

1. C_L includes probe and fixture capacitance.

FIGURE 2. AC TEST OUTPUT LOAD CIRCUIT WAVEFORM



AC testing inputs are driven at 2.4V for logic high and 0.4V for logic low. Timing measurements are made at 2V for logic high and 0.8V for logic low for both inputs and outputs.

FIGURE 3. READ-CYCLE TIMING

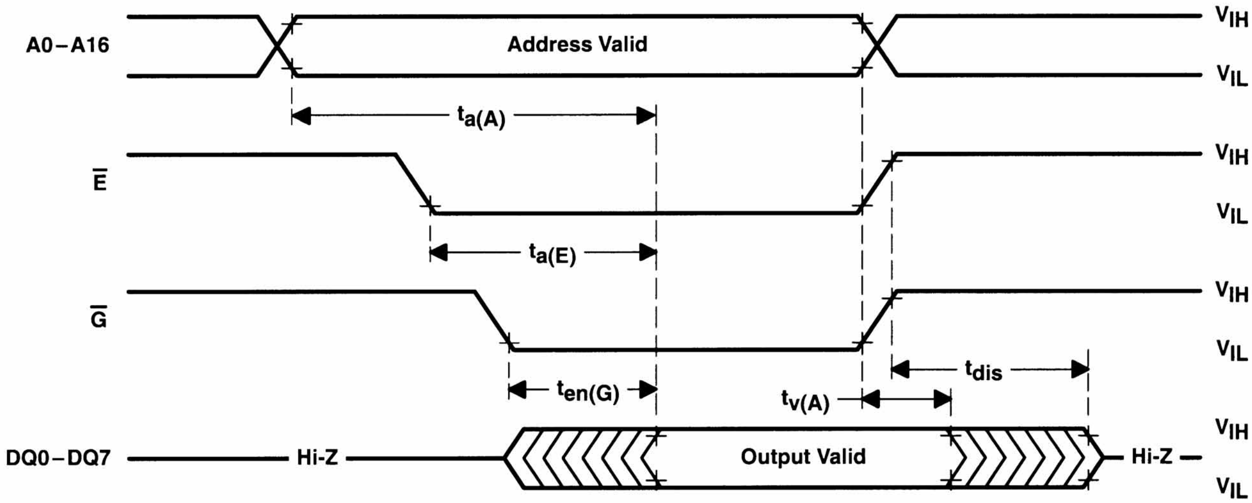
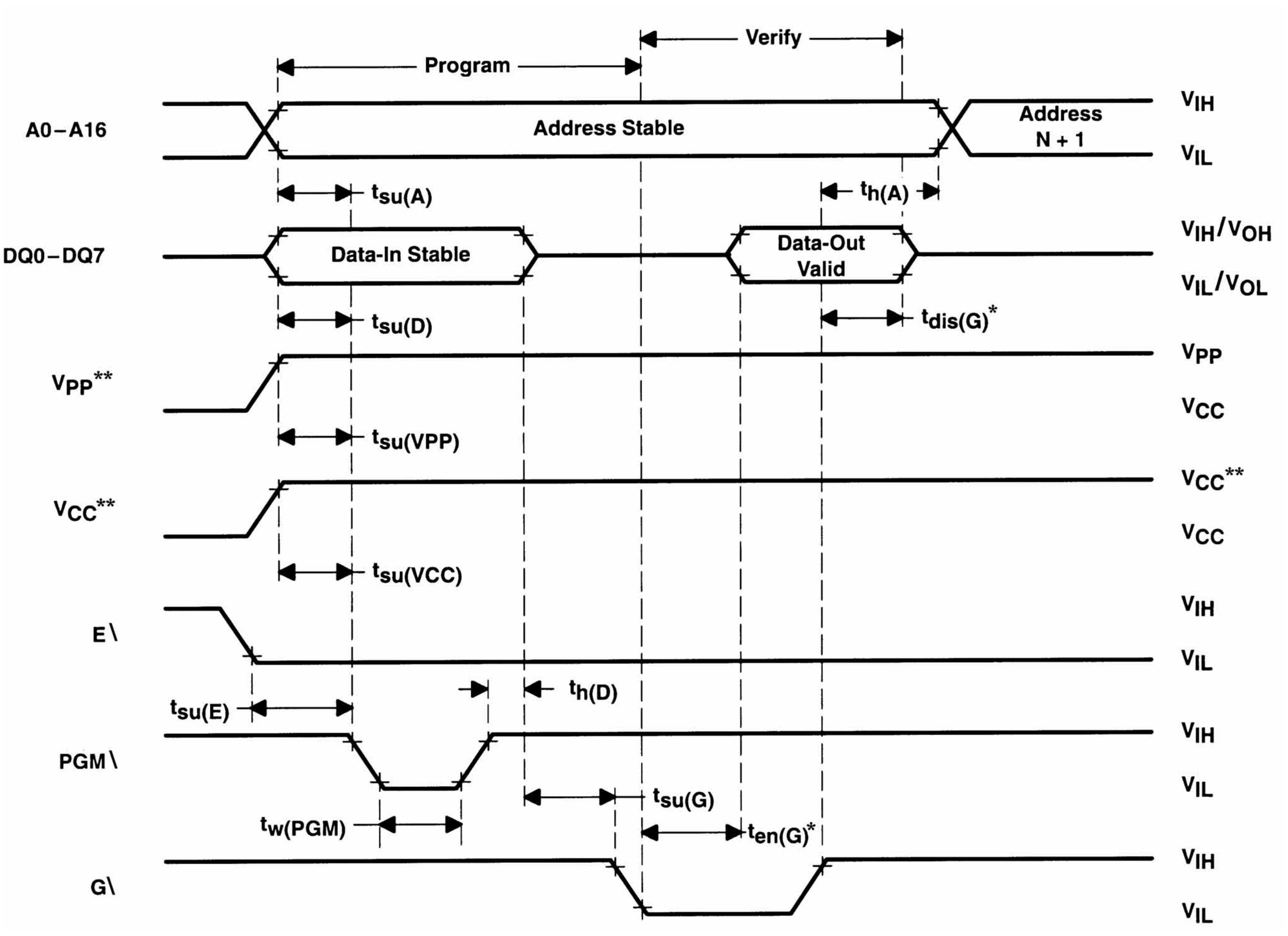


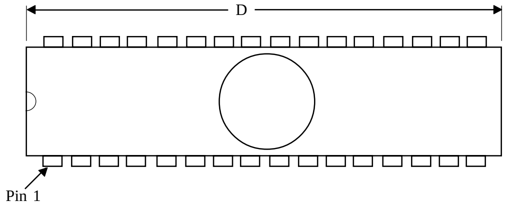
FIGURE 4. PROGRAM-CYCLE TIMING (SNAP! PULSE PROGRAMMING)

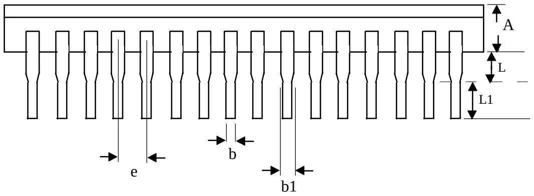


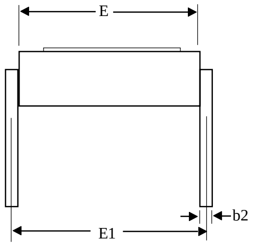
* $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
** 13V V_{PP} and 6.5V V_{CC} for SNAP! Pulse programming.

MECHANICAL DEFINITION*

ASI Case #114 (Package Designator J or ECA)
SMD 5962-89614, Case Outline X







SYMBOL	SMD Specifications	
	MIN	MAX
A	---	0.225
b	0.014	0.026
b1	0.045	0.065
b2	0.008	0.018
D	---	1.680
E	0.510	0.620
e	0.100 BSC	
E1	0.600 BSC	
L1	0.125	0.200
L	0.015	0.070

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

All measurements are in inches.

ORDERING INFORMATION

EXAMPLE: SMJ27C010A-12JM

Device Number	Speed ns	Package Type	Process
SMJ27C010A	-12	J	*
SMJ27C010A	-15	J	*
SMJ27C010A	-20	J	*

EXAMPLE: AS27C010A-15ECAM

Device Number	Speed ns	Package Type	Process
AS27C010A	-12	ECA	*
AS27C010A	-15	ECA	*
AS27C010A	-20	ECA	*

*AVAILABLE PROCESSES

M = Extended Temperature Range	-55°C to +125°C

ASI TO DSCC PART NUMBER CROSS REFERENCE*

ASI Package Designator ECA

TI Part #**	SMD Part #
AS27C010A-12ECAM	5962-8961420QYA
AS27C010A-15ECAM	5962-8961419QYA
AS27C010A-20ECAM	5962-8961417QYA

ASI Package Designator J

TI Part #**	SMD Part #
SMJ27C010A-12JM	5962-8961420QXA
SMJ27C010A-15JM	5962-8961419QXA
SMJ27C010A-20JM	5962-8961417QXA

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* *ASI part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.*

** *Parts are listed on SMD under the old Texas Instruments part number. ASI purchased this product line in November of 1999.*