

LVDS Interface ICs



# 56bit LVDS Receiver

## 8:56 DeSerializer

**BU7985KVT****●Description**

LVDS Interface IC of ROHM "Serializer" "Deserializer" operate from 8MHz to 150MHz wide clock range, and number of bits range is from 35 to 70. Data is transmitted seven times (7X) stream and reduce cable number by 3(1/3) or less. The ROHM's LVDS has low swing mode to be able to expect further low EMI.

**●Features**

- Wide dot clock range : Single(112MHz)/Dual(180MHz)(NTSC, VGA, SVGA, WXGA UXGA)
- Support clock frequency from 20MHz up to 112MHz.
- User programmable LVCMOS data output triggering timing  
by using either rising or falling edge of clock.
- User programmable LVCMOS data and clock output driving ability.
- Support Fail-Safe Hi-z Operation.
- 56bit LVDS transmitter is recommended to use BU7988KVT.

**●Applications**

Flat Panel Display

**●Precaution**

- This chip is not designed to protect from radioactivity.

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● Block Diagram

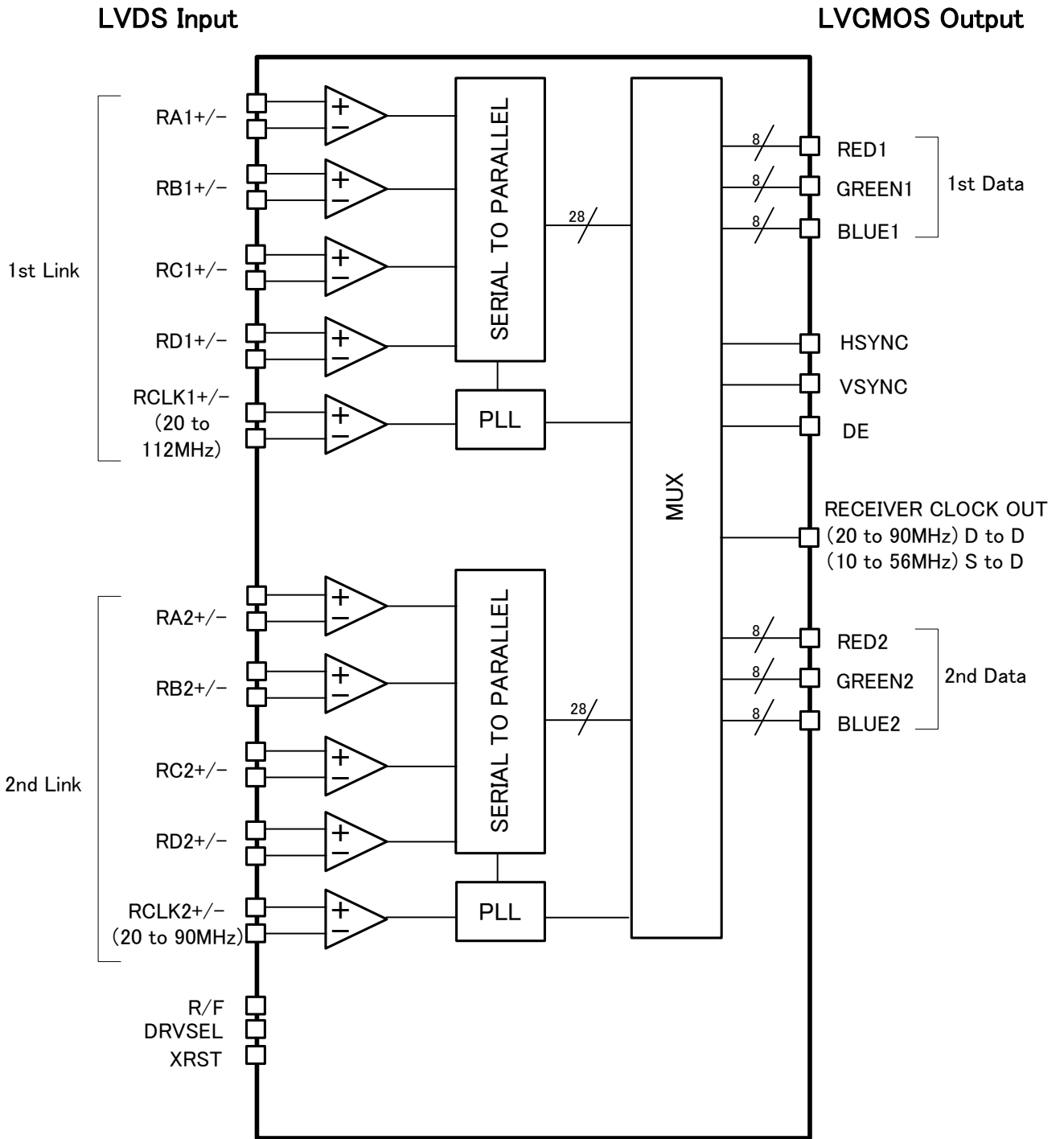


Figure-1 Block Diagram

● TQFP100V Package Outline and Specification

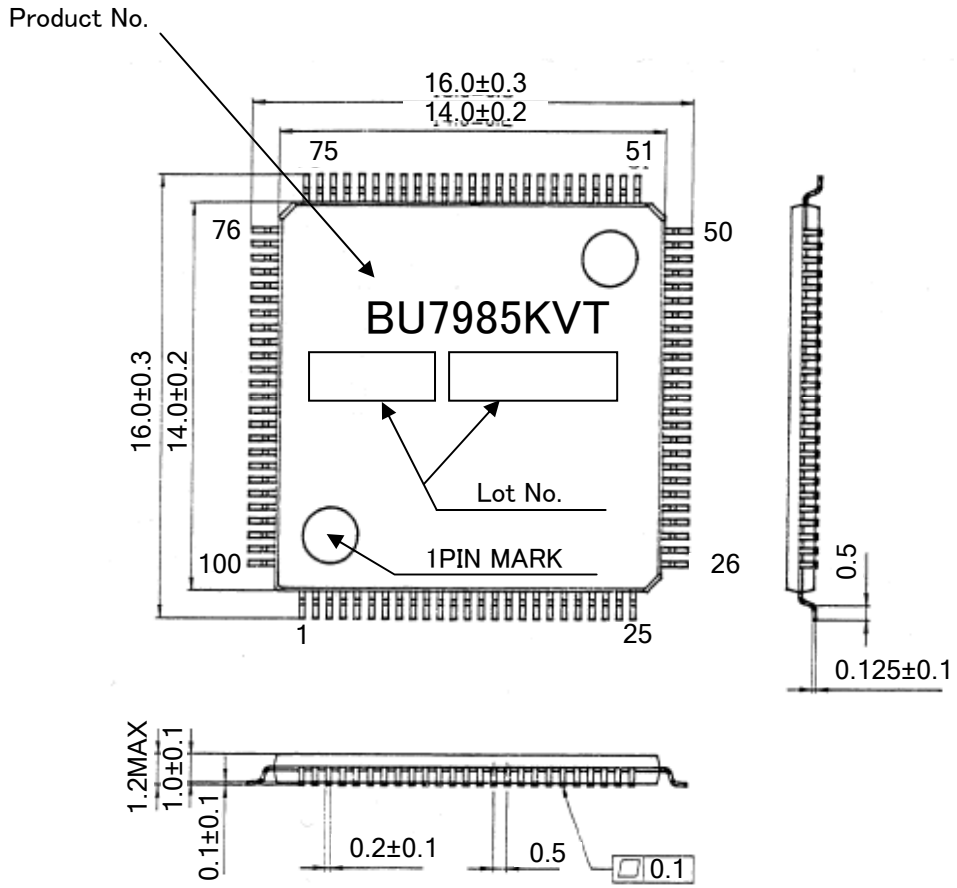


Figure-2 TQFP100V Package Outline and Specification



## ● Pin Description

Table 1 : Pin Description

| Pin Name       | Pin No.                        | Type                           | Descriptions   |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
|----------------|--------------------------------|--------------------------------|--|-------|-------|------|---|---|-----------|---|---|-------------|---|---|------------------------------|---|---|--------------------------------|
| RA1+, RA1-     | 78, 77                         | LVDS IN                        | LVDS Data Input for 1st Link.<br>The 1st pixel input data when Dual Link.<br>+ : Positive input of LVDS data differential pair.<br>- : Negative input of LVDS data differential pair.  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| RB1+, RB1-     | 80, 79                         | LVDS IN                        |  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| RC1+, RC1-     | 83, 82                         | LVDS IN                        |  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| RD1+, RD1-     | 87, 86                         | LVDS IN                        |  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| RCLK1+, RCLK1- | 85, 84                         | LVDS IN                        | LVDS Clock Input for 1st Link.   |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| RA2+, RA2-     | 90, 89                         | LVDS IN                        | LVDS Data Input for 2nd Link.<br>These pins are disabled when Single Link.<br>+ : Positive input of LVDS data differential pair.<br>- : Negative input of LVDS data differential pair.   |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| RB2+, RB2-     | 92, 91                         | LVDS IN                        |  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| RC2+, RC2-     | 95, 94                         | LVDS IN                        |  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| RD2+, RD2-     | 99, 98                         | LVDS IN                        |  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| RCLK2+, RCLK2- | 97, 96                         | LVDS IN                        | LVDS Clock Input for 2nd Link.   |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| R17 ~ R10      | 52, 51, 50, 47, 46, 45, 44, 43 | OUT                            | The 1st Pixel Data Outputs.  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| G17 ~ G10      | 62, 61, 60, 59, 58, 55, 54, 53 | OUT                            |  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| B17 ~ B10      | 72, 71, 68, 67, 66, 65, 64, 63 | OUT                            |  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| R27 ~ R20      | 19, 18, 17, 14, 13, 12, 11, 10 | OUT                            | The 2nd Pixel Data Outputs.  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| G27 ~ G20      | 29, 26, 25, 24, 23, 22, 21, 20 | OUT                            |  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| B27 ~ B20      | 39, 38, 37, 36, 35, 32, 31, 30 | OUT                            |  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| DE             | 75                             | OUT                            | Data Enable Output.  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| VSYNC          | 74                             | OUT                            | Vsync Output.  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| HSYNC          | 73                             | OUT                            | Hsync Output.  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| CLKOUT         | 40                             | OUT                            | Clock Output.  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| DRVSEL         | 9                              | IN                             | Output Driverbility Select.<br>L: Data output 2mA / Clock output 4mA<br>H: Data output 4mA / Clock output 8mA  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| R/F            | 8                              | IN                             | Output Clock Triggering Edge Select.<br>H: Rising edge, L: Falling edge.   |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| MODE1,MODE0    | 6, 5                           | IN                             | Pixel Data Mode.<br><table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>MODE1</th> <th>MODE0</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>Dual Link</td> </tr> <tr> <td>L</td> <td>H</td> <td>Single Link</td> </tr> <tr> <td>H</td> <td>L</td> <td>Dual Link With Fail-Safe Hiz</td> </tr> <tr> <td>H</td> <td>H</td> <td>Single Link With Fail-Safe Hiz</td> </tr> </tbody> </table> | MODE1 | MODE0 | Mode | L | L | Dual Link | L | H | Single Link | H | L | Dual Link With Fail-Safe Hiz | H | H | Single Link With Fail-Safe Hiz |
| MODE1          | MODE0                          | Mode                           |  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| L              | L                              | Dual Link                      |  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| L              | H                              | Single Link                    |  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| H              | L                              | Dual Link With Fail-Safe Hiz   |  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |
| H              | H                              | Single Link With Fail-Safe Hiz |  |       |       |      |   |   |           |   |   |             |   |   |                              |   |   |                                |

| Pin Name | Pin No.                          | Type   | Descriptions   |
|----------|----------------------------------|--------|--|
| XRST     | 4                                | IN     | H: Normal operation,<br>L: Power down (all outputs are pulled to ground) |
| VDD      | 15, 27, 33, 41, 48, 56, 69       | Power  | Power Supply Pins for LVCMOS outputs and digital circuitry.              |
| GND      | 3, 7, 16, 28, 34, 42, 49, 57, 70 | Ground | Ground Pins for LVCMOS outputs and digital circuitry.                    |
| LVDS VDD | 81,93                            | Power  | Power Supply Pins for LVDS inputs.                                       |
| LVDS GND | 76, 88, 100                      | Ground | Ground Pins for LVDS inputs.   |
| PLL VDD  | 2                                | Power  | Power Supply Pin for PLL circuitry.                                      |
| PLL GND  | 1                                | Ground | Ground Pin for PLL circuitry.  |

## ● Electrical characteristics

### ■ Rating

Table 2 : Absolute maximum rating

| Item                      | Symbol | Value |         | Unit |
|---------------------------|--------|-------|---------|------|
|                           |        | Min.  | Max.    |      |
| Supply voltage            | VDD    | -0.3  | 4.0     | V    |
| Input voltage             | VIN    | -0.3  | VDD+0.3 | V    |
| Output voltage            | VOOUT  | -0.3  | VDD+0.3 | V    |
| Storage temperature range | Tstg   | -55   | 125     | °C   |

Table 3 : Package Power

| PACKAGE  | Power Dissipation (mW) | De-rating (mW/°C)*1 |
|----------|------------------------|---------------------|
| TQFP100V | 900                    | 9.0                 |
|          | 1400*2                 | 14.0*2              |
|          | 2550*2                 | 25.5*2              |

\*1:At temperature Ta >25°C

\*2:Package power when mounting on the PCB board.

The size of PCB board :70 × 70 × 1.6 (mm<sup>3</sup>) / 140 × 150 × 1.6 (mm<sup>3</sup>)

The material of PCB board : The FR4 glass epoxy board.(3% or less copper foil area)

(It is recommended to apply the above package power requirement to PCB board when the small swing input mode is used)

Table 4 : Recommended Operating Conditions

| Parameter                   | Symbol           | Rating |     |     | Units | Conditions        |
|-----------------------------|------------------|--------|-----|-----|-------|-------------------|
|                             |                  | Min    | Typ | Max |       |                   |
| Supply Voltage              | V <sub>DD</sub>  | 3.0    | 3.3 | 3.6 | V     | VDD,LVDSVDD,PLLVD |
| Operating Temperature Range | T <sub>opr</sub> | -20    | -   | 85  | °C    |                   |

## ■ DC characteristics

**Table 5 : LVCMOS DC Specifications** (VDD=3.0V~3.6V, Ta=-20°C~+85°C)

| Symbol           | Parameter                 | Rating                |     |                       | Units | Conditions  |
|------------------|---------------------------|-----------------------|-----|-----------------------|-------|---|
|                  |                           | Min                   | Typ | Max                   |       |   |
| V <sub>IH</sub>  | High Level Input Voltage  | V <sub>DD</sub> × 0.8 | -   | V <sub>DD</sub>       | V     |   |
| V <sub>IL</sub>  | Low Level Input Voltage   | GND                   | -   | V <sub>DD</sub> × 0.2 | V     |   |
| V <sub>OH</sub>  | High Level Output Voltage | 2.4                   | -   | V <sub>DD</sub>       | V     | I <sub>OH</sub> = -2mA, -4mA (data)<br>I <sub>OH</sub> = -4mA, -8mA (clock) |
| V <sub>OL</sub>  | Low Level Output Voltage  | 0.0                   | -   | 0.4                   | V     | I <sub>OL</sub> = 2mA, 4mA (data)<br>I <sub>OL</sub> = 4mA, 8mA (clock)     |
| I <sub>INC</sub> | Input Leak Current        | -10                   | -   | +10                   | μA    | 0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>                                      |
| I <sub>OZ</sub>  | Output Leak Current       | -10                   | -   | +10                   | μA    | Output=HiZ, 0V ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub>                         |

**Table 6 : LVDS Receiver DC Specifications** (VDD=3.0V~3.6V, Ta=-20°C~+85°C)

| Symbol           | Parameter                         | Rating |     |     | Units | Conditions                                       |
|------------------|-----------------------------------|--------|-----|-----|-------|--|
|                  |                                   | Min    | Typ | Max |       |  |
| V <sub>TH</sub>  | Differential Input High Threshold | -      | -   | 100 | mV    | V <sub>OC</sub> =1.2V                            |
| V <sub>TL</sub>  | Differential Input Low Threshold  | -100   | -   | -   | mV    | V <sub>OC</sub> =1.2V                            |
| I <sub>INL</sub> | Input Current                     | -20    | -   | +20 | μA    | V <sub>IN</sub> =2.4V/0V<br>V <sub>DD</sub> =3.6 |

## ■ Supply Current

Table 7 : Supply Current (VDD=3.3V, Ta=25°C)

| Symbol            | Parameter                                       | Rating |     |     | Units | Conditions                   |          |
|-------------------|---|--------|-----|-----|-------|------------------------------|----------|
|                   |   | Min    | Typ | Max |       |                              |          |
| I <sub>RCCG</sub> | Receiver supply current<br>(Gray scale pattern) | -      | 88  | -   | mA    | MODE[1:0]=L L, H L<br>CL=8pF | f=90MHz  |
|                   |   | -      | 62  | -   | mA    | MODE[1:0]=L H, H H<br>CL=8pF | f=112MHz |
| I <sub>RCCW</sub> | Receiver supply current<br>(Checker pattern)    | -      | 137 | -   | mA    | MODE[1:0]=L L, H L<br>CL=8pF | f=90MHz  |
|                   |   | -      | 89  | -   | mA    | MODE[1:0]=L H, H H<br>CL=8pF | f=112MHz |
| I <sub>RCCS</sub> | Receiver Power Down<br>Supply Current           | -      | -   | 10  | μA    | XRST=L                       |          |

## 256 Gray Scale Pattern

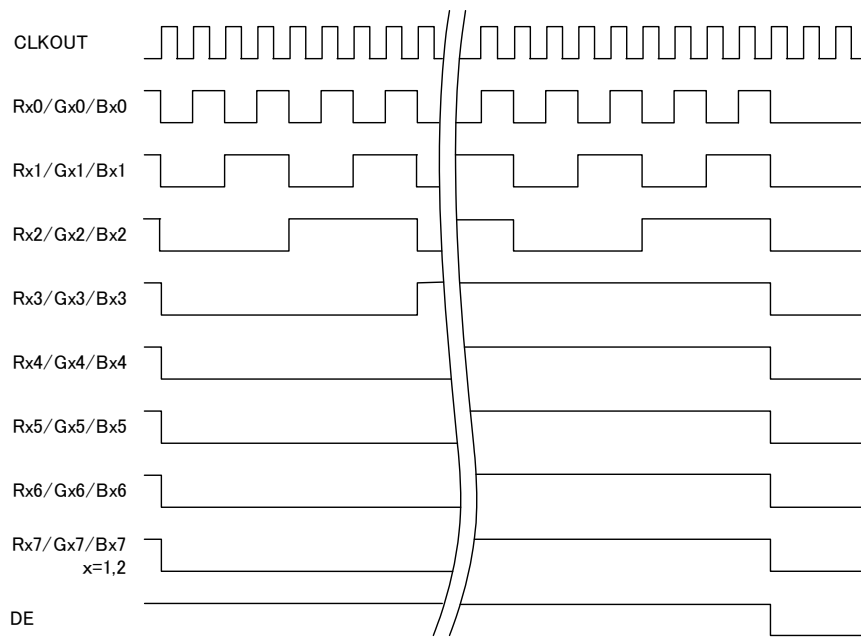


Figure-4 Gray scale pattern

## Double Checker Pattern

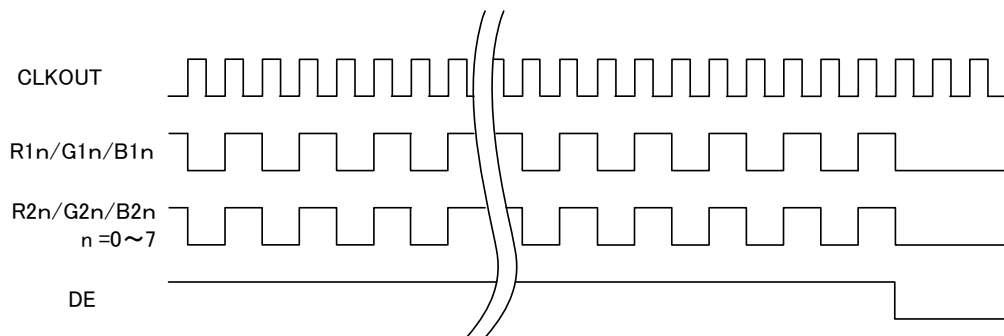


Figure-5 Checker pattern

## ■ AC characteristics

**Table 8 : Switching Characteristics** (VDD=3.0V~3.6V, Ta=-20°C~+85°C)

| Symbol     | Parameter                                   | Min                          | Typ                   | Max                          | Units |    |
|------------|---|------------------------------|-----------------------|------------------------------|-------|----|
| $t_{RCP}$  | CLK OUT Period                              | Dual-in / Dual-out           | 11.11                 | $t_{RCIP}$                   | 50    | ns |
|            |   | Single-in / Dual-out         | 17.85                 | $2t_{RCIP}$                  | 100   |    |
| $t_{RCH}$  | CLKOUT High Time                            | -                            | $0.5t_{RCP}$          | -                            | ns    |    |
| $t_{RCL}$  | CLKOUT Low Time                             | -                            | $0.5t_{RCP}$          | -                            | ns    |    |
| $t_{RS}$   | LVC MOS Data Setup to CLKOUT                | $0.3t_{RCP}$                 | -                     | -                            | ns    |    |
| $t_{RH}$   | LVC MOS data hold from CLKOUT               | $0.3t_{RCP}$                 | -                     | -                            | ns    |    |
| $t_{TLH}$  | LVC MOS Low to High Transition Time         | -                            | 3.0                   | 5.0                          | ns    |    |
| $t_{THL}$  | LVC MOS Low to Low Transition Time          | -                            | 3.0                   | 5.0                          |       |    |
| $t_{RIP1}$ | Input Data Position0 ( $T_{RCIP} = 8.9ns$ ) | -0.25                        | 0.0                   | +0.25                        | ns    |    |
| $t_{RIP0}$ | Input Data Position1 ( $T_{RCIP} = 8.9ns$ ) | $\frac{t_{RCIP}}{7} - 0.25$  | $\frac{t_{RCIP}}{7}$  | $2\frac{t_{RCIP}}{7} + 0.25$ | ns    |    |
| $t_{RIP6}$ | Input Data Position2 ( $T_{RCIP} = 8.9ns$ ) | $2\frac{t_{RCIP}}{7} - 0.25$ | $2\frac{t_{RCIP}}{7}$ | $2\frac{t_{RCIP}}{7} + 0.25$ | ns    |    |
| $t_{RIP5}$ | Input Data Position3 ( $T_{RCIP} = 8.9ns$ ) | $3\frac{t_{RCIP}}{7} - 0.25$ | $3\frac{t_{RCIP}}{7}$ | $3\frac{t_{RCIP}}{7} + 0.25$ | ns    |    |
| $t_{RIP4}$ | Input Data Position4 ( $T_{RCIP} = 8.9ns$ ) | $4\frac{t_{RCIP}}{7} - 0.25$ | $4\frac{t_{RCIP}}{7}$ | $4\frac{t_{RCIP}}{7} + 0.25$ | ns    |    |
| $t_{TOP3}$ | Input Data Position5 ( $T_{RCIP} = 8.9ns$ ) | $5\frac{t_{RCIP}}{7} - 0.25$ | $5\frac{t_{RCIP}}{7}$ | $5\frac{t_{RCIP}}{7} + 0.25$ | ns    |    |
| $t_{RIP2}$ | Input Data Position6 ( $T_{RCIP} = 8.9ns$ ) | $6\frac{t_{RCIP}}{7} - 0.25$ | $6\frac{t_{RCIP}}{7}$ | $6\frac{t_{RCIP}}{7} + 0.25$ | ns    |    |
| $t_{RRLL}$ | Phase Lock Loop Set                         | -                            | -                     | 10.0                         | ms    |    |
| $t_{RCIP}$ | CLKIN Period                                | 8.9                          | -                     | 50                           | ns    |    |
| $t_{ck12}$ | Skew Time between RCLK1 and RCLK2           | -                            | -                     | $\pm 0.3t_{RCIP}$            | ns    |    |

# ● AC Timing

## ■ LVCMOS

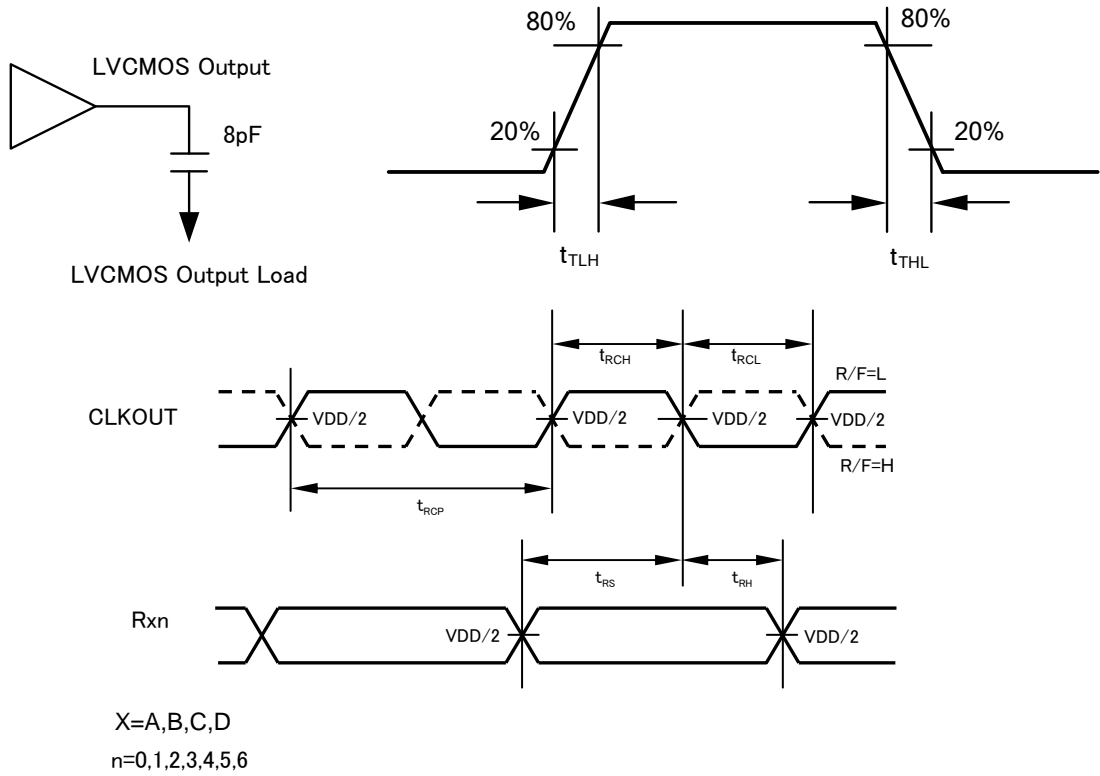


Figure-6 LVCMOS output timing

## ■ Phase-locked loops set time

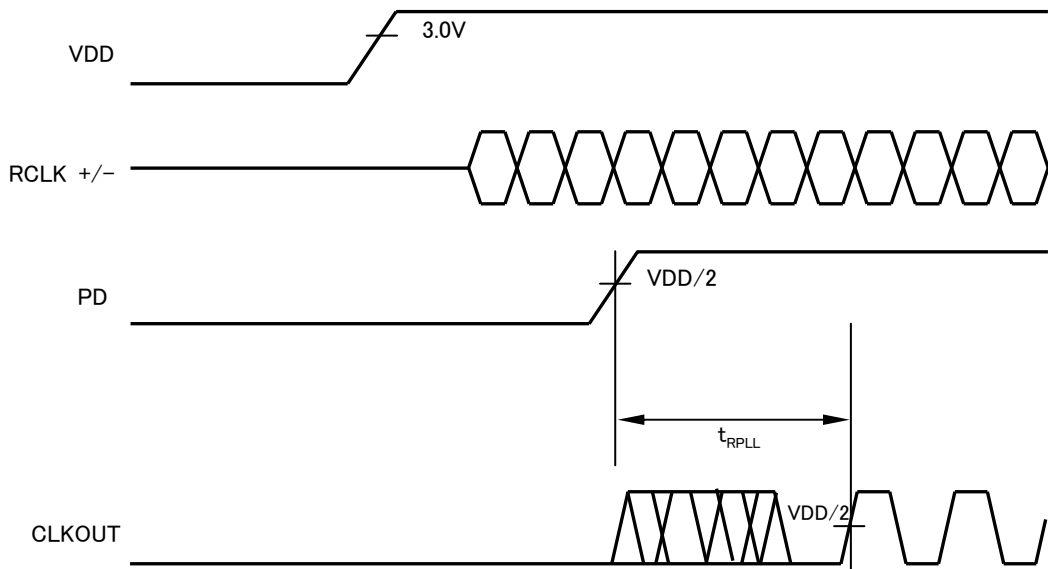


Figure-7 Phase-locked loops set time

## AC Timing Diagrams

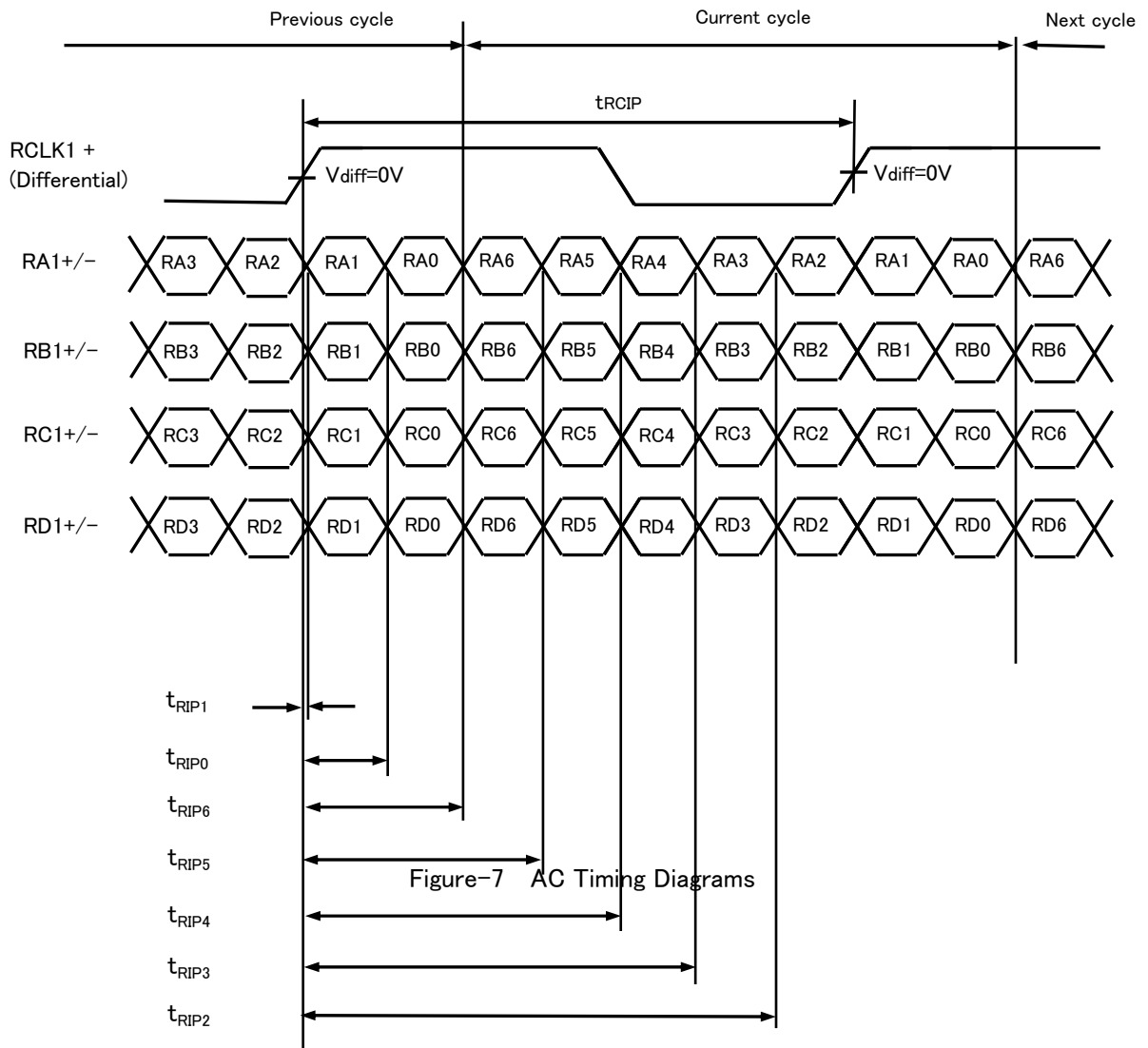
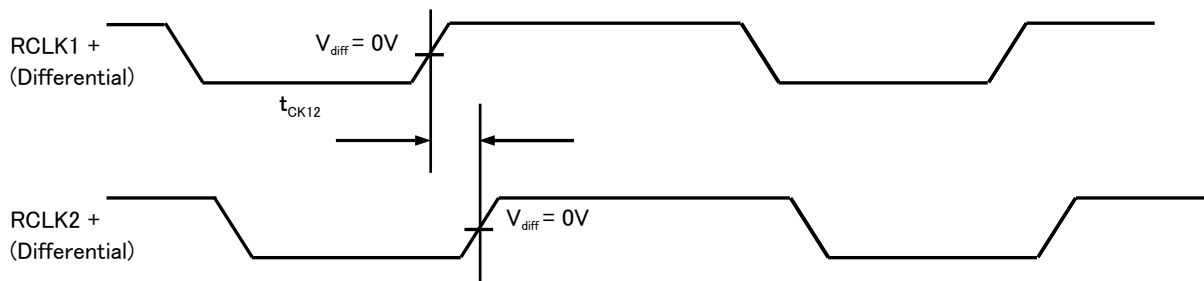


Figure-8 LVDS data and clock input timing



Note :  $V_{diff}=(R_{yx+})-(R_{yx-}), (RCLKx+)-(RCLKx-),$

● LVDS Data, Clock Input and Output Timing

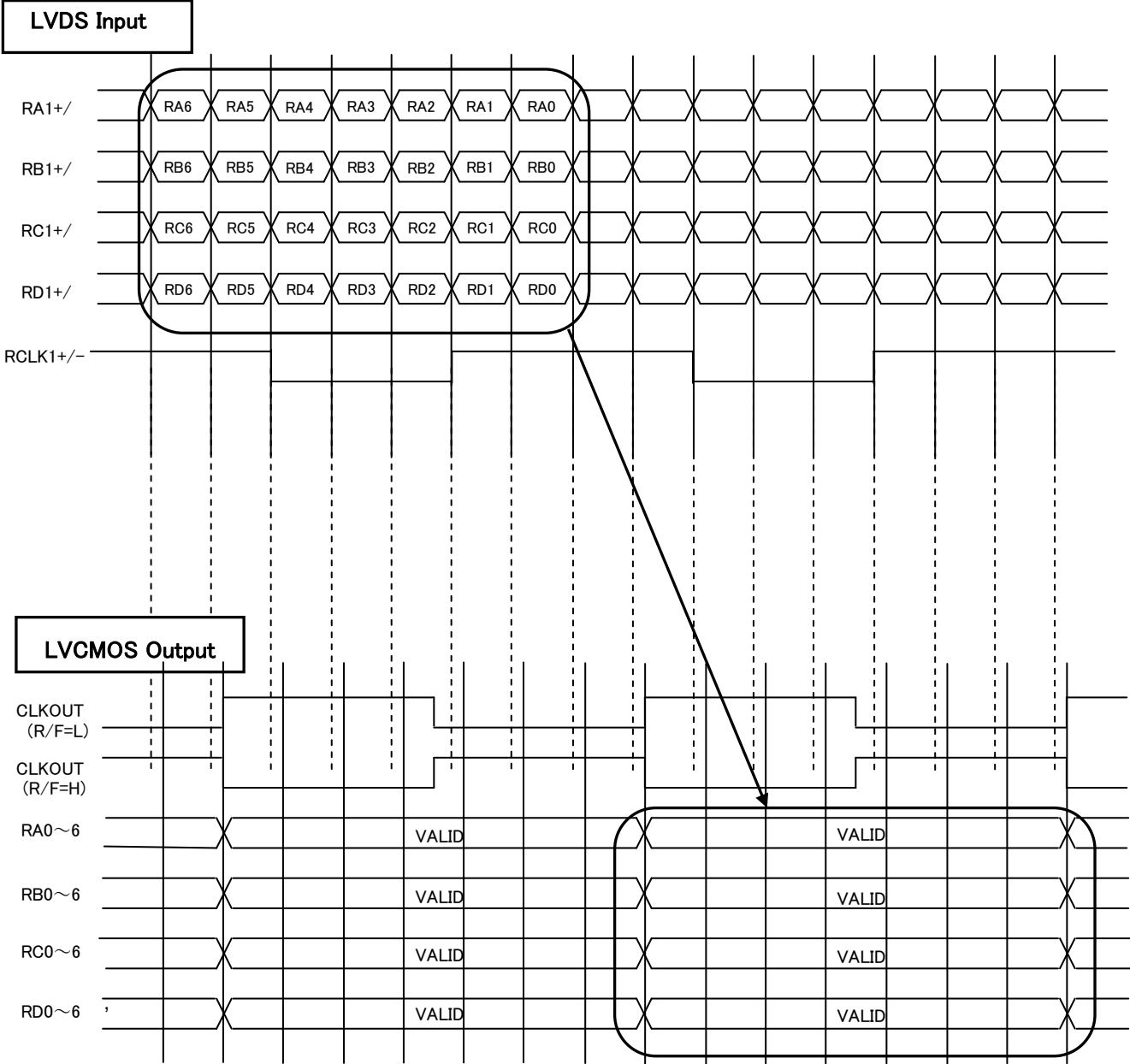


Figure-9 LVDS Data, Clock Input and Output Timing

● Pixel Map Table for Dual Link

Table 9: Pixel Map

| 1st Pixel Data |       |       |                                   | 2nd Pixel Data |       |       |                                   |
|----------------|-------|-------|-----------------------------------|----------------|-------|-------|-----------------------------------|
| TFT Panel Data |       |       | BU7985KVT<br>LVCMOS Output<br>Pin | TFT Panel Data |       |       | BU7985KVT<br>LVCMOS Output<br>Pin |
|                | 24Bit | 18Bit |                                   |                | 24Bit | 18Bit |                                   |
| LSB            | R10   | –     | R10                               | LSB            | R20   | –     | R20                               |
|                | R11   | –     | R11                               |                | R21   | –     | R21                               |
|                | R12   | R10   | R12                               |                | R22   | R20   | R22                               |
|                | R13   | R11   | R13                               |                | R23   | R21   | R23                               |
|                | R14   | R12   | R14                               |                | R24   | R22   | R24                               |
|                | R15   | R13   | R15                               |                | R25   | R23   | R25                               |
|                | R16   | R14   | R16                               |                | R26   | R24   | R26                               |
| MSB            | R17   | R15   | R17                               | MSB            | R27   | R25   | R27                               |
| LSB            | G10   | –     | G10                               | LSB            | G20   | –     | G20                               |
|                | G11   | –     | G11                               |                | G21   | –     | G21                               |
|                | G12   | G10   | G12                               |                | G22   | G20   | G22                               |
|                | G13   | G11   | G13                               |                | G23   | G21   | G23                               |
|                | G14   | G12   | G14                               |                | G24   | G22   | G24                               |
|                | G15   | G13   | G15                               |                | G25   | G23   | G25                               |
|                | G16   | G14   | G16                               |                | G26   | G24   | G26                               |
| MSB            | G17   | G15   | G17                               | MSB            | G27   | G25   | G27                               |
| LSB            | B10   | –     | B10                               | LSB            | B20   | –     | B20                               |
|                | B11   | –     | B11                               |                | B21   | –     | B21                               |
|                | B12   | B10   | B12                               |                | B22   | B20   | B22                               |
|                | B13   | B11   | B13                               |                | B23   | B21   | B23                               |
|                | B14   | B12   | B14                               |                | B24   | B22   | B24                               |
|                | B15   | B13   | B15                               |                | B25   | B23   | B25                               |
|                | B16   | B14   | B16                               |                | B26   | B24   | B26                               |
| MSB            | B17   | B15   | B17                               | MSB            | B27   | B25   | B27                               |
|                | HSYNC | HSYNC | HSYNC                             |                | HSYNC | HSYNC | HSYNC                             |
|                | VSYNC | VSYNC | VSYNC                             |                | VSYNC | VSYNC | VSYNC                             |
|                | DE    | DE    | DE                                |                | DE    | DE    | DE                                |

● CMOS Data Output Timing for Dual Link

Example : SXGA+(1400 × 1050)

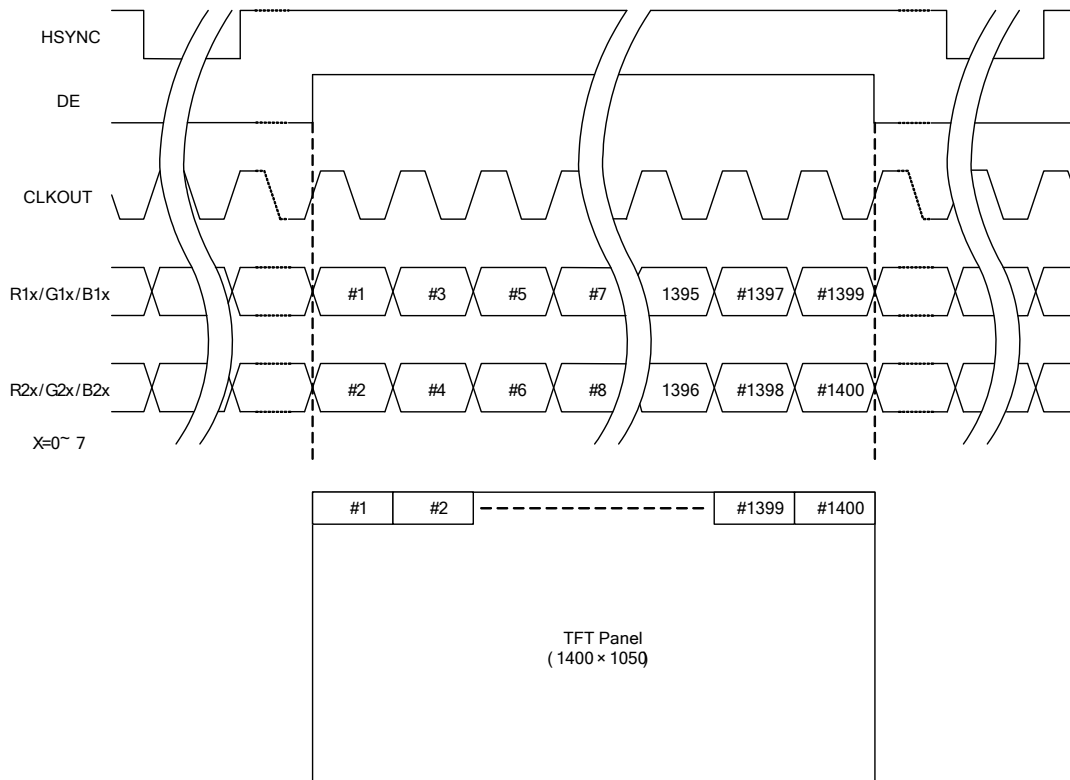


Figure-10 Data Output Timing for Dual Link

● CMOS Data Output Timing for Single Link

Example : SXGA+(1400 × 1050)

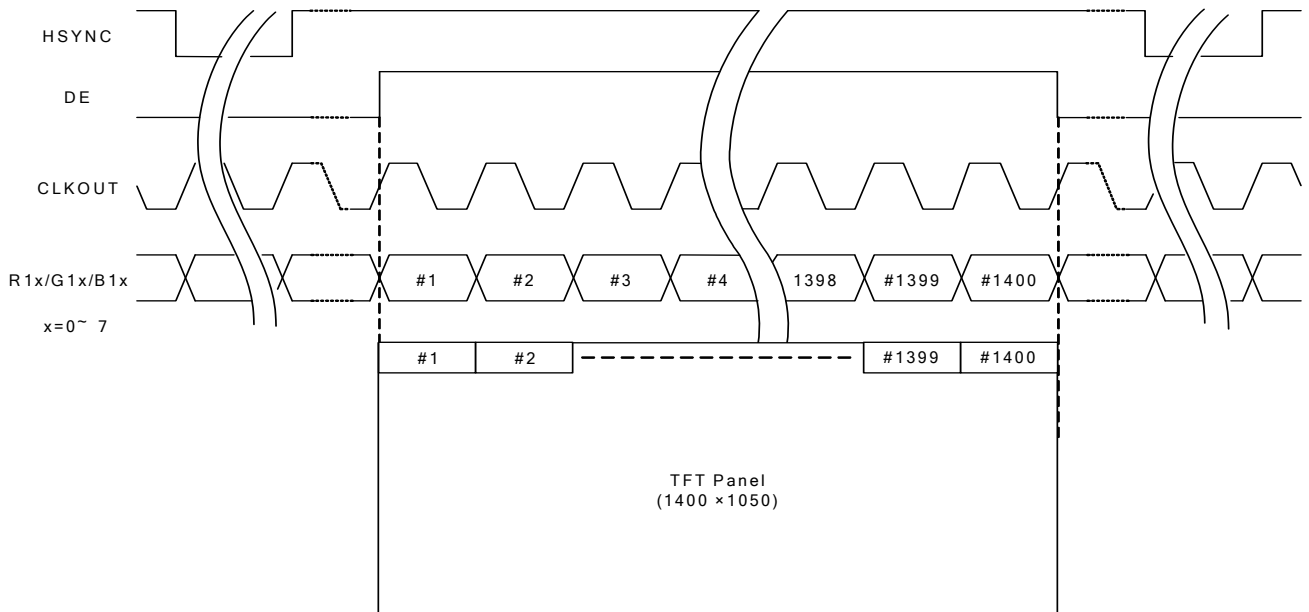


Figure-11 Data Output Timing for Dual Link

● LVDS Data Inputs Timing Diagrams in Dual Link  
(Dual-in / Dual-out Mode)

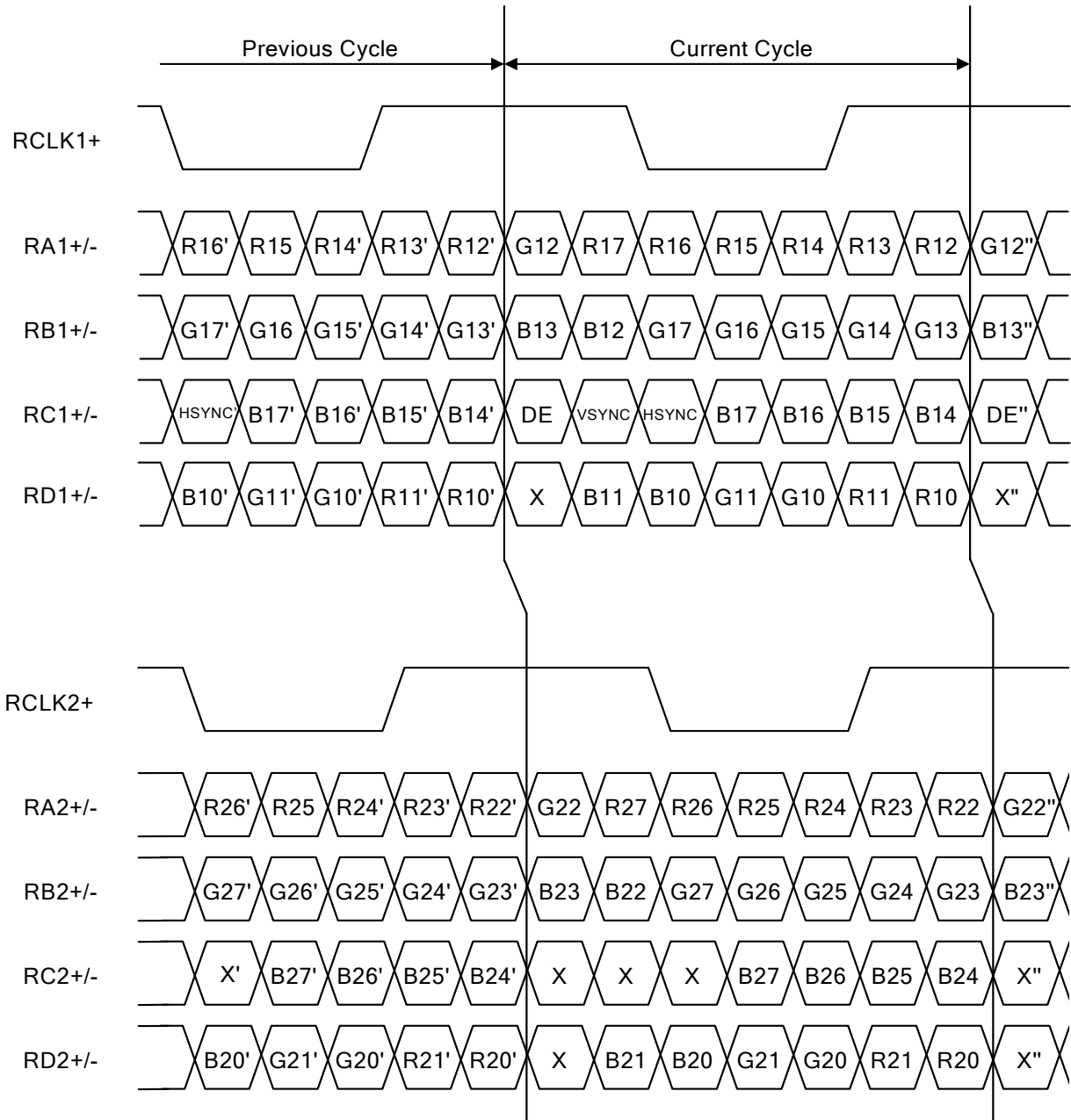


Figure-12 Data Input Timing for Dual Link

● **LVDS Data Inputs Timing Diagrams in Single Link**  
**(Single-in / Dual-out Mode)**

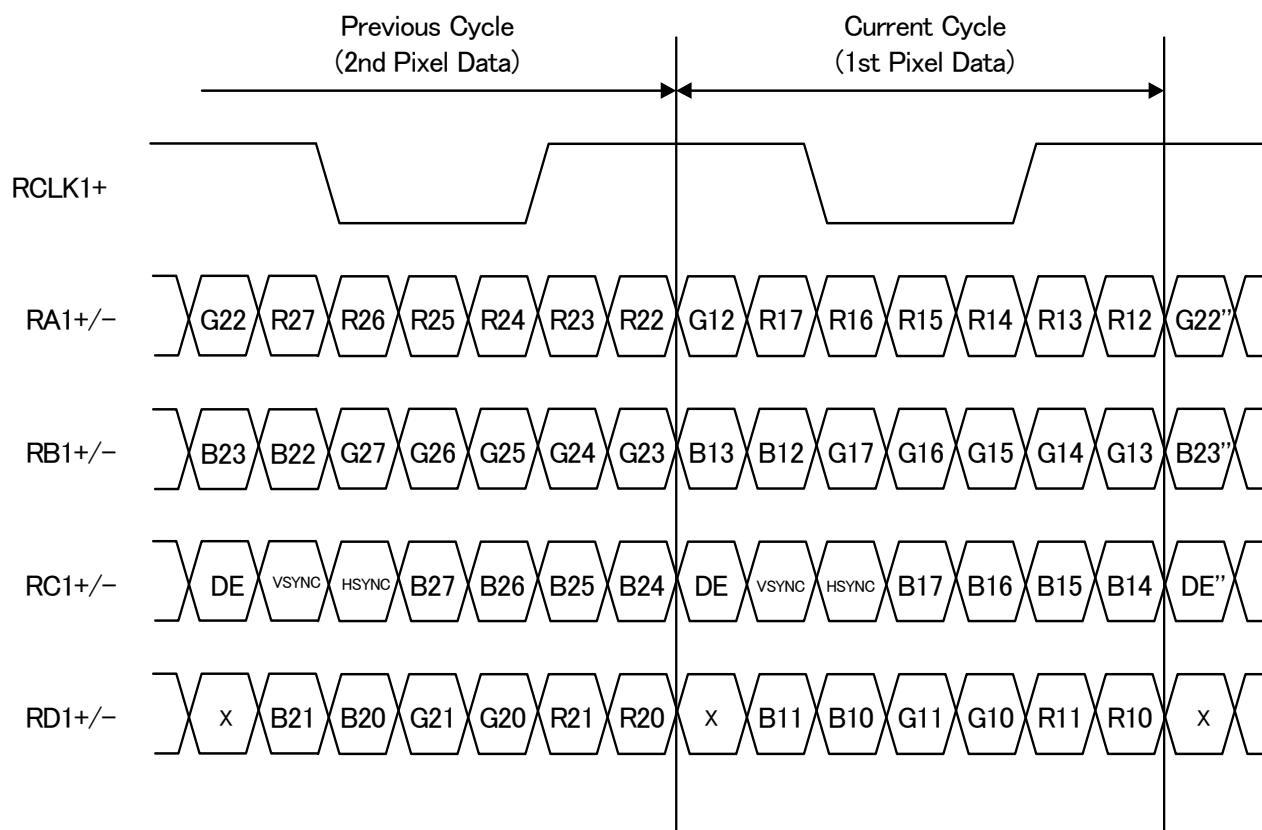


Figure-13 Data Input Timing for Single Link

● **Fail-Safe Hi-Z Operation**

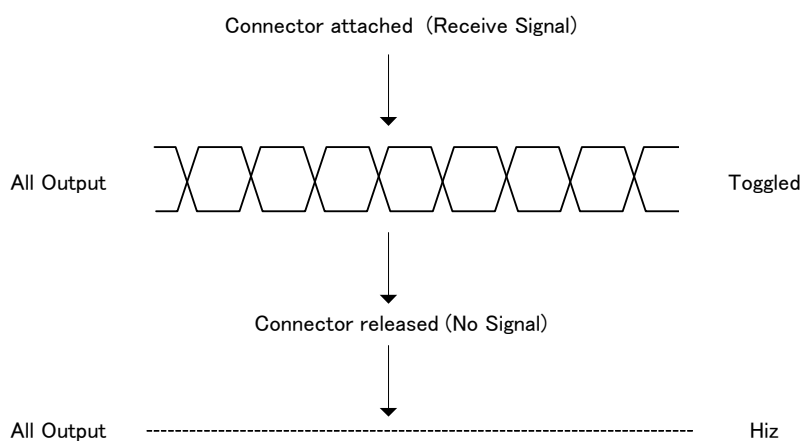


Figure-14 Fail-Sage Hi-Z Operation

## ●About the Power On Reset

Power On Reset is not mandatory for this device.

(The PD pin should be set to high level when Power On Reset procedure is not used.)

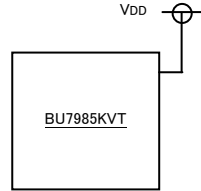


Figure-9 Terminal connection when Power On Reset is not used

However, Power On Reset procedure is strongly recommend for internal logic initialization by following two methods.

- ① The method of using CR circuit.
- ② The method of using external specific IC.

It is recommend to do enough examination for target application.

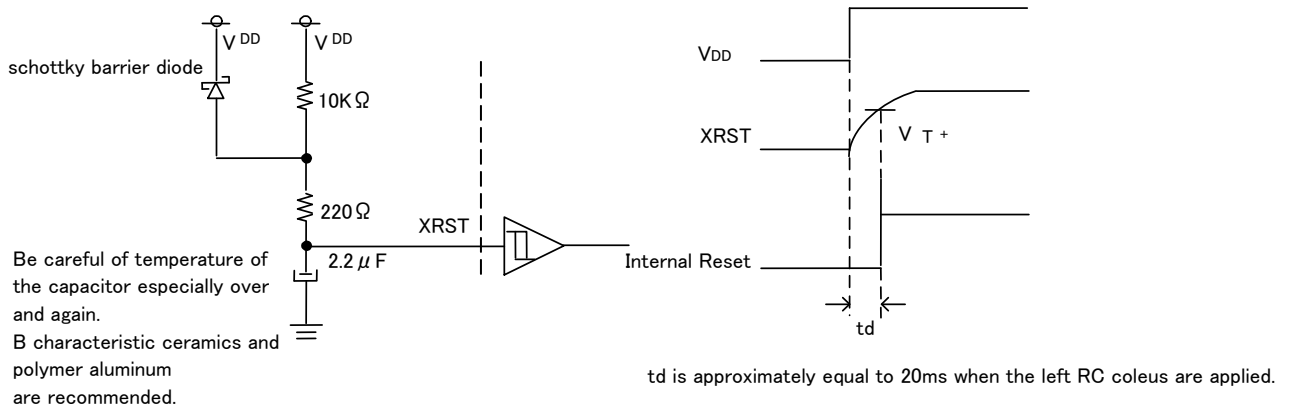


Figure-15 Power On Reset by external a CR circuit

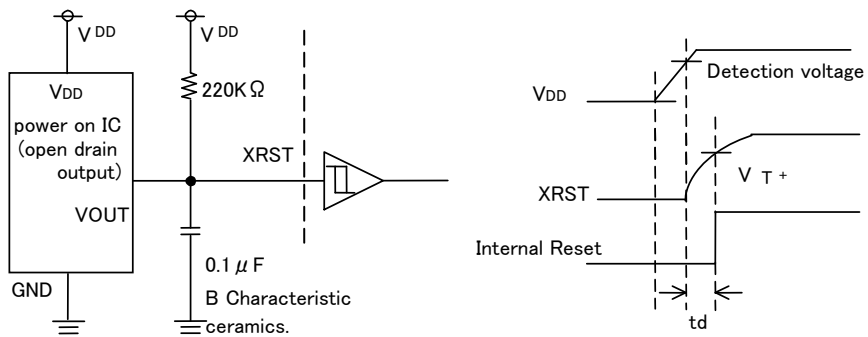
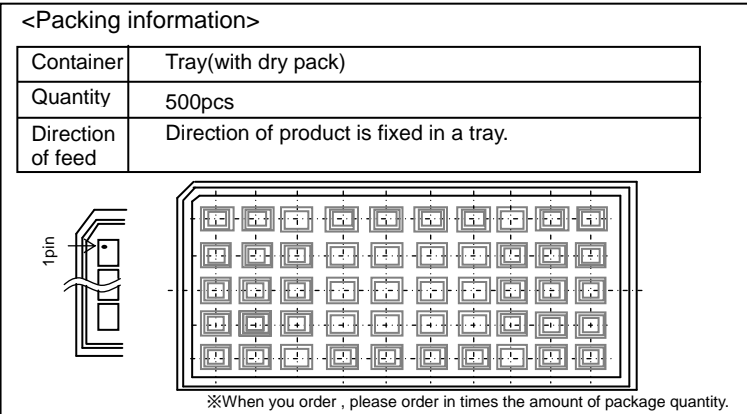
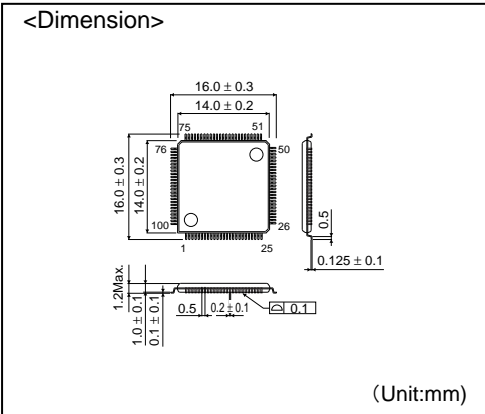


Figure-16 Power On Reset by specific IC

# TQFP100V



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