

M62230FP

LCD Matrix Regulator

REJ03D0855-0201
Rev.2.01
Nov 14, 2007

Description

The M62230FP is a semiconductor circuit for LCD matrix regulator, which will generate the divided-voltage to drive LCD matrix.

By changing the connection of R pin (i.e., Change the internal resistor ratio), M62230FP can support divided voltage ratio ranging from 1/5 bias to 1/13 bias.

The high stability and any desired voltage levels is possible, since the variable voltage regulator for V_{REF} is built-in.

Features

- Adjustable type voltage divider.
(The setting range of internal resistor is from 1/5 bias to 1/13 bias)
- 5 resident buffer-Amp. (5 divided output)
- Low power dissipation. (1.8 mA Typ.)
- Resident voltage-variable regulator for V_{REF} .

Application

To drive LCD.

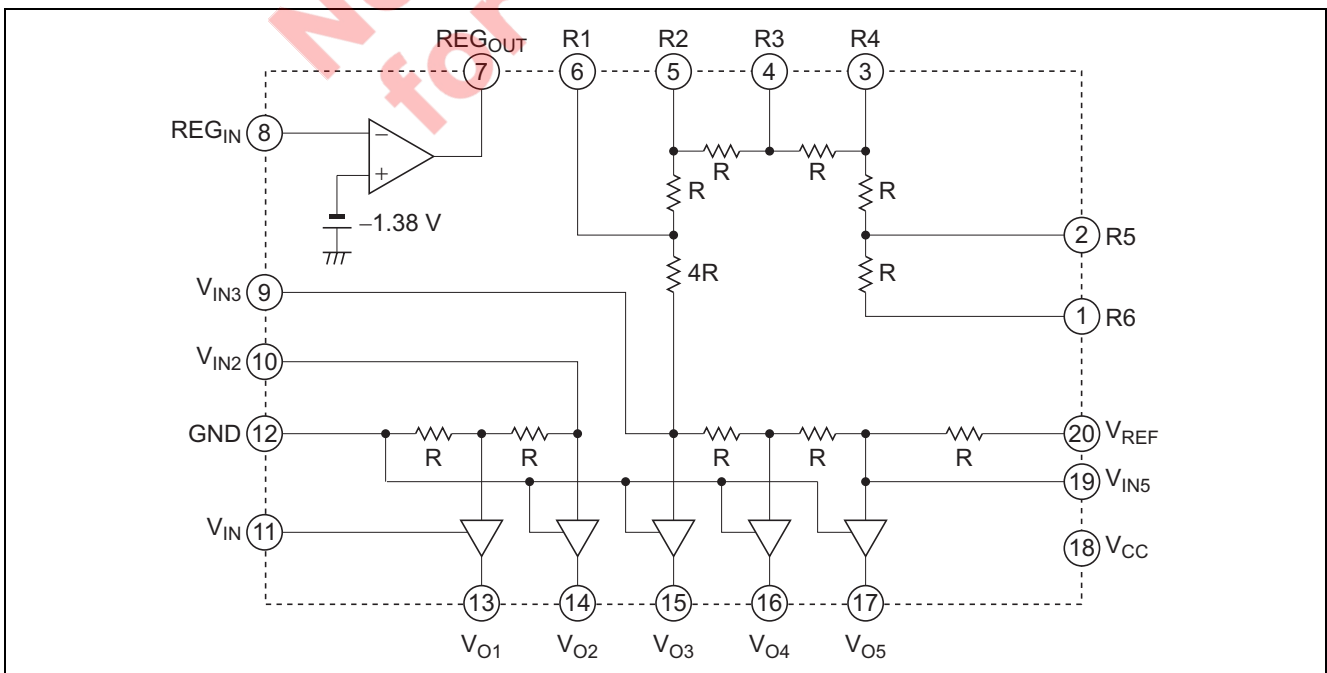
Recommend Operating Conditions ($T_a = 25^\circ\text{C}$)

Supply voltage range: $\text{GND} - V_{CC}$: (if $V_1 > -1 \text{ V}$, it is necessary to support V_{IN})... -30 to -10 V

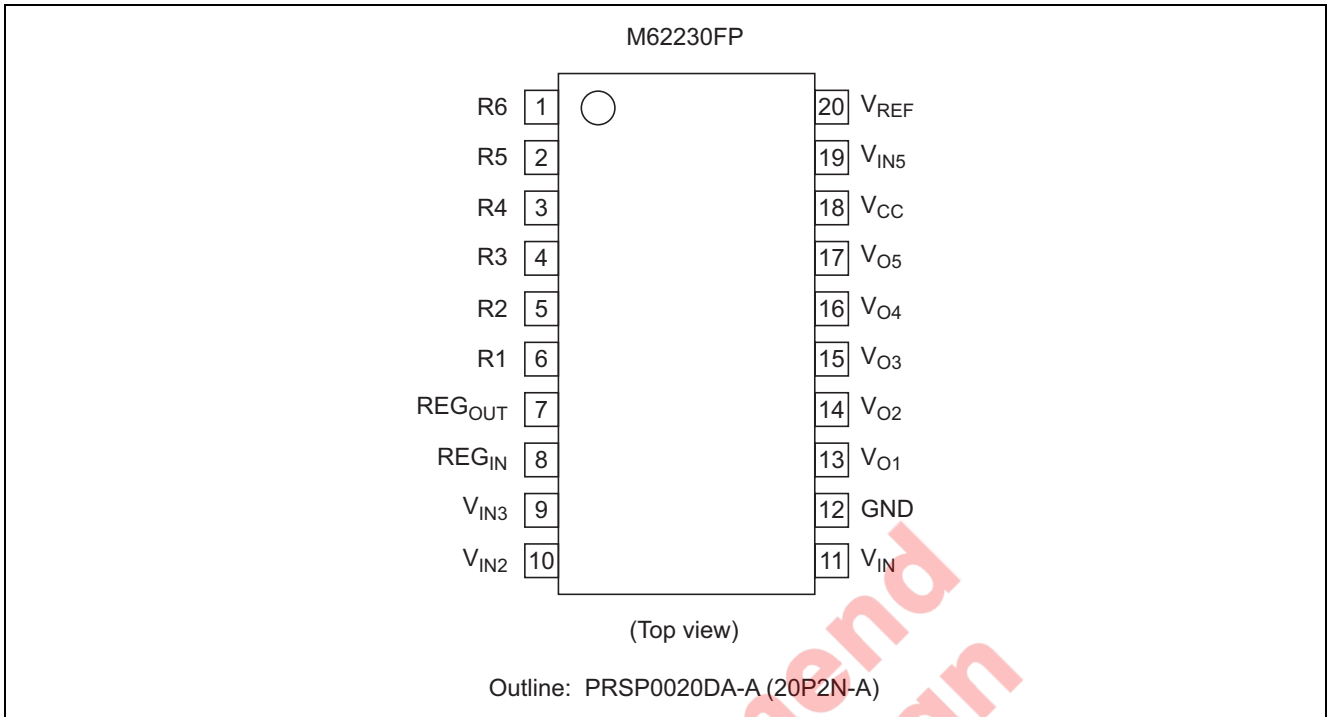
Recommend input voltage $\text{GND} - V_{REF}$: $V_{REF} \geq V_{CC}$ -30 to -6 V

(To set V_{CC} , V_{REF} , in order that both $|0 - V_2|$ & $|V_{CC} - V_5|$ are larger than 1 V)

Block Diagram



Pin Arrangement



Not recommended
for new design

Explanation of Terminals

Pin No.	Symbol	Function
1	R6	If the voltage of each pin can satisfy the following condition: $V_{O6} \geq V_{O5} \geq V_{O4} \geq V_{O3} \geq V_{O2} \geq V_{O1}$ These pins will be used. Please refer to page 5 to set the bias ratio.
2	R5	
3	R4	
4	R3	
5	R2	
6	R1	
7	REG _{OUT}	Regulator output for V _{REF} to use
8	REG _{IN}	The inverting input pin of REG OP-Amp
9	V _{IN3}	V _{IN3} input
10	V _{IN2}	V _{IN2} input
11	V _{IN}	V _{IN} Power if V1 > -1.0 V, it is necessary to support V _{IN} if V1 < -1.0 V, this pin connect to GND
12	GND	GND Pin
13	V _{O1}	Divided-voltage output pin To set V _{CC} & V _{REF} , in order that 0 - V2 ≥ 1 V To set V _{CC} & V _{REF} , in order that V5 - V _{CC} ≥ 1 V
14	V _{O2}	
15	V _{O3}	
16	V _{O4}	
17	V _{O5}	
18	V _{CC}	V _{CC} power (-Power)
19	V _{IN5}	V _{IN5} input
20	V _{REF}	Reference voltage input pin

Not recommended
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Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

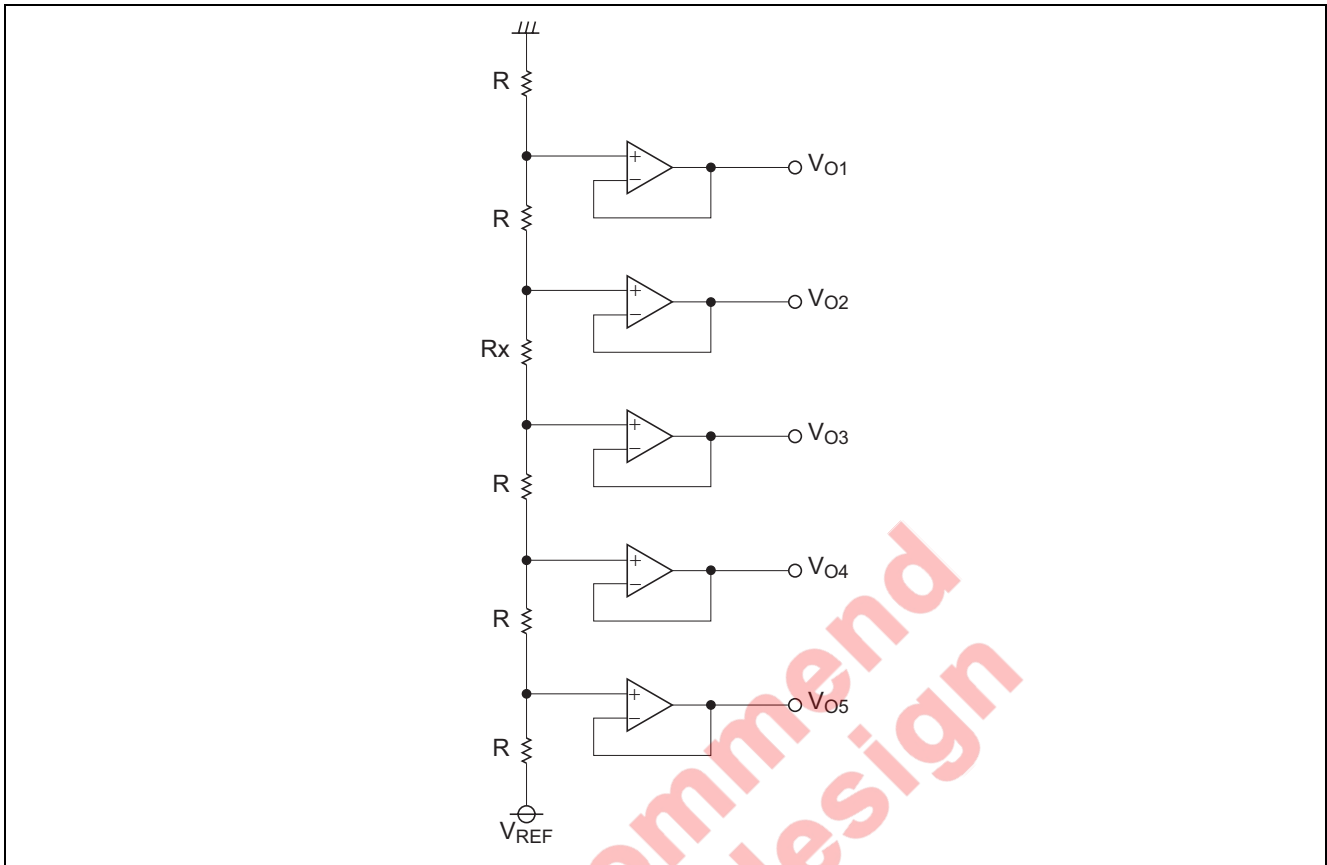
Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V _{CC}	-36 to 0	V	
Maximum output current	I _{OUT}	30	mA	
Power dissipation	P _d	550	mW	Ta = 25°C
Thermal derating	K _θ	5.5	mW/°C	Ta > 25°C
Operating temperature	Topr	-20 to +75	°C	
Storage temperature	Tstg	-40 to +125	°C	

Electrical Characteristics

(V_{CC} = -16 V, V_{IN} = GND, V_{REF} = -12 V, Resistor setting = 5R, Ta = 25°C, unless otherwise noted)

Item	Symbol	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
Supply voltage	V _{CC}	-35	—	-10	V	
Dissipation current	I _{CC}	—	1.80	—	mA	V _{REF} = -16 V
Output voltage ratio 1	R _{VO1}	1.98	2.00	2.02	—	V ₂ / V ₁
Output voltage ratio 2	R _{VO2}	1.98	2.00	2.02	—	(V ₅ - V ₃) / (V ₅ - V ₄)
Output voltage ratio 3	R _{VO3}	8.90	9.00	9.10	—	V ₅ / V ₁
Output voltage ratio 4	R _{VO4}	4.45	4.50	4.55	—	V ₅ / V ₂
Output voltage ratio 5	R _{VO5}	4.45	4.50	4.55	—	V ₅ / (V ₅ - V ₃)
Output voltage ratio 6	R _{VO6}	8.90	9.00	9.10	—	V ₅ / (V ₅ - V ₄)
Resistor ratio 1	R _{R1}	—	4	—	—	Resistor between V _{IN3} and R ₁ / resistor between R ₁ and R ₂
Resistor ratio 2	R _{R2}	—	5	—	—	Resistor between V _{IN3} and R ₂ / resistor between R ₁ and R ₂
Resistor ratio 3	R _{R3}	—	6	—	—	Resistor between V _{IN3} and R ₃ / resistor between R ₁ and R ₂
Resistor ratio 4	R _{R4}	—	7	—	—	Resistor between V _{IN3} and R ₄ / resistor between R ₁ and R ₂
Resistor ratio 5	R _{R5}	—	8	—	—	Resistor between V _{IN3} and R ₅ / resistor between R ₁ and R ₂
Resistor ratio 6	R _{R6}	—	9	—	—	Resistor between V _{IN3} and R ₆ / resistor between R ₁ and R ₂
Resistance	R	—	20	—	kΩ	Resistor between R ₁ and R ₂
Load regulation of output voltage 1	ΔV ₁	—	—	20	mV	+200 μA < I _{OUT1} < +10 mA
Load regulation of output voltage 2-1	ΔV ₂₋₁	—	—	20	mV	+200 μA < I _{OUT2} < +10 mA
Load regulation of output voltage 3-1	ΔV ₃₋₁	—	—	20	mV	+200 μA < I _{OUT3} < +10 mA
Load regulation of output voltage 2-2	ΔV ₂₋₂	—	—	20	mV	-10 mA < I _{OUT2} < -200 μA
Load regulation of output voltage 3-2	ΔV ₃₋₂	—	—	20	mV	-10 mA < I _{OUT3} < -200 μA
Load regulation of output voltage 4	ΔV ₄	—	—	20	mV	-20 mA < I _{OUT4} < -200 μA
Load regulation of output voltage 5	ΔV ₅	—	—	20	mV	-20 mA < I _{OUT5} < -200 μA
Output voltage of regulator	V _{REG}	-1.45	-1.38	-1.31	V	Buffer output
Load regulation of V _{REF}	R _{EG-L}	—	—	50	mV	-10 mA < I _{REG} < +2 mA

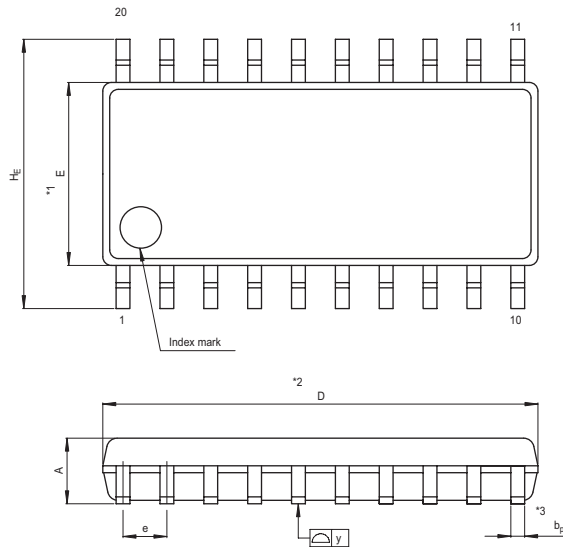
The Setting Method of Divided-voltage



Rx	Bias Ratio	Example of Setting
R	1/5	9 pin-6 pin short, 10 pin-5 pin short
2R	1/6	9 pin-6 pin short, 10 pin-4 pin short
3R	1/7	9 pin-6 pin short, 10 pin-3 pin short
4R	1/8	10 pin-6 pin short
5R	1/9	10 pin-5 pin short
6R	1/10	10 pin-4 pin short
7R	1/11	10 pin-3 pin short
8R	1/12	10 pin-2 pin short
9R	1/13	10 pin-1 pin short

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-5.3x12.6-1.27	PRSP0020DA-A	20P2N-A	0.3g



NOTE)
 1. DIMENSIONS **1* AND **2* DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION **3* DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	12.5	12.6	12.7
E	5.2	5.3	5.4
A ₂	—	1.8	—
A ₁	0	0.1	0.2
A	—	—	2.1
b _p	0.35	0.4	0.5
c	0.18	0.2	0.25
θ	0°	—	8°
H _E	7.5	7.8	8.1
e	1.12	1.27	1.42
y	—	—	0.1
L	0.4	0.6	0.8

Not recommended for new design

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Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

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1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510