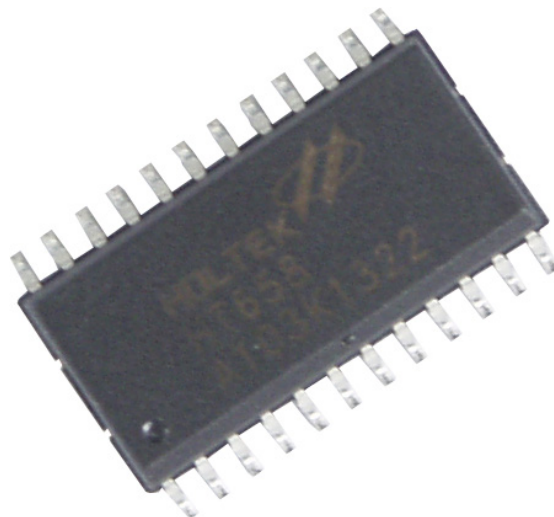


FEATURES

- Operating voltage: 2.4V~12V
- Low power and high noise immunity CMOS technology
- Low standby current
- Capable of decoding 18 bits of information
- Pairs with HOLTEK's HT640 encoder
- 10 address pins
- 8 data pins
- Trinary address setting
- Two times of receiving check
- Built-in oscillator needs only a 5% resistor
- Valid transmission indicator
- Easily interface with an RF or an infrared transmission medium
- Minimal external components



APPLICATIONS

- Burglar alarm system
- Smoke and fire alarm system
- Garage door controllers
- Car door controllers
- Car alarm system
- Security system
- Cordless telephones
- Other remote control systems

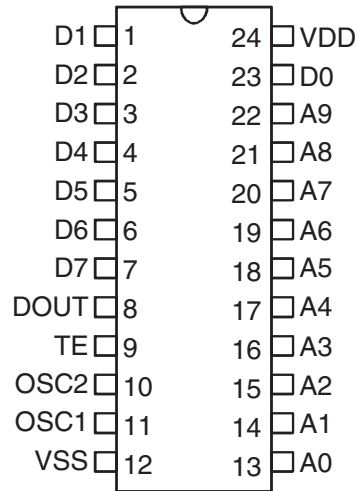
GENERAL DESCRIPTION

The HT640/S encoder is a CMOS LSI for remote control system applications. It is paired with the HT658/S decoder. The HT640 encoder is capable of encoding 18 bits of information, which consists of 10 address bits and 8 data bits. The programmable address / data is transmitted together with the header bits via an RF or an infrared transmission medium upon receipt of a trigger signal on the TE line.

Note:

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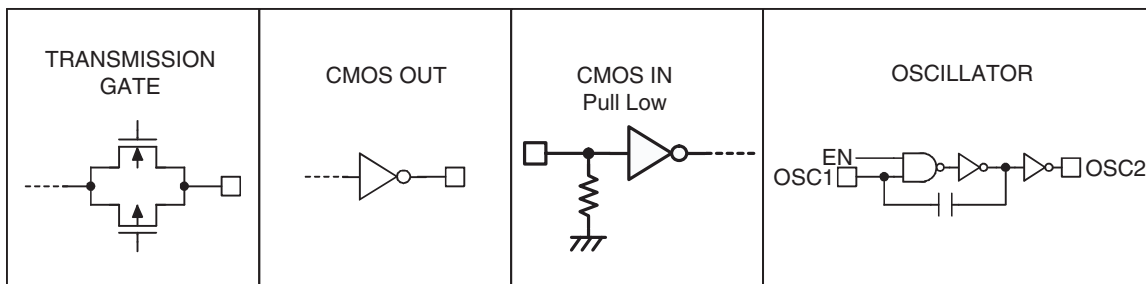
PIN OUT



PIN DESCRIPTIONS

Pin Name	I/O	Internal Connection	Description
A0-A11	I	TRANSMISSION GATE	Input pins for address A0-A9 setting They can be externally set to VDD, VSS, or left open.
D0-D7	I	TRANSMISSION GATE	Input pins for data (D0-D7) setting They can be externally set to VDD, VSS, or left open.
DOUT	O	CMOS OUT	Encoder data serial transmission output
TE	I	CMOS In Pull-low	Transmission enable, active high
OSC1	I	OSCILLATOR	Oscillator input pin
OSC2	O	OSCILLATOR	Oscillator output pin
VSS	I		Negative power supply (GND)
VDD	I		Positive power supply

APPROXIMATE INTERNAL CIRCUITS



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage -0.3V to 13V
 Input Voltage.....VSS-0.3V to VDD+0.3V

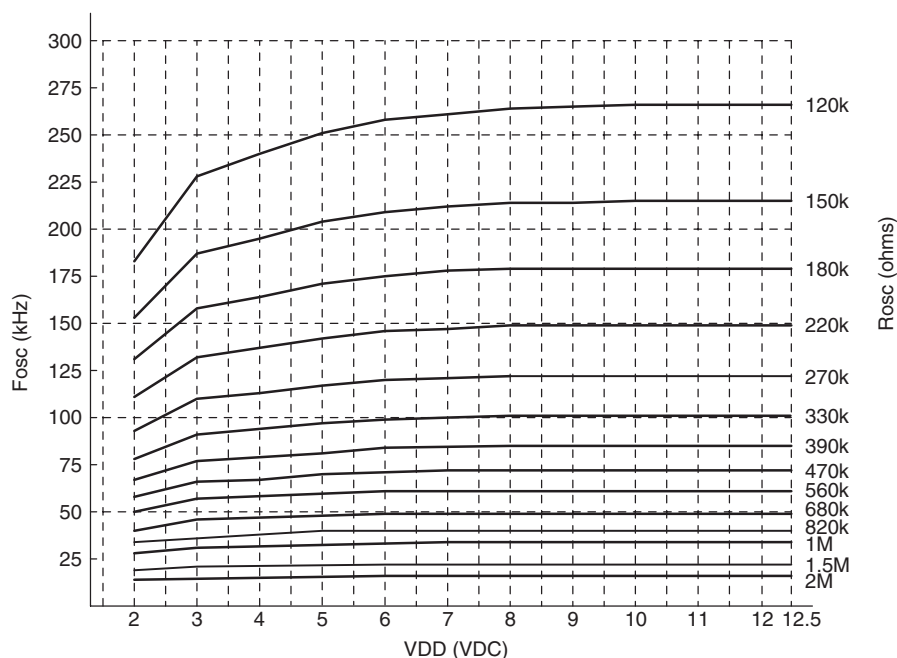
Storage Temperature..... -50°C to 125°C
 Operating Temperature..... -20°C to 75°C

*Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extened periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
V _{DD}	Operating Voltage			2.4		12	V
I _{STB}	Standby Current	3V	Oscillator stops		0.1	1	μA
		12V			2	4	μA
I _{DD}	Operating Current	5V	No load f _{OSC} =100kHz		250	500	μA
		12V			1200	2400	μA
I _{DOUT}	Output Drive Current	5V	V _{OH} =0.9V _{DD} (Source)	0.6	1.2		mA
		5V	V _{OL} =0.1V _{DD} (Sink)	0.6	1.2		mA
V _{IH}	H Input Voltage			0.8V _{DD}		V _{DD}	V
V _{IL}	L Input Voltage			0		0.2V _{DD}	V
f _{OSC}	Oscillator Frequency	10V	R _{OSC} =330k		100		kHz
R _{TE}	TE Pull-low Resistance	5V	V _{TE} =5V		1.5	3	MΩ

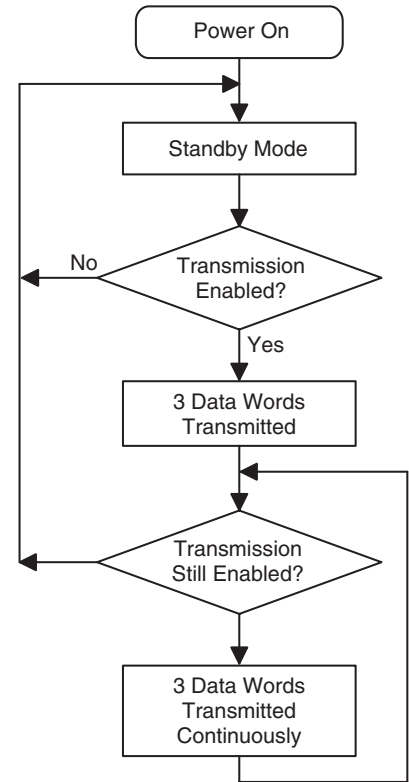
ENCODER OSCILLATOR FREQUENCY VS SUPPLY VOLTAGE



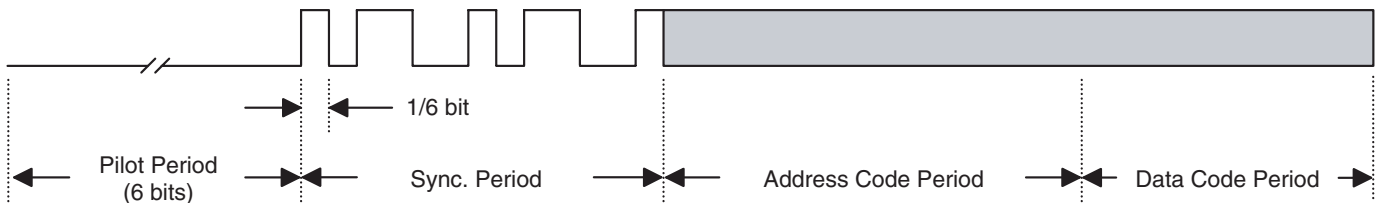
FUNCTIONAL DESCRIPTION

The HT640/S encoder begins a three-word transmission cycle when the transmission enable line (TE) is pulled high. This cycle will repeat itself as long as the TE line is held high. Once TE falls low, the encoder output completes its final cycle and then stops as shown in the Encoder/Decoder Timing diagram. When a transmission enable signal is applied, the encoder scans and transmits the status of the 18 bits of address/data serially in the order A0 to A9, D0 to D7.

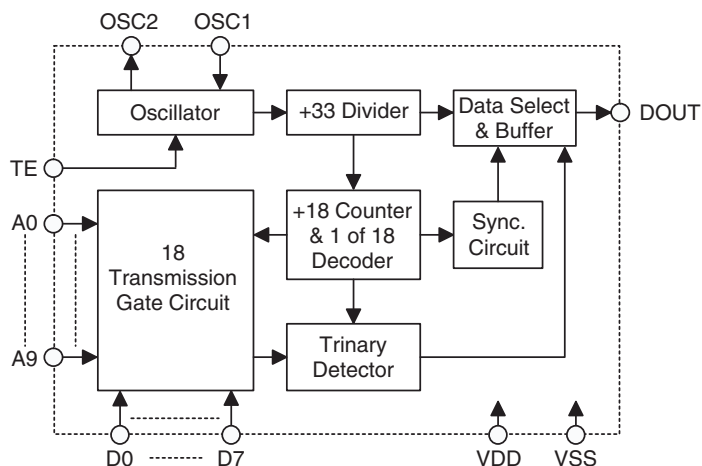
The status of each address/data pin can be individually preset to logic high, low, or floating. The floating state data input is interpreted as logic low by the decoders since the decoder output only has two states. The address pins are usually set to transmit particular security codes by DIP switches or PCB wiring, while the data is selected using push buttons or electronic switches. The floating state allows the HT640/S to be used without pull-up or pull-down resistors on the data and address input lines.



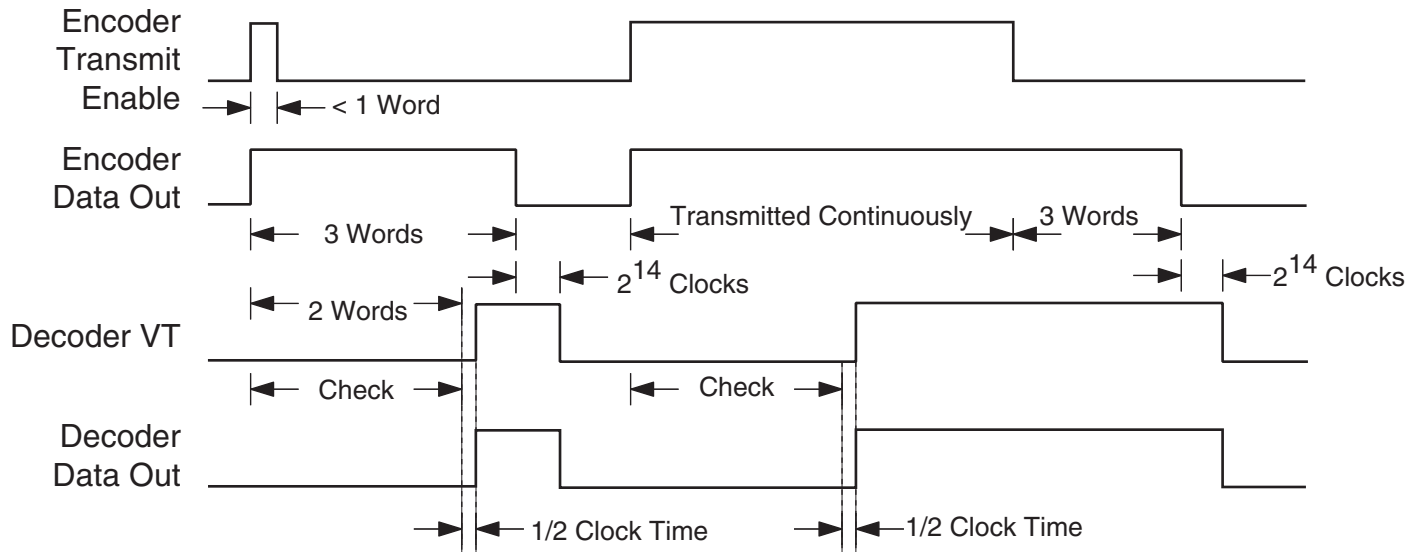
DATA STRUCTURE



BLOCK DIAGRAM



ENCODER/DECODER TIMING



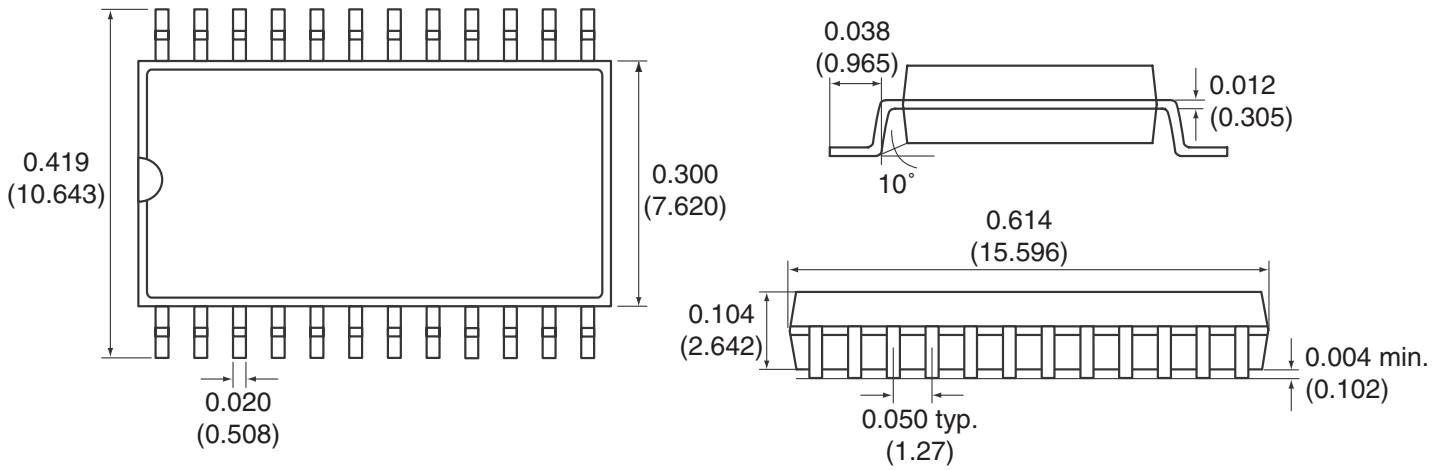
ENCODER/DECODER DATA STRUCTURE

	SYNC BITS	ADDRESS BITS										DATA BITS							
A&D BITS PULLED TO VCC	[Timing diagram showing high-level pulses for sync, address, and data bits]																		
A&D BITS OPEN	[Timing diagram showing high-impedance pulses for sync, address, and data bits]																		
A&D Bits PULLED TO GND	[Timing diagram showing low-level pulses for sync, address, and data bits]																		
SYNC PERIOD	SYNC BITS	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	D0	D1	D2	D3	D4	D5	D6	D7
15.1mS	5.6mS	26mS										21mS							
TIME DEPENDANT ON OSCILLATOR RESISTOR CHOSEN (390k)																			
22.30%	8.27%	38.40%										31.02%							
PERCENTAGES OF TOTAL TIME FOR ONE WORD PLUS SYNC																			

Bit Pattern Interpretation



SOP-24 PACKAGE DIMENSIONS



APPLICATION CIRCUIT

