

## 0.25-Ω Low-Voltage Dual SPDT Analog Switch

### DESCRIPTION

The DG3535/DG3536 is a sub 1 Ω (0.25 Ω at 2.7 V) dual SPDT analog switches designed for low voltage applications.

The DG3535/DG3536 has on-resistance matching (less than 0.05 Ω at 2.7 V) and flatness (less than 0.2 Ω at 2.7 V) that are guaranteed over the entire voltage range. Additionally, low logic thresholds makes the DG3535/DG3536 an ideal interface to low voltage DSP control signals.

The DG3535/DG3536 has fast switching speed with break-before-make guaranteed. In the On condition, all switching elements conduct equally in both directions. Off-isolation and crosstalk is - 69 dB at 100 kHz.

The DG3535/DG3536 is built on Vishay Siliconix's high-density low voltage CMOS process. An epitaxial layer is built in to prevent latchup. The DG3535/DG3536 contains the additional benefit of 2000 V ESD protection.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For MICRO FOOT analog switching products manufactured with tin/silver/copper (SnAgCu) device terminations, the lead (Pb)-free "-E1" suffix is being used as a designator.

### FEATURES

- Low Voltage Operation
- Low On-Resistance -  $r_{ON}$ : 0.25 Ω at 2.7 V
- - 69 dB OIRR at 2.7 V, 100 kHz
- MICRO FOOT® Package
- ESD Protection > 2000 V


**RoHS**  
COMPLIANT

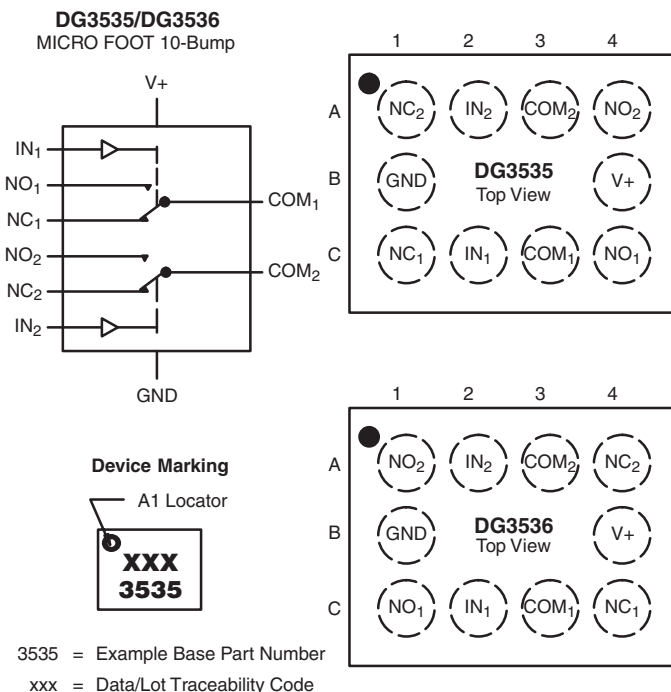
### BENEFITS

- Reduced Power Consumption
- High Accuracy
- Reduce Board Space
- 1.6 V Logic Compatible
- High Bandwidth

### APPLICATIONS

- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems
- Relay Replacement

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



### TRUTH TABLE

Logic	NC1 and NC2	NO1 and NO2
0	ON	OFF
1	OFF	ON

### ORDERING INFORMATION

Temp Range	Package	Part Number
- 40 to 85 °C	MICRO FOOT: 10 Bump (4 x 3, 0.5 mm Pitch, 238 μm Bump Height)	DG3535DB-T5-E1 DG3535DB-T1-E1 DG3536DB-T5-E1



ABSOLUTE MAXIMUM RATINGS			
Parameter		Limit	Unit
Reference V+ to GND		- 0.3 to + 6	V
IN, COM, NC, NO <sup>a</sup>		- 0.3 to (V+ + 0.3 V)	
Continuous Current (NO, NC, COM)		± 300	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 500	
Storage Temperature	(D Suffix)	- 65 to 150	°C
Package Solder Reflow Conditions <sup>b</sup>	IR/Convection	250	
ESD per Method 3015.7		> 2	kV
Power Dissipation (Packages) <sup>c</sup>	MICRO FOOT: 10 Bump (4 x 3 mm) <sup>d</sup>	457	mW

Notes:

- a Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b Refer to IPC/JEDEC (J-STD-020B)
- c All bumps welded or soldered to PC Board.
- d Derate 5.7 mW/°C above 70 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V+ = 3.0 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, V <sub>IN</sub> = 0.5 V or 1.4 V <sup>e</sup>	Temp <sup>a</sup>	Limits - 40 to 85 °C			Unit
				Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	V <sub>NO</sub> , V <sub>NC</sub> , V <sub>COM</sub>		Full	0		V+	V
On-Resistance <sup>d</sup>	r <sub>ON</sub>	V+ = 2.7 V, V <sub>COM</sub> = 0.6/1.5 V I <sub>NO</sub> , I <sub>NC</sub> = 100 mA	Room Full		0.25	0.4 0.5	Ω
r <sub>ON</sub> Flatness <sup>d</sup>	r <sub>ON</sub> Flatness		Room			0.15	
On-Resistance Match Between Channels <sup>d</sup>	Δr <sub>DS(on)</sub>		Room			0.05	
Switch Off Leakage Current	I <sub>NO(off)</sub> I <sub>NC(off)</sub>	V+ = 3.3 V, V <sub>NO</sub> , V <sub>NC</sub> = 0.3 V/3 V, V <sub>COM</sub> = 3 V/0.3 V	Room Full	- 2 - 20		2 20	nA
	I <sub>COM(off)</sub>		Room Full	- 2 - 20		2 20	
	Channel-On Leakage Current		I <sub>COM(on)</sub>	Room Full	- 2 - 20		
<b>Digital Control</b>							
Input High Voltage <sup>d</sup>	V <sub>INH</sub>		Full	1.4			V
Input Low Voltage	V <sub>INL</sub>		Full			0.5	
Input Capacitance	C <sub>in</sub>		Full		10		pF
Input Current	I <sub>INL</sub> or I <sub>INH</sub>	V <sub>IN</sub> = 0 or V+	Full	1		1	μA

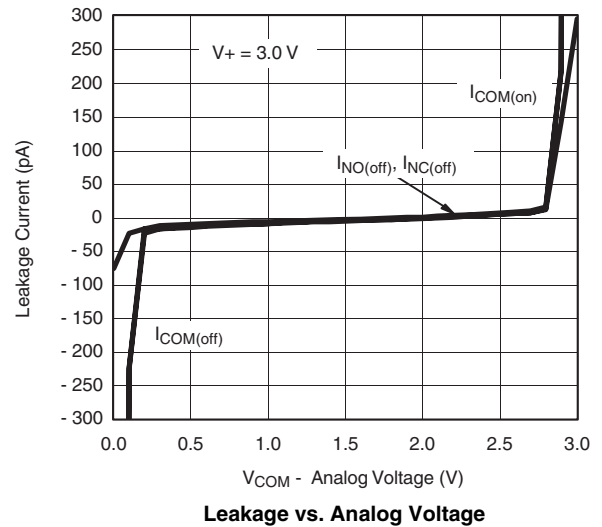
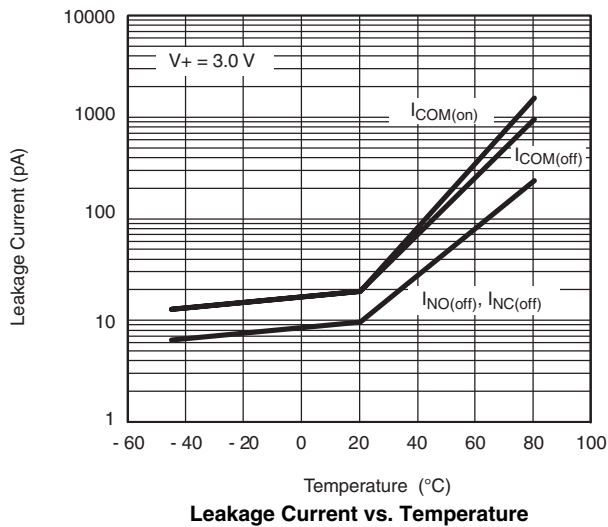
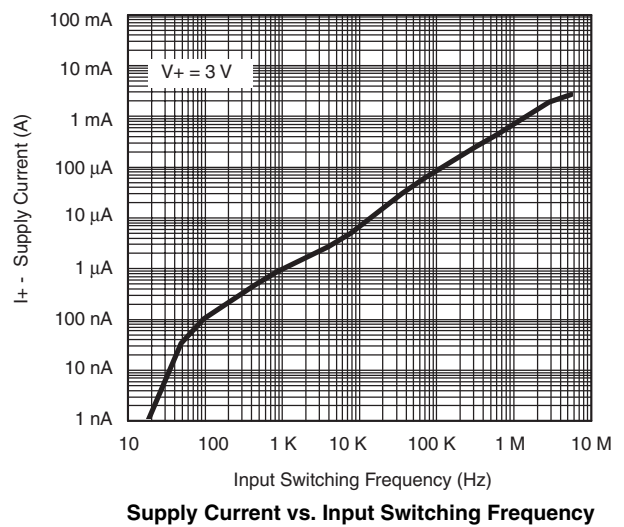
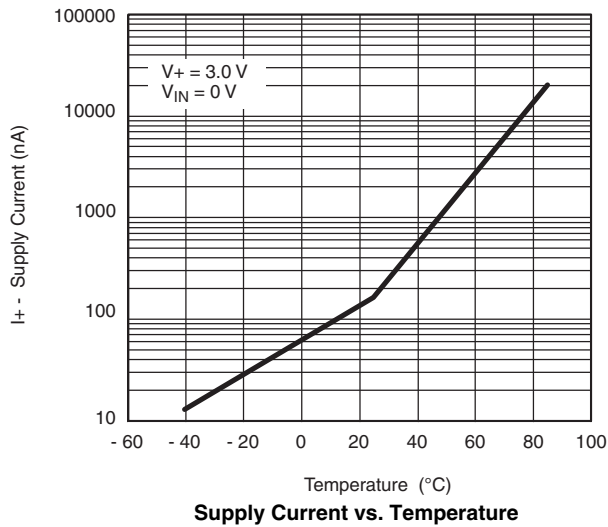
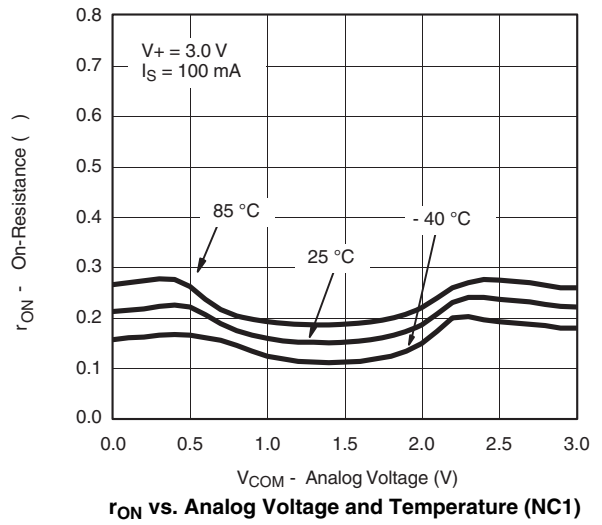
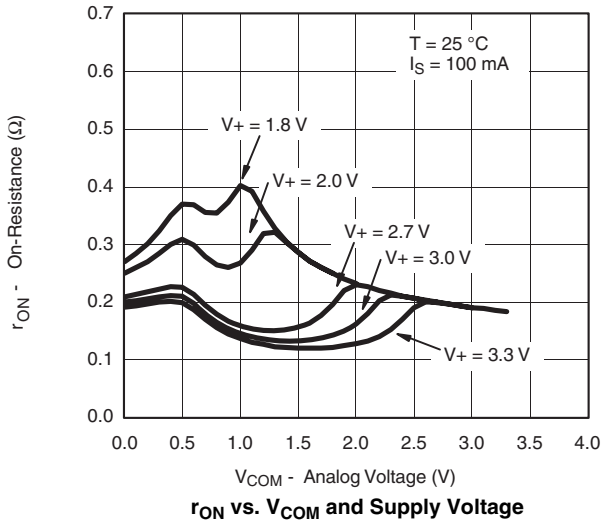


SPECIFICATIONS (V+ = 3.0 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, V <sub>IN</sub> = 0.5 V or 1.4 V <sup>e</sup>	Temp <sup>a</sup>	Limits - 40 to 85 °C			Unit
				Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
<b>Dynamic Characteristics</b>							
Turn-On Time	t <sub>ON</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 2.0 V, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF	Room Full		52 82 90		ns
Turn-Off Time	t <sub>OFF</sub>		Room Full		43 73 78		
Break-Before-Make Time	t <sub>d</sub>		Room	1	6		
Charge Injection <sup>d</sup>	Q <sub>INJ</sub>	C <sub>L</sub> = 1 nF, V <sub>GEN</sub> = 1.5 V, R <sub>GEN</sub> = 0 Ω	Full		21		pC
Off-Isolation <sup>d</sup>	OIRR	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 100 kHz	Room		- 69		dB
Crosstalk <sup>d</sup>	X <sub>TALK</sub>		Room		- 69		
N <sub>O</sub> , N <sub>C</sub> Off Capacitance <sup>d</sup>	C <sub>NO(off)</sub>	V <sub>IN</sub> = 0 or V+, f = 1 MHz	Room		145		pF
	C <sub>NC(off)</sub>		Room		145		
Channel-On Capacitance <sup>d</sup>	C <sub>NO(on)</sub>		Room		406		
	C <sub>NC(on)</sub>		Room		406		
<b>Power Supply</b>							
Power Supply Current	I+	V <sub>IN</sub> = 0 or V+	Room Full		0.001 1.0 1.0		μA

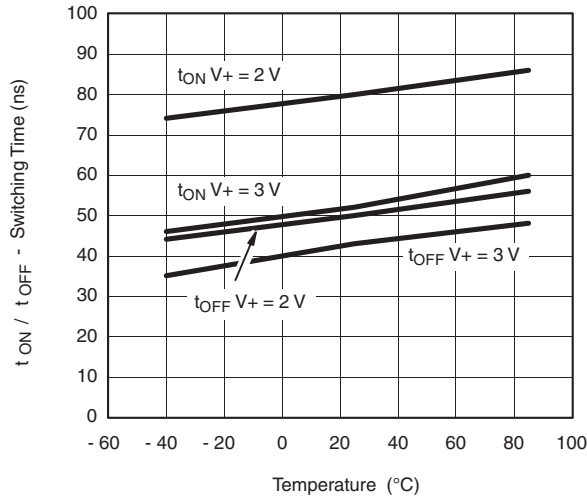
Notes:

- a. Room = 25 °C, Full = as determined by the operating suffix.
- b. Typical values are for design aid only, not guaranteed nor subject to production testing.
- c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- d. Guarantee by design, nor subjected to production test.
- e. V<sub>IN</sub> = input voltage to perform proper function.

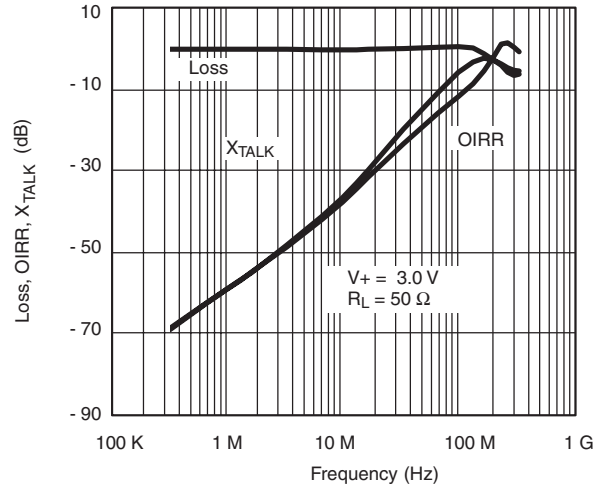
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



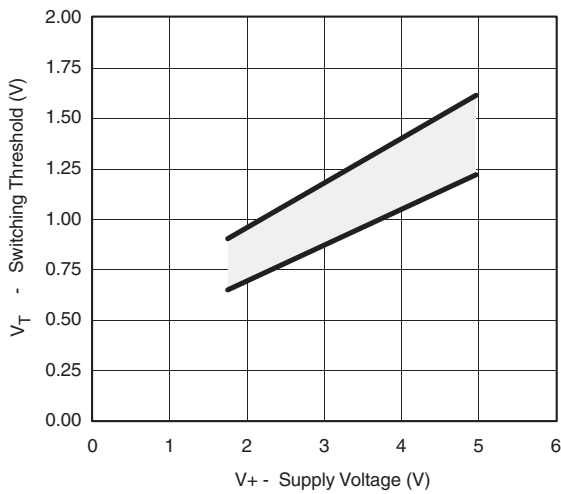
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



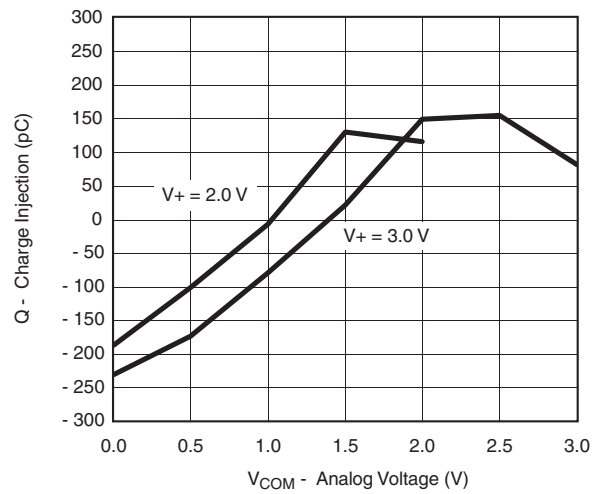
**Switching Time vs. Temperature**



**Insertion Loss, Off-Isolation Crosstalk vs. Frequency**

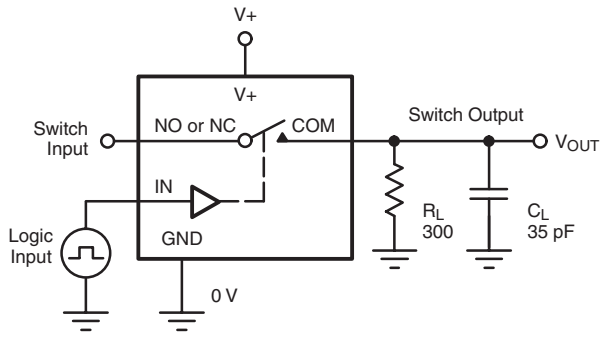


**Switching Threshold vs. Supply Voltage**



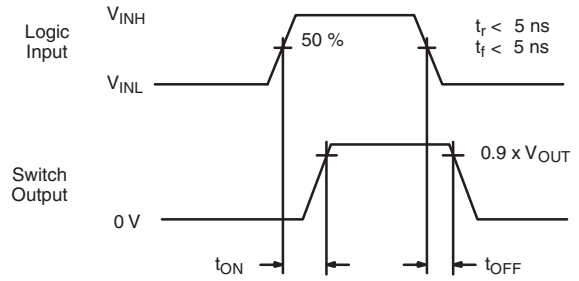
**Charge Injection vs. Analog Voltage**

TEST CIRCUITS



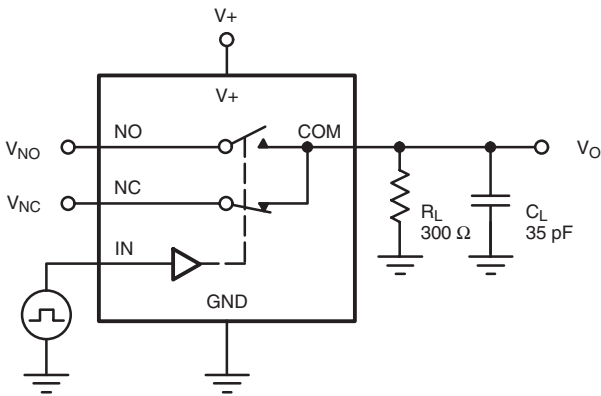
$C_L$  (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left( \frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On  
 Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



$C_L$  (includes fixture and stray capacitance)

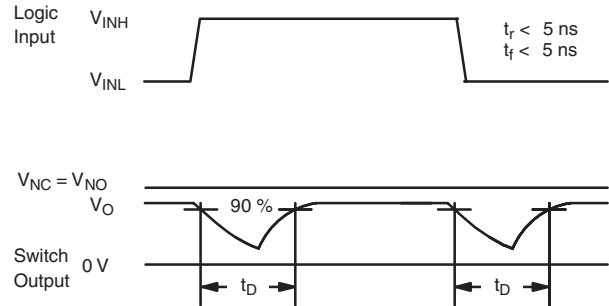
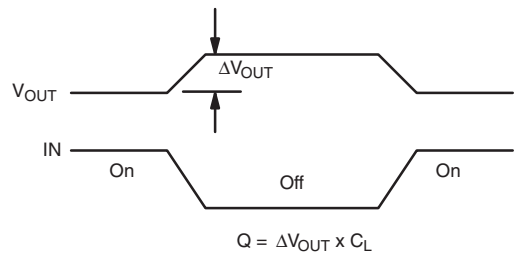
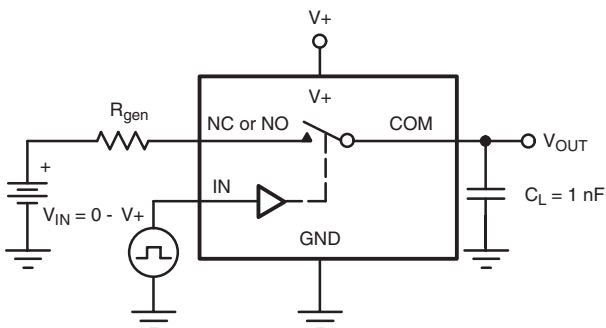


Figure 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

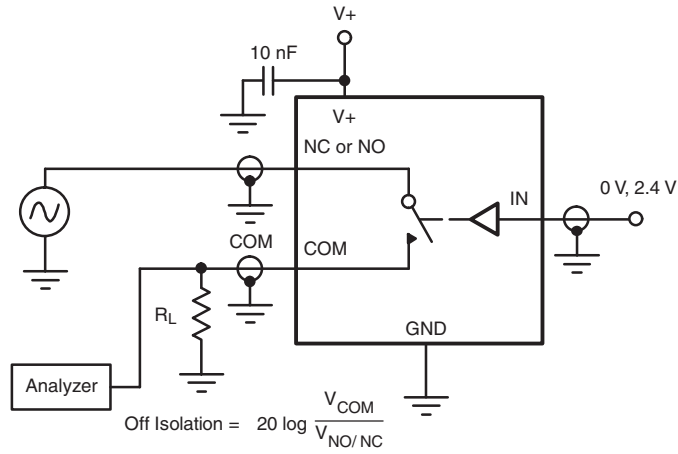


Figure 4. Off-Isolation

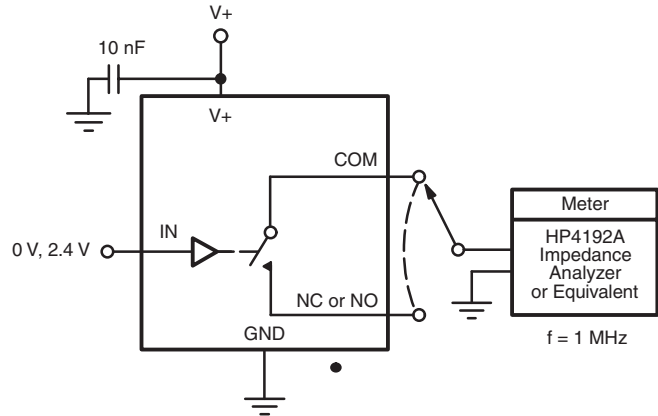
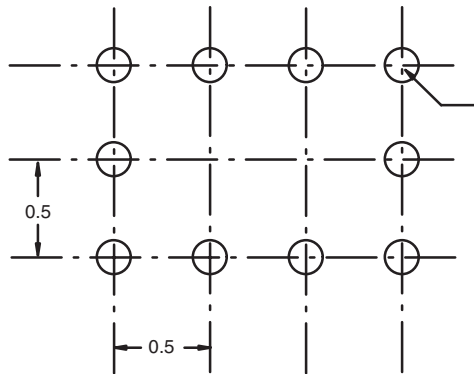


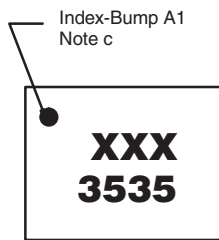
Figure 5. Channel Off/On Capacitance

### PACKAGE OUTLINE

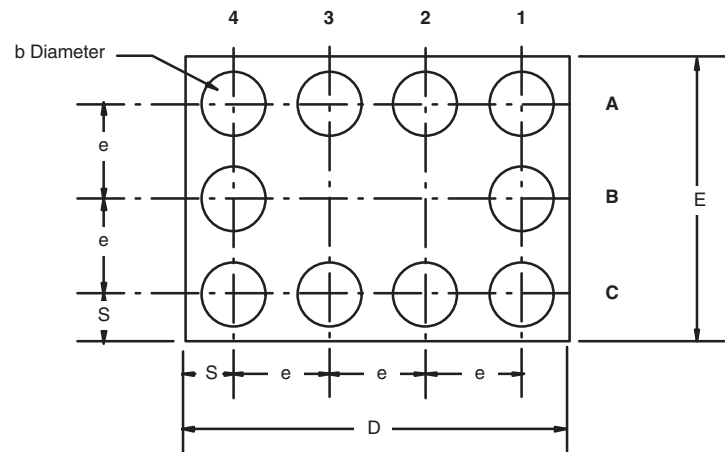
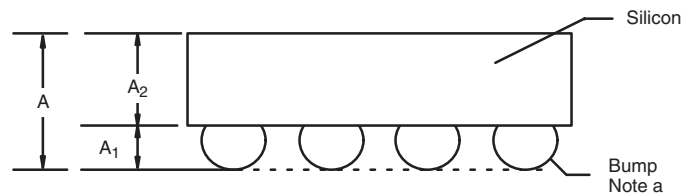
#### MICRO FOOT: 10 BUMP (4 x 3, 0.5 mm PITCH, 0.238 mm BUMP HEIGHT)



Recommended Land Pattern



Top Side (Die Back)



Notes (Unless Otherwise Specified):

- a. Bump is Lead Free Sn/Ag/Cu.
- b. Non-solder mask defined copper landing pad.
- c. Laser Mark on silicon die back; back-lapped, no coating. Shown is not actual marking; sample only.

Dim	Millimeters <sup>a</sup>		Inches	
	Min	Max	Min	Max
A	0.688	0.753	0.0271	0.0296
A <sub>1</sub>	0.218	0.258	0.0086	0.0102
A <sub>2</sub>	0.470	0.495	0.0185	0.0195
b	0.306	0.346	0.0120	0.0136
D	1.980	2.020	0.0780	0.0795
E	1.480	1.520	0.0583	0.0598
e	0.5 BASIC		0.0197 BASIC	
S	0.230	0.270	0.0091	0.0106

Notes:

- a. Use millimeters as the primary measurement.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?72961>.





## Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.