Dual Non-Inverting Buffer

The NLU2G16 MiniGate[™] is an advanced high-speed CMOS dual non-inverting buffer in ultra-small footprint.

The NLU2G16 input and output structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

Features

- High Speed: $t_{PD} = 3.5 \text{ ns (Typ)} @ V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation: $I_{CC} = 1 \mu A$ (Max) at $T_A = 25^{\circ}C$
- Power Down Protection Provided on inputs
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input and Output Pins
- Ultra-Small Packages
- These are Pb-Free Devices

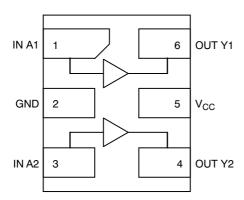


Figure 1. Pinout (Top View)

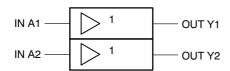


Figure 2. Logic Symbol



ON Semiconductor®

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MARKING DIAGRAMS



UDFN6 MU SUFFIX CASE 517AA





ULLGA6 1.0 x 1.0 CASE 613AD





ULLGA6 1.2 x 1.0 CASE 613AE





ULLGA6 1.45 x 1.0 CASE 613AF



C or 4 = Device Marking M = Date Code

PIN ASSIGNMENT

1	IN A1			
2	GND			
3	IN A2			
4	OUT Y2			
5	V _{CC}			
6	OUT Y1			

FUNCTION TABLE

Α	Υ
L	L
H	H

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
V _{CC}	DC Supply Voltage		-0.5 to +7.0	V
V _{IN}	DC Input Voltage		-0.5 to +7.0	V
V _{OUT}	DC Output Voltage		-0.5 to +7.0	V
I _{IK}	DC Input Diode Current	V _{IN} < GND	-20	mA
I _{OK}	DC Output Diode Current	±20	mA	
Io	DC Output Source/Sink Current	±12.5	mA	
I _{CC}	DC Supply Current Per Supply Pin	±25	mA	
I _{GND}	DC Ground Current per Ground Pin	±25	mA	
T _{STG}	Storage Temperature Range		-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Sec	onds	260	°C
TJ	Junction Temperature Under Bias	150	°C	
MSL	Moisture Sensitivity	Level 1		
F _R	Flammability Rating Oxygen	Index: 28 to 34	UL 94 V-0 @ 0.125 in	
I _{LATCHUP}	Latchup Performance Above V _{CC} and Below G	±500	mA	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.

2. Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage	1.65	5.5	V
V _{IN}	Digital Input Voltage	0	5.5	V
V _{OUT}	Output Voltage	0	5.5	V
T _A	Operating Free-Air Temperature	-55	+125	°C
Δt/ΔV	Input Transition Rise or Fall Rate $ V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V} $ $ V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V} $	0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

			v _{cc}	T,	_A = 25 °	С	T _A = +	-85°C		55°C to 5°C	
Symbol	Parameter	Conditions	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V _{IH}	Low-Level Input Voltage		1.65	0.75 x V _{CC}			0.75 x V _{CC}				V
			2.3 to 5.5	0.70 x V _{CC}			0.70 x V _{CC}				
V _{IL}	Low-Level Input Voltage		1.65			0.25 x V _{CC}		0.25 x V _{CC}		0.25 x V _{CC}	V
			2.3 to 5.5			0.30 x V _{CC}		0.30 x V _{CC}		0.30 x V _{CC}	
V _{OH}	High-Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4$ mA $I_{OH} = -8$ mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V _{OL}	Low-Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50 \mu\text{A}$	2.0 3.0 4.5		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4$ mA $I_{OL} = 8$ mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I _{IN}	Input Leakage Current	$0 \le V_{IN} \le 5.5 V$	0 to 5.5			±0.1		±1.0		±1.0	μΑ
lcc	Quiescent Supply Current	$0 \le V_{IN} \le V_{CC}$	5.5			1.0		10		40	μΑ

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ nS}$)

		v _{cc}	Test	т	_A = 25 °	С	T _A = 4	-85°C	T _A = -5 +12		
Symbol	Parameter	(V)	Condition	Min	Тур	Max	Min	Max	Min	Max	Unit
t _{PLH} ,	t _{PHL} Input A to Output Y 3.6 4.5 to	3.0 to	C _L = 15 pF		4.5	7.1		8.5		10	ns
^l PHL		3.6	C _L = 50 pF		6.4	10.6		12		14.5	
		4.5 to	C _L = 15 pF		3.5	5.5		6.5		8.0	
		5.5	C _L = 50 pF		4.5	7.5		8.5		10	
C _{IN}	Input Capacitance				4.0	10		10		10	pF
C _{PD}	Power Dissipation Capacitance (Note 3)	5.0			8.0						pF

^{3.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

SWITCHING WAVEFORMS

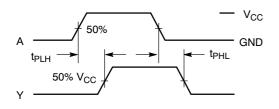
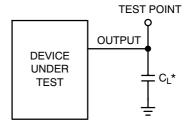


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance

Figure 4. Test Circuit

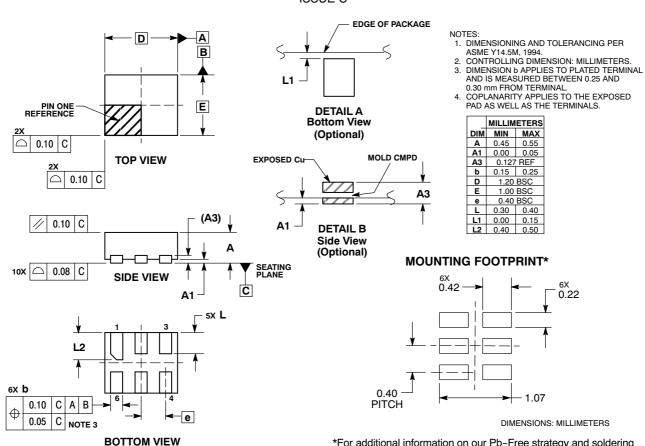
ORDERING INFORMATION

Device	Package	Shipping [†]
NLU2G16MUTCG	UDFN6 (Pb-Free)	3000 / Tape & Reel
NLU2G16AMX1TCG	ULLGA6, 1.45 x 1.0, 0.5P (Pb-Free)	3000 / Tape & Reel
NLU2G16BMX1TCG	ULLGA6, 1.2 x 1.0, 0.4P (Pb-Free)	3000 / Tape & Reel
NLU2G16CMX1TCG	ULLGA6, 1.0 x 1.0, 0.35P (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

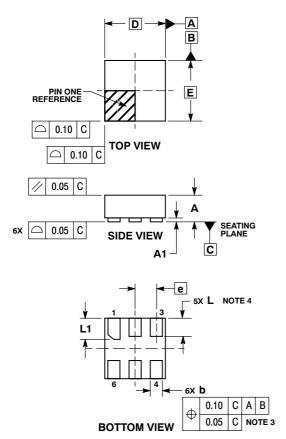
UDFN6, 1.2x1.0, 0.4P CASE 517AA-01 ISSUE C



^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

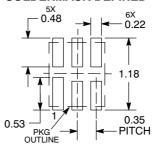
ULLGA6 1.0x1.0, 0.35P CASE 613AD-01 ISSUE A



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION & APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
 4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.
 - PACKAGE IS ALLOWED.

_	MILLIMETERS					
DIM	MIN	MAX				
Α	-	0.40				
A1	0.00	0.05				
b	0.12	0.22				
D	1.00 BSC					
E	1.00 BSC					
е	0.35 BSC					
L	0.25	0.35				
L1	0.30	0.40				

MOUNTING FOOTPRINT SOLDERMASK DEFINED*

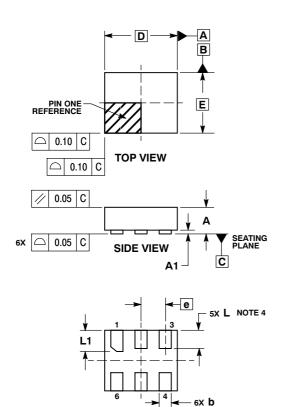


DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

ULLGA6 1.2x1.0, 0.4P CASE 613AE-01 ISSUE A



BOTTOM VIEW

0.10 C A B

0.05 C NOTE 3

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NOTES:

- ITES:

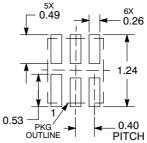
 DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

 CONTROLLING DIMENSION: MILLIMETERS. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

 A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

	MILLIMETERS						
DIM	MIN	MAX					
Α		0.40					
A1	0.00	0.05					
b	0.15	0.25					
D	1.20	BSC					
E	1.00	BSC					
е	0.40 BSC						
L	0.25	0.35					
L1	0.35	0.45					

MOUNTING FOOTPRINT SOLDERMASK DEFINED*

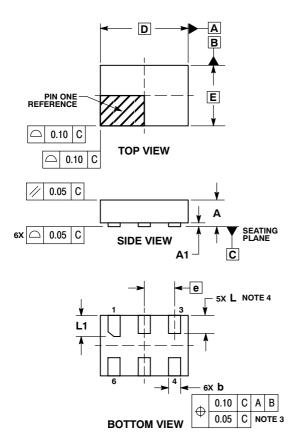


DIMENSIONS: MILLIMETERS

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

ULLGA6 1.45x1.0, 0.5P CASE 613AF-01 **ISSUE A**

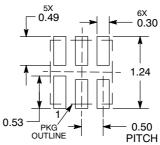


NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION 5 APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
- A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

	MILLIMETERS						
DIM	MIN	MAX					
Α	-	0.40					
A1	0.00	0.05					
b	0.15	0.25					
D	1.45 BSC						
E	1.00 BSC						
е	0.50 BSC						
L	0.25	0.35					
L1	0.30	0.40					

MOUNTING FOOTPRINT SOLDERMASK DEFINED*



DIMENSIONS: MILLIMETERS

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