ARIZONA MICROTEK, INC.

AZP51
AZP52
AZP53
AZP54

Low Phase Noise Sine Wave to LVPECL Buffer/Divider

FEATURES

- 3.0 to 3.6 V operating supply range
- LVPECL Outputs
- Optimized for Low Phase Noise
- Frequency Input to >650 MHz
- QFN 8 (1.5x1.5 mm), SC-70 or SOT-23 packages
- All Packages Green / RoHS Compliant / Lead (Pb) Free

PACKAGE AVAILABILITY

BASE PART	PACKAGE	PART NO.	MARKING	NOTES
AZP51 (÷1)	SC-70 Green / RoHS Compliant / Lead (Pb) Free	AZP51SG	D1G <Date Code>	1,2
AZP52 (÷2)	SC-70 Green / RoHS Compliant / Lead (Pb) Free	AZP52SG	D2G <Date Code>	1,2
AZP53 (÷1,2)	QFN 8 (1.5x1.5 mm) Green / RoHS Compliant / Lead (Pb) Free	AZP53PG	D3 <Date Code>	1,3
AZP54 (÷1)	SOT-23 Green / RoHS Compliant / Lead (Pb) Free	AZP54VG	D4G <Date Code>	1,2

1 Add R1 at end of part number for 7 inch , R2 for 13 inch Tape & Reel.
2 Date code format: "Y" for year followed by "WW" for week.
3 See Arizona Microtek web site for date code format.

DESCRIPTION

The AZP51 series is a family of sine wave to LVPECL buffers optimized for low phase noise. It is particularly useful in converting sine wave crystal or SAW based oscillator outputs into LVPECL outputs. The IC also includes an optional ÷2 function to provide better frequency range coverage when using a SAW based oscillator.

The D input is internally biased to $V_{DD}/2$. A sine wave input of at least 750 mv p-p ensures the AZP51 series meets its AC specifications. This input (D) should be capacitively coupled from the oscillator stage to ensure best output duty cycle.

AZP51S (÷1), AZP52S (÷2), SC-70 Package

The Enable input (EN) is active high with an internal pullup. When EN is high or not connected, the outputs (Q,$\overline{Q}$) are active. When EN is low, Q and $\overline{Q}$ are disabled in a high impedance (tri-state) condition. Refer to the Functional Operation table for more information.

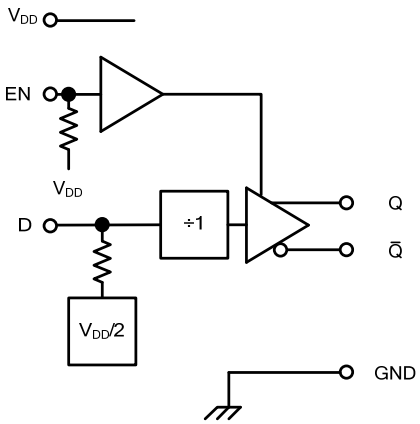
AZP53P (÷1, ÷2), QFN 8 1.5x1.5mm Package

The EN_SEL input selects the operational polarity for the EN input, so the EN input can be set to active high or active low operation. Refer to the Functional Operation table for more information.

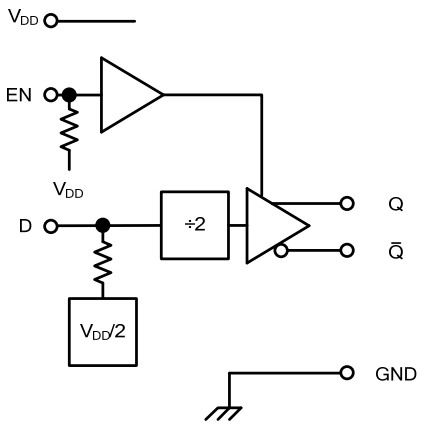
AZP54V (÷1) SOT-23 Package

The Enable input (EN) is active low with an internal pulldown. When EN is low or not connected, the outputs (Q,$\overline{Q}$) are active. When EN is high, Q and $\overline{Q}$ are disabled in a high impedance (tri-state) condition. Refer to the Functional Operation table for more information.

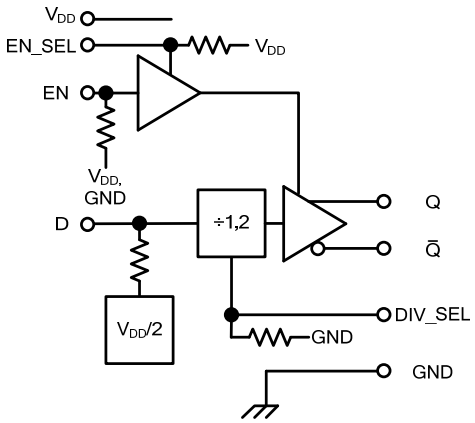
BLOCK DIAGRAMS



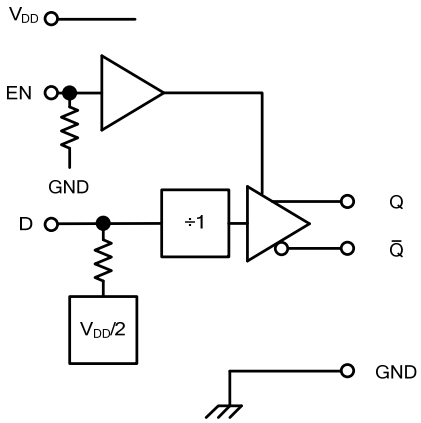
AZP51



AZP52



AZP53



AZP54

SIGNAL DESCRIPTION

PIN/PAD	FUNCTION
D	Sine or LVCMOS Input
Q,$\overline{Q}$	LVPECL Outputs
EN	Output Enable
DIV_SEL	Divide Select (AZP53 only)
EN_SEL	Enable Select (AZP53 only)
V_{DD}	Positive Supply
GND	Negative Supply (Ground)

DIV-SEL OPERATION

PART NUMBER	DIV-SEL	DIVIDE RATIO
AZP51 AZP54	-[2]	÷1
AZP52	-[2]	÷2
AZP53	NC[1],L H	÷1 ÷2

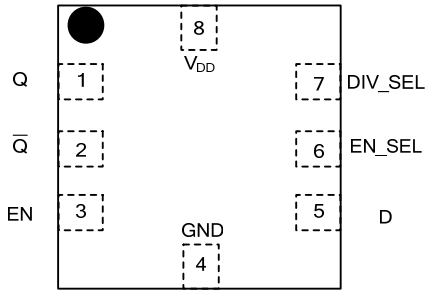
1. NC – no connection
2. Internally connected

FUNCTIONAL OPERATION

PART NUMBER	INPUTS			EN LOGIC	EN PULLUP/ PULLDOWN	OUTPUTS	
	EN_SEL[7]	EN	D			Q	$\overline{Q}$
AZP51 AZP52	-[2]	NC[1], H	L	Active High[4]	Pullup	L[8]	H[8]
			H			H[8]	L[8]
		L	X[5]			Z[6]	Z[6]
AZP53	NC[1], H	NC[1], L	L	Active Low[3]	Pulldown	L[8]	H[8]
			H			H[8]	L[8]
		H	X[5]			Z[6]	Z[6]
	L	NC[1], H	L	Active High[4]	Pullup	L[8]	H[8]
			H			H[8]	L[8]
		L	X[5]			Z[6]	Z[6]
AZP54	-[2]	NC[1], L	L	Active Low[3]	Pulldown	L	H
			H			H	L
		H	X[5]			Z[6]	Z[6]

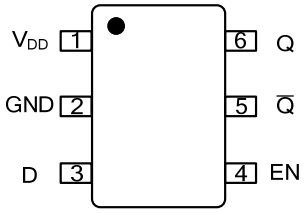
1. NC – no connection
2. Internally tied
3. Active Low: Output enabled when EN low, Tri-state when EN high
4. Active High: Output enabled when EN high, Tri-state when EN low
5. X – Don't care
6. Z – High impedance
7. EN_SEL input has an internal pullup resistor
8. ÷1 modes only

AZP53P
QFN 8, 1.5x1.5 mm



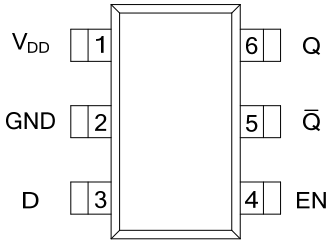
TOP VIEW

AZP51S, 52S
SC-70



TOP VIEW

AZP54V
SOT-23



TOP VIEW

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Rating	Unit
V_{DD}	Power Supply	0 to +5.5	Vdc
V_I	Input Voltage	-0.5 to V_{DD}+0.5	Vdc
T_A	Operating Temperature Range	-40 to +85	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C

DC Characteristics (V_{DD} = 3.0V to 3.6V unless otherwise specified, T_A = -40 to 85 C)

Symbol	Characteristic	Conditions		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage[1]	-40 C	V_{DD} = 3.3V	2.05		2.415	V
		25 C		2.05		2.480	
		85 C		2.05		2.540	
V_{OL}	Output LOW Voltage[1]	-40 C	V_{DD} = 3.3V	1.365		1.615	V
		25 C		1.430		1.680	
		85 C		1.490		1.740	
I_Z	Output Leakage Current, Tri-state[2]	EN=Disable[3]		-10		10	µA
V_{IH}	High Level Input Voltage	EN_SEL[4] DIV_SEL[4] EN		2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
R_{PU}	Pullup Resistor[4]	EN_SEL			50k		Ω
R_{PD}	Pulldown Resistor[4]	DIV_SEL			50k		Ω
R_P	Pullup/Pulldown Resistor[5]	EN			50k		Ω
R_{BIAS}	Bias Resistor	D Input to Internal V_{DD}/2 Reference			10k		Ω
I_{DD}	Power Supply Current				22	35	mA

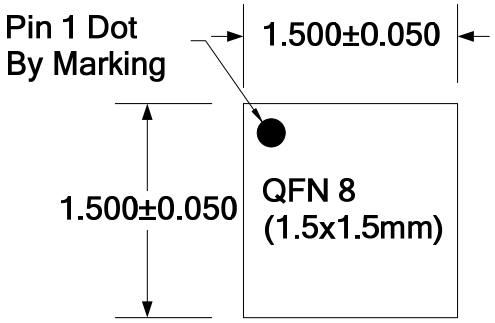
1. Specified with outputs terminated through 50Ω resistors to V_{DD} - 2V or Thevenin equivalent.
2. Measured at Q/$\overline{Q}$ pins.
3. See functional tables for Disable state definition.
4. AZP53 only.
5. See functional operation table for pullup/pulldown mode selection.

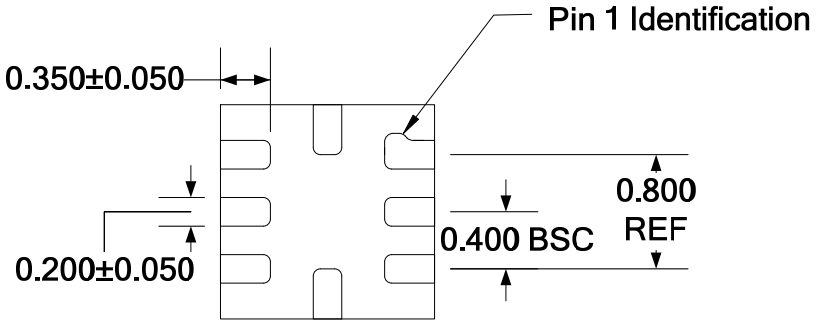
AC Characteristics (V_{DD} = 3.0V to 3.6V, T_A = -40 to 85 C)

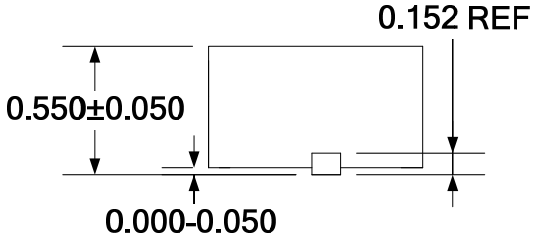
Symbol	Characteristic	Min	Max	Unit
t_r / t_f	Output Rise/Fall[1] (20% - 80%)	0.25	0.7	ns
f_{MAX}	Maximum Input Frequency – Sine wave[2]		650	MHz
t_{pd}	Propagation Delay[1,3,6] D to Q/$\overline{Q}$	1.0	3.0	ns
t_{en}	Enable[1,4] EN to Q/$\overline{Q}$		200	ns
t_{dis}	Disable[1,5] EN to Q/$\overline{Q}$		80	ns
n_P	Phase Noise[1,3] 10 MHz offset		-158	dBc/ Hz

1. Specified with outputs terminated through 50Ω resistors to V_{CC} - 2V or Thevenin equivalent.
2. 750 mv p-p sine wave, AC coupled to D input.
3. 155 MHz 750 mv p-p sine wave input.
4. EN asserted (enabled) to Q/$\overline{Q}$ outputs producing specified V_{OH} & V_{OL} levels.
5. EN deasserted (disabled) to Q/$\overline{Q}$ outputs ≤ V_{OL} min.
6. Measured from 50% D to 50% Q/$\overline{Q}$.

PACKAGE DIAGRAM
P – QFN 8 1.5x1.5mm

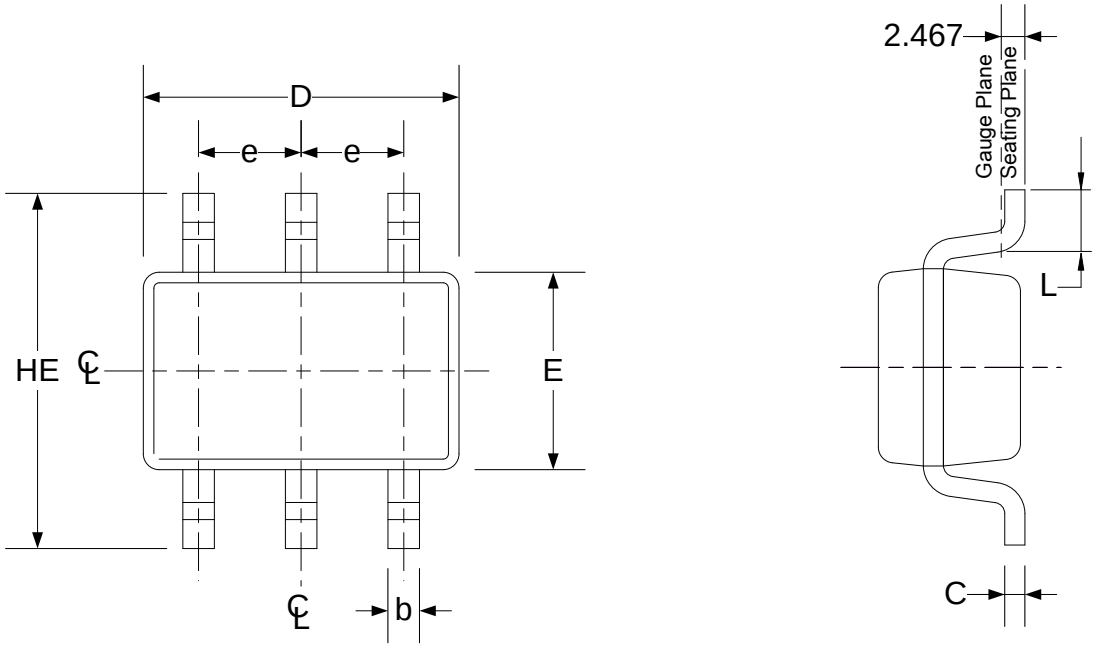


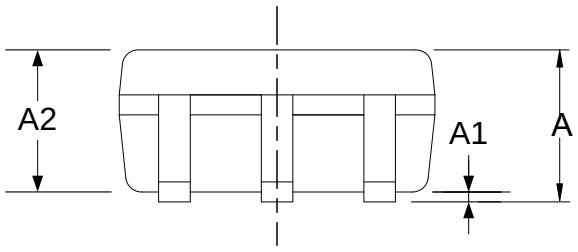




Note: All dimensions are in mm

PACKAGE DIAGRAM
S – SC-70 6L

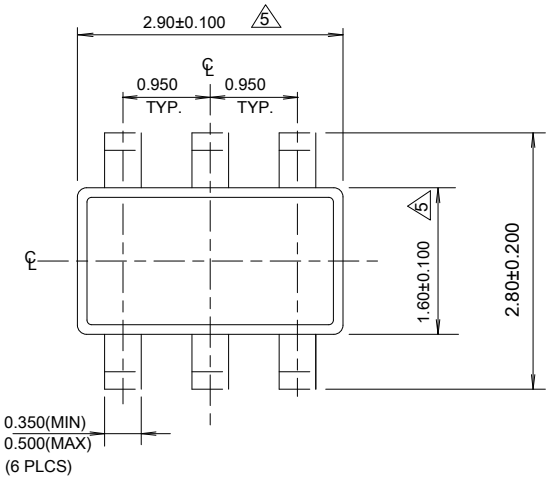




SYMBOL	MIN	MAX
E	1.15	1.35
D	1.85	2.25
HE	2.00	2.30
A	0.80	1.00
A2	0.80	0.91
A1	0.00	0.09
e	0.65 BSC	
b	0.15	0.30
c	0.08	0.25
L	0.21	0.41

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & GATE BURR.

PACKAGE DIAGRAM
V – SOT-23 6L



NOTE:

1. Dimensions and tolerances are as per ANSI Y14.5M, 1982.
2. Package surface to be matte finish VDI 11~13.
3. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
4. The footlength measuring is based on the gauge plane method.

5. Dimension are exclusive of mold flash and gate burr.

6. Dimension are exclusive of solder plating.