

74AC377, 74ACT377 Octal D-Type Flip-Flop with Clock Enable

Features

- I_{CC} reduced by 50%
- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Outputs source/sink 24mA
- See 273 for master reset version
- See 373 for transparent latch version
- See 374 for 3-STATE version
- ACT377 has TTL-compatible inputs

General Description


The AC/ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (\overline{CE}) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The \overline{CE} input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

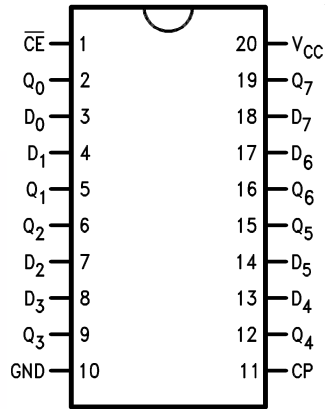
Ordering Information

| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74AC377SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74AC377SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74AC377MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74ACT377SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74ACT377SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74ACT377MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74ACT377PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

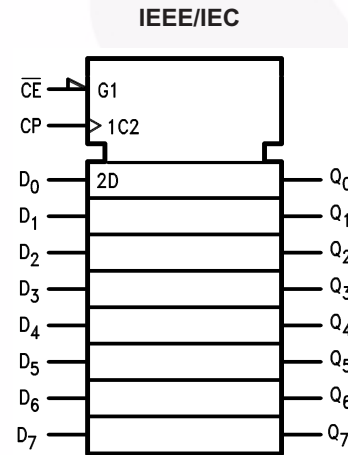
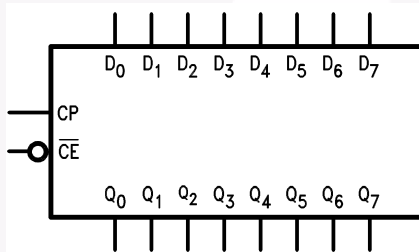
Connection Diagram



Pin Descriptions

| Pin Names | Description |
|--------------------------------|---------------------------|
| D ₀ -D ₇ | Data Inputs |
| \overline{CE} | Clock Enable (Active LOW) |
| Q ₀ -Q ₇ | Data Outputs |
| CP | Clock Pulse Input |

Logic Symbols



Mode Select-Function Table

| Operating Mode | Inputs | | | Outputs |
|-------------------|--------|-----------------|----------------|----------------|
| | CP | \overline{CE} | D _n | Q _n |
| Load '1' | ↗ | L | H | H |
| Load '0' | ↗ | L | L | L |
| Hold (Do Nothing) | ↗ | H | X | No Change |
| | X | H | X | No Change |

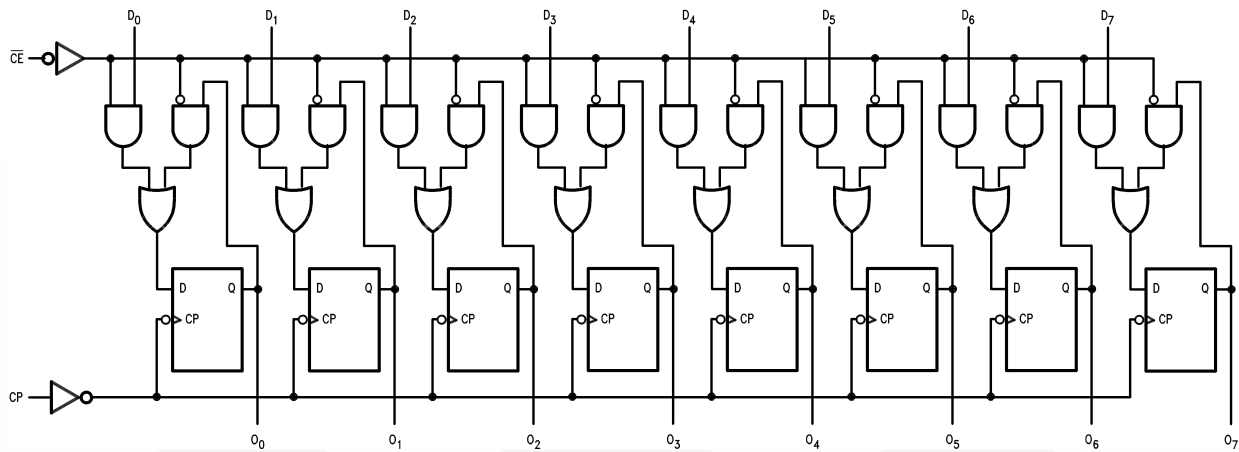
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

↗ = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|-----------------------|---|--------------------------|
| V_{CC} | Supply Voltage | -0.5V to +7.0V |
| I_{IK} | DC Input Diode Current $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$ | -20mA +20mA |
| V_I | DC Input Voltage | -0.5V to $V_{CC} + 0.5V$ |
| I_{OK} | DC Output Diode Current $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$ | -20mA +20mA |
| V_O | DC Output Voltage | -0.5V to $V_{CC} + 0.5V$ |
| I_O | DC Output Source or Sink Current | $\pm 50mA$ |
| I_{CC} or I_{GND} | DC V_{CC} or Ground Current per Output Pin | $\pm 50mA$ |
| T_{STG} | Storage Temperature | -65°C to +150°C |
| T_J | Junction Temperature | 140°C |

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Rating |
|-----------------------|--|------------------------------|
| V_{CC} | Supply Voltage AC ACT | 2.0V to 6.0V 4.5V to 5.5V |
| V_I | Input Voltage | 0V to V_{CC} |
| V_O | Output Voltage | 0V to V_{CC} |
| T_A | Operating Temperature | -40°C to +85°C |
| $\Delta V / \Delta t$ | Minimum Input Edge Rate, AC Devices: V_{IN} from 30% to 70% of V_{CC} , V_{CC} @ 3.3V, 4.5V, 5.5V | 125mV/ns |
| $\Delta V / \Delta t$ | Minimum Input Edge Rate, ACT Devices: V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V | 125mV/ns |

DC Electrical Characteristics for AC

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | T _A = -40°C to +85°C | | Units | |
|--------------------------------|---|------------------------|---|--|-------------------|---------------------------------|------|-------|--|
| | | | | Typ. | Guaranteed Limits | | | | |
| V _{IH} | Minimum HIGH Level Input Voltage | 3.0 | V _{OUT} = 0.1V or V _{CC} - 0.1V | 1.5 | 2.1 | 2.1 | | V | |
| | | 4.5 | | 2.25 | 3.15 | 3.15 | | | |
| | | 5.5 | | 2.75 | 3.85 | 3.85 | | | |
| V _{IL} | Maximum LOW Level Input Voltage | 3.0 | V _{OUT} = 0.1V or V _{CC} - 0.1V | 1.5 | 0.9 | 0.9 | | V | |
| | | 4.5 | | 2.25 | 1.35 | 1.35 | | | |
| | | 5.5 | | 2.75 | 1.65 | 1.65 | | | |
| V _{OH} | Minimum HIGH Level Output Voltage | 3.0 | I _{OUT} = -50μA | 2.99 | 2.9 | 2.9 | | V | |
| | | 4.5 | | 4.49 | 4.4 | 4.4 | | | |
| | | 5.5 | | 5.49 | 5.4 | 5.4 | | | |
| | | 3.0 | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -12mA | | 2.56 | 2.46 | | | |
| | | 4.5 | | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA | | 3.86 | 3.76 | | |
| | | 5.5 | | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA ⁽¹⁾ | | 4.86 | 4.76 | | |
| V _{OL} | Maximum LOW Level Output Voltage | 3.0 | I _{OUT} = 50μA | 0.002 | 0.1 | 0.1 | | V | |
| | | 4.5 | | 0.001 | 0.1 | 0.1 | | | |
| | | 5.5 | | 0.001 | 0.1 | 0.1 | | | |
| | | 3.0 | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 12mA | | 0.36 | 0.44 | | | |
| | | 4.5 | | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA | | 0.36 | 0.44 | | |
| | | 5.5 | | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA ⁽¹⁾ | | 0.36 | 0.44 | | |
| I _{IN} ⁽³⁾ | Maximum Input Leakage Current | 5.5 | V _I = V _{CC} , GND | | ±0.1 | ±1.0 | | μA | |
| I _{OLD} | Minimum Dynamic Output Current ⁽²⁾ | 5.5 | V _{OLD} = 1.65V Max. | | | 75 | | mA | |
| I _{OHD} | | | V _{OHD} = 3.85V Min. | | | -75 | | mA | |
| I _{CC} ⁽³⁾ | Maximum Quiescent Supply Current | 5.5 | V _{IN} = V _{CC} or GND | | 4.0 | 40.0 | | μA | |

Notes:

- All outputs loaded; thresholds on input associated with output under test.
- Maximum test duration 2.0ms, one output loaded at a time.
- I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

DC Electrical Characteristics for ACT

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | T _A = -40°C to +85°C | | Units |
|------------------|---|------------------------|--|---|-------------------|---------------------------------|------|-------|
| | | | | Typ. | Guaranteed Limits | | | |
| V _{IH} | Minimum HIGH Level Input Voltage | 4.5 | V _{OUT} = 0.1V or V _{CC} - 0.1V | 1.5 | 2.0 | 2.0 | | V |
| | | 5.5 | | 1.5 | 2.0 | 2.0 | | |
| V _{IL} | Maximum LOW Level Input Voltage | 4.5 | V _{OUT} = 0.1V or V _{CC} - 0.1V | 1.5 | 0.8 | 0.8 | | V |
| | | 5.5 | | 1.5 | 0.8 | 0.8 | | |
| V _{OH} | Minimum HIGH Level Output Voltage | 4.5 | I _{OUT} = -50μA | 4.49 | 4.4 | 4.4 | | V |
| | | 5.5 | | 5.49 | 5.4 | 5.4 | | |
| | | 4.5 | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA | | 3.86 | 3.76 | | |
| | | 5.5 | | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA ⁽⁴⁾ | | 4.86 | 4.76 | |
| V _{OL} | Maximum LOW Level Output Voltage | 4.5 | I _{OUT} = 50μA | 0.001 | 0.1 | 0.1 | | V |
| | | 5.5 | | 0.001 | 0.1 | 0.1 | | |
| | | 4.5 | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA | | 0.36 | 0.44 | | |
| | | 5.5 | | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA ⁽⁴⁾ | | 0.36 | 0.44 | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | V _I = V _{CC} , GND | | ±0.1 | ± 1.0 | | μA |
| I _{CCT} | Maximum I _{CC} /Input | 5.5 | V _I = V _{CC} - 2.1V | 0.6 | | 1.5 | | mA |
| I _{OLD} | Minimum Dynamic Output Current ⁽⁵⁾ | 5.5 | V _{OLD} = 1.65V Max. | | | 75 | | mA |
| | | | V _{OHD} = 3.85V Min. | | | -75 | | mA |
| I _{CC} | Maximum Quiescent Supply Current | 5.5 | V _{IN} = V _{CC} or GND | | 4.0 | 40.0 | | μA |

Notes:

- All outputs loaded; thresholds on input associated with output under test.
- Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics for AC

| Symbol | Parameter | V _{CC} (V) ⁽⁶⁾ | T _A = +25°C | | | T _A = -40°C to +85°C | | Units |
|------------------|---|------------------------------------|------------------------|------|------|---------------------------------|------|-------|
| | | | Min. | Typ. | Max. | Min. | Max. | |
| f _{MAX} | Maximum Clock Frequency | 3.3 | 90 | 125 | | 75 | | MHz |
| | | 5.0 | 140 | 175 | | 125 | | |
| t _{PLH} | Propagation Delay, CP to Q _n | 3.3 | 3.0 | 8.0 | 13.0 | 1.5 | 14.0 | ns |
| | | 5.0 | 2.0 | 6.0 | 9.0 | 1.5 | 10.0 | |
| t _{PHL} | Propagation Delay, CP to Q _n | 3.3 | 3.5 | 8.5 | 13.0 | 2.0 | 14.5 | ns |
| | | 5.0 | 2.5 | 6.5 | 10.0 | 1.5 | 11.0 | |

Note:

6. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V

AC Operating Requirements for AC

| Symbol | Parameter | V _{CC} (V) ⁽⁷⁾ | T _A = +25°C, C _L = 50pF | | T _A = -40°C to +85°C, C _L = 50pF | | Units |
|----------------|---|------------------------------------|---|--------------------|--|--|-------|
| | | | Typ. | Guaranteed Minimum | | | |
| t _S | Setup Time, HIGH or LOW, D _n to CP | 3.3 | 3.5 | 5.5 | 6.0 | | ns |
| | | 5.0 | 2.5 | 4.0 | 4.5 | | |
| t _H | Hold Time, HIGH or LOW, D _n to CP | 3.3 | -2.0 | 0 | 0 | | ns |
| | | 5.0 | -1.0 | 1.0 | 1.0 | | |
| t _S | Setup Time, HIGH or LOW, CE to CP | 3.3 | 4.0 | 6.0 | 7.5 | | ns |
| | | 5.0 | 2.5 | 4.0 | 4.5 | | |
| t _H | Hold Time, HIGH or LOW, CE to CP | 3.3 | -3.5 | 0 | 0 | | ns |
| | | 5.0 | -2.0 | 1.0 | 1.0 | | |
| t _W | CP Pulse Width, HIGH or LOW | 3.3 | 3.5 | 5.5 | 6.0 | | ns |
| | | 5.0 | 2.5 | 4.0 | 4.5 | | |

Note:

7. Voltage range 3.3 is 3.0V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics for ACT

| Symbol | Parameter | V _{CC} (V) ⁽⁸⁾ | T _A = +25°C, C _L = 50pF | | | T _A = -40°C to +85°C, C _L = 50pF | | Units |
|------------------|--|------------------------------------|--|------|------|---|------|-------|
| | | | Min. | Typ. | Max. | Min. | Max. | |
| f _{MAX} | Maximum Clock Frequency | 5.0 | 140 | 175 | | 125 | | MHz |
| t _{PLH} | Propagation Delay, CP to Q _n | 5.0 | 3.0 | 6.5 | 9.0 | 2.5 | 10.0 | ns |
| t _{PHL} | Propagation Delay, CP to Q _n | 5.0 | 3.5 | 7.0 | 10.0 | 2.5 | 11.0 | ns |

Note:

8. Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements for ACT

| Symbol | Parameter | V _{CC} (V) ⁽⁹⁾ | T _A = +25°C, C _L = 50pF | | T _A = -40°C to +85°C, C _L = 50pF | | Units |
|----------------|--|------------------------------------|--|--------------------|---|--|-------|
| | | | Typ. | Guaranteed Minimum | | | |
| t _S | Setup Time, HIGH or LOW, D _n to CP | 5.0 | 2.5 | 4.5 | 5.5 | | ns |
| t _H | Hold Time, HIGH or LOW, D _n to CP | 5.0 | -1.0 | 1.0 | 1.0 | | ns |
| t _S | Setup Time, HIGH or LOW, $\overline{\text{CE}}$ to CP | 5.0 | 2.5 | 4.5 | 5.5 | | ns |
| t _H | Hold Time, HIGH or LOW, $\overline{\text{CE}}$ to CP | 5.0 | -1.0 | 1.0 | 1.0 | | ns |
| t _W | CP Pulse Width, HIGH or LOW | 5.0 | 2.0 | 4.0 | 4.5 | | ns |

Note:

9. Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

| Symbol | Parameter | Conditions | Typ. | Units |
|-----------------|-------------------------------|------------------------|------|-------|
| C _{IN} | Input Capacitance | V _{CC} = OPEN | 4.5 | pF |
| C _{PD} | Power Dissipation Capacitance | V _{CC} = 5.0V | 90.0 | pF |

Physical Dimensions

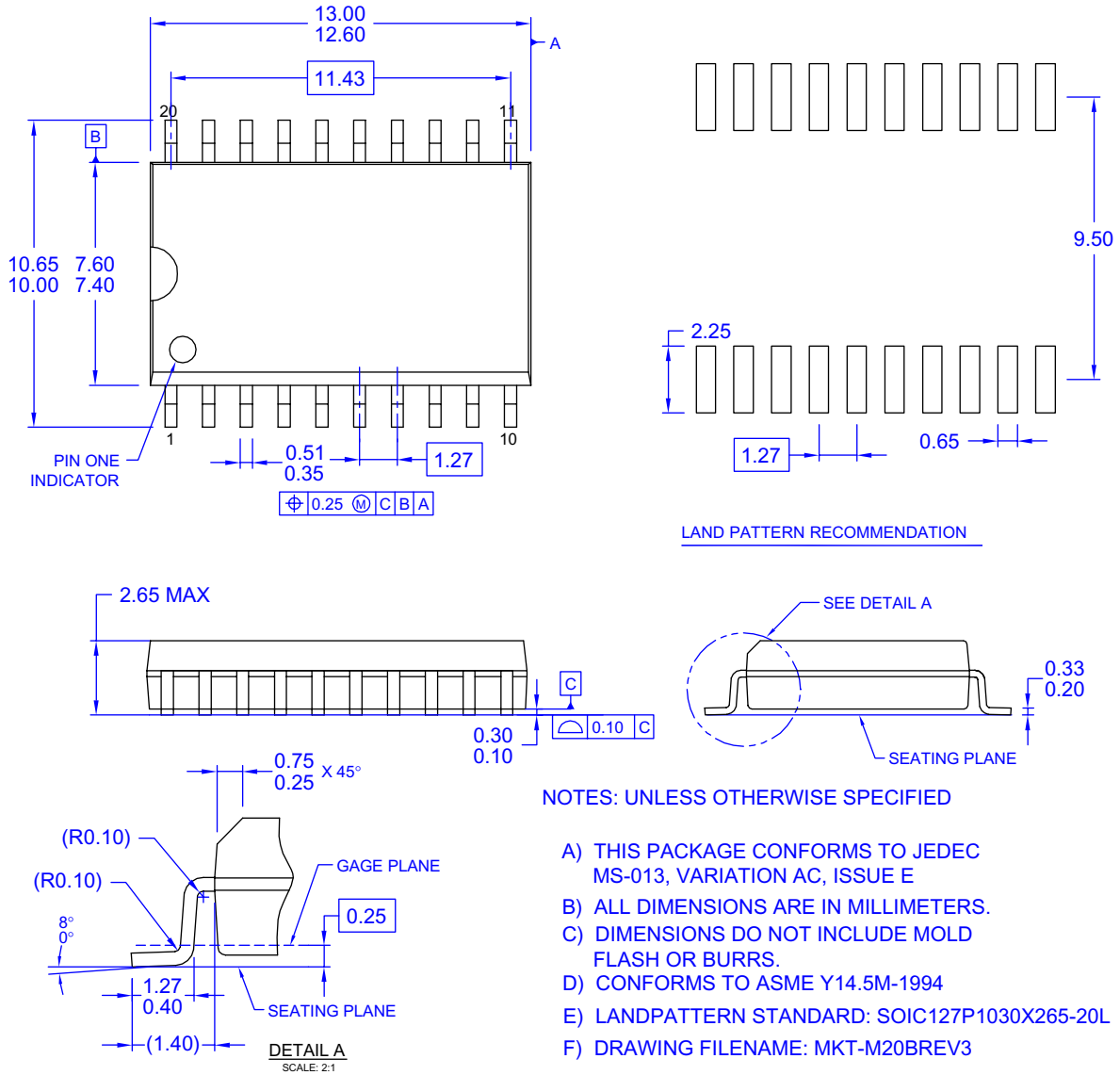


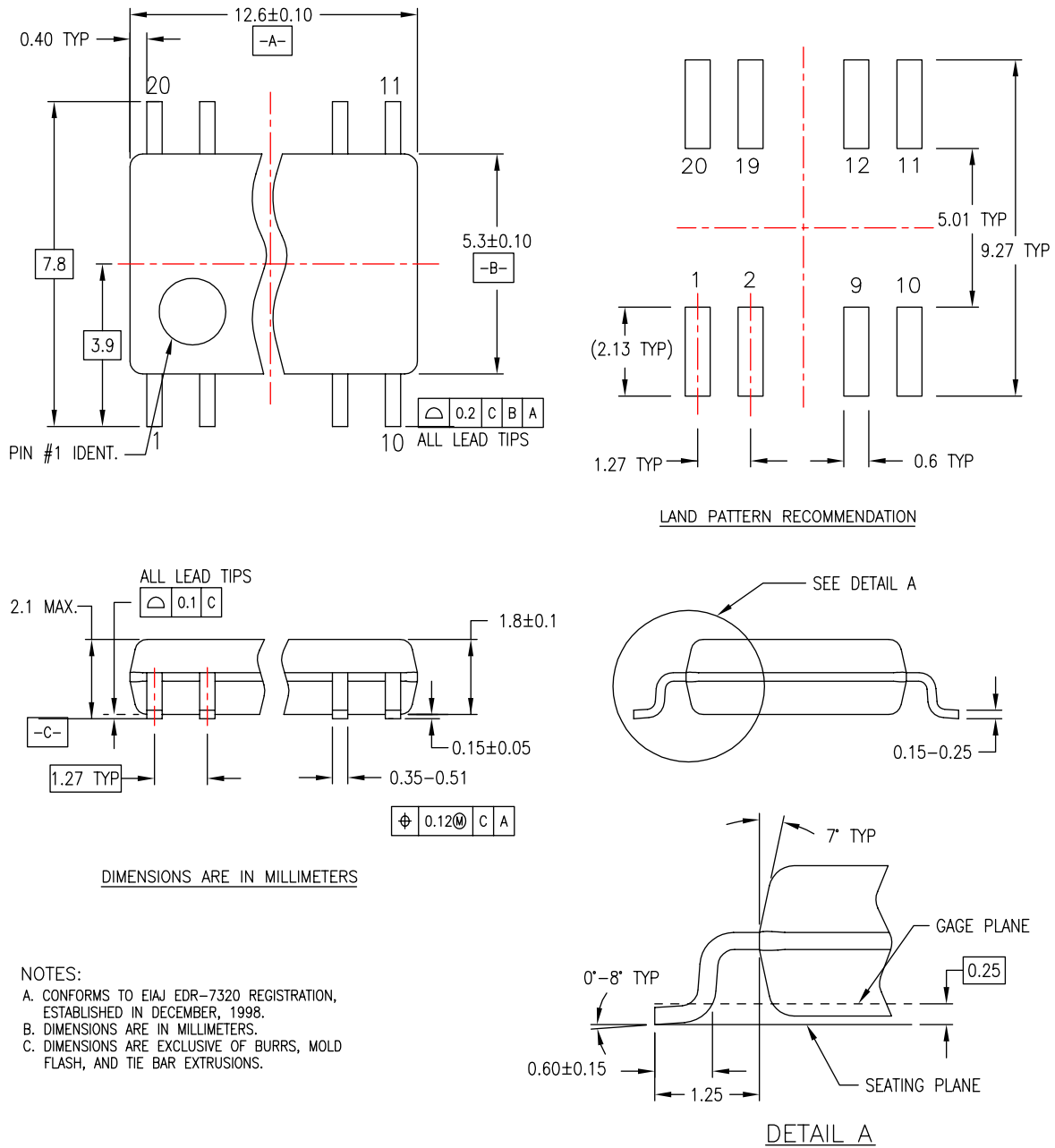
Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

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Physical Dimensions (Continued)



- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

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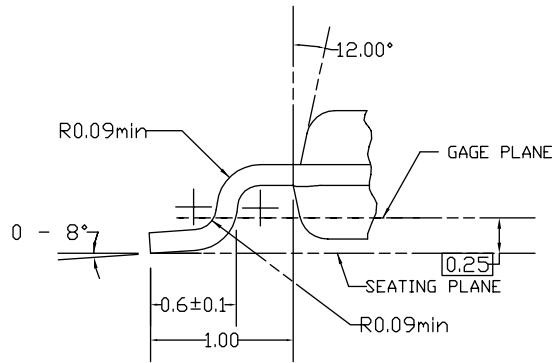
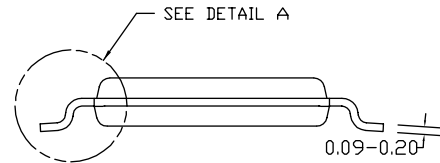
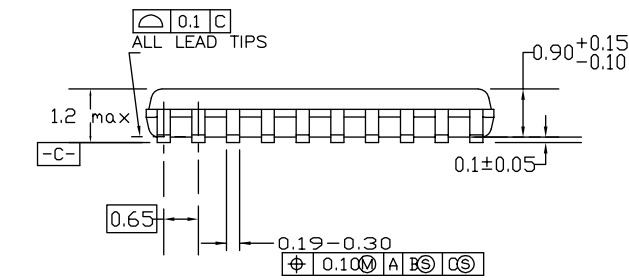
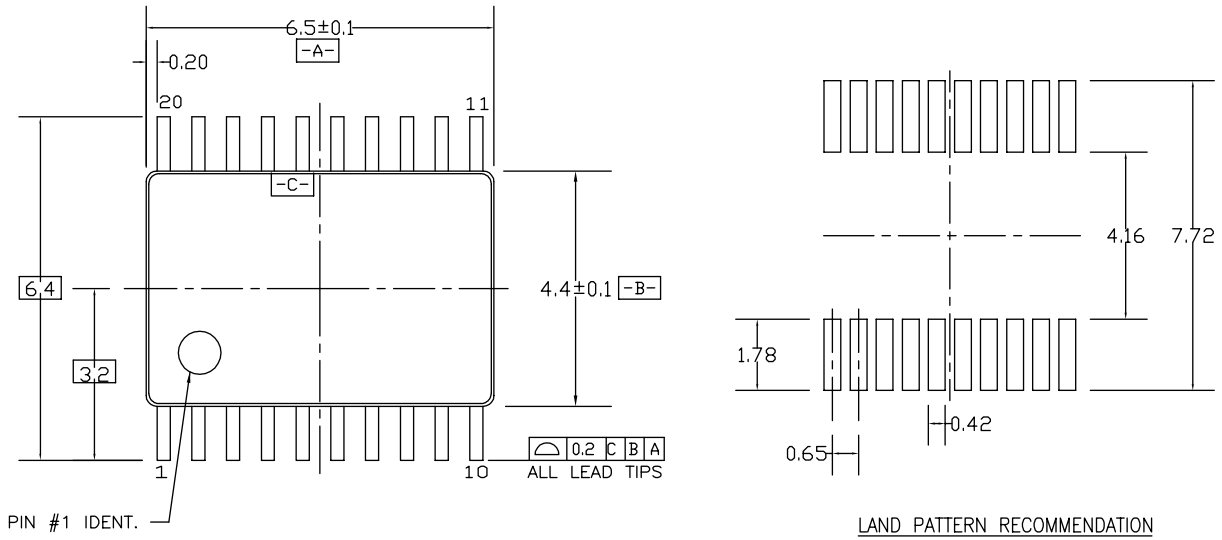
Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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Physical Dimensions (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REV D1

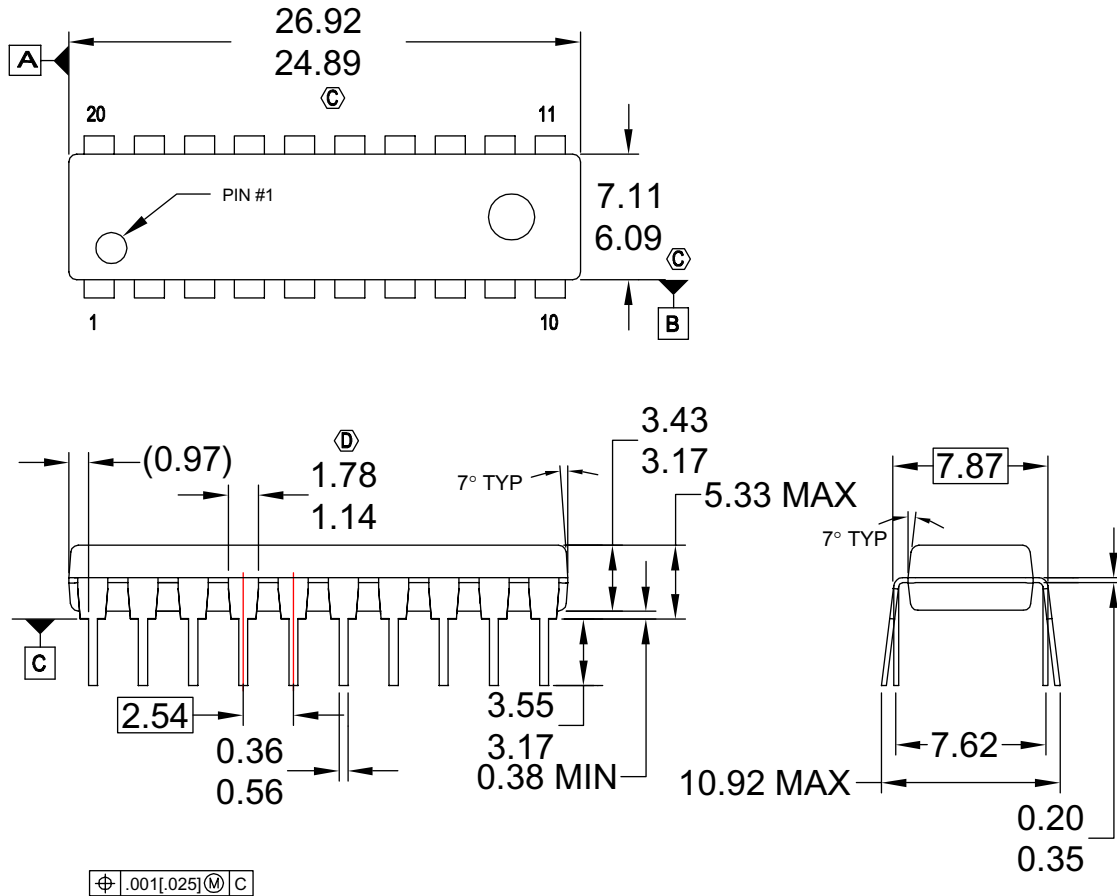
Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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Physical Dimensions (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MS-001, VARIATIONS AD.
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25MM.
- D. DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED 0.25MM.
- E. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- F. DRAWING FILE NAME: N20AREV8

Figure 4. 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

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