

**Silicon PNP Power Transistors**

**2SB546A**

**DESCRIPTION**

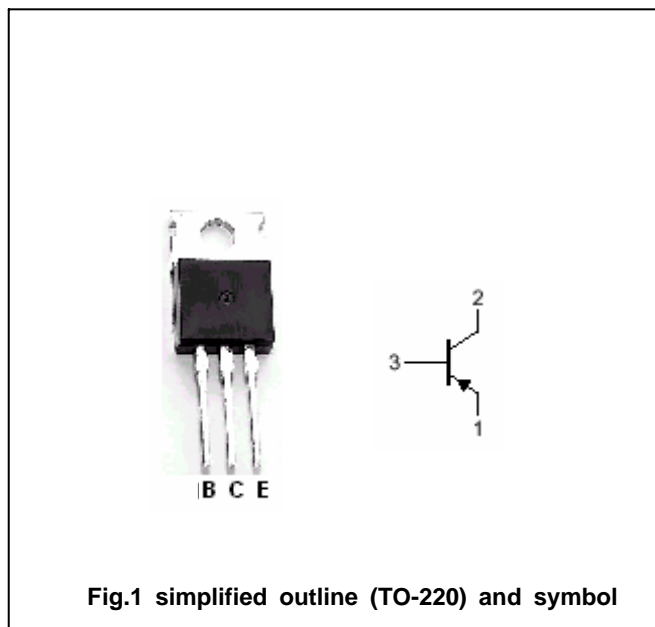
- With TO-220C package
- Complement to type 2SD401A
- Collector current  $I_C = -2A$
- Collector-base voltage  $V_{CBO} = -200V$

**APPLICATIONS**

- For use in general purpose power amplifier, vertical output application

**PINNING**

PIN	DESCRIPTION
1	Emitter
2	Collector; connected to mounting base
3	Base



**Absolute maximum ratings (Ta=25 )**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$V_{CBO}$	Collector-base voltage	Open emitter	-200	V
$V_{CEO}$	Collector-emitter voltage	Open base	-150	V
$V_{EBO}$	Emitter-base voltage	Open collector	-5	V
$I_C$	Collector current		-2	A
$I_{CM}$	Collector current-peak		-3	A
$P_T$	Total power dissipation	$T_C = 25$	30	W
$T_j$	Junction temperature		150	
$T_{stg}$	Storage temperature		-55~150	

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## CHARACTERISTICS

T<sub>j</sub>=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V <sub>(BR)CEO</sub>	Collector-emitter breakdown voltage	I <sub>C</sub> =-10mA; I <sub>B</sub> =0	-150			V
V <sub>(BR)CBO</sub>	Collector-base breakdown voltage	I <sub>C</sub> =-0.5mA; I <sub>E</sub> =0	-200			V
V <sub>(BR)EBO</sub>	Emitter-base breakdown voltage	I <sub>E</sub> =-0.5mA; I <sub>B</sub> =0	-5			V
V <sub>CEsat</sub>	Collector-emitter saturation voltage	I <sub>C</sub> =-500mA; I <sub>B</sub> =-50mA			-1.0	V
I <sub>CBO</sub>	Collector cut-off current	V <sub>CB</sub> =-150V; I <sub>E</sub> =0			-50	μA
I <sub>EBO</sub>	Emitter cut-off current	V <sub>EB</sub> =-5V; I <sub>C</sub> =0			-50	μA
h <sub>FE</sub>	DC current gain	I <sub>C</sub> =-0.4A; V <sub>CE</sub> =-10V	40		240	
f <sub>T</sub>	Transition frequency	I <sub>C</sub> =-0.4A; V <sub>CE</sub> =-10V		5		MHz

◆ h<sub>FE</sub> classifications

M	L	K
40-80	60-120	100-200

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PACKAGE OUTLINE

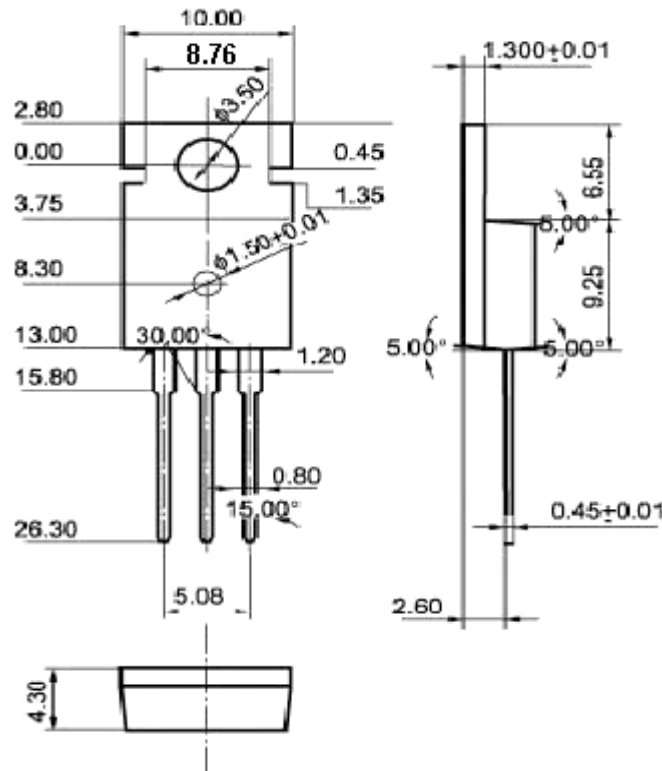


Fig.2 Outline dimensions (unindicated tolerance:  $\pm 0.10$  mm)

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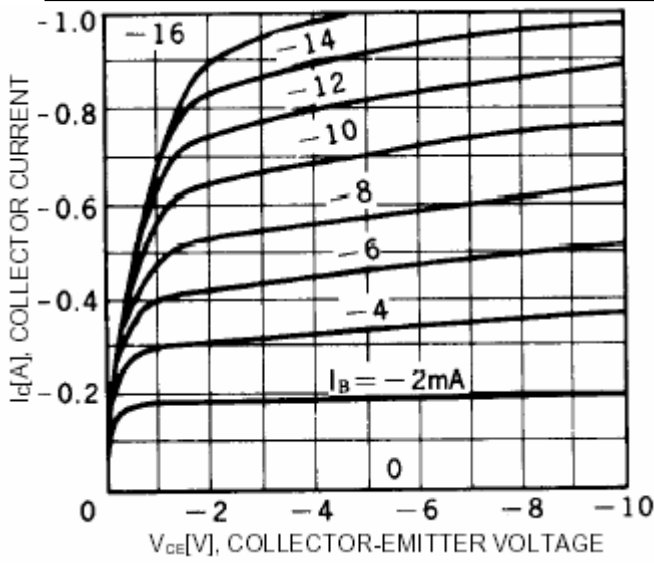


Fig.3 Static Characteristic

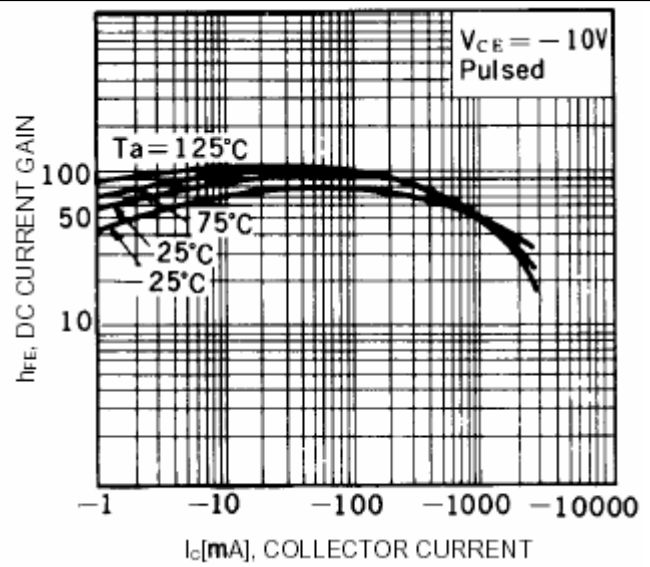


Fig.4 DC current Gain

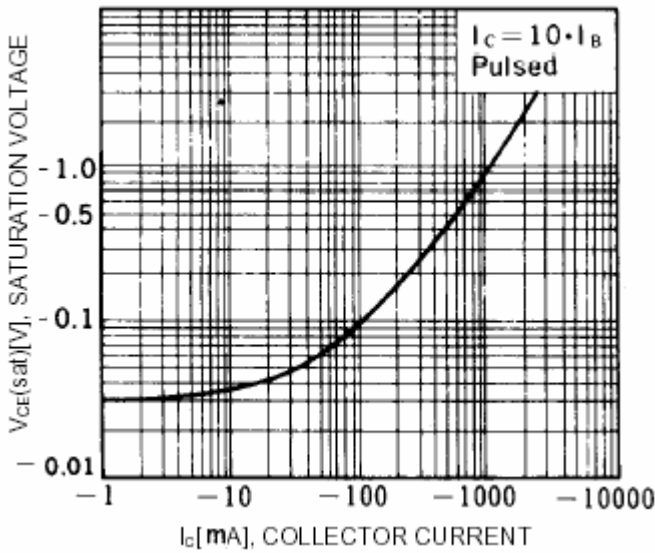


Fig.5 Collector-Emitter Saturation Voltage

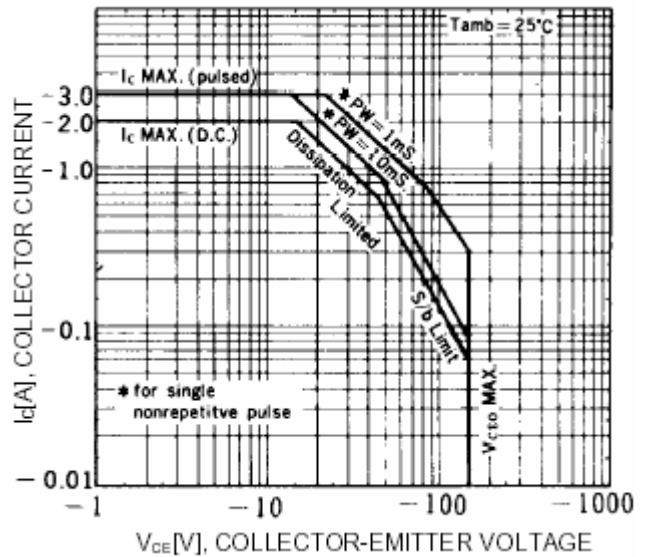


Fig.6 Safe Operating Area

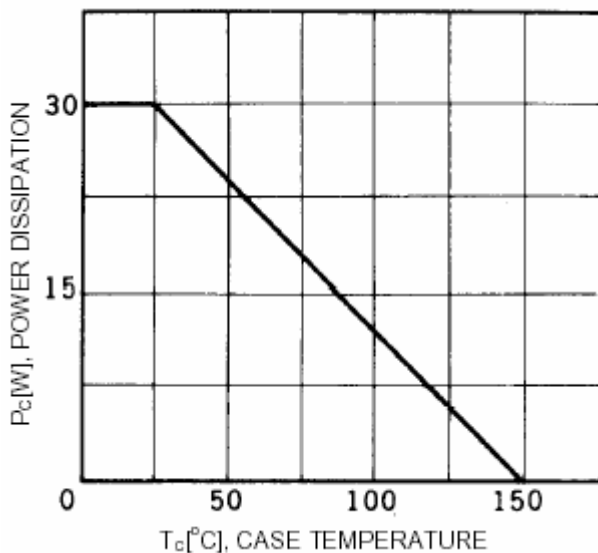


Fig.7 Power Derating