



P-Channel 100-V (D-S) 175 °C MOSFET

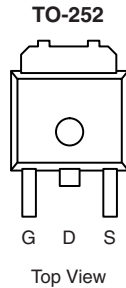
PRODUCT SUMMARY			
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ)
- 100	0.043 at V _{GS} = - 10 V	- 37	54 nC
	0.048 at V _{GS} = - 4.5 V	- 35	

FEATURES

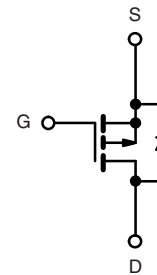
- TrenchFET[®] Power MOSFET



RoHS COMPLIANT



Drain Connected to Tab



Ordering Information: SUD50P10-43L-E3 (Lead (Pb)-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	- 100	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 175 °C) ^b	I _D	T _C = 25 °C	- 37.1 ^a	A
		T _C = 125 °C	- 31 ^a	
		T _A = 25 °C	- 9.2 ^{b, c}	
		T _A = 125 °C	- 7.7 ^{b, c}	
Pulsed Drain Current	I _{DM}	- 40		
Continuous Source Current (Diode Conduction)	I _S	T _C = 25 °C	- 50 ^a	
		T _A = 25 °C	- 6.9 ^{b, c}	
Avalanche Current	I _{AS}	- 35		
Single Pulse Avalanche Energy	E _{AS}	61	mJ	
Maximum Power Dissipation	P _D	T _C = 25 °C	136	W
		T _C = 70 °C	95	
		T _A = 25 °C	8.3 ^{b, c}	
		T _A = 70 °C	5.8 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 sec	15	18	°C/W
		Steady State	40	50	
Junction-to-Case (Drain)	R _{thJC}	0.85	1.1		

Notes:

- a. Package limited.
- b. Surface Mounted on 1" x 1" FR4 Board.
- c. t = 10 sec.
- d. Maximum under Steady State conditions is 40 °C/W.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-100			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-109		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			5.9		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1		-3	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = -10\text{ V}$	-40			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -9.2\text{ A}$		0.036	0.043	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -7.7\text{ A}$		0.040	0.048	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}, I_D = -9.2\text{ A}$		38		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -50\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		4600		pF
Output Capacitance	C_{oss}			230		
Reverse Transfer Capacitance	C_{rss}			175		
Total Gate Charge	Q_g	$V_{DS} = -50\text{ V}, V_{GS} = -10\text{ V}, I_D = -9.2\text{ A}$		106	160	nC
				54	81	
Gate-Source Charge	Q_{gs}	$V_{DS} = -50\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -9.2\text{ A}$		14		
Gate-Drain Charge	Q_{gd}			26		
Gate Resistance	R_g	$f = 1\text{ MHz}$		4		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -50\text{ V}, R_L = 6.5\text{ }\Omega$ $I_D \cong -7.7\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		15	25	ns
Rise Time	t_r			20	30	
Turn-Off Delay Time	$t_{d(off)}$			110	165	
Fall Time	t_f			100	150	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -50\text{ V}, R_L = 6.5\text{ }\Omega$ $I_D \cong -7.7\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		42	65	ns
Rise Time	t_r			160	240	
Turn-Off Delay Time	$t_{d(off)}$			100	150	
Fall Time	t_f			100	150	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			-50	A
Pulse Diode Forward Current ^a	I_{SM}				-40	
Body Diode Voltage	V_{SD}	$I_S = -7.7\text{ A}$		-0.8	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -7.7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		60	90	ns
Body Diode Reverse Recovery Charge	Q_{rr}			150	225	nC
Reverse Recovery Fall Time	t_a			46		ns
Reverse Recovery Rise Time	t_b			14		

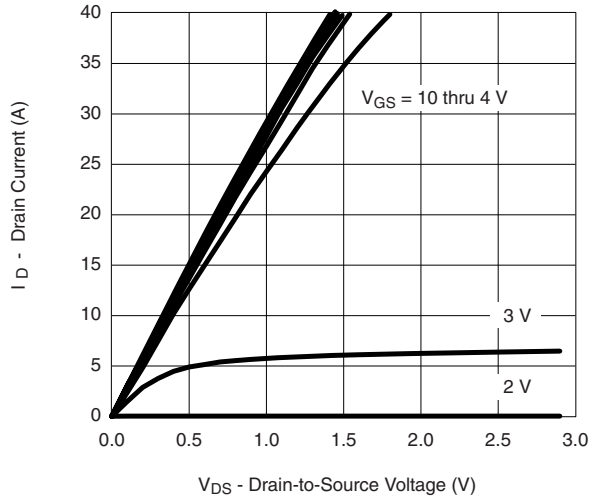
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

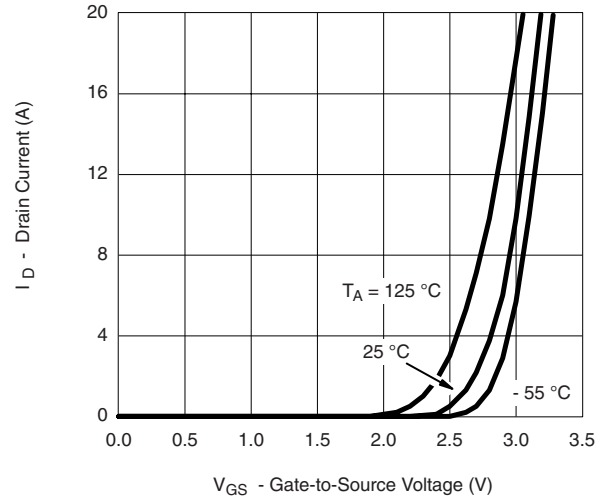
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



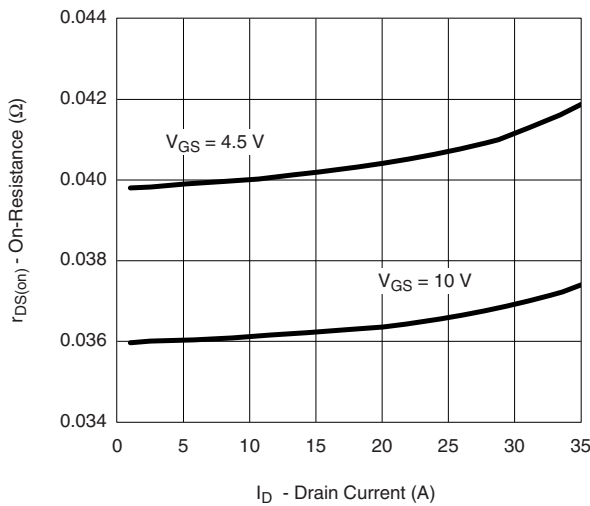
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



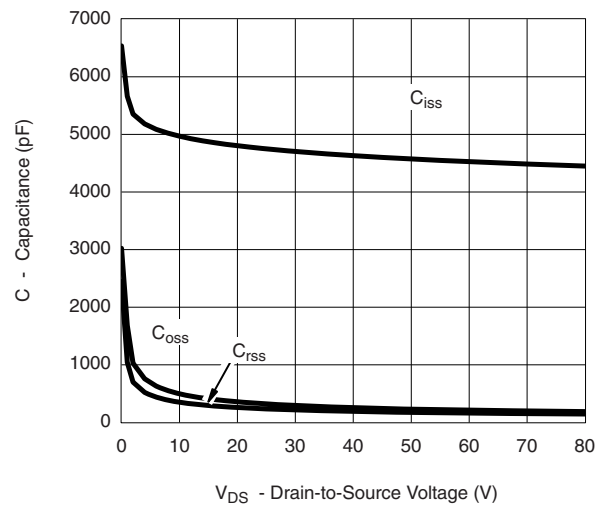
Output Characteristics



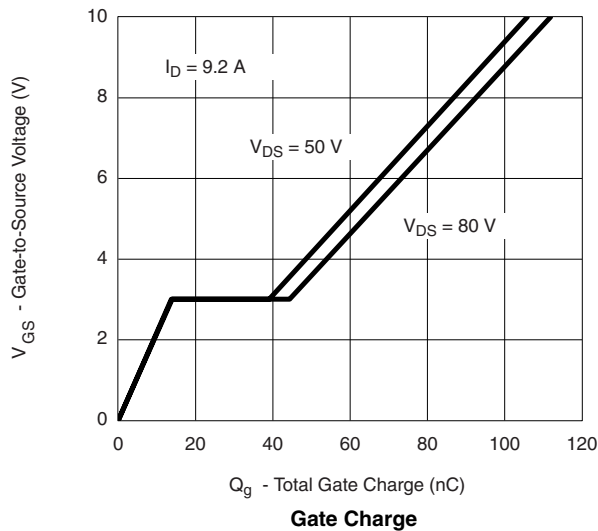
Transfer Characteristics



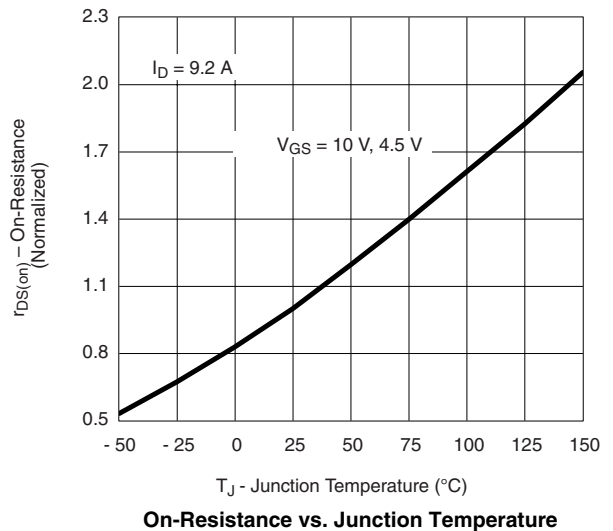
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge



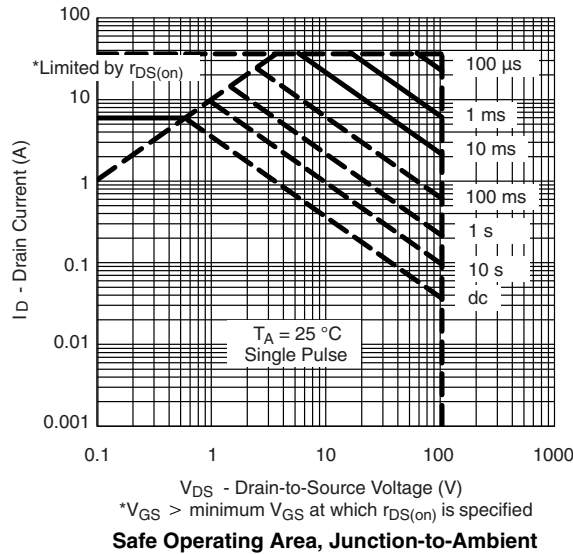
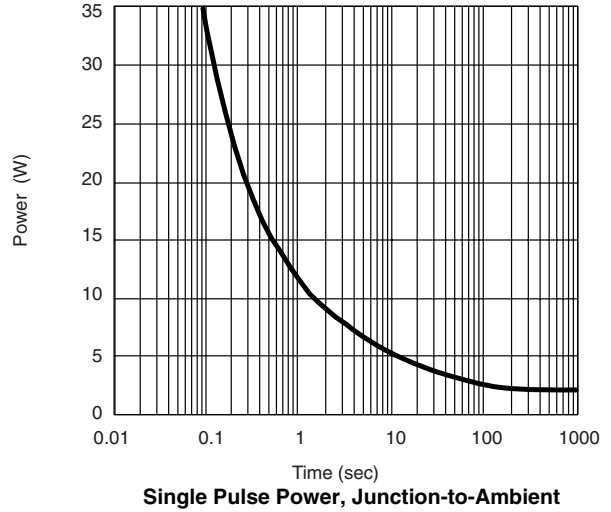
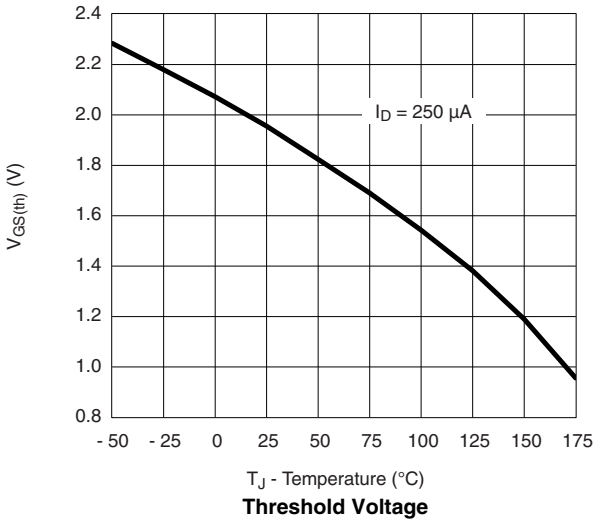
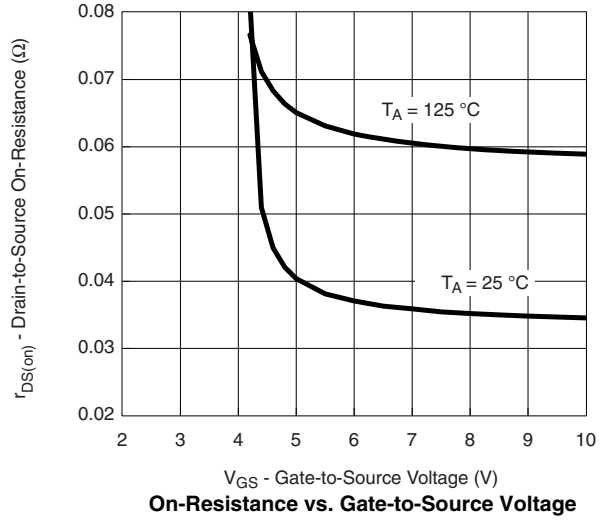
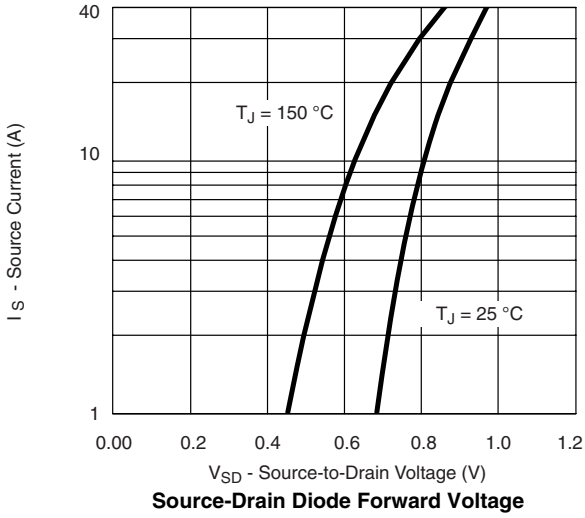
On-Resistance vs. Junction Temperature

SUD50P10-43L



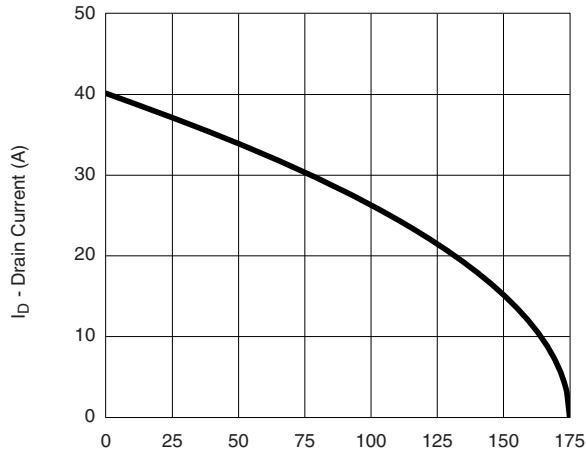
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

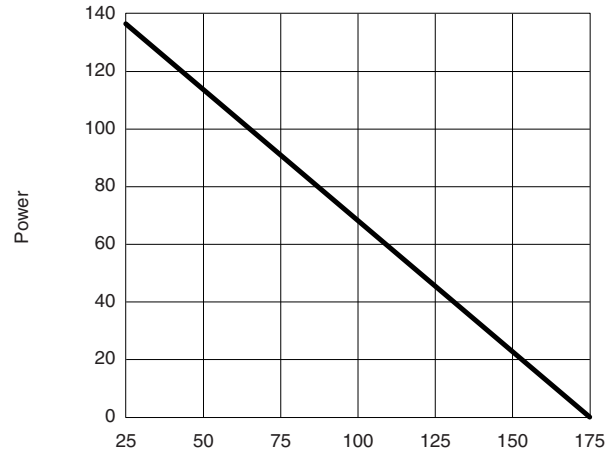




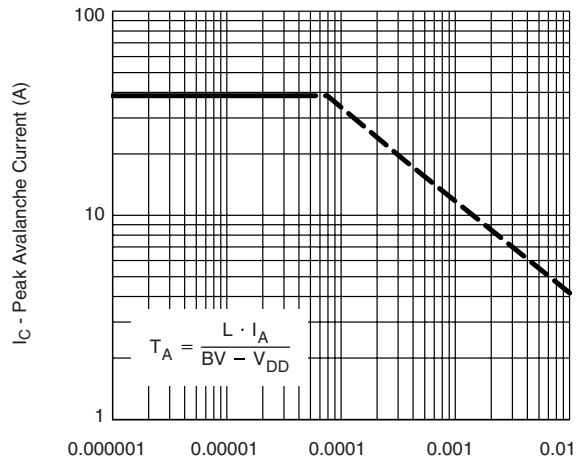
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



T_C - Case Temperature (°C)
Current Derating*



T_C - Case Temperature (°C)
Single Pulse Power, Junction-to-Ambient



T_A - Time In Avalanche (sec)
Single Pulse Avalanche Capability

$$T_A = \frac{L \cdot I_A}{BV - V_{DD}}$$

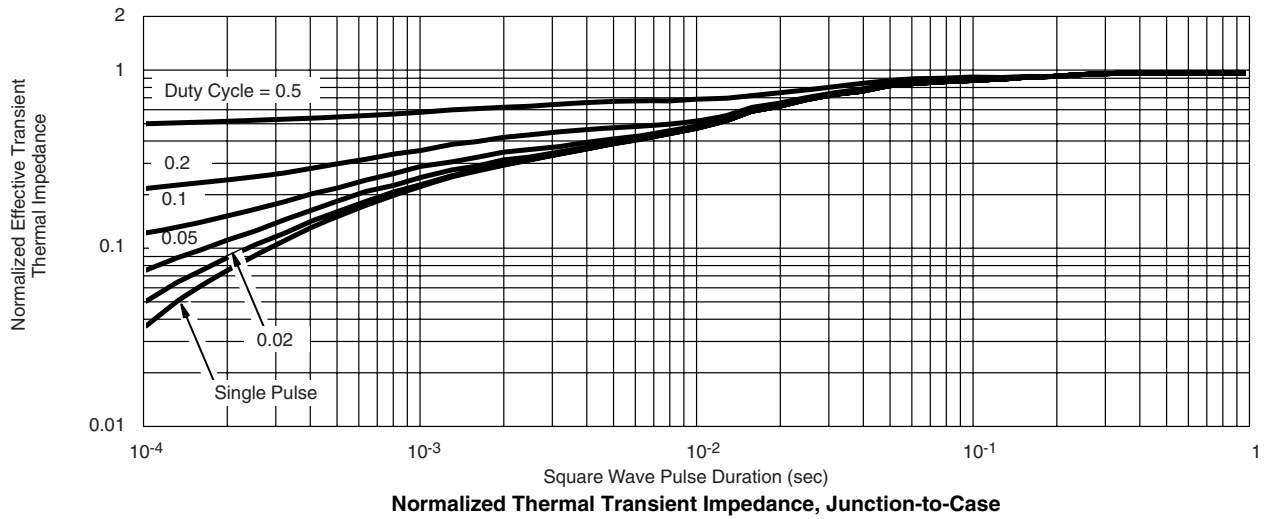
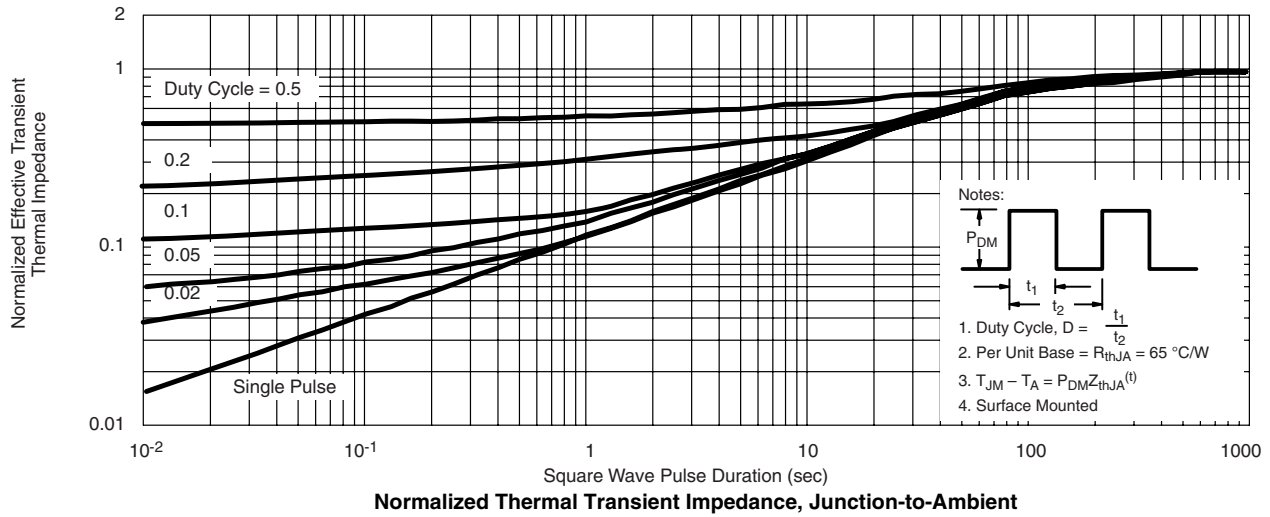
*The power dissipation P_D is based on T_{J(max)} = 175 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

SUD50P10-43L



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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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