MXO45LV / MXO45HSLV

METAL DIP CLOCK OSCILLATOR

FEATURES

- Standard 14 Pin or 8 Pin DIP Footprint
- HCMOS/TTL Compatible
- Fundamental and 3rd Overtone Crystals
- Frequency Range 1.0 – 50 MHz
- Frequency Stability, ±50 ppm Standard (±25 ppm and ±20 ppm available)
- +3.3Vdc Operation
- Operating Temperature to –40°C to +85°C
- Output Enable Option
- **RoHS/Green Compliant**

DESCRIPTION

The MXO45LV/MXO45HSLV is a DIP packaged Clock oscillator offering reliable performance at an economical cost. The enhanced stability means it is the perfect choice for today's communications applications that require tight frequency control.

ORDERING INFORMATION

MXO □ - □ □ - M

SUPPLY VOLTAGE

45LV = 14 Pin DIP/STD Output
45TLV = 14 Pin DIP/Tristate Output
45HSLV = 8 Pin DIP/STD Output
45HSTLV = 8 Pin DIP/Tristate Output

FREQUENCY STABILITY

6 = ± 20 ppm (-20°C to +70°C only)
5 = ± 25 ppm
3 = ± 50 ppm (standard)
2 = ± 100 ppm

FREQUENCY IN MHz

M - indicates MHz and decimal point. Frequency is recorded with minimum 4 significant digits to the right of the "M".

OPERATING TEMPERATURE RANGE

C = -20°C to +70°C (standard)
I = -40°C to +85°C

Example Part Number: MXO45LV-3C-32M7680 or MXO45HSLV-3C-32M7680

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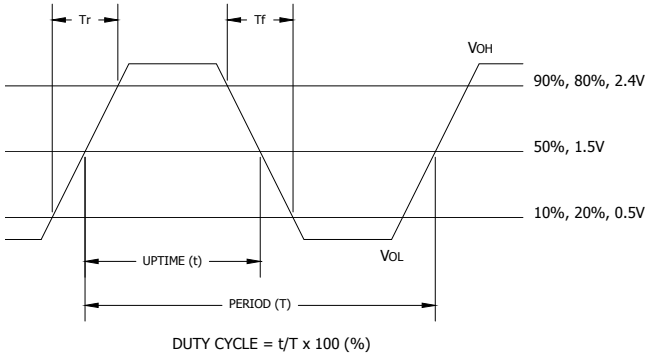
ELECTRICAL CHARACTERISTICS

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Absolute Maximums	Maximum Supply Voltage	V_{CC}	-	-0.5	-	7.0	V
	Storage Temperature	T_{STG}	-	-55	-	125	°C
	Frequency Range	f_O	-	1.5	-	50	MHz
	Frequency Stability (See Note 1 and Ordering Information)	$\Delta f/f_O$	-	-	-	20,25,50 or 100	± ppm
	Operating Temperature Commercial Industrial	T_A	-	 -20 -40	25	 70 85	°C
Electrical and Waveform Parameters	Supply Voltage	V_{CC}	± 10 %	3.0	3.3	3.6	V
	Supply Current	I_{CC}	1.5 MHz to 20 MHz C_L=50pF 20.1 MHz to 50 MHz C_L=50pF	- -	7 20	12 40	mA
	Output Load CMOS TTL	 C_L	 1.5 MHz to 50 MHz 1.5 MHz to 50 MHz	 - -	 - -	 50 10	 pF TTL
	Output Voltage Levels Logic '1' Level Logic '0' Level	 V_{OH} V_{OL}	 CMOS Load 10 TTL LOAD CMOS TTL Load	 0.9*V_{CC} V_{CC}-0.6V - -	 - - -	 - 0.1*V_{CC} 0.4	V
	Output Current Logic '1' Level Logic '0' Level	 I_{OH} I_{OL}	 V_{OH} = 2.2V V_{CC} = 3.0V V_{OL} = 0.4V V_{CC} = 3.0V	 - -	 - -	 -8 8	mA
	Output Duty Cycle	SYM	@ 50% Level	45	-	55	%
	Rise and Fall Time	T_R, T_F	@ 10% - 90% Levels 1.5 MHz to 25 MHz C_L=50pF 25.1 MHz to 50 MHz C_L=50pF	 - -	 6 3	 8 4	ns
	Start Up Time	T_S	Application of V_{CC}	-	-	10	ms
	Enable Function (See Note 2) Enable Input Voltage Disable Input Voltage	 V_{IH} V_{IL}	 Pin 1 Logic '1', Output Enabled Pin 1 Logic '0', Output Disabled	 2.0 -	 - -	 - 0.8	V
	Enable Time	T_{PLZ}	Pin 1 Logic '1'	-	-	10	ms
	Phase Jitter	tjms	Bandwidth 12 kHz - 20 MHz	-	-	1	ps RMS

Notes:

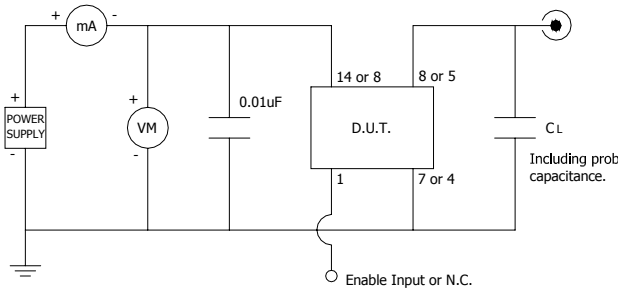
1. Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and first year aging at an average operating temperature of +40 °C.
2. Reference CTS Application Note 014-0002-0.

CMOS/TTL OUTPUT WAVEFORM



DUTY CYCLE = t/T x 100 (%)

TEST CIRCUIT, CMOS LOAD



ENABLE TRUTH TABLE

PIN 1	PIN 5 or PIN 8
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

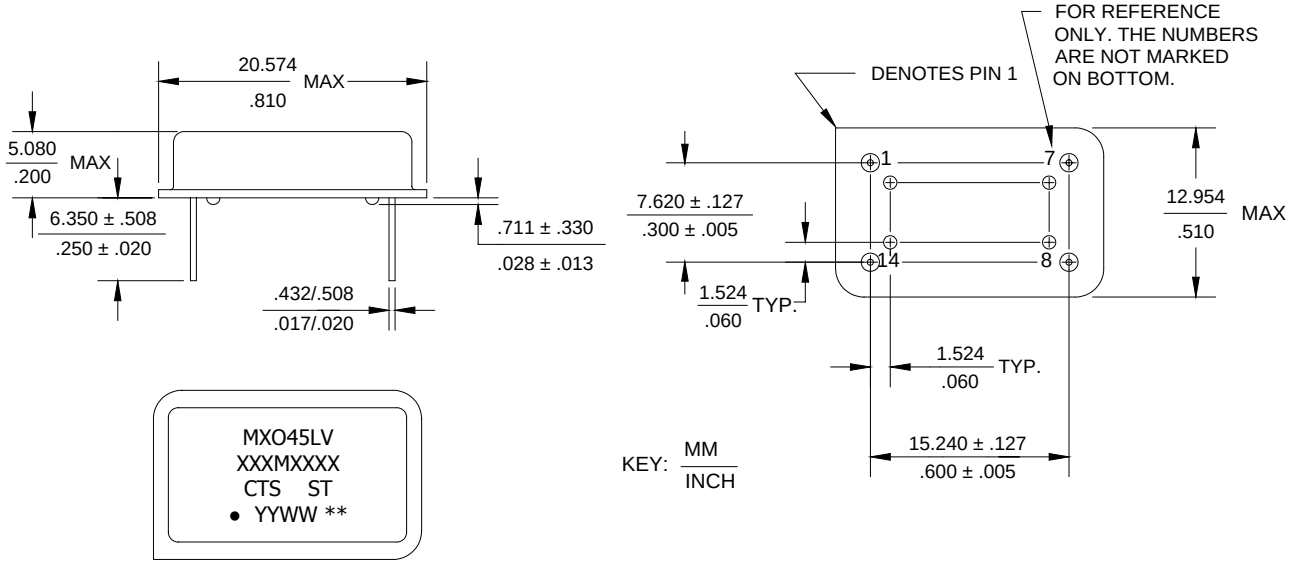
D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
1	EOH	Enable Input
7 or 4	GND	Circuit & Package Ground
8 or 5	Output	RF Output
14 or 8	V_{CC}	Supply Voltage

MECHANICAL SPECIFICATIONS

PACKAGE DRAWING

DIP-14



MARKING INFORMATION

1. XXXMXXXX - Frequency marked with 4 significant digits after the 'M'.
2. ST – Frequency stability/temperature code. (Reference Ordering Information.)
3. YYWW – Date code, YY – year, WW – week.
4. ** - Manufacturing Site Code.

NOTES

1. Lead finish (e1), SnAgCu.
2. Reflow conditions per JEDEC J-STD-020.

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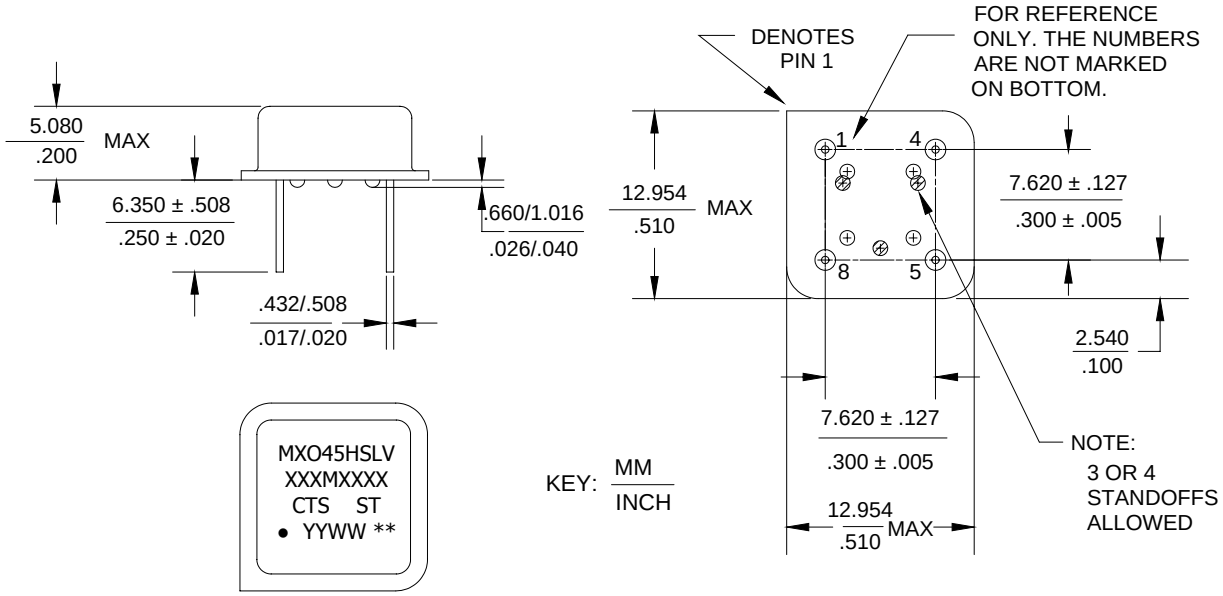
PACKAGE DRAWING

DIP-8



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ENVIRONMENTAL SPECIFICATIONS

Temperature Cycle:	400 cycles from –55°C to +125°C, 10 minute dwell at each temperature, 1 minute transfer time between temperatures.
Mechanical Shock:	1,500g's, 0.5mS duration, ½ sinewave, 3 shocks each direction along 3 mutually perpendicular planes (18 total shocks).
Sinusoidal Vibration:	0.06 inches double amplitude, 10 to 55 Hz and 20g's, 55 to 2,000 Hz, 3 cycles each in 3 mutually perpendicular planes (9 times total).
Gross Leak:	No leak shall appear while immersed in an FC40 or equivalent liquid at +125°C for 20 seconds.
Fine Leak:	Mass spectrometer leak rates less than $2x10^{-8}$ ATM cc/sec air equivalent.
Resistance to Solder Heat:	Product must survive 3 reflows of +260°C peak, 10 seconds maximum.
High Temperature Operating Bias:	2,000 hours at +125°C, maximum bias, disregarding frequency shift.
Frequency Aging:	1,000 hours at +85°C, full bias, less than ±5 ppm shift.
Moisture Sensitivity Level:	Level 1 per JEDEC J-STD-020.

QUALITY AND RELIABILITY

Quality systems meet or exceed the requirements of ISO 9000:2000 standards.

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