Data Sheet | February 13, 2009 | FN6687.0

Dual Input Li-ion/Li-Polymer Battery Charger With Battery Removal Detection

The ISL9228 is a fully integrated low-cost single-cell Li-ion or Li-polymer battery charger. The charger accepts two power inputs, normally one from a USB (Universal Serial Bus) port and the other from a desktop cradle. The ISL9228 is an ideal charger for smart handheld devices that need to communicate with a personal computer via USB.

The ISL9228 features 28V maximum voltages for both the cradle and the USB inputs. Due to the 28V rated inputs, low-cost, large output tolerance adapters can be used safely. The 28V rating eliminates the over voltage protection circuit required in a low input voltage charger.

When both inputs are powered, the cradle input is used to charge the battery. The charge current is programmable for the cradle input with a small resistor. The end-of-charge current is also programmable by another external resistor. The charger incorporates Thermaguard™ which protects the IC against over temperature. If the die temperature rises above a typical value of +125°C, a thermal foldback function reduces the charge current automatically to prevent further temperature rise. The charger has two indication pins. The $\overline{PPR}$ (power present) pin outputs an open-drain logic LOW when either the cradle or the USB input power is attached. The $\overline{CHG}$ (charge) pin is also an open-drain output that indicates a logic LOW when the charge current is above a minimum current level. When the charge current is below the preset minimum current, the $\overline{CHG}$ pin will turn to logic high to indicate the end-of-charge condition.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL9228IRZ	9228	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9228IRZ-T	9228	-40 to +85	10 Ld 3x3 DFN Tape and Reel	L10.3x3C

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- Complete Charger for Single-Cell Li-ion/Polymer Batteries
- **Dual Input Power Sources for Cradle and USB**
- **Battery Removal Detection**
- Integrated Pass Elements
- Fixed 380mA USB Charge Current
- Programmable Cradle Charge Current
- **Charge Current Thermaguard™ for Thermal Protection**
- **28V Maximum Voltages for Cradle and USB Inputs**
- 1% Constant Voltage Accuracy
- Adapter Presence and Charge Indications
- Less than 0.5µA Leakage Current off the Battery when No Input Power Attached
- Programmable End-of-Charge Current
- Ambient Temperature Range: -40°C to +85°C
- No External Blocking Diode Required
- Pb-Free (RoHS Compliant)

Applications

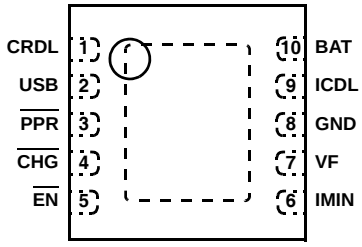
- Smart Handheld Devices
- Cell Phones, PDAs, MP3 Players
- Digital Still Cameras
- Handheld Test Equipment

Related Literature

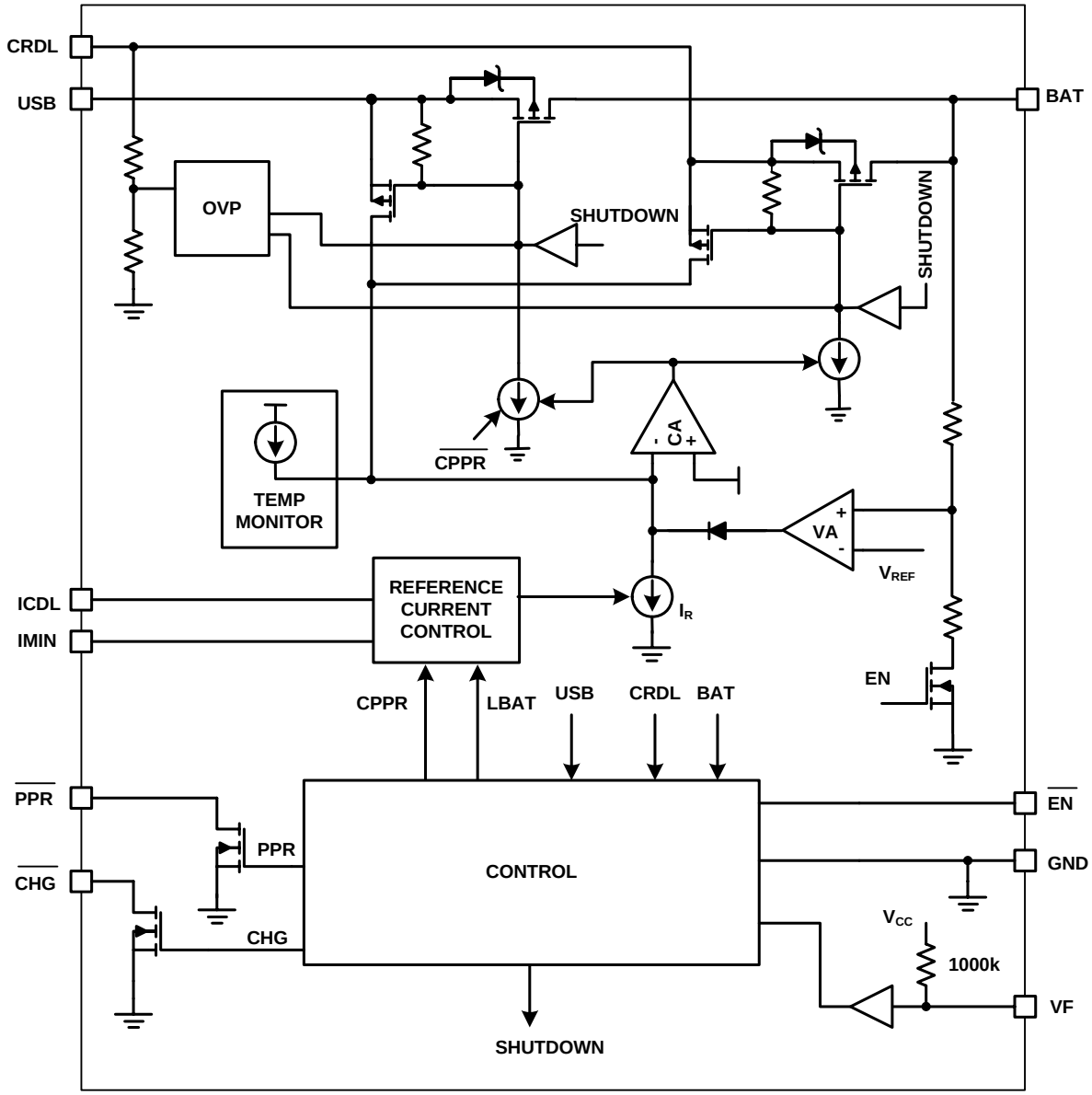
- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Technical Brief TB389 “PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages”

Pinout

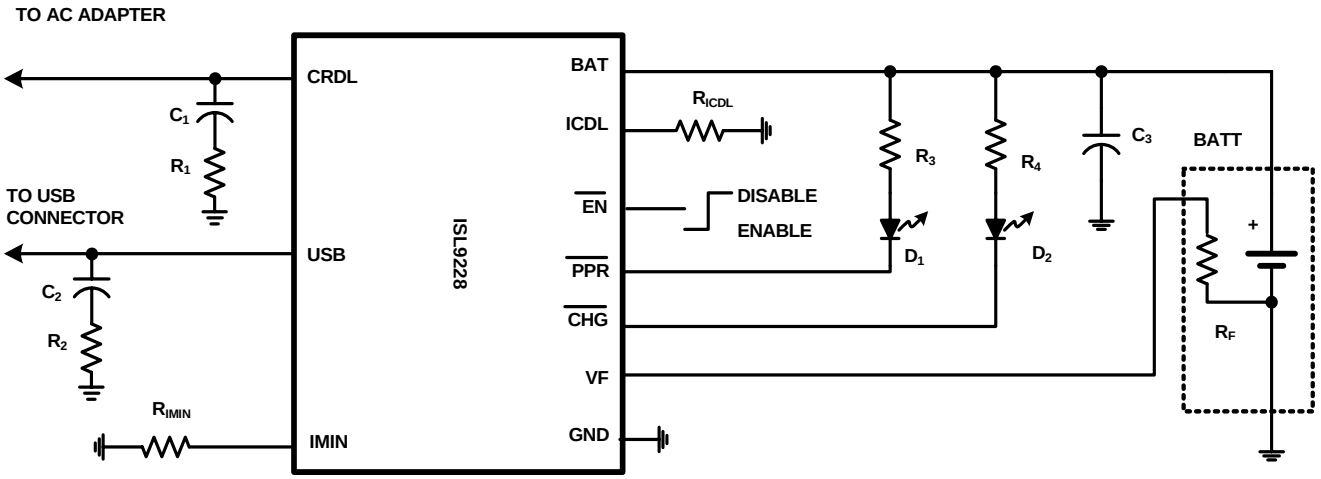
ISL9228
(10 LD DFN)
TOP VIEW



Block Diagram



Typical Applications



COMPONENT SELECTION

R_{ICDL}	12.4kΩ for 0.55A cradle charge current
R_{IMIN}	10kΩ for 55mA end-of-charge current
R_3, R_4	350Ω
R_F	ID Resistor, typically 20kΩ
C_1, C_2, C_3	1µF ceramic capacitor
R_1, R_2	1Ω
D_1, D_2	LEDs

Absolute Maximum Ratings

Supply Voltage (CRDL, USB) . . . . . -0.3V to 28V
Other Input Voltage ($\overline{EN}$, VF, ICDL, IMIN, BAT) . . . . . -0.3V to 7V
Open-Drain Pull-Up Voltage ($\overline{PPR}$, $\overline{CHG}$) . . . . . -0.3V to 7V

Recommended Operating Conditions

Ambient Temperature Range . . . . . -40°C to +85°C
Supply Voltage
USB Pin . . . . . 4.3V to 5.5V
CRDL Pin . . . . . 4.3V to 24V
Typical Cradle Charge Current . . . . . 100mA to 1A
Typical USB Charge Current 380mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
DFN Package (Notes 1, 2)	40	2.5

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For theta θ_{JC} the "case temp." location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Typical Values Are Tested at USB = CRDL = 5V and ambient temperature is at +25°C, Unless Otherwise Noted. All Maximum and Minimum Values Are Guaranteed Under the Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER-ON RESET						
Rising USB/CRDL Threshold			3.4	3.9	4.2	V
Falling USB/CRDL Threshold			2.7	3.2	3.5	V
VIN-BAT OFFSET VOLTAGE						
Rising Edge	V_{OS}	V_{BAT} = 4.0V, use $\overline{CHG}$ pin with output current to indicate the comparator output (Note 3)	-	150	250	mV
Falling Edge	V_{OS}		20	80	-	mV
STANDBY CURRENT						
BAT Pin Sink Current	$I_{STANDBY}$	$\overline{EN}$ = HIGH or both inputs are floating	-	0.05	0.5	µA
CRDL Pin Supply Current	I_{CRDL}	$\overline{EN}$ = HIGH	-	150	220	µA
USB Pin Supply Current	I_{USB}		-	150	220	µA
CRDL/USB Pin Supply Current		$\overline{EN}$ = LOW or floating	-	0.55	0.8	mA
VOLTAGE REGULATION						
Output Voltage	V_{CH}	Load = 10mA	4.158	4.2	4.242	V
Output Voltage	V_{CH}	Load = 10mA (T_J = +25°C)	4.174	4.2	4.226	V
CRDL PMOS On-Resistance		V_{BAT} = 3.8V, $I_{CHARGER}$ = 0.3A, (T_J = +25°C)	200	600	850	mΩ
USB PMOS On-Resistance		V_{BAT} = 3.8V, $I_{CHARGER}$ = 0.3A, (T_J = +25°C)	200	600	850	mΩ
CHARGE CURRENT (Note 4)						
ICDL Pin Output Voltage	V_{ICDL}	V_{BAT} = 3.8V	1.19	1.22	1.25	V
CRDL Input Constant Charge Current	I_{CHARGE}	R_{ICDL} = 12.4kΩ, V_{BAT}: 2.7V to 3.8V	520	550	580	mA
CRDL Input Trickle Charge Current	$I_{TRICKLE}$	R_{ICDL} = 12.4kΩ, V_{BAT} = 2.2V Given as a % of the CRDL I_{CHARGE}	16	18	20	%
CRDL and USB End-of-Charge Threshold	I_{MIN}	R_{IMIN} = 10.0kΩ	46.5	55	63.5	mA
USB Input Constant Charge Current	I_{CHARGE}	V_{BAT}: 2.7V to 3.8V	332	380	410	mA
USB Input Trickle Charge Current	$I_{TRICKLE}$	V_{BAT} = 2.2V	66	80	91	mA

Electrical Specifications

Typical Values Are Tested at USB = CRDL = 5V and ambient temperature is at +25°C, Unless Otherwise Noted. All Maximum and Minimum Values Are Guaranteed Under the Recommended Operating Conditions **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PRECONDITIONING CHARGE THRESHOLD						
Preconditioning Charge Threshold Voltage	V_{MIN}		2.5	2.6	2.7	V
RECHARGE THRESHOLD						
Recharge Threshold Voltage	V_{RCH}		3.8	3.9	4.0	V
BATTERY REMOVAL DETECTION						
Maximum External Resistor	R_{ID}	V_{IL} = 0.4V	100	-	-	kΩ
VF Pin Internal Pull Up Resistance			700	1000	1300	kΩ
INTERNAL TEMPERATURE MONITORING						
Current Foldback Threshold	T_{FOLD}		-	125	-	°C
LOGIC INPUT AND OUTPUT						
$\overline{EN}$ and VF Pins Logic Input High	V_{IH}		1.3	-	-	V
$\overline{EN}$ and VF Pins Logic Input Low	V_{IL}		-	-	0.4	V
$\overline{EN}$ Pin Internal Pull Down Resistance			350	600	850	kΩ
$\overline{CHG}$/$\overline{PPR}$ Sink Current		Pin Voltage = 0.8V	10	-	-	mA

NOTES:

3. The 4.0V V_{BAT} is selected so that the $\overline{CHG}$ output can be used as the indication for the offset comparator output indication. If the V_{BAT} is lower than the POR threshold, no output pin can be used for indication.
4. The charge current can be affected by the thermal foldback function if the IC under the test setup cannot dissipate the heat.

Typical Operating Performance

The test conditions for the Typical Operating Performance are: V_{IN} = 5V, T_A = +25°C, R_{ICDL} = 12.4kΩ, R_{IMIN} = 10.0kΩ, V_{BAT} = 3.7V unless Otherwise Noted.

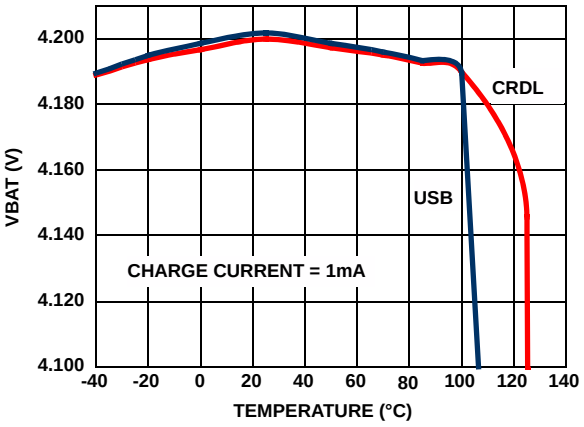


FIGURE 1. CHARGER OUTPUT VOLTAGE vs TEMPERATURE

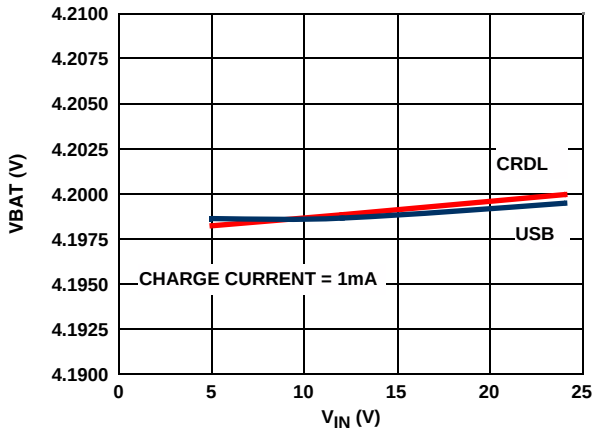


FIGURE 2. CHARGER OUTPUT VOLTAGE vs INPUT VOLTAGE

Typical Operating Performance

The test conditions for the Typical Operating Performance are: V_{IN} = 5V, T_A = +25°C, R_{ICDL} = 12.4kΩ, R_{IMIN} = 10.0kΩ, V_{BAT} = 3.7V unless Otherwise Noted. **(Continued)**

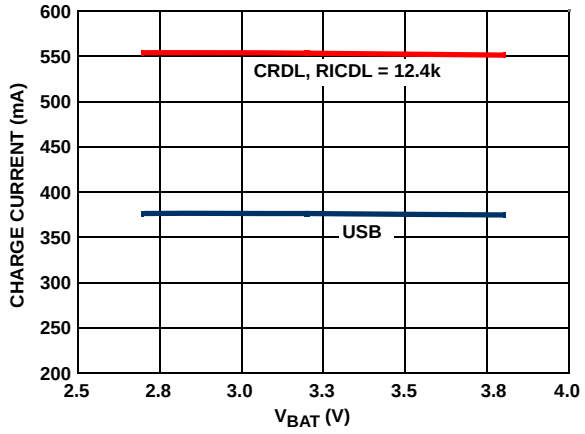


FIGURE 3. CHARGE CURRENT vs OUTPUT VOLTAGE

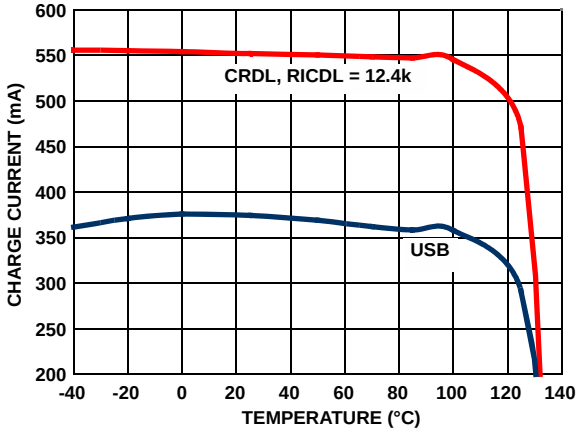


FIGURE 4. CHARGE CURRENT vs AMBIENT TEMPERATURE

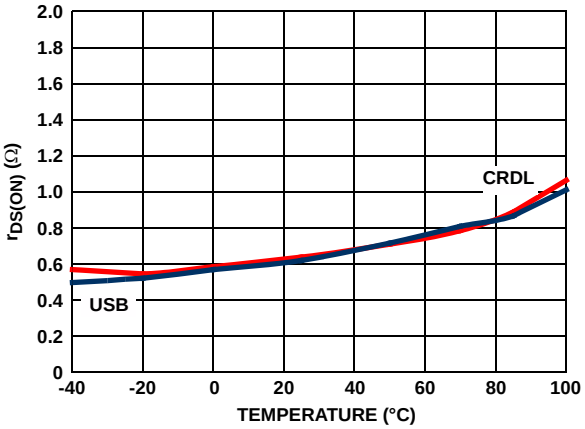


FIGURE 5. $r_{DS(ON)}$ vs TEMPERATURE AT 3.7V OUTPUT

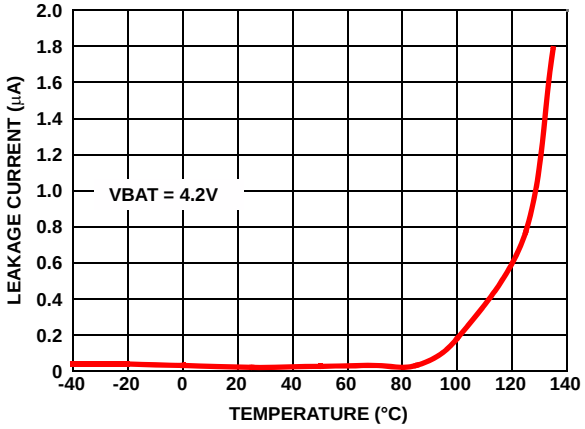


FIGURE 6. REVERSE CURRENT vs TEMPERATURE

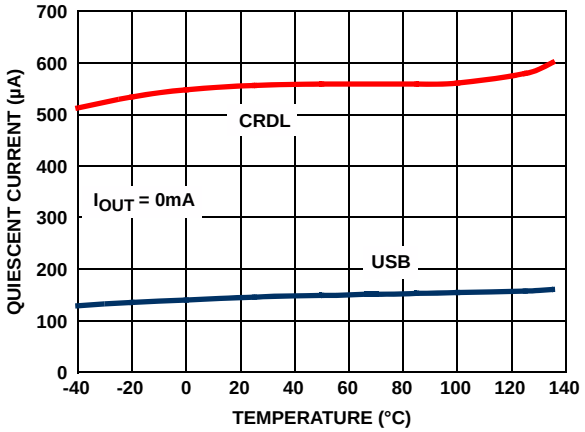


FIGURE 7. CRADLE INPUT QUIESCENT CURRENT vs TEMPERATURE

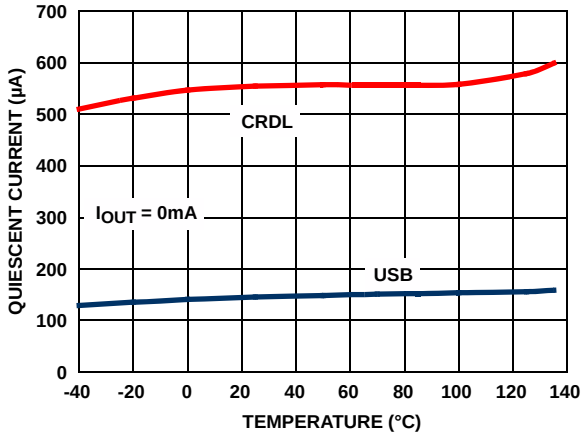


FIGURE 8. USB INPUT QUIESCENT CURRENT vs TEMPERATURE

Typical Operating Performance

The test conditions for the Typical Operating Performance are: V_{IN} = 5V, T_A = +25°C, R_{ICDL} = 12.4kΩ, R_{IMIN} = 10.0kΩ, V_{BAT} = 3.7V unless Otherwise Noted. **(Continued)**

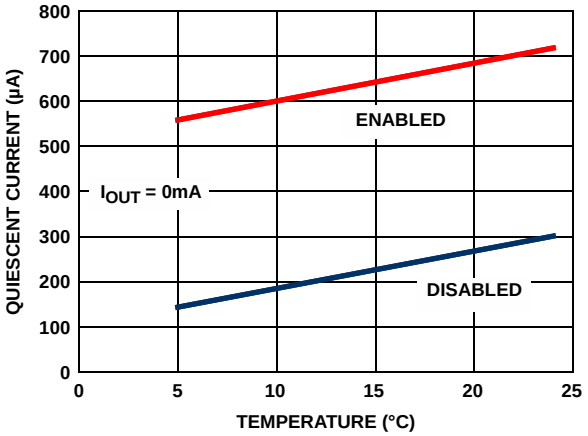


FIGURE 9. CRADLE INPUT QUIESCENT CURRENT vs INPUT VOLTAGE

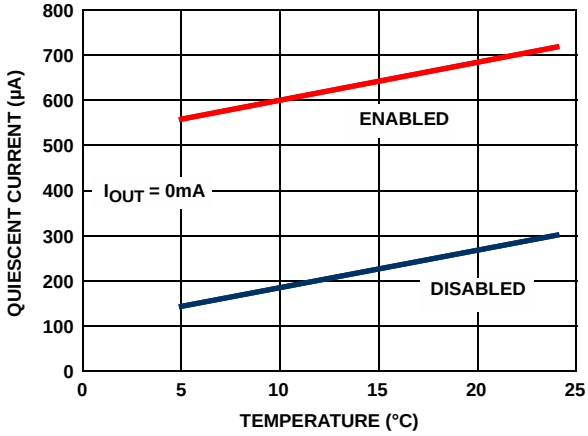


FIGURE 10. USB INPUT QUIESCENT CURRENT vs INPUT VOLTAGE

Functional Pin Description

CRDL (Pin 1)

Cradle input. This pin is usually connected to a cradle power input. The maximum input voltage is 28V. The charge current from this pin is programmable with the ICDL pin up to 1A. When this pin is connected to a power source, no charge current is drawn from the USB pin. A 1µF or larger value ceramic capacitor is recommended for decoupling.

USB (Pin 2)

USB input. This pin is usually connected to a USB port power connector. Other sources that are also acceptable. The charge current from the USB pin is fixed at typically 380mA. A 1µF or larger value ceramic capacitor is recommended for decoupling. It is also recommended to have a 1Ω resistor in series with the decoupling capacitor to prevent an over-shoot voltage when a USB cable is plugged in.

$\overline{PPR}$ (Pin 3)

Power presence indication. An open-drain output pin which turns ON when either the USB input voltage or the CRDL input voltage is within the power good range (refer to the Description section for definition of power good condition), regardless if the charger is enabled or disabled. Otherwise turns OFF. This pin provides a wake-up signal to a microprocessor when either the cradle or the USB power is connected.

$\overline{CHG}$ (Pin 4)

Charge indication pin. An open-drain output which turns ON when the charge current is above programmable threshold. Otherwise turns OFF.

$\overline{EN}$ (Pin 5)

Enable logic input. Connect to LOW or leave floating to enable the charger.

IMIN (Pin 6)

IMIN is the programmable input for the end-of-charge current. IMIN is calculated by Equation 1:

$$I_{MIN} = \frac{550}{R_{IMIN}} \quad (mA) \qquad \text{(EQ. 1)}$$

Where R_{IMIN} is in kΩ. IMIN is applicable for both cradle and USB charging.

VF (Pin 7)

VF is an input pin for the battery ID resistor connection. This pin has an internal 1000kΩ pull-up resistor. Thus a typical 20kΩ ID resistor will pull this pin to logic low state, indicating a valid battery connection. If the battery is removed, the VF pin will be pulled to a logic high state by the internal resistor, the charger will be disabled as a result, regardless of the status of the $\overline{EN}$ pin. The maximum ID resistor is 100kΩ.

GND (Pin 8)

System ground.

ICDL (Pin 9)

The ICDL pin has two functions. The first function is to program the cradle charge current during the constant-current mode. The voltage of this pin is 1.22V during the constant-current mode of the cradle charger. The constant-current mode current is programmed by Equation 2:

$$I_{CDL} = \frac{6820}{R_{ICDL}} \quad (mA) \qquad \text{(EQ. 2)}$$

where R_{ICDL} is the resistor in kΩ, connected to the ICDL pin (see the Typical Application).

It is recommended that the charge current be programmed in the range of 100mA to 1000mA.

The second function of the ICDL pin is to monitor the actual charge current. The voltage of this pin, V_{ICDL}, is proportional to the actual charge current, I_{CHG}.

The cradle charge current should be programmed equal or higher than the USB current; otherwise, the ICDL pin voltage will be higher than 1.22V during the constant current mode when the USB charger is working. The charger still works properly but the accuracy of the current monitoring voltage degrades and saturates at approximately 2.1V.

BAT (Pin 10)

Charger output pin. Connect this pin to the battery pack or the battery cell. A 1µF or larger value ceramic capacitor is recommended for decoupling. The charger relies on the battery for stability so a battery should always be connected to the BAT pin.

Description

The ISL9228 is designed for a single-cell Li-ion or Li-polymer battery charging circuit that accepts both a USB port and a desktop cradle as its power source. While the charge current from the USB input source is fixed at 380mA, the charge current from the cradle input is programmable between 0.1A and 1.0A by the resistor R_{ICDL}. Similarly, the end-of-charge current is programmable by connecting a resistor at the IMIN pin. The end-of-charge threshold can be calculated with Equation 1 in “Functional Pin Description” on page 7. The same threshold applies to both the cradle and the USB inputs.

Input Auto Selection

When both input sources are present, the charger selects only one power source to charge the battery. When the CRDL input is higher than the POR threshold, CRDL is selected as the power source. Otherwise the USB input is selected. If the CRDL input voltage is below the battery voltage but the USB input voltage is higher than the battery voltage, then the USB input is used to charge the battery. The control circuit always breaks both internal power devices before switching from one power source to the other to avoid a cross conduction of both power MOSFETs.

USB Charge Current

When the USB port is selected as the power source, the charge current enabled by the logic input at the $\overline{EN}$ pin. When the $\overline{EN}$ is driven to logic LOW, the charger is enabled.

Typically the P-channel MOSFET for the USB input has an $r_{DS(ON)}$ of 600mΩ at room temperature. With a 380mA charge current, the typical head room is 228mV. Thus, if the input voltage drops to a level that the voltage difference between the USB pin and the BAT pin is less than 228mV, the $r_{DS(ON)}$ becomes a limiting factor of the charge current; and the charger drops out the constant current regulation.

Cradle Charge Current

The cradle charge current is programmed with the external resistor connected between the ICDL pin and the GND pin. The current can be calculated with Equation 2 in “ICDL (Pin 9)” on page 7. The typical $r_{DS(ON)}$ of the P-channel MOSFET for the CRDL input is 600mΩ at room temperature. When the head room between the input and output voltages is small, the actual charge current, similar to the USB case, could be limited by the $r_{DS(ON)}$. On the other hand, if the head room between the input and output voltages is large, the charge current may be limited by the thermal foldback threshold.

Floating Charge Voltage

The floating voltage during the constant voltage phase is 4.2V. The floating voltage has an 1% accuracy over the ambient temperature range of -40°C to +85°C.

Trickle Charge Current

When the battery voltage is below the minimum battery voltage V_{MIN} given in the electrical specification, the charger operates in a trickle/preconditioning mode, where the charge current is typically 18% of the programmed charge current for the cradle input. If power comes from the USB input, the trickle current is approximately 80mA.

End-Of-Charge Indication

When an EOC condition (charge current falls below I_{MIN} during constant voltage charge) is encountered, the CHG pin internal open-drain MOSFET turns off. The I_{MIN} threshold is programmable by the resistor at the IMIN pin for both cradle and USB inputs. Once the EOC condition is reached, the status is latched and can be reset at one of the following conditions:

1. The part is disabled and re-enabled
2. The selected input source has been removed and re-applied
3. The BAT pin voltage falls below the recharge threshold (~3.9V)

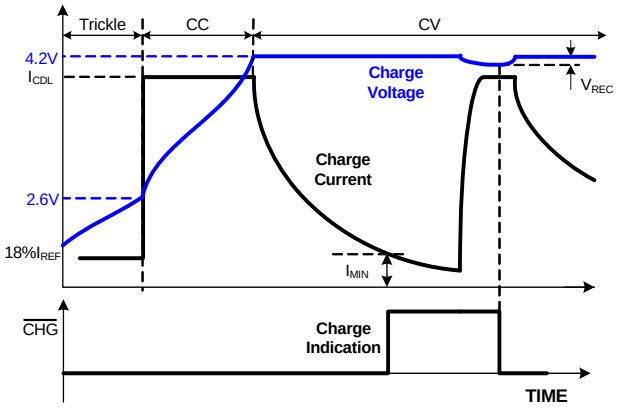


FIGURE 11. TYPICAL CHARGE CYCLE

Figure 11 shows the typical charge profile including the end-of-charge event.

Power Presence Indication

When either the USB or the cradle input voltage is above the POR threshold, the PPR pin internal open-drain MOSFET turns on indicating the presence of input power.

Power-Good Conditions

Even if there is a power present, the charger will not deliver any current to the output if the power-good conditions are not met. The following two conditions together define the power-good voltage range:

1. VCDRL or VUSB > VPOR
2. VCDRL or VUSB - VBAT > VOS

where VPOR is the power on reset threshold, VOS is the offset voltage for the input and output voltage comparator. All these thresholds have hysteresis, as given in the “Electrical Specification” table on page 4. The charger will not charge the battery if the input voltage does not meet the power-good conditions.

Thermal Foldback (Thermaguard™)

The thermal foldback function reduces the charge current when the internal temperature reaches the thermal foldback threshold, which is typically +125°C. This protects the charger from excessive thermal stress at high input voltages.

Input Bypass Capacitors

Due to the inductance of the power leads of the wall adapter or USB source, the input capacitor type must be properly selected to prevent high voltage transient during a hot-plug event. A tantalum capacitors is a good choice for its high ESR, providing damping to the voltage transient. Multi-layer ceramic capacitors, however, have a very low ESR and hence when chosen as input capacitors, a 1-Ω series resistor must be used, as shown in the Typical Applications Section, to provide adequate damping.

State Diagram

The state diagram for the charger functions is shown in Figure 12. The diagram starts with the Power-Off state. When at least one input voltage rises above the POR threshold, the charge resets it self. If both input voltages are in the power good range, the charger selects the CRDL input as the power source. Then if the $\overline{EN}$ pin is at a logic HIGH voltage, the charger stays in disabled state. If the $\overline{EN}$ pin goes LOW, the fast charge starts. Any time the $\overline{EN}$ pin turns HIGH, the charger returns to the disabled state. When the EOC condition is reached, the $\overline{CHG}$ will turn to logic HIGH to indicate a charge complete status but the charge will continue. The EOC condition is then latched until one of the three re-charge conditions is encountered, as shown in Figure 11.

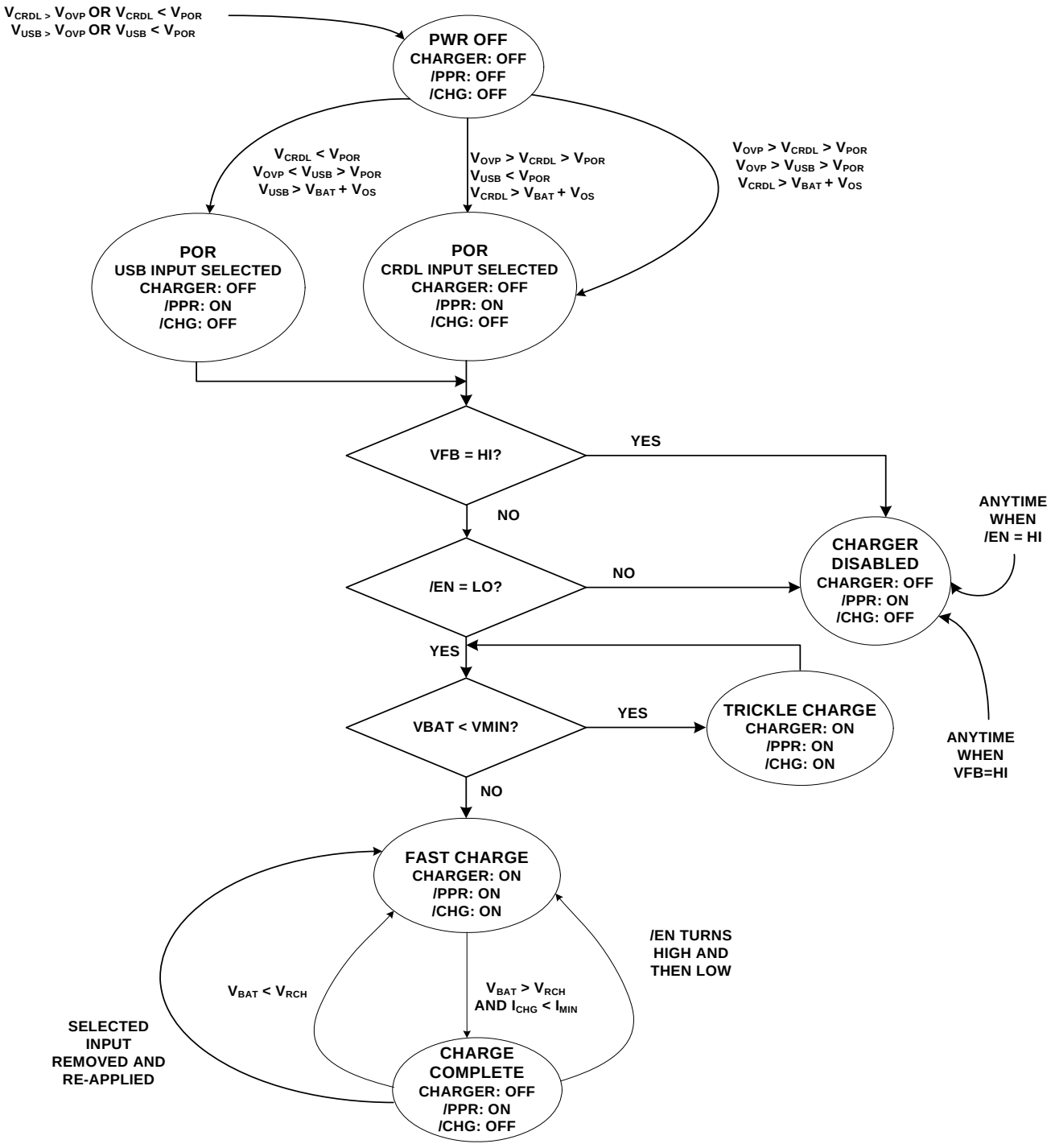
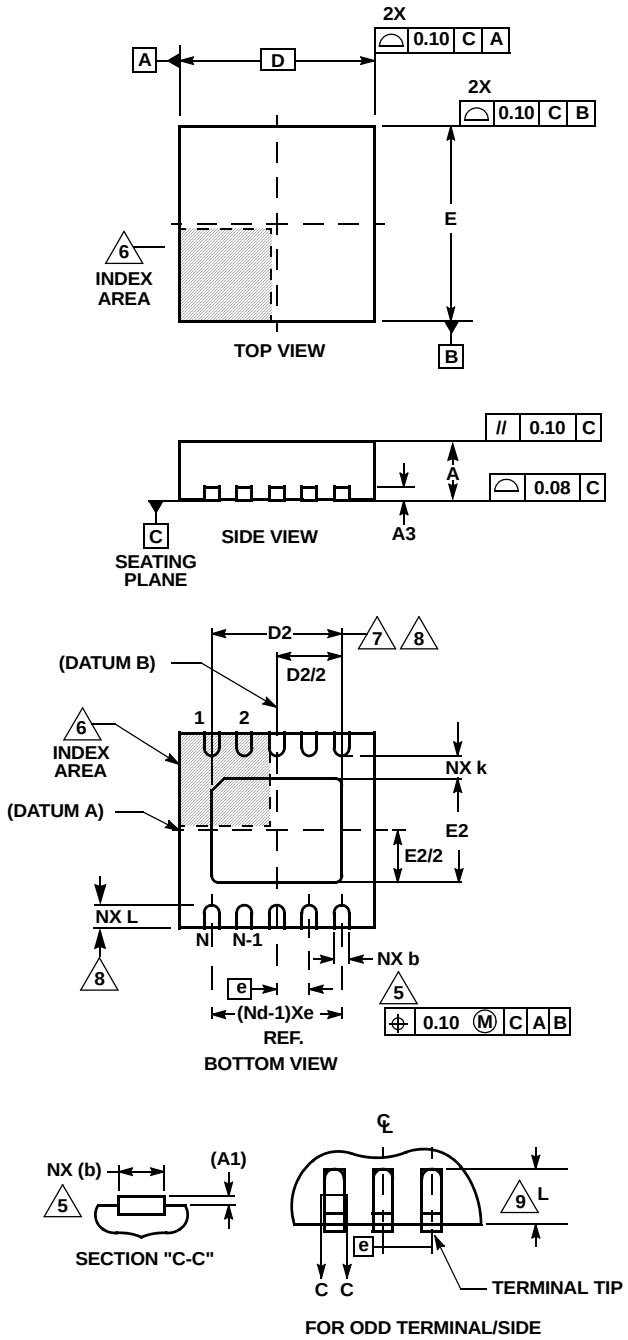


FIGURE 12. STATE DIAGRAM

Dual Flat No-Lead Plastic Package (DFN)



L10.3x3C

10 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.85	0.90	0.95	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.30	5, 8
D		3.00 BSC		-
D2	2.33	2.38	2.43	7, 8
E		3.00 BSC		-
E2	1.59	1.64	1.69	7, 8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.35	0.40	0.45	8
N		10		2
Nd		5		3

Rev. 1 4/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. COMPLIANT TO JEDEC MO-229-WEED-3 except for dimensions E2 & D2.